VERIFICATION AND VALIDATION OF POWER CONVERTERS FOR USE IN FUTURE POWER SYSTEM ARCHITECTURES

by

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ABSTRACT

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Electronics are more widely penetrating almost every area of society and as they do, the demand to supply them with regulated power increases considerably. The scale of the electronic power distribution systems needed ranges from those in very small handheld consumer electronic devices all the way up to those needed in large buildings, ships, and cities. The energy supplied within these power distribution systems can come from many different generation sources that operate either individually or simultaneously. When power electronics are controlled properly, simultaneous generation sources can be employed in a way that optimizes them according to the user's desired parameters. Energy storage, especially lithium-ion batteries, has emerged as a viable candidate for backing up and buffering traditional generation sources. It is difficult, from both a cost and feasibility perspective, to setup and experimentally study large power systems employing distributed generation sources. Computer aided models can be employed reliability to study the many different configuration and control strategies. Before they can be properly employed, accurate device models must be available of all the different distributed sources, power

electronic converters, and loads, respectively. Most of these devices are commercially procured and the vendors are rarely able and willing to supply all the proprietary circuit and control technologies needed to develop models of them at the component level. New strategies are needed to develop these computer aided models and to learn how to put them through a full verification and validation (V&V) procedure that ensures they meet the requirements needed to study these systems against all possible use cases. In the work presented here, a medium voltage (MV) AC/DC testbed has been designed, installed, and experimentally studied to emulate one zone of a zonal shipboard power system. The testbed has several different power generation sources, power electronic converters, and loads that are all being modeled and then put through a V&V procedure. The testbed, computer aided model development, and V&V process employed on several power electronic converters will be discussed here.

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CHAPTER 1

INTRODUCTION

Modern ships will employ distributed systems to maximize performance by localizing commodity specific equipment within specialized zones to limit complexity and increase survivability [1-3]. These zones consist of motors, generators, distribution equipment, loads, power converters, and any additional storage capacity designed to limit the propagation of damage to adjacent zones. Compartmentalization of these components and design of these individual zones is determined by addressing specific design threat outcomes and ensuring that the ship will perform within an acceptable range during these conditions [2]. Although zonal architectures can consist of any number of zones, some suggest the size of each zone should be limited to approximately 15% of the length of the ship to limit the amount of safety significant or mission critical equipment within a single zone [3]. For shipboard power systems, each zone is connected using a longitudinal bus with a distribution node at each zone. Local generation, load, and storage element branching occurs from this node. Although ships may be designed with a single bus, the redundancy provided by two longitudinal buses, running forward to aft on the starboard and port side of the ship, provides greater survivability and quality of service in the event one bus is removed from service due to a fault or damage [1-3].

The design of each zone varies based on the location of equipment within the ship and the individual function this equipment is designed to perform. A simplified zonal structure is shown in Figure 1.1 and consists of a power generation unit, AC and DC busses, loads, storage capacity, and a controller designed to monitor and shuffle power due to load demand. The controller monitors the state of health (SoH) and state of charge (SoC) of the

storage capacity, shown as a lithium-ion battery in this example. The controller governs the sourcing or sinking of power from or to the battery to limit excessive harmonic fluctuations observed by the generator. Specifically, the battery sinks energy when the generator is underloaded and sources energy when the generator is overloaded reducing the power requirement seen by the generator and simultaneously reducing the mechanical stress which can lead to increased generator maintenance or failure [4].

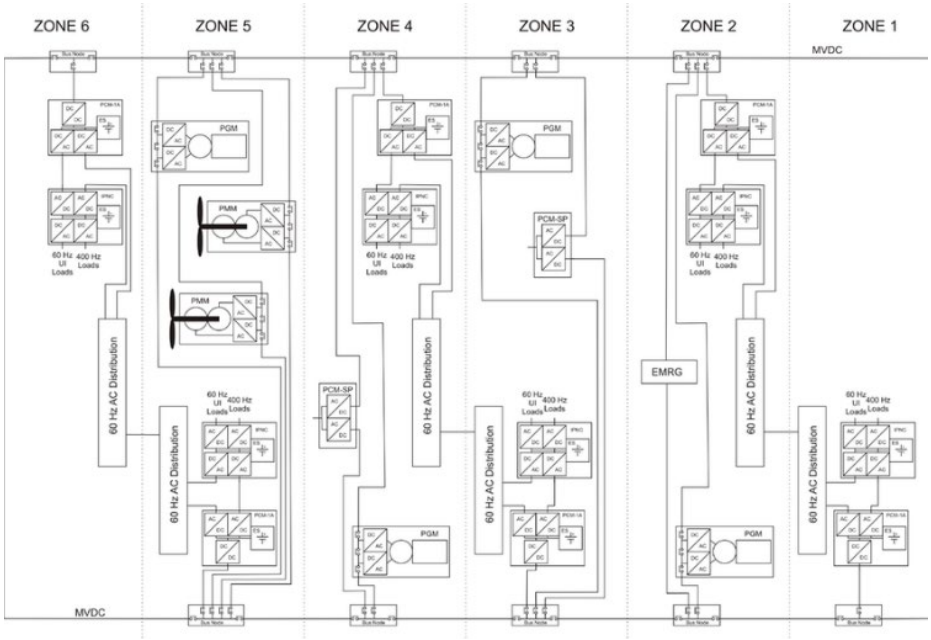

Figure 1.1: Simplified zonal architecture design [1].

Future power system architectures will incorporate a variety of engine-generator sets, power supplies, loads, and the support equipment required to transmit and rectify this energy. Although it is possible to procure each of these components separately and incorporate them into a testbed for evaluation, the feasibility and cost of this process would be substantial in time and space and only provide specific results related to the equipment and setup utilized. One solution that limits the amount of time and money allocated toward hardware is the use of software applications to emulate these components. However, in

creating these computer models, it is necessary to show that they fulfill their stated function and adequately model the individual component and larger power system in which the component resides. This approach has become known as Model Based Systems Engineering (MBSE) and it is driving the design of countless engineering projects. Learning how to use this approach properly in the design of next generation power systems is a primary focus of the research documented here.

During development of emulated components, a process of verification and validation (V&V) must be performed to ensure that the software and computer model accurately capture the necessary details within the domain in which the model is being developed. Initial verbiage describing this process was published by Schlesinger et al in 1979 [5] and has been adapted to processes involving computational modeling by standards such as IEEE-STD-610 [6]. In the context of hardware emulation, verification is an iterative process that requires a developer to routinely check that the model being developed continues to fall within the specifications set forth before the modeling effort began. Then validation is performed to show that the model does meet the required expectations. By following this process, most of the problem identification and resolution occurs during the verification process where multiple models might be created before a valid model is chosen, but often the most parsimonious model with the highest fidelity becomes the fully verified and validated model for a given application [7].

As mentioned, model V&V is performed over a predetermined domain or application because it is normally not feasible to fully V&V a model over a complete gamut of possibility. Therefore, determining that a model is valid requires that the accuracy of its output variables fall within an acceptable range for each question, scenario, or purpose that

the model is being designed to answer and these acceptable ranges must be determined and set prior to the commencement of the modeling effort [7-9]. This validation can then be performed by comparing simulation data with empirical results obtained from actual hardware using testing scenarios designed according to the requirements of the model [8]. In the work presented here, a few different high voltage power electronic voltage converters have been studied and put through a V&V process. The converters are part of a larger testbed that has been setup to emulate one zone of a shipboard power system. The testbed will be discussed along with the V&V process the converters have been put through to serve as a reference for those interested in repeating this activity in the future.

1.1 IDEAL TESTBED

The Intelligent Distributed Energy Analysis Laboratory (IDEAL) was constructed and commissioned in 2019 as a testbed to study the intelligent control of power electronic converters and the use of a battery to buffer rotating AC sources [10-12]. It is also a useful tool for the development, study, and analysis of computer models that simulate the performance aspects of different components within the system. A pictorial one-line diagram of the IDEAL MV DC/AC testbed as it is assembled is shown in Figure 1.2 and an electrical one-line diagram is shown in Figure 1.3.

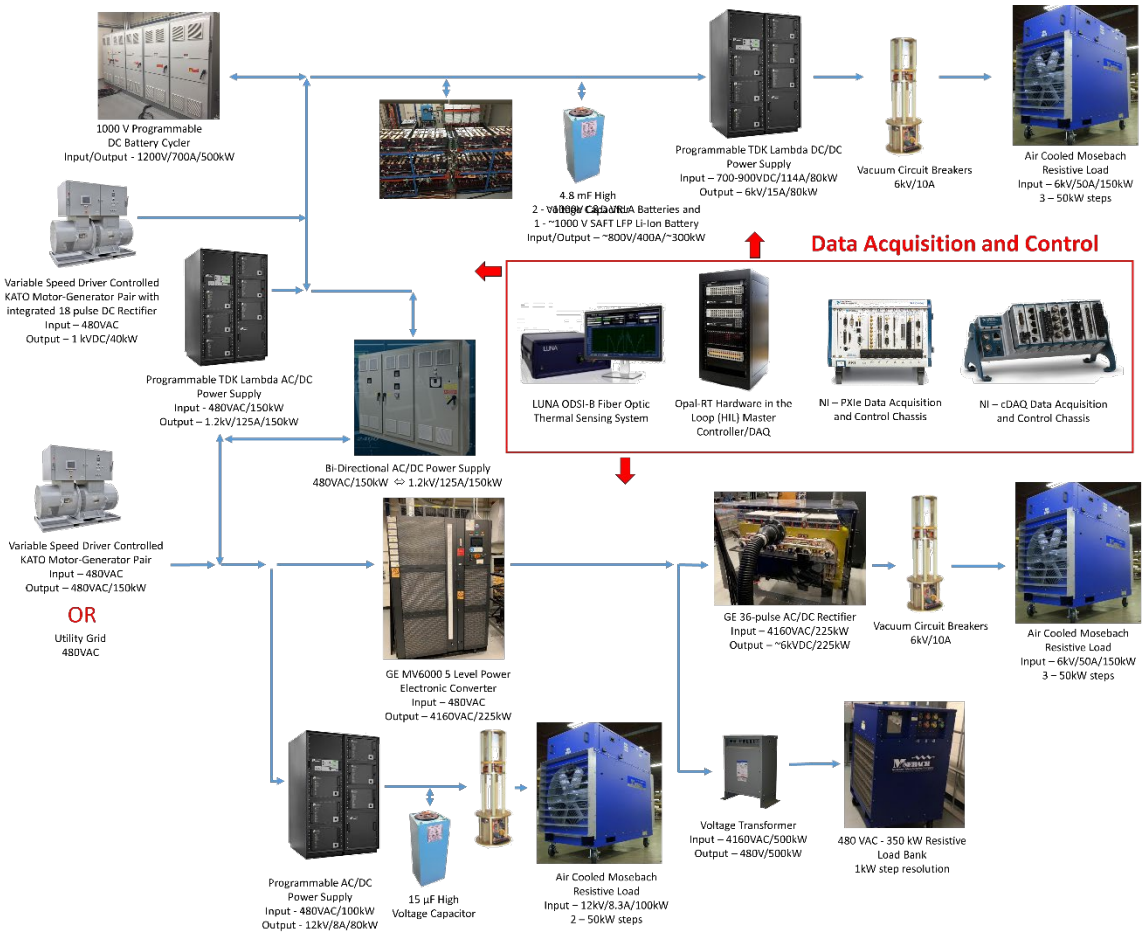

Figure 1.2: Pictorial one-line diagram of the IDEAL MV DC/AC distributed generation source testbed as it is assembled in the UT Arlington Pulsed Power and Energy Laboratory.

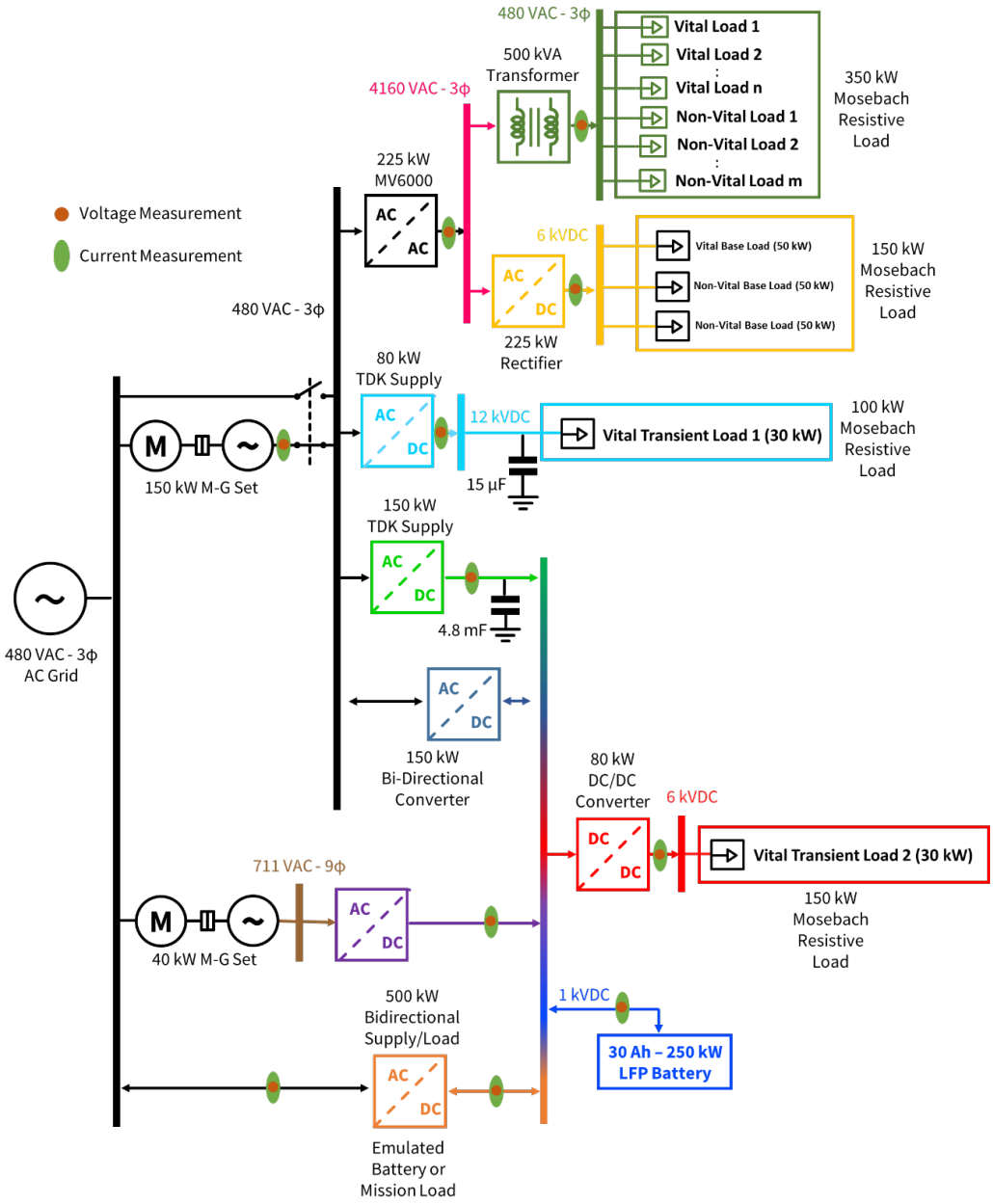

Figure 1.3: Electrical one-line diagram of the IDEAL MV DC/AC testbed.

From the one-line diagrams, the reader can see how the testbed converts AC power to DC power to supply 6 kV and 12 kV MVDC loads and how the 1 kVDC energy storage is used to supply its own load or buffer the AC source. Also sourced is a medium-voltage AC motor drive that creates a 4160 VAC bus to source additional AC loads and AC/DC rectifiers. The testbed's primary source of power is the 150-kW electrical motor-generator (M-G) set, though the

installation is such that the electrical grid can be used to power all or some of the testbed as needed. Each individual testbed component will be discussed in the following subsections along with justification for why they were chosen and how they are used to study the reliability, control, and operational challenges facing the integration of a high voltage, ~1 kVDC, electrochemical energy storage device with an M-G set's three-phase, 480 VAC bus while supplying transient loads.

1.1.1 150 kW KATO Electrical Motor – Generator (M-G) Set

At the far left of Figure 1.3, a variable frequency drive (VFD) controlled electrical M-G set, procured from KATO Engineering, is shown. The generator supplies three-phase, 480 VAC to the testbed and acts as the primary source of power under normal operation. The M-G set utilizes a 300 HP four-pole induction motor to spin a four-pole synchronous generator to 1500 – 2000 RPM. The motor is energized using a VFD through a 400 A electrical feed supplied at 480 VAC. The generator is excited using a direct contact brushless exciter. Photographs of the generator shortly after they were installed in the lab are shown in Figure 1.4.

Figure 1.4: Photographs showing the M-G set (left) and internals of the control and VFD cabinets (right).

KATO designed the generator to allow for the amplitude of its output voltage and its output frequency to be adjusted remotely by the user using two respective analog control signals. The voltage is variable from -20% (384 VAC) to +20% (576 VAC) of the nominal 480 VAC using a 0 – 10 V analog signal. The output frequency is adjustable from -17% (50 Hz) to +11% (67 Hz) of the nominal 60 Hz using a second 0 – 10 V analog control signal. This feature was added so that the generator's output could be modulated using a real time OPAL-RT HIL simulation platform which is desirable since the inherent electrical and mechanical properties of the M-G set do not directly match those of a fielded diesel or gas-turbine driven M-G set. Operation of the M-G set is controlled locally on a human machine interface panel, as well as remotely with a LAN connection.

The M-G's output supplies three different circuit branches that feed off the 480 VAC point of common coupling (PCC), seen in Figure 1.2 and Figure 1.3. Those branches are into a 225 kW – 480 VAC to 4160 VAC five level power electronic motor drive, an 80 kW – 480 VAC to 12 kVDC switch mode power supply, and a 150 kW – 480 VAC to 1.2 kVDC switch mode power supply. Each of these circuit branches will be described in the next few sub-sections.

1.1.2 480 VAC Distribution Box

The testbed is configured so that all three branches off the PCC can either be sourced by the M-G set or by the utility grid. The input connections to the power supply are fed using CAM Loks and a distribution box is used to either supply M-G power or grid power through manual selection. This is shown photographically in Figure 1.5. The distribution box is designed such that only one of the two connections can be chosen, preventing any possibility of user error. Each of the cables exiting the distribution box feed through its own dedicated Hall Effect current sensor that is used to measure the three-phase power supplied to each branch being sourced.

Figure 1.5: M-G or utility grid power distribution box.

1.1.3 GE MV6000 Power Electronic Drive

Working from the top down in the one-line diagram in Figure 1.3, the first branch fed off the PCC is into a 225 kW MV6000 power electronic drive manufactured by General Electric (GE). The MV6000, shown pictured in Figure 1.6, can be sourced by the M-G set or by the utility grid through configuration of the distribution box.

Figure 1.6: Photograph of the GE MV6000 power electronic drive.

The MV6000 is typically utilized in industry as a VFD for MV motors. Its input is an eighteen - phase shifting transformer that steps up 480 VAC to 4160 VAC, RMS. The 18 phases are fed into a 36 pulse diode rectifier that rectifies the 4160 VAC to roughly 6 kVDC and that is

placed onto a capacitive DC link. The DC link feeds a five - level IGBT inverter that generates a three - phase 4160 VAC output. Like how the M-G set's voltage and frequency output can be modulated by a HIL model, so can the MV6000's voltage and frequency. Using two respective 0 – 10 V analog signals, the output voltage can be varied from 80% to 110% of its rated 4160 VAC output and its frequency can be varied from 50 Hz to 70 Hz. Because the MV6000 is a switch mode converter, the output does have a switching component to it that must be filtered for a true sinusoidal output to be obtained. That is not included in the setup here. A custom LabVIEW controller has been implemented to operate the MV6000 and the 4160 VAC output bus can source two different circuit branches from its own respective PCC.

1.1.4 4160 Distribution Box

The MV6000 supplies two different branches using a 4160 VAC distribution box, seen in Figure 1.7. Each of the three-phases are connected into its own copper distribution bus using Eaton's Cooper Power series connectors. Similar connectors are then used to split the bus such that it can feed the two different loads connected.

Figure 1.7: Photograph of the 4160 VAC distribution box installed in the laboratory.

4160/480 VAC Step Down Transformer and 350 kW – 480 VAC Mosebach Electronic Load

One of the two respective electrical branches supplied by the 4160 VAC PCC is into a 500 kVA step-down transformer that converts the 4160 VAC to 480 VAC. A 350 kW - 480 VAC electronic load is connected at the output of the transformer that serves as either a base load or as a variable step load on the bus. The 480 VAC load, seen in Figure 1.8, offered as a standard product from Mosebach, is purely resistive with 1 kW step resolution. It is controlled using a 24 V digital logic supplied by the National Instruments (NI) control system.

Figure 1.8: Photograph of the 480 VAC load.

1.1.5 GE 18 Pulse Transformer and GE 36 Pulse Diode Rectifier

The second electrical branch fed from the 4160 VAC PCC is into a GE 18-phase shifting transformer that is identical to the one at the input of the MV6000. The only difference in this transformer from that in the MV6000 is that its input rating is 4160 VAC, instead of 480 VAC, and has a unity gain. The output of the 18-phase transformer is rectified using the same type of 36 pulse diode rectifier that the MV6000 uses. It rectifies the 4160 VAC to roughly 6 kVDC by using

a multi-pulse rectifier in place of a simple three-phase rectifier, which reduces the ripple of the rectified DC voltage over a conventional six-pulse.

The transformer and rectifier were procured from GE as piece parts that had to be integrated into a single package, seen in Figure 1.9. A custom steel frame was designed and positioned on casters so that it can be moved around as needed. The rectifier, designed in three module blocks by GE, sits above the transformer on an isolated fiberglass reinforced frame. Forced air cooling is needed to ensure the transformer and rectifier stay below their rated thermal limits during electrical operation. An air flow rate of 160 m^3/min is recommended to ensure safe operation. To achieve this, a 15 HP blower is used to force air through the transformer enclosure. The transformer has integrated temperature diagnostics that are monitored by an NI control system to prevent overheating.

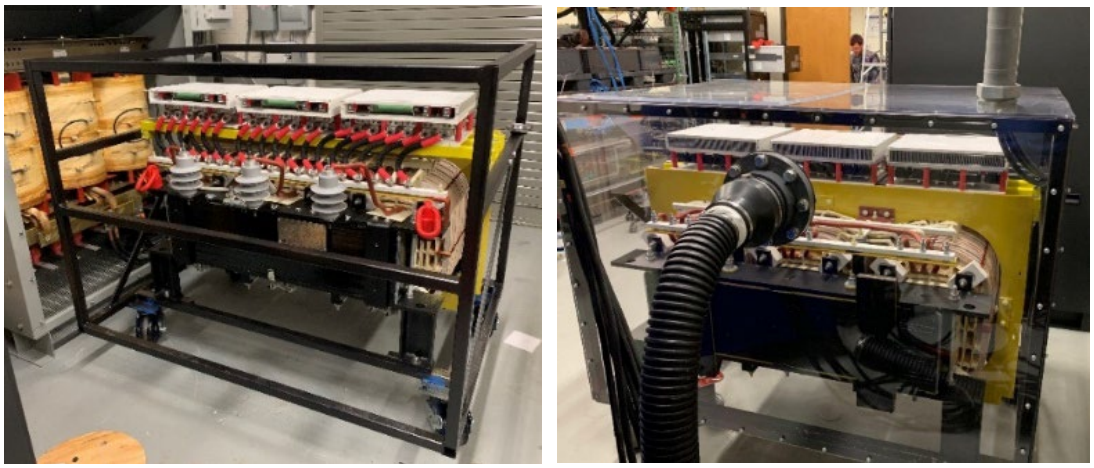

Figure 1.9: Photograph of the 225 kW, eighteen - phase transformer and thirty-six pulse AC/DC rectifier within the custom enclosure fabricated for safety and for forced air cooling. In both pictures, the transformer is below, and the white rectifiers are seen above.

1.1.6 6 kVDC and 12 kVDC Electrical Loads

The two 6 kVDC busses in the testbed are each loaded using their own 150 kW, 6 kVDC resistive load fabricated by Mosebach. The 12 kVDC bus is loaded by its own 100 kW resistive load bank that is also fabricated by Mosebach. They are shown photographically in Figure 1.10.

The 6 kVDC loads have of three 50 kW steps, each of which are connected to the source through a single pole vacuum contactor manufactured by Ross Engineering, model hbdc51-no-40-2-0-bd. The contactors can switch up to 10 A at 50 kV and have an electrode life of roughly 50,000 switching cycles. The contactors are triggered using 24 V logic from the host controller and internal to the load is conversion of that digital signal to the 120 VAC that actuates the contactors. The 12 kVDC load has two – 50 kW steps that are connected using the same type of Ross relays. Each load is instrumented with voltage, current, and power sensors that transmit data back to the host data acquisition (DAQ) and controller. There is some flexibility in the way in which the resistive networks within each load are connected but is limited. The possible configurations within each 6 kVDC load are listed in

Table 1.1 and those for the 12 kVDC load are listed in Table 1.2.

Figure 1.10: Photograph of the two 6 kVDC – 150-kW resistive loads (left) and all three load banks lined up in operational state (right).

Table 1.1 Possible load power levels within the Mosebach 6 kVDC load.

Resistor Combination	Resistance [kΩ]	Voltage [kV]	Power [kW]	Current [A]
1	0.68	6	50.1	8.35
2	0.68	6	50.1	8.35
3	0.684	6	50.1	8.35
1 + 2	1.37	6	25.1	4.18
1 + 2 + 3	2.05	6	16.7	2.78

Table 1.2: Possible load power levels within the Mosebach 12 kVDC load.

Resistor Combination	Resistance [kΩ]	Voltage [kV]	Power [kW]	Current [A]
1 + 2	2.74	12	50.1	4.18
3 + 4	2.74	12	50.1	4.18
2 + 3	3.13	12	43.9	3.66
1 + 2 + 3	4.30	12	31.9	2.66
1 + 2 + 4	3.91	12	35.1	2.93
1 + 2 + 3 + 4	5.47	12	25.1	2.09
1 + 2 // 3 + 4	1.37	12	105.3	8.78

1.1.7 80 kW TDK Lambda 480 VAC to 12 kVDC Programmable AC/DC Power Supply

The middle, teal, branch on the 480 VAC PCC in Figure 1.3 consists of the 480 VAC to 12 kVDC switch mode power supply that is operable up to roughly 80 kW. This power supply is comprised of two – 12 kVDC liquid cooled supplies manufactured by TDK Lambda and are part of their 303L series of supplies. These two independent supplies, seen as the lower two supplies in Figure 1.11, operate in parallel using a master-slave configuration and are designed for use as capacitor chargers but are capable of being used as DC supplies if loaded with a capacitive buffer. To accomplish this, a 15 μF capacitor is connected across their output to ensure there is always load for them to supply. The topology of this power supply may or may not be representative of future shipboard AC/DC converters but having them installed enables IDEAL to serve as a testbed on which power conversion technologies can be deployed and studied. The 12 kVDC power supply

is controlled remotely using analog voltage following that is supplied by NI LabVIEW or OPAL-RT controllers.

Figure 1.11: Photograph showing the installation of the three – 50 kW TDK Lambda power supplies used to convert 480 VAC to 1.2 kVDC (upper two supplies are the two 12 kVDC supplies and the lower three are the 1.2 kVDC supplies)

1.1.8 150 kW TDK Lambda 480 VAC to 1.2 kVDC Programmable AC/DC Power Supply

The third and final electrical branch supplied off the 480 VAC PCC is a 150 kW AC/DC liquid cooled power supply also manufactured by TDK Lambda. The supply is made up of three units seen as the upper three supplies in Figure 1.11. The input to the supply is 480 VAC and its DC output is variable from 30 VDC to 1.2 kVDC. The power converter is assembled as three independent 50 kW supplies that operate in a master-slave configuration. Like the 12 kVDC supply, this supply is designed as a capacitor charger so it must always have a capacitive load connected. This is achieved by floating an 11 kV, 4.8 mF capacitor on its output and the supply's current or voltage is modulated using 0 – 10 V analog signals supplied by the controller being used. In normal operation, the output current of the supply is remotely modulated and controlled using the overarching NI or OPAL-RT controllers. This enables them to also be used to emulate other types of rectifier topologies, as needed.

1.1.9 1 kVDC Lithium-Iron Phosphate Battery

The 1.2 kVDC power supply sources power onto a ~1 kVDC bus that is buffered using a high-power lithium-ion battery. The battery, seen in Figure 1.13, is assembled using Saft VL30AFE cells and is capable of loading roughly 96 kW continuously and sourcing 250 kW continuously and the battery can either source power onto the ~1 kVDC PCC or sink power from the AC source through the 1.2 kVDC power supply. If transient loads are sourced, the battery can act as a base load to the AC source such that it can supply continuous power, even during short periods of load inactivity. This allows the AC source to maintain acceptable AC power quality within MIL-STD-1399. One intention of the testbed is to demonstrate the ability to maintain power quality in this type of operational scenario and to develop and validate the overarching system controller that is needed to achieve this goal.

Figure 1.12: Photograph of the ~1 kVDC LFP-LI battery.

1.1.10 TDK Lambda 1 kVDC – 6 kVDC Programmable Power Supply

The ~1 kVDC bus is loaded by two different branches. The first one is into a programmable DC/DC power supply manufactured by TDK Lambda, model LC253OEM. The power supply is nominally rated to supply roughly 54 kW to its load (though 80 kW is achievable for several minutes). This supply is also designed as a capacitive power supply though it is operated in a DC test mode in this application. Its output current is similarly modulated using a 0 – 10 V analog signal from an NI or OPAL-RT controller and the output of the supply is loaded using the second 6 kVDC Mosebach resistive load previously discussed.

1.1.11 1.2 kV Programmable Power Supply and Load

The second branch off the ~1 kVDC PCC is into a Chroma 17030 programmable cycler, seen in Figure 1.12, that can act as either programmable power supply or as a programmable load with ratings of 1.2 kVDC/ 700 ADC/ 500kW. The cycler can serve as a non-linear load on the ~1 kVDC bus or as a secondary power supply, as needed, and is controlled using Chroma's own software or a 0 – 10 V analog control signal in constant current (CC), constant voltage (CV), constant resistance (CR), and constant power (CP) modes of operation. The system has a slew rate of roughly 10 ms and is regenerative with the building's 480 VAC utility grid.

Figure 1.13: Photograph of UTA's 1200V/700A/500kW Chroma 17030 cycler.

1.1.12 150 kW Unico Bi-Directional 480 VAC ⇔ 1.1 kVDC Power Converter

Only in the last month, a new bi-directional power converter has been added off of the 480 VAC PCC that will either replace or augment the 480 VAC to 1.2 kVDC power converter already discussed. A limitation of the TDK supply is that it is only able to provide power from the 480 VAC side to the 1 kVDC bus but not backwards. This has limited the lithium-ion energy storage to only being able to buffer the generator when Transient Load 2 is sourced. Whenever Transient Load 1 is sourced or other loads are brought up, the generator alone must source those meaning that power quality can be adversely affected. By adding this new bi-directional power supply, the energy storage is now able to buffer any load in the power system once the control code has been written and implemented. Another graduate student will implement this future.

The converter has a slew rate of roughly 10 ms and can supply or source a peak current of 400 A but it it's power dependence limits the peak current at the upper voltage range. The current supplied or sourced on the DC side is controlled using a ±10 V analog control signal supplied by the control system. Once operational, this will significantly expand the capabilities of the testbed.

Figure 1.14: Photo of the Unico 150 kW, 480 VAC ⇔1.1 kVDC bi-directional power converter (seen at left in photo) and isolation transformer (seen at lower right in photo).

1.1.13 40 kW to 480 VAC Electric Motor - 9 Phase 711 VAC Electric Generator with 1 kVDC Rectified Output

Another recent addition to the testbed is a 40-kW electric motor generator set manufactured by KATO engineering. A 60 HP, 480 VAC motor is controlled by a VFD. The motor is coupled to a 40-kW electrical generator that produces a 9 phase, 120 Hz, AC output with a RMS voltage of roughly 711 VAC. It is an 8 Pole, 1800 RPM, synchronous generator with a direct connected rotating brushless exciter. Like the other KATO motor-generator set, the AC output voltage and frequency can both be dynamically controlled using a 0 – 10 V analog control signal. The output of the generator is rectified using an 18 pulse SCR rectifier that is controlled using a gate trigger circuit designed and sold by Applied Power Systems (APS). The controller runs open-loop currently meaning that there is no active feedback to regulate the rectifier's output voltage or current. Using either a voltage probe or a current sensor fed back into the overarching LabVIEW controller, the loop could easily be closed but that has not been done so far. A future student will implement that functionality. Additionally, APS is working to supply a controlled loop controller

that can be used in lieu of a controller implemented using the LabVIEW controller. The motor-generator/rectifier set has been installed to study the feasibility of using directly rectified and controlled motor-generator sets to supply transient loads. This has advantages and disadvantages when compared to traditional AC/DC power electronic converters. A photograph of the M-G set is shown in the left side of Figure 1.15. A closer look at the nine fused generator output phases, behind which are the rectifier, are shown in the right-hand side of the figure.

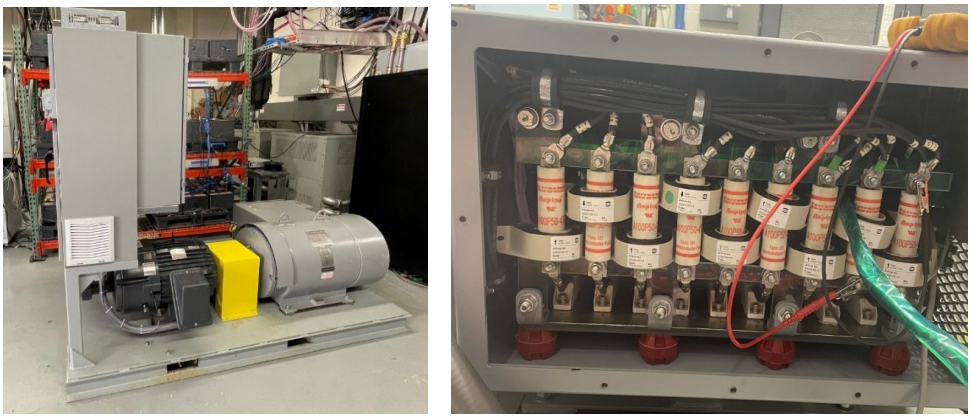

Figure 1.15: Photo of the 40 kW KATO motor-generator/rectifier set that produces a rectified 1 kVDC output onto the 1 kVDC bus (left) and 9 phase fused output and SCR switches (right).

1.1.14 Voltage and Current Monitoring

AC and DC voltage and current measurements are made throughout the testbed, measured, and digitized using multiple NI CompactDAQ (cDAQ) cards mounted in a few different NI cDAQ chassis. A NI PXI chassis, instrumented with several voltage measurement cards, and the OPAL-RT HIL system are also used for data acquisition and monitoring. The networked cDAQs and the OPAL-RT work together to provide real-time control of the hardware. Each system monitors voltage and current waveforms needed to make real time decisions. Network variables are used to share measurements across platforms. The sample rate varies across systems to optimize processing speed and resolution needed for testbed performance analysis. Nearly all current

measurements are made using closed loop Hall Effect current sensors. The primary ones used are Harting 100 A and 300 A sensors that have a bandwidth of 50 kHz. Voltage measurements are made using a few different types of differential voltage probes. The first is a 1.4 kV, 25 MHz, differential voltage probe manufactured by Pico Technology (model TA057), the second is a 7.0 kV, 70 MHz, differential voltage probe also manufactured by Pico Technologies (model TA044), and the third is a Cal Test Electronics CT4079-NA 50 MHz/±15 kV High Voltage Differential Probe. The bandwidth and voltages of these probes allow for all voltages within the testbed to be sufficiently monitored in real time.

1.1.15 Thermal Monitoring

Simultaneous thermal measurements are made using a four channel, Luna ODiSI 6100 fiber optic sensor (FOS) system. Briefly described, the ODiSI 6100 is used to measure temperature or strain at discrete locations down the length of a very thin, ~80 μm diameter, fiber optic cable using a single channel data acquisition system, four of which are installed in the instrument. Luna's optical frequency domain reflectometry (OFDR) technology senses using distributed Rayleigh scatter inherent to the fiber and relies on fiber bragg grating (FBG) arrays inscribed into the fiber. By interrogating the FBGs, the Rayleigh backscatter of a fiber creates a unique pattern that is measured by the instrument. Instead of a clear peak or set of peaks, however, the reflected amplitude, phase, and spectrum of the scatter are random patterns that are unique and repeatable for each sensor. The signature is calibrated for each sensor and when placed in contact with a device to be sensed, it is capable of measuring temperature changes over a range of -268°C to 900°C with 1ºC accuracy and strain over a range of ±12,000 με. Measurement resolutions as low as 1 mm can be achieved using short fibers, less than a few meters, and resolution as low as 5 mm can be achieved using longer fibers, as long as 50 m. Using the four FOS channels, it is possible

to measure the temperature of every terminal of the lithium-ion battery and high spatial resolution of the other electronic components within the testbed as well.

In addition to the Luna ODiSI FOS, thermal measurements are made using NI 9213 cDAQ cards installed in the NI cDAQ chassis. Each of those cards can sample 16 simultaneous thermocouple measurements at sample rates as high as 75 kHz. Type T thermocouples are distributed throughout the testbed, including on the bodies and terminals of the battery, within the loads, inside power supplies, etc.

1.1.16 User Interface and Virtual Extension

The user controls the testbed via the control box shown in Figure 1.16. The color-coded one-line diagram in Figure 1.3 describes what each button controls within the testbed. On the left side is a three-position toggle switch used to command the testbed into ‘combat’, ‘cruise’, or ‘standby’ modes of operation. Previous researchers David Dodson and Brian McRee designed this controller. These different modes dictate the slew rates of the M-G sets in the model and is used by the control system to define how the system is optimized. The two white round buttons are used to increment (right) and decrement (left) the load sourced by the 480 VAC Mosebach load. Each button press increments or decrements the load by an amount defined by the user in the VI.

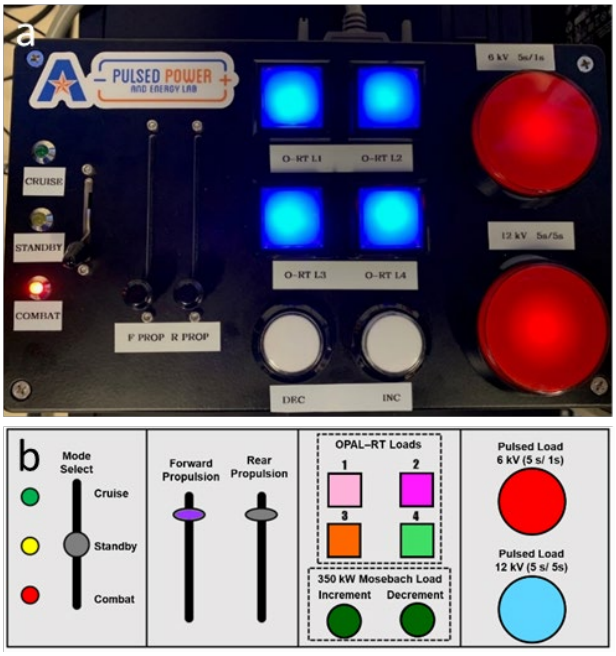

Figure 1.16: (a) The testbed can be controlled through user input with a control box external to the system. (b) Diagram describing the functionality of each button on the control box.

Finally, the two large round buttons are used to actuate the 6 kVDC and 12 kVDC TDK Lambda power supplies. The top button commands the 6 kVDC supply to output a 5 second on/ 1 second off pulsed profile into the 6 kVDC Mosebach load. The lower button commands the 12 kVDC supply to output a 5 second on/ 5 second off pulsed profile into the 12 kVDC Mosebach load. Each button press actuates a single instance of its respective load profile, whose power level is set by the user, and holding either button causes the profile to be repeated for as long as it is held. Additional functionality will be introduced into the testbed using the sliding potentiometers and the four blue square buttons that will command loads within the simulated zones in the extended multi-zone model developed and executed on an OPAL-RT HIL platform.

1.1.17 NI and OPAL-RT Control

A custom DAQ and control system has been written using NI LabVIEW software. Previous researchers David Dodson and Brian McRee designed the initial version of this controller in 2019 and it has been modified significantly with the help of Dr. Gregory Turner since that time. The main LabVIEW virtual instrument (VI) that has been written to interface with the cDAQs is shown in Figure 1.17. There are many sections that make up the VI. The first, shown in the left blue column, is for controlling the 12 kVDC, 1.2 kVDC, and 6 kVDC power supplies, respectively. The program gives each of those supplies control reference set points as well as their inhibit and enable commands. Once enabled onto their respective bus, the control box in Figure 1.16, is used to command the supplies.

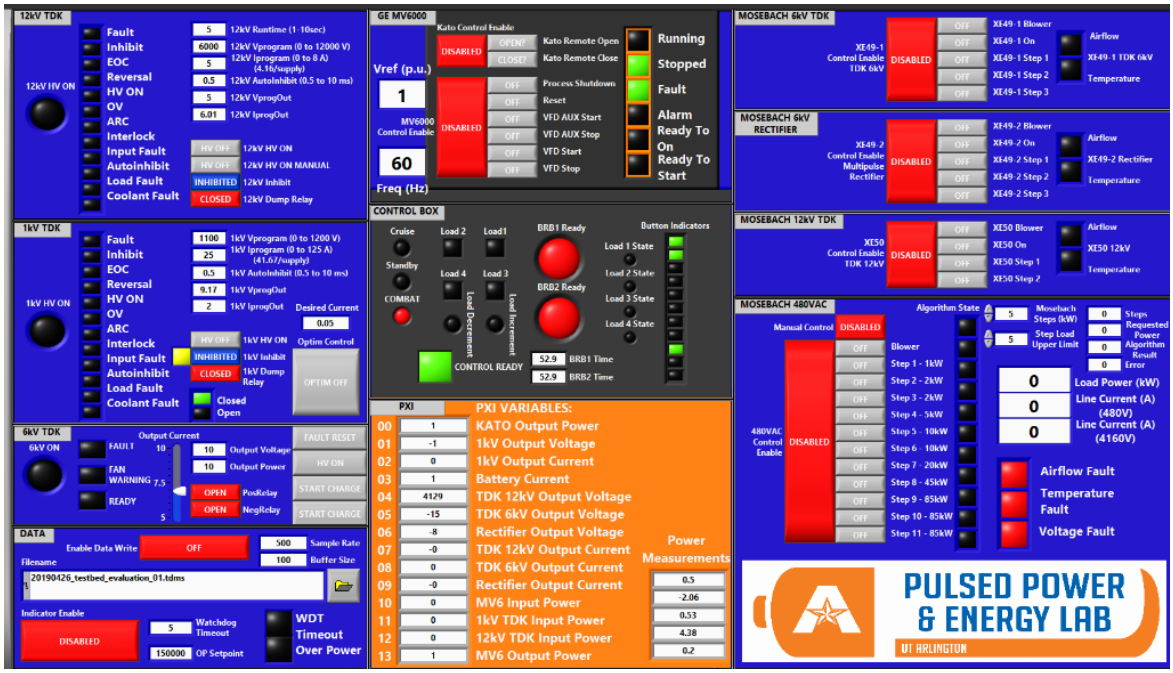

Figure 1.17: Main control VI used to interface and control all the power supplies and loads within the testbed.

Moving to the right in the VI, the upper black section is where the MV6000 is controlled. The user is able to set the MV6000's voltage and frequency there when the analog control feature

is not being used. There are several other interface commands that are required by the MV6000 for safe operation and those are handled there. Moving down, there is a digital version of the control box that reflects its present state. This is more for user convenience than anything else and for helping to verify that the box is sending the proper commands. Moving down to the orange section in the middle, this is where network variables are received from another VI collecting and recording data from the NI PXI chassis that is monitoring data throughout the testbed. These variables are received by the main VI which then serves as the interface between the hardware and the OPAL-RT. Finally, the rightmost blue column in the VI is where each of the four respective Mosebach loads is controlled. It is here where each respective 50 kW step in the MVDC loads can be added or removed and where the 480 VAC load's step resolution can be set.

There are three separate VIs used to monitor and collect data from the PXI chassis and for interfacing with the 1 kV battery. The one interfacing with PXI chassis will not be shown in detail here as it is primarily used for displaying graphs of the real time data being collected and there are two VIs used to interface with the 1 kV battery. The first is for the purpose of communicating with the battery management system (BMS). The VI reports back all 260 individual cell voltages and any faults the BMS reports. The second VI is used to safely erect the battery's 28 i individual modules into a single battery and connect it onto the ~1 kVDC bus.

1.1.18 Control System Improvements Since 2019

System level monitoring and control is achieved with two separate PC's running LabVIEW and National Instruments (NI) data acquisition equipment. The first system uses a NI PXI chassis data acquisition system to measure a comprehensive set of voltages and currents in every branch of the system. Power in all branches of the system is calculated from these real-time voltage and current readings with the NI Virtual Instrument (VI) panel. All data from the PXI chassis is

transferred to the main system controller using LabVIEW network variables across an ethernet connection between the systems. In the main controller, an additional set of NI data acquisition hardware maintains direct control of the system using analog and digital input and output signals. This includes control of all loads, power supplies, as well as the hardware control and system communication with the motor/generator set and the GE MV6000 power electronic drive. Control of system loads is achieved with digital output directly from the main user interface of the LabVIEW software. In addition to the software control interface, a control box with physical buttons is maintained to allow for tactile control of mission loads [10-11]. The control box is connected through a digital input NI data acquisition chassis. Polling software has been developed to de-bounce these inputs and develop interrupt level response for these user level inputs.

1.1.19 Load Hierarchy

As already presented earlier, the testbed consists of three DC load banks and one AC load bank, seen in Figure 1.2. Using software, each of the load banks can be split into multiple smaller loads such that they are representative of load architectures onboard a ship. Loads in the system are categorized in a generalized prioritization hierarchy. At the highest level, loads may be classified as base load, shed-able load, and transient load. Base load in general, is always on and should always be serviced. Shed-able loads may be turned off and sacrificed when sufficient power generation is unavailable and are shed according to a priority level assigned by the controller until sufficient load has been dropped. Though transient loads can also be shed-able in unique circumstances, they are considered high priority and should always be serviced. As seen in Figure 1.2 and Figure 1.3, Vital Transient Load 2 is serviced off the same 1 kVDC bus as the LFP battery allowing the load to be serviced either partially or fully by either the motor/generator set or the battery. In that sense, this load is a shed-able load from the motor/generator set so long as the

battery has enough state of charge (SoC) to meet the load demand. When available, it is best to service Vital Transient Load 2 using the generator to maintain battery SoC, but its transient on/off profile can inject poor power quality in the form of harmonics into the AC bus. Mitigating these negative impacts can be achieved by buffering the front and back ends of the transient load's profile using the energy storage. When the battery's SoC is sufficiently high, the software has been designed to initially source the front end of this load profile using the battery while ramping up the supply of power from generator. This is implemented by ramping the current limit imposed on the 480 VAC to 1.2 kVDC power supply located between the 480 VAC PCC and the 1 kVDC bus. The ramp rate can be adjusted by the user dynamically or operated according to preset values assigned for each respective operational mode of the controller, described later. As the generator ramps its power up to whatever percentage of the load demand the controller sees allowable, the power supplied by the battery ramps down at the same rate. Upon deactivation of the load, the generator can maintain its steady baseload into the battery, recharging it for future operation. When it makes sense to start decreasing the load on the generator, the current set-point on the power supply is ramped down in a similar fashion allowing the generator to see smooth transitions on both ends of the transient load's operation. Only recently, the testbed has been configured such that it is possible to share the energy storage into the upper two branches off the 480 VAC PCC. This is possible with the addition of the Unico power converter discussed earlier and because it is so new, it has not been introduced into the control system as of this writing. Prior to its install, Vital Transient Load 1 must be serviced directly by the 480 VAC PCC and cannot be shed from the motor/generator since it is a vital load. Though the front end of the transient load profile cannot be buffered by the battery, it can be buffered upon deactivation in a similar fashion to the shedding of Vital Transient Load 2. Though this is not ideal, it does mitigate the harmonic injection that

would be introduced from the rapid unloading of the generator without this capability. Maintenance and monitoring of the energy storage SoC is therefore a key factor in making the value judgements needed in the decision process of load prioritization. Some experiments demonstrating the buffering using the battery will be presented later.

1.1.20 Load Shedding

As already implied, each load is further sub-categorized as being either vital or non-vital. This classification allows every load to be prioritized depending upon the current operational mode of the power system. Three operational states have been defined whose transition events are described in Figure 1.18. Cruise mode prioritizes vital and non-vital loads equally and ensures hotel load operation for shipboard crew. Stand-By mode allows non-vital load shedding in anticipation of the activation of vital systems. Stand-By also prioritizes the top-off of the energy storage elements. Combat mode prioritizes all vital loads such as communication and radar loads, among others, during the operation of transient loads.

An example load prioritization profile is identified below for a combat scenario (highest priority first):

- Vital Base Load
- Vital Transient Load (unsupported by energy storage)
- Vital Transient Load (supported by energy storage)
- Vital Shed-able Load
- Non-Vital Base Load
- Non-Vital Shed-able Load

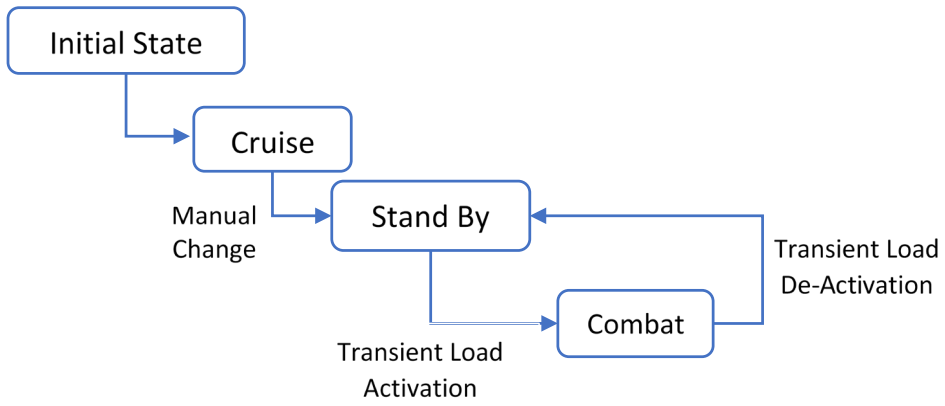

Figure 1.18: Flowchart of combined software and hardware operational state transitions.

Within each operational state, a sub-state machine controls the operation of loads within the system. This is of particular importance in Combat mode when Vital Transient loads, which are considered as either active or inactive, are used. Considering two of these loads in the present power system, there are four possible states to consider, seen in the first column of Table 3. Operation of a vital transient load from the main control box create event(s) that cause the state to change. A button press causes a falling edge event on the digital input to the system and activates the load. Once the button is pressed and the load has activated, there is a finite amount of time before the load automatically de-activates and becomes ready again. The top row of the state transition table lists all the events that cause transitions. It would be rare for edges from these buttons to occur simultaneously as they are under human control. However, the state table, and therefore the software, does account for these possibilities to ensure coverage of these corner cases.

Due to use of the LabVIEW programming language, the state machine is handled with nested decision-making case structures that follow through the state transition table. The fall-through cases have all been programmed as a 'no-event' decision and this allows the state machine to normally stay in its current state by default. Dynamic performance is optimized in this way since

actual events are relatively rare in the scope of the user interface experience. Figure 1.19 shows a segment of the LabVIEW controller that is at the heart of the state machine.

Table 1.3: State transition table considering two vital transient loads.

Transition Events / Present State	VT Load 1 Activation	VT Load 1 De-Activation	VT Load 2 Activation	VT Load 2 De-Activation	VT Load Simultaneous Activation	VT Load Simultaneous De- Activation
No VT Loads Active	VT Load 1 Active	XX	VT Load 2 Active	XX	VT Load Both Active	XX
VT Load 1 Active	XX	No VT Load	VT Load Both Active	VT Load 1 Active	XX	XX
VT Load 2 Active	VT Load Both Active	XX	XX	No VT Load	XX	XX
VT Load Both Active	XX	VT Load 2 Active	XX	VT Load 1 Active	XX	No VT Load Active

Each vital load is activated by pushing a ‘big red button’ on the control box. Within the code, they are abbreviated as BRB1 and BRB2, respectively. The controller is keeping track of the falling edge (FE) and rising edge (RE) of the digital input from the NI hardware and a button push generates an event for the controller where the falling edges are considered activations and rising edges are de-activation. In Figure 1.18, the previous state of the system is a BRB1 Active state; therefore, the events that require consideration are the rising edge of BRB1 and the falling edge of BRB2. An exclusive OR operation is used to first consider that one and only one of these events has occurred. After the exclusive OR operation checks for a single edge event, the possibility of a multi-edge event or a no edge event must be considered. It is possible, but unlikely, that both a BRB1 rising and BRB2 falling edge happen at the same time. In this situation, the controller transitions from the BRB1 Active state to the BRB2 Active state instantaneously. However, if no edge occurs on either button, then the system remains in its current state because the controller registers no event.

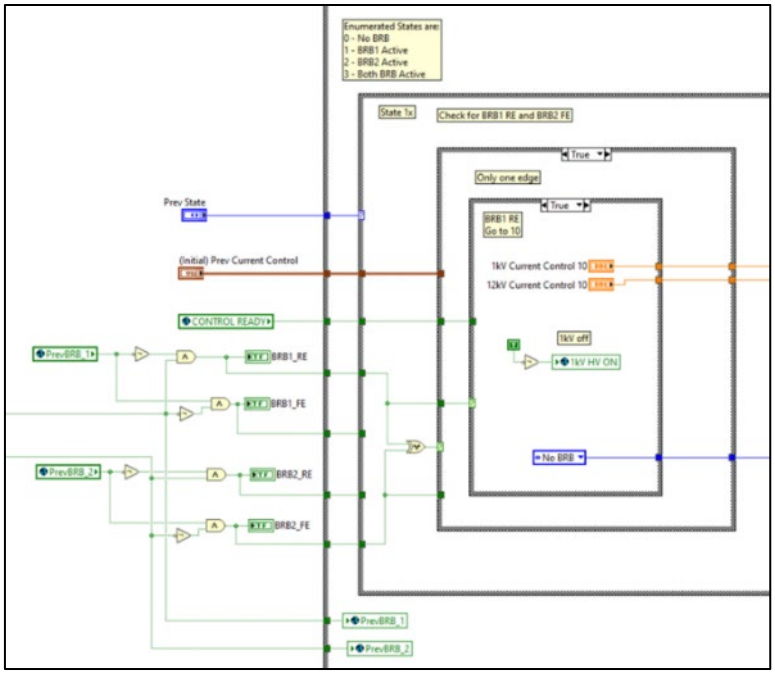

Figure 1.19: LabVIEW representation of a state machine for a two vital load system.

A few experiments performed using the hardware will be presented here to demonstrate the testbed's operation and the type of events the models being created must be able to represent. In the first experiment, Vital Transient Load 2 is buffered by the battery on both the activating and deactivating edges of the transient profile. Figure 1.20 presents data showing the battery rapidly turning on to meet the leading-edge demand of the profile when the load is activated. The power supplied by the generator immediately ramps from 0% to 90% of the load profile over one second. A linear ramp is shown here but this can be essentially any shape determined to effectively mitigate harmonic injection on the AC bus. The 90% load and 1.5 second rise time are both arbitrarily chosen for clear demonstration here but can be either intentionally set by the user or defined by the system controller in real time. When putting the 1 kV/6 kV DC/DC converter model through its V&V process, all possible ramp rates must be properly defined and considered for completeness, otherwise it is possible for the model to be inaccurate under certain circumstances. The generator maintains its power output on the falling edge of the load profile, supplying power

to recharge the battery and then starts to ramp down at the same arbitrary rate of its rise. Current into the battery quickly rises and then ramps down at the same rate. This results in a small net capacity increase for the battery. If the battery SoC is low, the generator could continue to supply the battery for some time before it begins to ramp down. These decisions are dependent upon the specific mode of operation and availability of system resources.

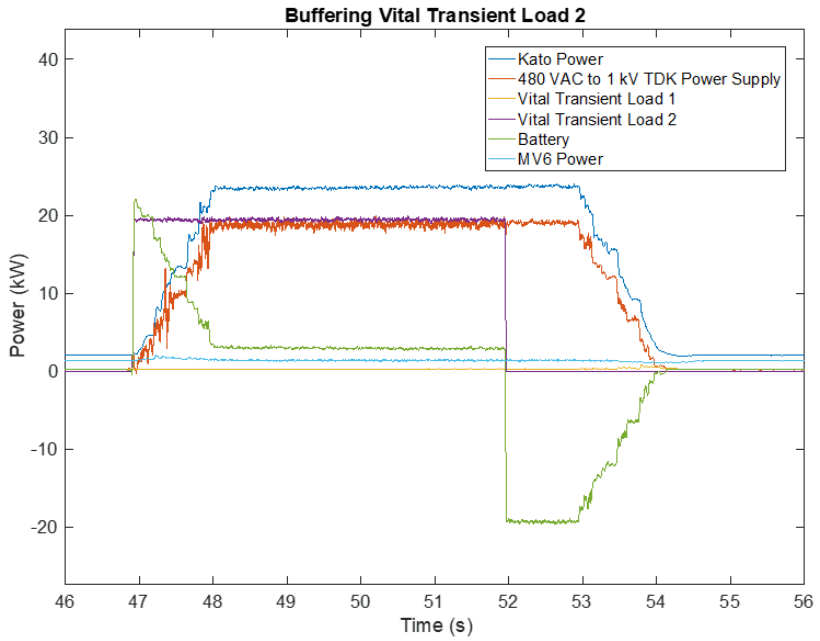

Figure 1.20: Demonstration of motor-generator buffering using the battery during the activation and de-activation of Vital Transient Load 2.

As previously mentioned, the 1 kVDC to 480 VAC UNICO inverter has not been fully commissioned yet and until that happens, is not possible to buffer the activation, or operation, of Vital Transient Load 1 unless the 480 VAC to 1.2 kVDC power supply is already drawing power. In this scenario, the 480 VAC to 1.2 kVDC power supply can be turned off at the same time Vital Transient Load 1 is activated. This causes the generator to maintain a near consistent base load and forces the battery to supply an active Vital Transient Load 2. It is possible to buffer the generator during deactivation of Vital Transient Load 1 by turning on the 480 VAC to 1.2 kVDC power supply at the same time the load turns off. Doing this will either supply recharge current to

the battery or supply an active Vital Transient Load 2. A demonstration of this functionality is shown in Figure 1.21. At the start of the plot, nothing but parasitic power draw is occurring. A few seconds into the experiment, Vital Transient Load 2 is activated. The battery supplies the initial transient load as the generator ramps up to over the supply of the load and even slightly recharges the battery. Just after 190 second into the experiment, Vital Transient Load 1 is engaged. Because the battery is sufficiently charged, it absorbs all of Vital Transient 2's load nearly instantaneously as Vital Transient Load 1 comes on. The activation rates of the supplies are slightly different and since the 1.2 kVDC is faster it can turn off before the 12 kV power supply is engaged causing a momentary dip in the generator power. This is not ideal and requires additional controller work to alleviate, but it shows how the controller is at worst able to prevent rapid changes in power no longer than 0.2 seconds in duration. The battery supplies Vital Transient Load 2 while the generator supplies Vital Transient Load 1 until former turns off. When Vital Transient Load 1 turns off just over 200 seconds into the experiment, the 1.2 kVDC power supply turns on to maintain base load, recharging the battery. In this case, because it is faster, it results in a short excess draw on the generator that again needs to be improved. The battery is recharged until Vital Transient Load 2 is engaged again. When this occurs, power from the 1.2 kVDC converter supplies the load and partially recharges the battery resulting in no change in the generator's power. Finally, when Vital Transient Load 2 turns off, the base load continues to be maintained by recharging the battery until it is recharged enough to begin the slow ramp down process shown earlier.

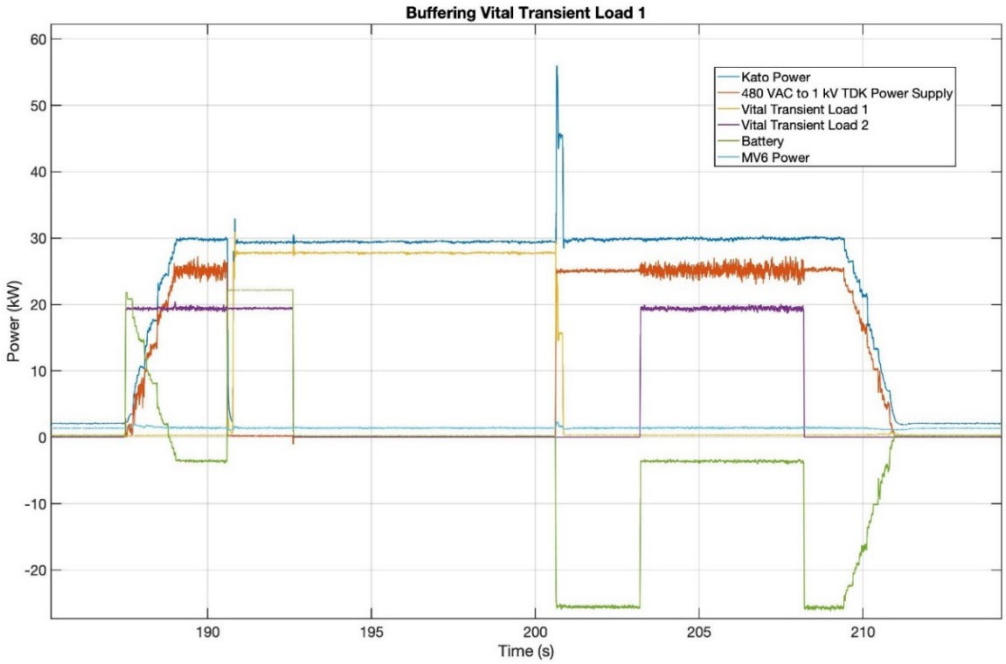

Figure 1.21: Demonstration of motor-generator buffering using the battery during the activation and de-activation of Vital Transient Load 1.

In this final example, a load shedding event is demonstrated. The motor/generator set in the IDEAL testbed can supply ~150 kW. The total of all possible loads can well exceed that value so automated load shedding is required to protect the generator during an over-load condition. A load-shedding algorithm has been implemented removing loads in a prioritized manner until the generator's total load is below an over-power threshold. This value is set arbitrarily by the user. Considering the setup in Figure 1.2 and Figure 1.3, shedding will remove non-vital loads, connected to the 4160 VAC to 480 VAC transformer to reduce the motor/generator's output power below the threshold. If shedding the non-vital load(s) alone does not sufficiently decrease the generator's demand, the battery is available to shed Vital Transient Load 2 from the generator so long as its SoC is sufficiently high. Beyond that only vital loads can be shed. To demonstrate some of this capability, an experiment has been performed with data collected shown in Figure 1.22. The over-power threshold has been set at 90 kW for this experiment. At the start of the experiment

the generator is base loaded with roughly 58 kW. A second or so into the experiment, the Non-Vital Load comes on drawing just over 15 kW, increasing the generator's load to just under 75 kW. Shortly after that, Vital Transient Load 2 is engaged drawing 45 kW. That load is initially supplied by the battery to buffer the transient loading of generator. As the generator ramps up to carry the load, the over-power threshold is exceeded. There are two possible options for decreasing load on the generator. The first is to stop ramping the generator, shed no load from the system, and allow the battery to supply whatever is needed to keep the generator below the threshold. If the SoC of the battery is high enough and depending on the mode of operation, this is the most logical choice. The second option demonstrated here is for the Non-Vital Load to be shed and the generator to continue to supply as much of the vital transient load as it can. This makes sense when the SoC of the battery is low or the mode requires that energy storage be maintained for future use. When the non-vital load is shed, generator demand drops below the over-power threshold as it continues to ramp up its supply of Vital Transient Load 2. The generator is unable to supply all the baseload and all of Vital Transient Load 2 without again exceeding the over-power threshold. Therefore, the battery supplies just over 15 kW of the load while the generator supplies the rest keeping it just under 90 kW load. When Vital Transient Load 2 turns off, the generator ramps down recharging the battery while buffering the rapid change to the generator.

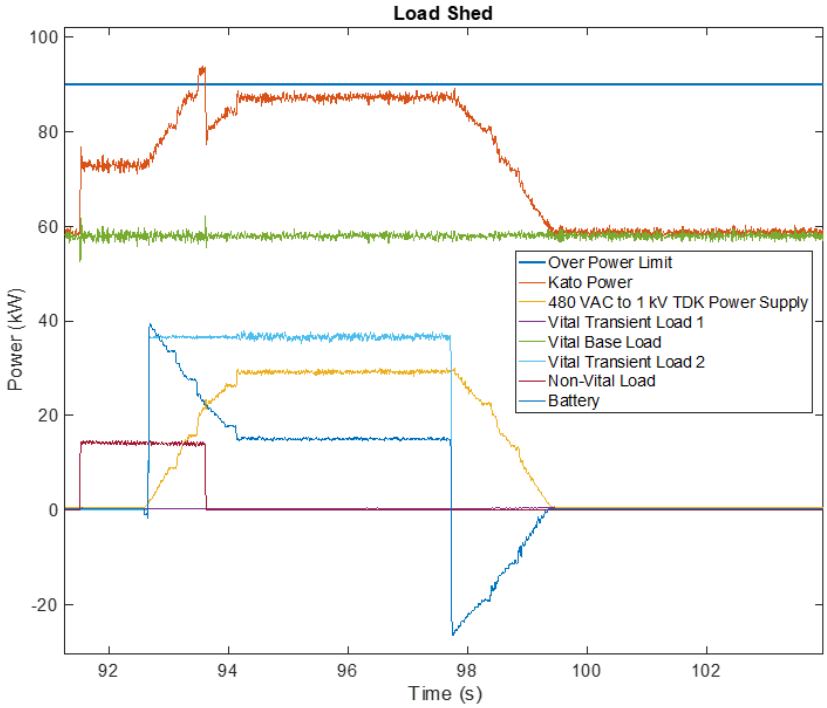

Figure 1.22: Demonstration of load shedding of non-vital loads in the event of an over-power scenario.

1.2 Research Overview and Modeling Options

In the proceeding sections a medium voltage AC/DC testbed has been presented as a platform on which to study the design and control of next generation shipboard power systems. The experimental data shown demonstrates the manner in which power electronic converters can be controlled in collaboration with energy storage to buffer traditional power generation sources. Data has also demonstrated the shedding of load to prevent overpowering the generator. The data has illustrated many of the variables that can be adjusted in the power system including ramp rate, power supplied, and battery SoC control for example. These are parameters that must be bounded and well defined before complete models can be created, verified, and validated. As power systems like the one presented here are designed, it is not always feasible to procure all the components and assemble them in a full system mock-up as has been done here. It is much more feasible to obtain data from each component individually, either from the manufacturer or through

independent testing, and to use that data to create system models that can be used to validate the design. To properly complete the V&V process, experimental data must be collected from each of the sources and power converters across the full range of variables so that the data can be used to train the model evaluate its performance. This process will be described in the sections to come and it is intended to serve as a reference for those exploring this methodology of power system design.

CHAPTER 2

MODELING

Modeling of any system is an invaluable process as it provides an insight to the performance and behavior of a system without requiring that it be purchased and setup for experimental study. It saves time, money, space, and effort. A typical simulation model uses a mathematical representation of component(s) and connects them in a way that represents the component(s) or system(s) of interest. Making a complete and accurate model requires intimate knowledge of what is being studied, and a verification and validation (V&V) procedure must be completed to ensure the model is valid across all use cases of interest.

Power electronics are key pieces of the effort presented here. When considering a power electronics system, a complete understanding of many different aspects of the architecture are required to develop a complete and accurate model. These include, but are certainly not limited to, understanding the schematic, control structure, circuit protections, thermal characteristics, aging characteristics, the physical size and weight, and a slew of other system information. The process is a long and tedious one but if every electrical component is accounted for and properly implemented, then a virtually complete model that captures the electrical behavior under all the necessary use-cases is possible.

Accounting for every component and control feature is not always feasible, especially when the item being modeled is procured from a third party that is not willing or able to share all the intimate details required. In these cases, it is only possible to model what is known as closely as possible and interpolation is needed to fill in the unknowns.

This creates a model that is as close to reality as possible, and this is what is being explored here.

Tracking all the electrical, thermal, mechanical, and aging characteristics of a model requires multiple domains in small- and large- scale operations and can be a mathematical and computational nightmare. A model is often not interested in capturing all the many characteristics of a system. Instead, the model should be limited to capturing only what is needed. When modeling a toaster for example, it may only be necessary to model the heat dissipated across the coils and not capture the time response of the sensor used to stop the heating process. Similarly, a model tracking steady-state operation of a generator may not care about tracking the small-signal start up controls. The key to successfully modeling a component is to properly define the required information and bounds of what the model must be accurate in predicting. The process of V&V is designed specifically for this purpose [12].

2.1.1 Verification and Validation (V&V) Process

Typically used in software design, the V&V process allows a designer to develop a piece of software with a specific purpose in mind, verify its operation, and validate its ability to accomplish the purpose at hand. Figure 2.1 presents a flow chart of the V&V process. This is representative of one of the countless V&V diagrams that are openly published [13, 14]. The reader will notice that there are many steps or phases that make up the V&V processes. The conceptual design and implementation are performed in the verification phase. The model's ability to meet its intended function and result is evaluated in the validation phase. For each of the verification steps, there is an accompanying

validation step that is performed. Those pairs will be discussed briefly along with how they apply to the work being performed here.

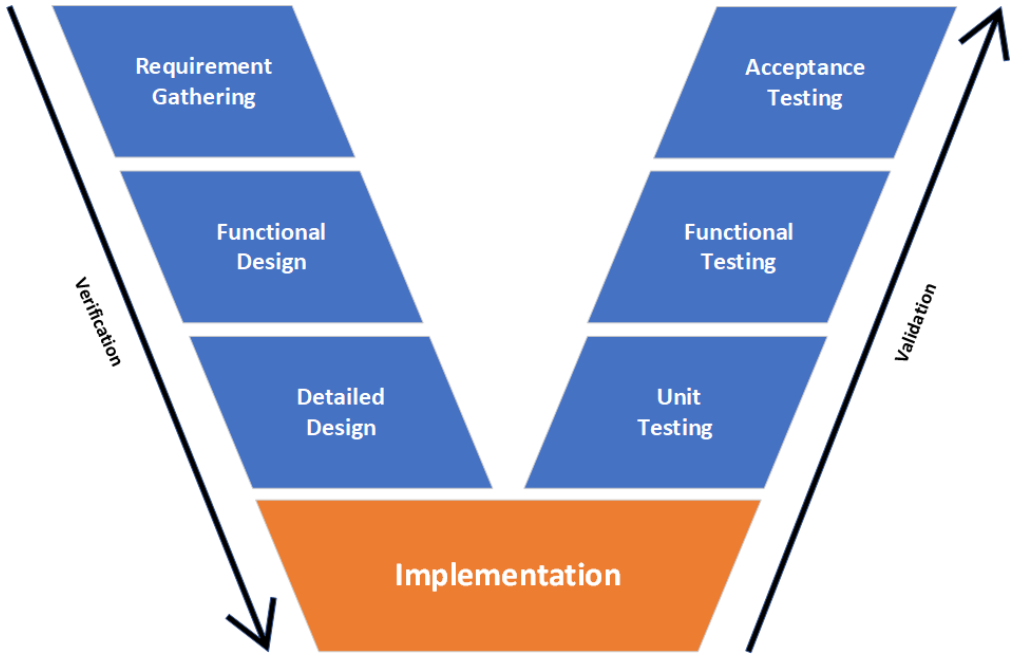

Figure 2.1: Verification and Validation flow chart.

2.1.1.1 Requirement Gathering and Acceptance Testing

The first step in the verification process, known as Requirement Gathering, is to gather and document the model requirements that set the bounds of necessary operation. Determining these requirements involves looking at the use-cases that the model is intended to capture. The question that should be answered here is, "What will this model be used for?" As an example, if a spring needs to be modeled, the defined use case of the spring must be well defined. Among its countless uses, a spring can be used as a shock, an oscillator, a damper, or even a scale. In these cases, and others, the spring may have a heavy compression force, but a light decompression force. If this were the case, there would be no sense in modeling a fast transient decompression. A spring typically has a symmetrical

compression and decompression, but if that were not the case, accounting for the differences would be important. A consideration might be the heat irradiated from the spring. In the case of a scale, this is probably not of much interest, but if it were a shock, the accumulated heat from the repetitive compression and decompression might be important to model.

Considering a spring in a hanging scale, the spring in question would be inside of the scale and in this situation, only the force of the decompression is of importance to the model. In a typical table scale, the compression force would be of interest. The next consideration is the quantification of the requirement, i.e., how accurate does the model need to be and this depends on the use case. A high-quality scale that has the precision of 1 mg, will require a more accurate model than one with the precision of 10 kg for example. At the end of the day, the accuracy and precision requirements are up to the designer to define based on their reason for creating the model.

In the Acceptance Testing stage of the validation process, an analysis of the model's ability to meet the defined requirements must be performed. This is achieved by comparing the model's result for each parameter of interest against the requirement assigned to it. For example, if it is required that the output impedance of a component be modeled to within 1% of the hardware's real value, the model must be run, and the output impedance must be compared to the real value to see if the accuracy is acceptable.

2.1.1.2 Functional Design and Functional Testing

During the Functional Design step of the verification process, a high-level overview of the model is put together by laying out the major modules of the system. An

example is a simple overview schematic. In a typical circuit, this phase would not include the individual circuit components but rather a high-level diagram showing all the modules that make up the system. This exercise sheds light on the interconnection methodologies required to operate the full system.

In the modeling of a power electronic converter, the controller becomes one of the key features that must be understood in this step. The controller must be modeled, and it can be incredibly difficult to do so, especially when it is coded and is not physical hardware. The functional design phase, with its birds-eye view of the system, is a useful place to conduct controller analysis and design.

During the Functional Testing step of the Validation process, experiments are planned. These experiments are used to evaluate the operation of the functional designs and the interconnection of the system(s) is/are evaluated. The detailed design phase will take care of the internal components within a module and ensuring the modules operate as expected, but the function design phase must ensure they are actively working together as expected. The individual modules that are designed as part of the functional design phase are tested based on their individual requirements. Testing the individual modules ensures their proper operation and that their future interconnection can be achieved. In other words, each module is tested against its expected operation to make sure it behaves in a way that is coherent with the needs and expected input/outputs of other connected modules. In the electrical domain, this often amounts to testing each module as a ‘two-port network’. Accomplishing this involves designing a set of tests to run on each module to evaluate the input and output characteristics. These tests will be run after the implementation stage as a step in the validation of the model.

2.1.1.3 Detailed Design and Unit Testing

In the Detailed Design step of the verification process, low-level design takes place, and this is the last step before the actual modeling effort begins in the Implementation step. A deeper dive into the relevant modules as described in the previous section is often of interest. Breaking down what extra pieces may be necessary in the implementation of the model is key to this step.

It is in Unit Testing step of the Validation process where the first evaluations of the model's performance occur. Each individual module must be studied and compared against its defined requirements before it is assembled as part of the larger system. Examples of the components to be studied in this step may include an input filter, internal rectifier, or output transformer for example. In the electrical domain, this often amounts to testing each module as a 'two-port network'. Accomplishing this involves designing a set of tests to run on each module to evaluate the input and output characteristics. These tests are run after the implementation stage as a step in the validation of the model. Naturally, the tests will vary based on the requirements of the module under study. Since the designs of these modules is largely taking place in this Detailed Design step, it makes sense to develop the validation tests in this section of the V&V process.

2.1.1.4 Implementation

During the implementation phase, the modeler must assess all the requirements and designs that have been defined and finally determine how the model will be implemented. Often there are many ways that the model can be implemented, and it becomes a challenge to identify the one whose pros outweigh its cons. In the work performed here, three

different approaches were studied and considered. Those will be briefly described here. Ultimately, a process known as system identification, using neural networks, was chosen to develop the models.

Transfer Function

Transfer functions are regularly used in control theory as they are a way of linearizing mathematic operations. As will be shown later, each of these methods requires knowledge of the input and output vectors of the system. These vectors need to be domain translated, usually using the Laplace or Fourier transform. Transfer functions typically follow Equation (1) where the output, $Y(s)$, is found by multiplying the transfer function, $H(s)$, by the input signal, $X(s)$. With knowledge of the input and output, $H(s)$ can easily be determined algebraically by dividing the output by the input.

$$Y(s) = H(s)X(s) \tag{1}$$

Transfer functions are extremely useful in their domain. The utilization of transfer functions was initially postulated for this effort as an effective solution for developing a system identification model. Transfer functions, however, are single input, single output (SISO), and power electronics are not. Though there is a single control signal, the models also rely on other inputs. This includes, but is not limited to, input and output voltage and input and output current. Some of these vectors are inputs and some are outputs, but the system is not SISO. Multiple transfer functions could be employed; however, this could

potentially involve a large amount of trial and error and algebraic loops. Due to the SISO restriction, transfer functions were not used to develop the models here.

State-space Analysis

State-space analysis is used to create a linear representation of the various states of a system. The benefit of this method is the ability to represent multiple states at the same time, unlike the SISO limitation of the transfer function model. This methodology can be done in several ways. The first is to take the system and develop state equations from known behavior of the system. This means knowing the mathematic equations of the system being modeled. It is incredibly useful for well-defined systems where the model developer knows most, if not all, relevant characteristics of the system. This poses an issue in the systems of interest in this effort since not all characteristics are known.

Another method of developing a state-space model is to create a state-space equation representing the 'generic' operation of the system. Then, using other methods, a compensating state-space or other mathematic model can be developed. Less knowledge of the system is required, and it allows the modeler to adapt other models to their specific use case. There is a reduced element of starting from a complete unknown. Iterative methods can be used to develop a black-box model of the system from input and output data. The state-space method was considered initially but became difficult because of some of the nonlinearities of the power electronics modeled here. It was eventually abandoned in favor of using neural networks as will be discussed next.

Neural Networks

In recent years, neural networks have become a popular buzz word in the computer and tech industry. Neural networks attempt to mimic the information networks of the human brain on a computer to model a system. This enables the computer to recognize patterns and solve problems using methods that are not readily apparent [15]. A collection of layers including an input layer, hidden layers, and an output layer, are connected and weighted within the neural network to make decisions and predict the output based on the input. Figure 2.2 shows the structure of a neural network.

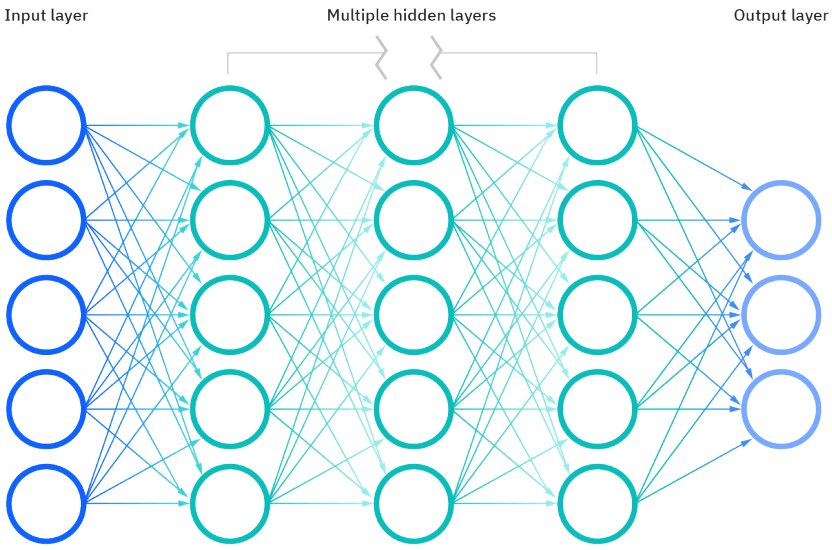

Figure 2.2: Connection diagram depicting the structure of a neural network used to solve problems and recognize patterns [16].

The neural network takes the inputs and outputs of a system and feeds them through a machine-learning-algorithm. A few examples include gradient descent, Levenberg-Marquardt, and conjugate gradient. In conjunction with other behind the scenes machine learning techniques, these methods attempt to create a connection of considerations. They

then assign weights to determine how important each consideration or data point is to the determination of the output states.

Each layer takes in a data point or multiple data points to create a new piece of data that is then weighted and fed to one or more nodes that go through the same process. The layers between the input and output layers are called hidden layers. This is the magic a neural network is producing. The number of these layers determines the number of considerations that can take place. In determining the connections between these nodes, the network is identifying patterns and making decisions of how the input and outputs are connected. In general, the more training sets, or data points, are evaluated the better the model. This points to collecting ridiculous amounts of data to develop a perfect model. This is obviously time and energy consuming and reducing the data volume requirement is key. In many scenarios, a model is trained, with a dataset, then the designer determines of the model is has a good enough fit or needs more data points. In the implementation of step of the V&V process, this consideration will occur.

This method was initially considered because of its success in modeling nonlinear systems. Most of the power electronics here, on some level, have an element of nonlinearity that make them difficult to model because they are computationally intensive. A neural network would ideally be able to map these nonlinearities and transfer them into an element that can be solved mathematically in a software like MATLAB/Simulink to decrease runtime and reduce complexity of the modeling effort. This is what was chosen here after preliminary success.

CHAPTER 3

FULL CIRCUIT MODELING OF THE 1.2 kV TDK AC/DC CONVERTER

Ultimately, the goal of the UTA Pulsed Power and Energy Laboratory (PPEL) is to have a fully defined software model of the IDEAL testbed that has been put through a V&V process. Earlier in the discussion of the IDEAL testbed, several commercially procured power converters were discussed. Those were procured from TDK Lambda and though they were very gracious with their time and support of this work, they themselves did not have simulation models of their own supplies. They supplied circuit level schematics of the supplies to help but the controller was difficult for them to transfer to us, as well as specific component values that were unique to our supplies, and therefore modeling the converters is a challenge. The efforts taken to model the converters will be discussed here.

The first one discussed is the 1.2 kV AC/DC TDK power converter. The first approach taken involves attempting to model the full circuit using Simulink. This is achieved using the known electrical components and connecting them in a circuit simulation. If every component is accurately modeled, ideally a circuit level model representative of the real hardware is created. As this approach began, a wall was hit in the Detailed Design step that made it exceedingly difficult to continue. Several of the component values were unknown and components within modules were unknown making it difficult to accurately model the system. There are efforts that could have been taken to alleviate these issues, and move the full circuit model effort forward, but it was elected to halt the circuit modeling effort in favor of using system identification.

Despite it not being the approach taken, there were lessons learned and the rest of this chapter is dedicated to the process taken in the development of a full circuit model up to the obstacles observed in the Detailed Design step. As mentioned, there are potential methods that could have been used to overcome the obstacles and those will be discussed well.

3.1 1 kV TDK Full Circuit Model Verification

The first converter discussed is the one that converts 480 VAC, 3 phase, to 0 – 1.2 kVDC. As described earlier, the main use case of this converter is to buffer power between the main 480 VAC generation bus and the 1 kVDC bus that sources one of many transient loads. It is also used to recharge the battery in steady state mode and to supply transient vital loads so those use cases must be considered as well. This means that the model must be able to represent the converter's transient level response. Once completed, it will be used within the larger system level model to develop and study relevant control architectures that are intended to improve AC power quality. Initially, since quite a bit of circuit level detail was provided by TDK, an attempt was made to utilize it to develop a component level model of the converter. As will be shown, the lack of controller and component knowledge made this approach very difficult. This chapter will discuss the 'full circuit' model approach taken to achieve an accurate and effective model. The V&V process described earlier is utilized. Creating a full circuit model requires a full schematic. Working with TDK Lambda, a good portion of the full system schematic was obtained, seen in Figure 3.1.

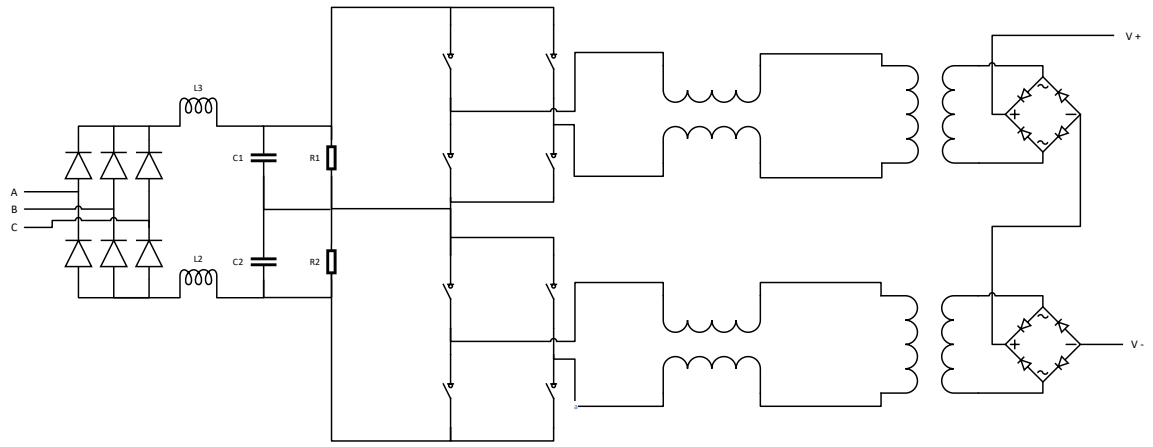

Figure 3.1: 1 kV TDK AC/DC baseline schematic consisting of a front-end rectifier, positive and negative bias, two inverters, chokes, and output rectifiers.

3.1.1 Requirements Gathering

The 1.2 kV converter has several use cases that guide the requirements definitions. To obtain improvement of AC power quality, the converter's output must be able to follow pre-defined ramp-rates and patterns that will mitigate transient effects on the AC generation. The 1 kVDC battery fills in the remaining power not supplied by the generator. The buffering use case requires the model to effectively track the on/off ramping, rapid on/off transitions with minimal ramp, and steady-state scenarios. The metrics being used for evaluation are seen in Table 3.1. The accuracy requirement is imposed on the output current as the input voltage is determined by the generator and the output voltage is determined by the battery. Using output current as the controlled value, it is the logical vector to evaluate accuracy against. The input voltage, input current, and output voltage are all studied to ensure they match the experimental data and to rule out any extraneous modeling error, but the output current is the main parameter of interest. MIL-STD-1399 has a voltage tolerance component as seen in Figure 3.2. From the 'User Voltage Tolerance Average Line-to-Line Voltage' to the 'User Voltage Tolerance Average Line-to-Line Voltage', there is an approximate 2.15% deviation. This metric was used to put an upper

limit on how the requirements of any of the model would be defined. To ensure this was always met, a 1% tolerance was enforced, giving plenty of head room for anyone using the models.

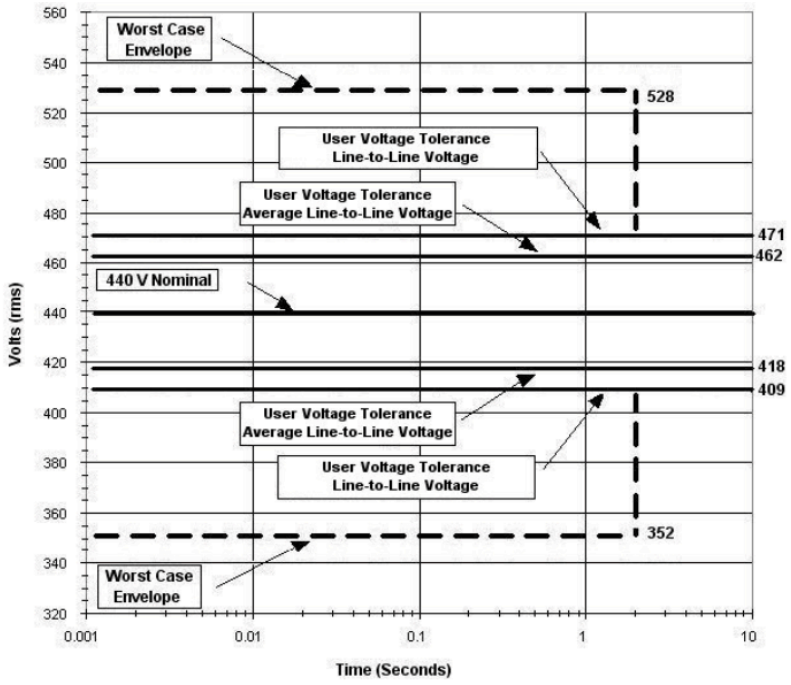

Figure 3.2: MIL-STD-1399 graphic showing the acceptable voltage deviations based on length of time the deviation occurs [17].

Table 3.1: 1 kV TDK Requirements

Parameter	Requirement
Steady-State Following	Within 1% Error
Ramp Rate	Within 1% Error
Square Pulse	Within 1% Error
Impedances	Within 1% Error

3.1.2 Functional Design

During the Functional Design step, the high-level schematic is explored to identify sub-modules and determine the interconnection requirements of them within the broader system. In this phase, the controller jumps out as glue that links all the modules together. With the full schematic laid out in Figure 3.1, the scope of the components that must be modeled can be seen. This is the full extent of what can be created using the schematics supplied by the manufacturer, however, these are only a few of the actual components that make up the supply. There are several components that surround the switches that are not known and all of these impact the way the controller behaves.

3.1.2.1 Control Framework

Outside of physical components, the control methodology is also unknown. This is a challenge, but not knowing the specifics may not be of dire importance. The focus of the 1.2 kV converter model is on larger scale operation, not in the 10 kHz+ range of the controller's switching frequency. This reduces the effect and reliance on a perfect model of the controller. As with most switch mode converters, some form of pulsed width modulation (PWM) is used and in the case of the 1.2 kV converter, a simple duty cycle adjusted PWM is assumed in favor of other topologies such as phase-shift modulation. Based on the use cases of the supply and model, a very simple control that follows the overall shape of the behavior of the converter can be used. A simple series PID controller was used to control the duty cycle of the inverter switches. The implementation of this controller is seen in Figure 3.3.

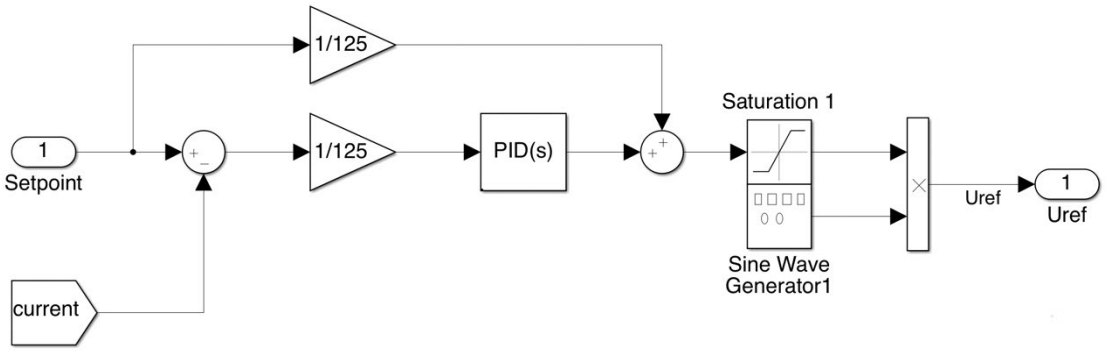

Figure 3.3: Simulink implementation of a PID controller setup as designed for the 1.2 kV converter.

3.1.2.2 Functional Test Design

The functional tests designed here are intended to examine the controller's behavior. The steady-state, ramp-rate following, and pulsed responses are of interest. The main determinant is the model's ability to match the hardware's output current under all ramp rates of interest. In the testbed, the converter must supply power from the generator to a transient load. Adjusting the power transfer ramp rate enables the generator's power quality to be improved. It is critical that the 1.2 kV converter's ramp rate be accurately modeled so that studies can be performed to understand at which ramp rates the power quality is improved and where it has little effect. The specifics of what required ramp-rates are needed to improve power quality using the 1.2 kV converter are not yet known but the converter has been experimentally tested across a slew of different ramp-rates to bound the problem

This tests the boundedness of the controller and evaluates its ability to follow the profiles it must supply in operation. The accuracy of the controller will be fully tested in the acceptance testing step. As such, the focus in on validating the controllability and ensuring the controller settles on the desired set points. A series of tests that are intended

to emulate the model against real use cases is planned. This will evaluate the capability of the system to follow the controller input signal and behave as expected in a controlled environment.

Pulsed Test

There are conditions where the generator may need to quickly supply transient loads that turn on and off rapidly. In these cases, it may not be feasible to ramp the generator and power quality may have to suffer in favor of ensuring critical loads are met. This condition must be accounted for, and the model must be capable of accurately capturing this scenario. In this case, the output current is limited by the converter's own internal slew rate limitations, such as the hypothetical example shown in Figure 3.4, and that must be quantified and mapped properly. Current set points are sent to the converter and the resulting output informs the modeler of the limitations of the supply.

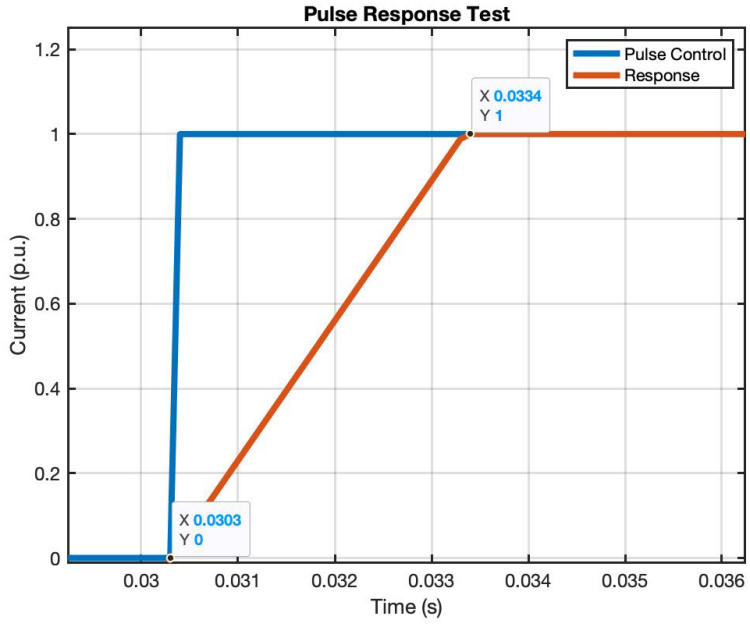

Figure 3.4: Plot showing the expected response of the 1.2 kV to a pulse control reference signal.

There is no ‘slowest’ ramp rate so the requirement falls with characterizing the ‘fastest’ ramp rate the supply can achieve. The supply has been experimentally studied to observe the fastest ramp-rate it can achieve, and the model must be able to mimic that performance. It is not possible for the supply to instantaneously change its current but if a transient control signal is applied, the power supply’s response to it will define the fastest ramp rate it can achieve, seen in Figure 3.5 below. This data suggests that the fastest possible ramp rate is around 340 A/s. The model must be capable of predicting this ramp rate response within 1% for the model to be accepted. A suite of experiments is run against the model to measure its accuracy, exploring each of the parameters in Table 3.1.

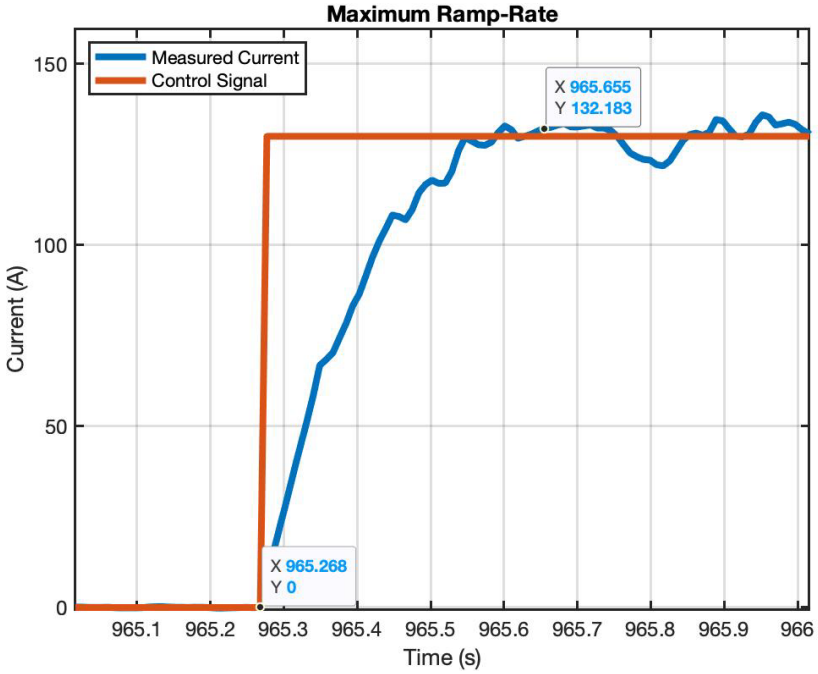

Figure 3.5: Ramp rate response of the 1.2 kV converter when supplied with a delta input control signal.

Ramp Rate

Ramp-rate experiments involve evaluating the converter across a spread of different ramp rates, beyond the minimum shown earlier, that further highlight the expected

use cases the hardware is expected to operate at. When slower ramps are studied, more test points are collected that can be used to compare the results against. Each ramp test includes a rising ramp and a falling ramp to characterize any hysteresis. A low ramp-rate of 1 A/s needs has been tested and a higher 100 A/s will be evaluated as well. Three different current saturation points that the ramp rises up to have been studied and the model's ability to capture the correct overshoot behavior, if there is any, is of interest.

Table 3.2: Ramp-rate test cases for the 1 kV TDK AC/DC converters.

Ramp-rate	Test 1	Test 2	Test 3
1 A/s	25 A	50 A	80 A
10 A/s	25 A	50 A	80 A
20 A/s	25 A	50 A	80 A
50 A/s	25 A	50 A	80 A
100 A/s	25 A	50 A	80 A

Steady State Test

Steady state experiments are designed to prove that the system follows the steady-state behavior of the physical hardware. In these tests, the supply is supplied with a specified reference control signal that is held constant for some period, seen in Figure 3.6. The control signal was held at 20%, 40%, 60%, 80%, and 100% of the supply's ratings. When supplied with these reference control signals, the model's output signal must maintain 1% accuracy when compared to the physical hardware's output current while both are held constant.

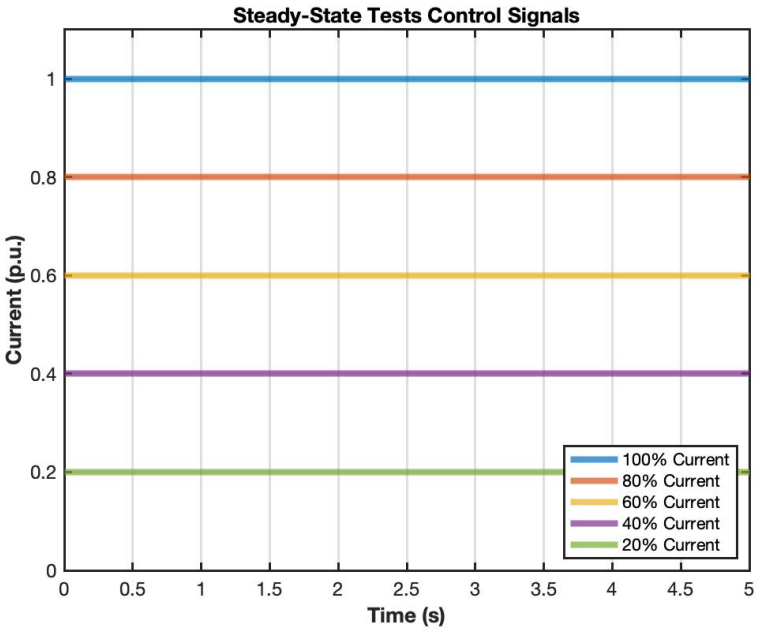

Figure 3.6: Plot depicting the control signals that will be fed into the 1.2 kV converter to evaluate the model response to a steady-state.

3.1.3 Detailed Design

The detailed design step focuses on individual modules that can then be broken up into several pieces and further simplified to reduce model complexity. The result is improved simulation stability and run-time. Before simplification, the system must be fully understood. A few examples are listed in the coming sections but before discussing these, it is important to remember that this step in the V&V process is where roadblocks were hit while using the circuit modeling approach. When consulting the schematics, three are several modules that make up the 1.2 kV converter that all have several components in them and not all of those values are unknown. Some modules contain components that are not actually even shown in the schematics. This limits the effort to produce a full circuit model because pieces of the model are unattainable. If the effort were to move forward, the 1.2 kV converter could be opened up and examined to get the component values by

inspection or through measurements, i.e. an LCR meter to measure a capacitor. This is unfortunately not worth the effort when other approaches are available. If is done properly, the schematic could be completed, and an accurate circuit model could be made. For this reason, this effort was abandoned but the reset of this chapter is devoted to better understanding what is missing.

3.1.3.1 Input Rectifier

Considering the schematic in Figure 3.7, the 1.2 kV converter's input full-bridge rectifier is supplied with 480 VAC, 3-phase and its output is filtered and biased. The two choke inductors and capacitors filter the ripple associated with diode rectification. The two resistors act as dividers to split the newly made DC bus into a positive and negative bus with a center common node. Splitting the bus reduces the size of the transformers and the insulation requirements. This creates two branches that are combined in a later stage. Before that combination, the two branches feed into two identical inverters. At this point the component values must be considered to mathematically determine the expected output of the input rectifier. As has been stated, several values are missing. It is speculated that this is either a proprietary consideration, or stems from a tuning effort where the values are hardware dependent. In this case, the diode type is not known, so the diode voltage drop cannot be modeled. This could ideally be removed from consideration based on the relatively small drop across diodes, but that has to be proven. Additionally, the choke inductance is unknown, potentially drastically changing the ripple on the output of the rectifier. These are just a few examples of the unknown components.

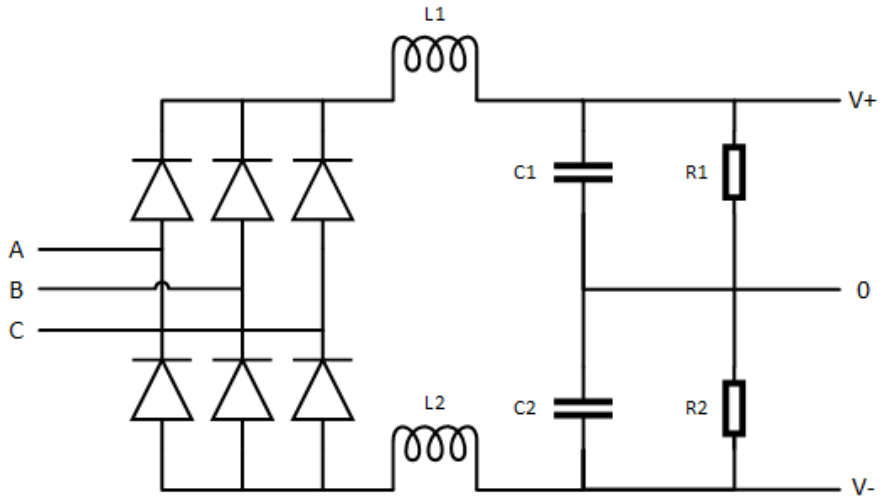

Figure 3.7: Detailed Schematic of the Input Full-bridge Rectifier of the 1.2 kV TDK AC/DC Converter.

3.1.3.2 Inverter and Transformer

The split bus from the input rectifier and bias circuit feeds multiple inverters and transformers. Figure 3.8 shows the connection of the inverters to the transformers through a pair of chokes. The on/off nature of the switches creates large peaks in voltage across the transformer due to the voltage current relationship of inductors and their inherent desire to restrict changes in current. The mutually coupled chokes are used to reduce noise stemming from this operation of the inverter. The choke and transformer values are unknown, and this is problematic. Ideally, the transformer ratio can be back calculated, assuming other parts of the system are known, but the impedance and saturation characteristics are unknown. The same thing goes for the chokes which could pose a significant voltage drop across them. Changing the values forces a different calculation on the transformer turns ratio creating two unknowns with one equation. If the effort were to continue, these would have to be manually measured from the hardware system.

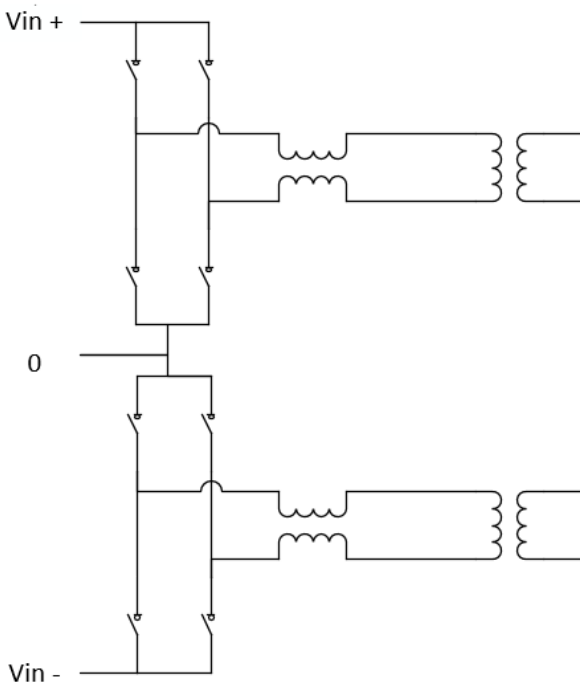

Figure 3.8: 1.2 kV TDK Inverters feeding into mutually coupled chokes then step-up transformers.

3.1.3.3 Output Rectifier

The output rectifier makes up the last power module discussed. Each transformers' output is connected to a full-bridge rectifier and those are connected in series to produce the full DC output voltage up to 1.2 kV. This is shown schematically in Figure 3.8. The secondary side of the transformer is relatively well known so the only remaining components are the output diodes and the input diodes, which are not known. Not knowing the diode type is not concerning since the diode drop is small and can be worked around. There must be some form of current sense happening in the output stage, but it is not clear from the schematic how that is achieved. A current measurement could be done in any number of ways and if it is not isolated, it would need to be considered to properly develop an accurate circuit model.

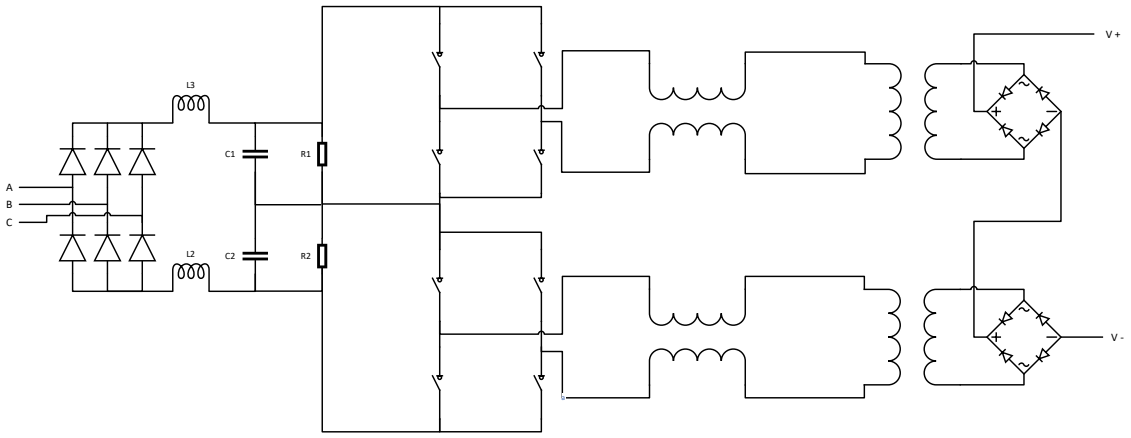

Figure 3.9: 1.2 kV TDK AC/DC baseline schematic consisting of a front-end rectifier, positive and negative bias, two inverters, chokes, and output rectifiers.

3.2 Model Discussion

Though results are not shown, there was considerable effort put into trying to make the circuit model approach work. Not having all the component values and not being able to take apart the supply to characterize those values is problematic. Had the supply been able to be taken apart and characterized, this method would have proved more valuable but funds simply were not available to take that risk. This type of modeling works very well if full knowledge of the system is known.

CHAPTER 4

1.2 kV TDK AC/DC SYSTEM IDENTIFICATION MODEL

While the circuit modeling approach has some advantages, it's not always a straightforward approach to capturing all the phenomena that needs to be captured. An alternative method known as system identification modeling is a way to model a system about which not much is known. This 'black-box' modeling approach requires minimal knowledge of the internal circuit to develop a model that is faster and requires less information. Even though much is known about the 1.2 kV converter beyond what was presented earlier, the V&V process can be completed using this approach.

4.1 1.2 kV Converter System Identification Model Verification

4.1.1 Requirements Gathering

The requirements remain the same as they were when the circuit modeling approach was taken, as listed earlier in Table 3.1 and again here in Table 4.1. As depicted earlier, the accuracy requirement is still held at 1% MIL-STD-1399 tolerance.

Table 4.1: 1 kV TDK AC/DC Converter Requirements

Parameter	Requirement
Steady-State Following	Within 1% Error
Ramp Rate	Within 1% Error
Square-Pulses	Within 1% Error

4.1.2 Functional Design

So that the model can be interfaced with other component level models, it was determined that the model must be able to work with the MATLAB Simscape Electrical library. Controlled voltage and current sources, like the ones shown in Figure 4.1, are used to turn the System Identification model into an electrical model that works with other

circuit or similarly designed models. The explicit connection of these to the neural network that is used to train them is not known at this point in the verification process as it will not be defined until the detailed design phase. At that point, the framework of the neural network is established, and its basic connection topology is similar to that shown in Figure 4.2.

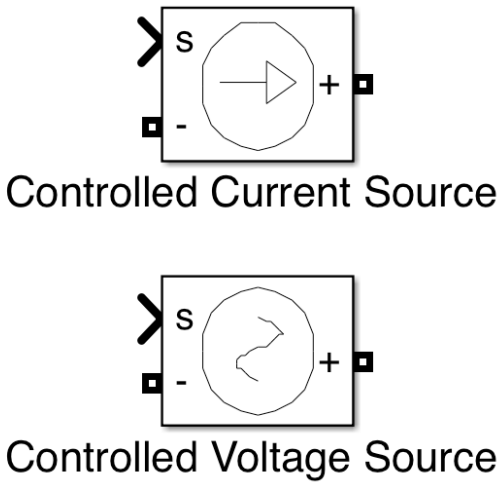

Figure 4.1: Simscape Electrical Controlled Current (top) and Controlled Voltage (bottom) sources for translating numeric signals to electrical ones.

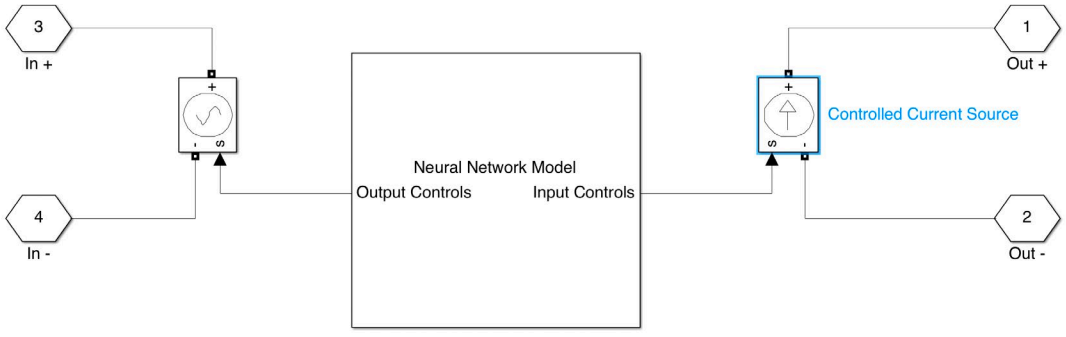

Figure 4.2: Potential connection between the neural network module and the electrical sources at the input and output.

4.1.2.1 Functional Test Design

Eventually, the model of the converter must be evaluated against data collected from the real hardware under the use cases the model is being designed to emulate. A series of experiments are defined to compare the fully integrated model to. The model will be run against the same functional tests as the circuit model defined earlier. These include varying ramp rate, rapid on/off, and steady state conditions.

4.1.3 Detailed Design

Having a high-level design is key to understanding how the 1.2 kV TDK supply operates so that a model can be defined. As shown earlier, there are many specifics that are not known. To fill the void of these unknowns, system identification protocols and principles of mathematics are employed to fill in the knowledge gaps. Assuming the converter has efficiency η, Equation (2) must hold.

$$p_{in} = \eta\, p_{out} \tag{2}$$

Knowing that electrical power is calculated using $p = vi$, it is readily apparent that there is a connection between the output voltage and current and the input voltage and current. The additional puzzle piece is in the control signal as it determines the desired output, and how the controller responds to that control signal is the problem that must be solved. The five main variables governing the model are the input voltage, input current, output voltage, output current, and control signal. The model intends to solve the relationship between these variables.

The 1.2 kV TDK AC/DC converter is designed to be a current controlled capacitor charger, so it makes sense to have the output current as the primary model output. Because it is a current controlled device, the output voltage is not controlled by the converter but is instead dictated by the current sourced and impedance of the load. This means that the output voltage should be a model input because it is determined by outside systems. The same logic can be used to predict the input voltage and current. The input voltage of the converter is regulated in IDEAL by the 480 VAC bus. This makes the input voltage an external factor of the converter, and thus an input into the model. Since the input power of the converter is determined by the output power, the input current is determined exclusively by the output power and system efficiency making it a model output. The actual relationships, including input and output impedances, ramp-rate, efficiency as a function of power supplied, ripple, transient recovery, and others, are not yet captured. These things determine how the actual system behaves when applied with certain stimuli. The Implementation section will delve into the system identification steps employed to capture these deeper characteristics of the system.

4.1.3.1 Detailed Testing Design

As described earlier in the full circuit approach description, a series of experiments must be defined to compare the model against the controlled evaluation of the physical hardware. In the model, a mathematical relationship is being developed. Testing this version of the model involves evaluating the model with a test data set to check its performance. Obtaining this data set can be achieved using two different methods. Data can be captured from the real connected systems, or representative data of potential inputs

and outputs can be used. The former method is the most reliable because it reduces the need to individually create data that may not be representative what the real hardware might produce. When defining the system identification models, a significant amount of data is required to ensure every use case is accounted for. For every test case that is experimentally performed using hardware, multiple experiments should be performed to train the model against. Representative data from the ramp-rate, steady-state, and pulsed on/off loads must be collected and compared against the model's output.

In some cases, the model with the lowest mean-squared error (MSE) model may not be the best choice due to a phenomenon called 'overfit'. Overfit is when the neural network is able to determine a connection or pattern in the training set, but it does not predict future behavior well [18]. This essentially means the model will not work well in predicting system behavior with data that is not exactly like the training set. Figure 4.3 shows a visual representation of underfit, good fit, and overfit. A model can become overfit for several reasons, but the main factor is using too many hidden layers such that the pattern followed is specific only to the data used to train the model.

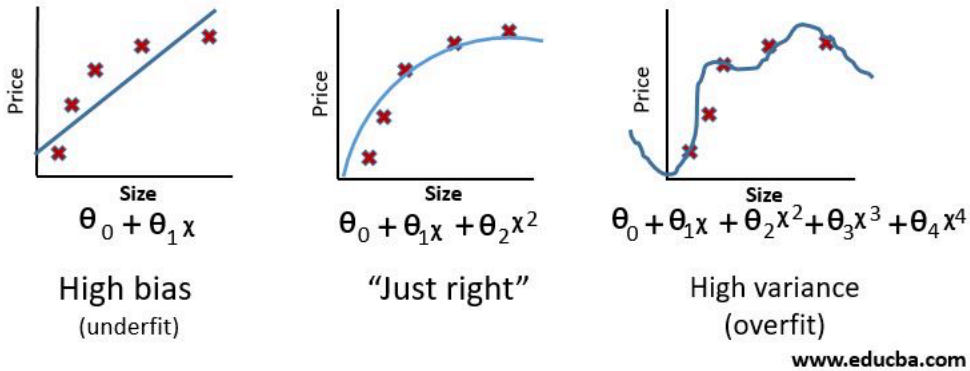

Figure 4.3: Examples of the types of fits a neural network can display. The left graph shows an underfit, the right graph shows an overfit, and the center shows a good fit [18].

As touched on earlier, having excess test data is useful so that it can be used to test the model for overfit. Ideally, some of the data collected during the training process is used for training and some is held for testing the model's behavior. This routes out any overfitted models when their output is significantly different than expected. No examples of overfit are shown here since the problem has not been widely experienced using the current algorithm. However, the reader may be interested to know that during the initial testing, before the final model input and outputs were selected, models that were developed to test the algorithm showed promising MSE results but poor predictive quality. Anyone who wishes to explore this algorithm should be wary of overfitting even though it is not pervasive here.

4.2 Implementation

Though the purpose of using the system identification method to develop a model is to eliminate the need for a deep knowledge of the device being measured, the full circuit model effort does provide some useful information. Exploring the circuit method on the 1.2 kV converter uncovered a significant amount of information about the internal components and construction of the system that might not have otherwise been known. The converter's non-linear behavior is evident throughout its topology. The use of capacitors and inductors on the front end and output rectifiers introduce non-linear behavior. The inverter switching mechanics exacerbate this problem as well. It is always helpful to know that non-linearities can become a problem when using system identification. The lack of internal knowledge makes it very difficult to develop the mathematical n^{th} order equations relating the internal components. Fortunately, there is a method of system identification that aids in determining non-linear system behavior.

An artificial neural network (ANN) is an example of machine learning that takes information, and helps the computer generate an output based on its knowledge use of example data. Machines utilize neural networks and algorithms to help them adapt and learn without having to be reprogrammed. Neural networks mimic the human brain, where each neuron or node is responsible for solving a small part of the problem. They pass on what they know and have learned to the other neurons in the network, until the interconnected nodes are able to solve the problem and give an output [19]. The key to neural network modeling is gathering a large sample size of data. Neural networks are incredibly effective at predicting behavior based on the training data set if enough data is collected and if it is collected from the physical hardware employed in use cases representative of its end use. Because the hardware is physically in place, this is easily accomplished using the 1.2 kV converter that is installed in the IDEAL testbed. It can be tested under the pulsed on/off, ramp rate, and steady state conditions it is intended to be used in to gather sufficient training data. A small sample of the data collected for each use case was presented in Figure 4.4.

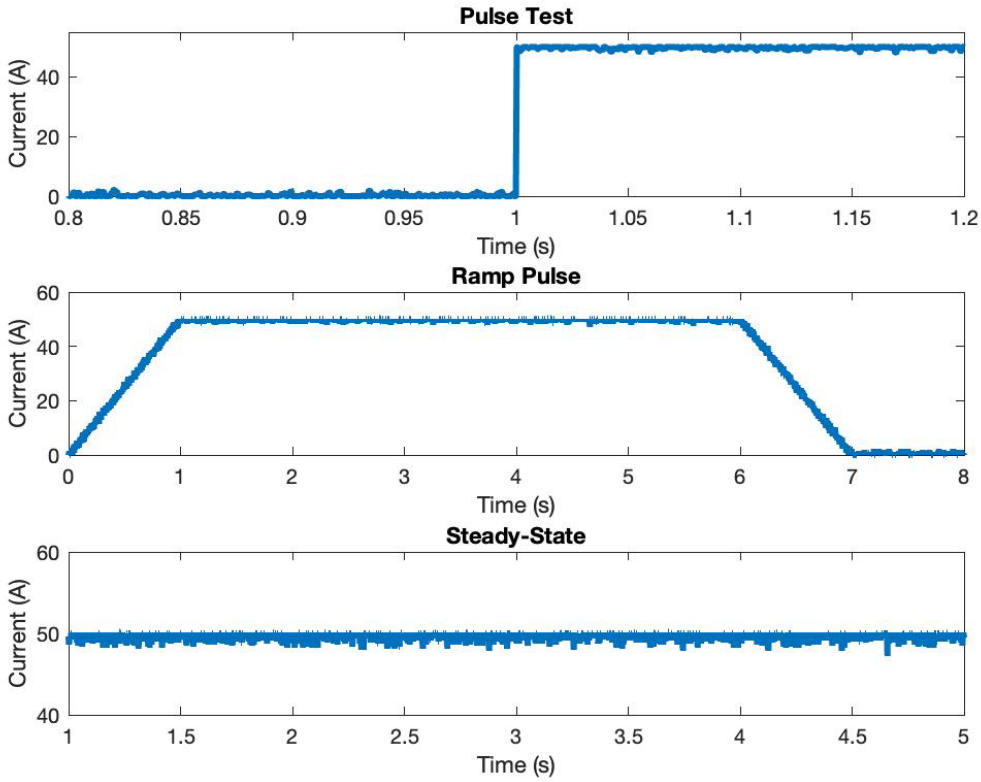

Figure 4.4: Sample use case data representing each of the defined use cases that will be fed into the neural network algorithm for the 1.2 kV TDK AC/DC converter.

4.2.1.1 Custom Neural Network Model Generation Algorithm

It takes considerable time to create the neural network model and it can become complicated quickly. A model generation utility was developed here to track model development, increase accuracy, minimize the complexity, and minimize the time required. The algorithm was compiled using MATLAB and allows for repetitive and consistent development of neural network models. The algorithm has been tested and proved effective at generating models using transfer function, steady-state models, and even polynomial models.

Signal Conditioning

The training data that is collected is not immediately ready to use for training. MATLAB is used to develop the neural network model and accomplishing this requires the data to be in the proper format. Format is not a question of file format or extension, rather a more specific condition of vector size and shape. The IDEAL testbed utilizes LabVIEW to sample and collected experimental voltage and current data. This section will not discuss the migration from NI LabVIEW to MATLAB but does discuss the conditioning requirements for model training once the data is in MATLAB as well as how the algorithm achieves this.

The first step in developing a system identification model is performed earlier in the V&V process. That step occurs when determining the training inputs and outputs. These are translated into a one-dimensional vector and in this effort, a column vector is used. Whether row or column vectors are used is irrelevant so long as they are all the same length. This step must be done for each input and output for every test. A row vector for input current will be generated for every use case experiment the model is to be trained on.

The algorithm developed for the purpose of conditioning and creating the model inputs is called the Data Formatter. This algorithm takes in the data collected during each experiment and creates a structure of the control and input and output voltage of the physical hardware. The model is trained all at once which means during training, every test must be examined. The Data Formatter connects each tests' inputs and outputs into single variables. Essentially, the output voltage of each test is stacked on top of each other to create a single output voltage variable. An example for the 1.2 kV converter's output voltage is seen in Figure 4.5.

```
kV1OutputV  = [     kV1Test1.Output_V;...
                    kV1Test2.Output_V;...
                    kV1Test3.Output_V;...
                    kV1Test4.Output_V;...
                    kV1Test6.Output_V];
```

Figure 4.5: Example of model input variable generation using the system output voltage.

In most neural network models, a measure of down sampling, filtering, and/or smoothing is applied to reduce computational complexity. Through the effort of developing these models, it was found that measurement noise at the power levels and switching frequencies the IDEAL testbed runs at can be very high, and it does influence the training data. The Data Formatter script applies filtering or smoothing as required. Performing these operations at the front end rather than during model training significantly reduces simulation time and provides measurable noise rejection as discussed in the model results section(s).

Once this is complete for each input and output variable, the next step is to combine the vectors into the training input and output data matrices. This effort is straight forward and conducted using very simple lines of code seen below:

```
trainInput   = [kV1Control kV1InputV kV1OutputV];
trainOutput  = [kV1InputI kV1OutputI];
```

Figure 4.6: Example of the sample setup of the training inputs and outputs for developing a neural network model.

The next segment of the model generation algorithm is the Iterator. This script iterates through different hidden node quantities set by the user and calls the Model Creator algorithm to generate a neural network model. The number of hidden nodes can initially be a wide window while the algorithm narrows down the path to the best model. Once that

is identified, the hidden nodes can be reduced to improve model quality. The Model Creator algorithm is where the actual model generation takes place. The script takes in training inputs, training outputs, and hidden nodes and then mathematically develops a neural network model. At the output of the Model Creator algorithm, a MATLAB object containing the trained neural network is created. This model is stored as an entry of a MATLAB cell until the completion of the Iterator script. At the end of the Iterator script, the model with the best MSE is identified.

Key Parameters

The output of the Model Generation algorithm also aids in model development by assisting in model development tracking. At the beginning of the Model Generation algorithm, before the initial run, there is an opportunity for the user to enter a set of parameters. These parameters include a smoothing window, number of points to down sample by, and the range of hidden nodes to evaluate. The algorithm displays each of these settings in a command window to alert the user of the current settings. The settings are also attached to the model during the Model creator step so that when the model is exported and chosen, all the relevant parameters are available. This is extremely helpful for model development and versioning. As an example, a large window of potential hidden nodes can be run with a large down sample value, which is reasonable, to narrow in on the window of nodes that will effectively model the system. Additionally, if the user desires to perform model retraining, this gives necessary insight to the system.

Results

At this point, the model generator algorithm is run to determine the best fitting model. For the 1.2 kV converter model 50 tests sets of each scenario are evaluated equating to 150 training sets. At the end of the algorithm, 24 hidden nodes were selected with a performance metric of 0.46 MSE.

4.3 1.2 kV Converter System Identification Model Validation

4.3.1 Unit Testing

The extra data mentioned in earlier sections is of particular interest during the Unit Testing step where the over-fit evaluation is performed. Various test data and their comparative results are shown and discussed below. In Figure 4.7, the results of two tests on the output current are displayed to confirm adherence of the neural network.

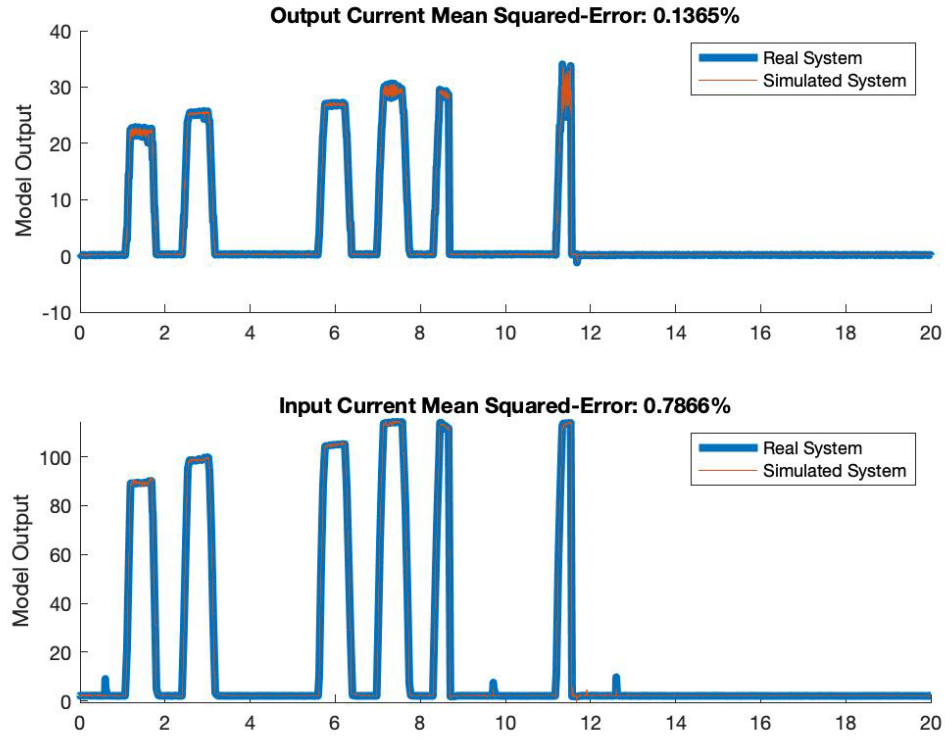

Figure 4.7: Plots showing the ability of the developed neural network model to accurately predict the model output using untrained data from the 1.2 kV converter.

From the untrained data set, there is excellent agreement between the model and experimental data. This is promising as it speaks to the controllability of the model. Additionally, the good performance on untrained data points to the model being a 'good-fit' meaning it is not overfit finding patterns only in the trained dataset. This is not enough to validate the model, but it is enough to validate the neural module and move to the connection of the neural model to the electrical sources.

4.3.2 Functional Testing

During the Functional Testing step, the electrical interface of the model is evaluated. The test data needs to be conditioned from numerical data into electrical signals. This is accomplished utilizing Simulink's Simscape Electrical library. A controlled voltage source is used to create a three-phase AC generation source that is fed into the 1.2 kV converter model. Depending on the experiment being evaluated, the electrical output can be supplied into a simple resistor, a battery, or another power converter feeding another load. Since the output voltage of the converter is a model input, it can also be used to set a controlled voltage source that receives power from the 1.2 kV converter model. The assortment of experiments described earlier can be seen with their comparisons in the following figures.

The first test is to evaluate the maximum ramp-rate using a square-pulse input as demonstrated earlier in Figure 3.4. In Figure 4.8, the front end of the square pulse illustrates the maximum ramp response from a step command. This is with a ramp rate of approximate 340 A/s which is spot on with the recorded value from the pulse test shown in Figure 3.5.

In Figure 4.9, the model is shown to effectively create ramp signals based on the control input. This demonstrates that the ramp rate of the model are following the responses it is commanded to do.

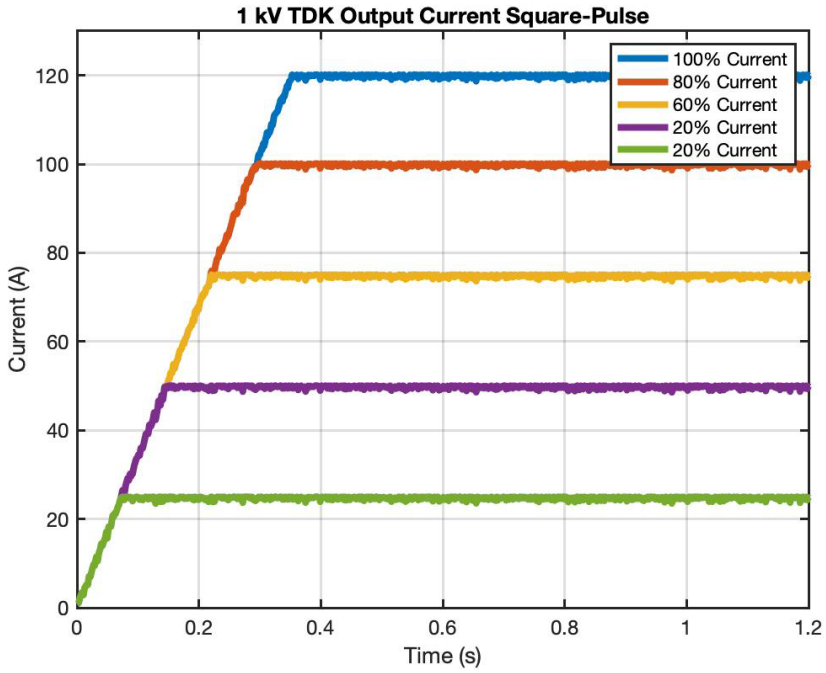

Figure 4.8: Plot of the output current response to input pulse test with varying peaks to illustrate the model's adherence to the maximum ramp-rate for the 1.2 kV converter.

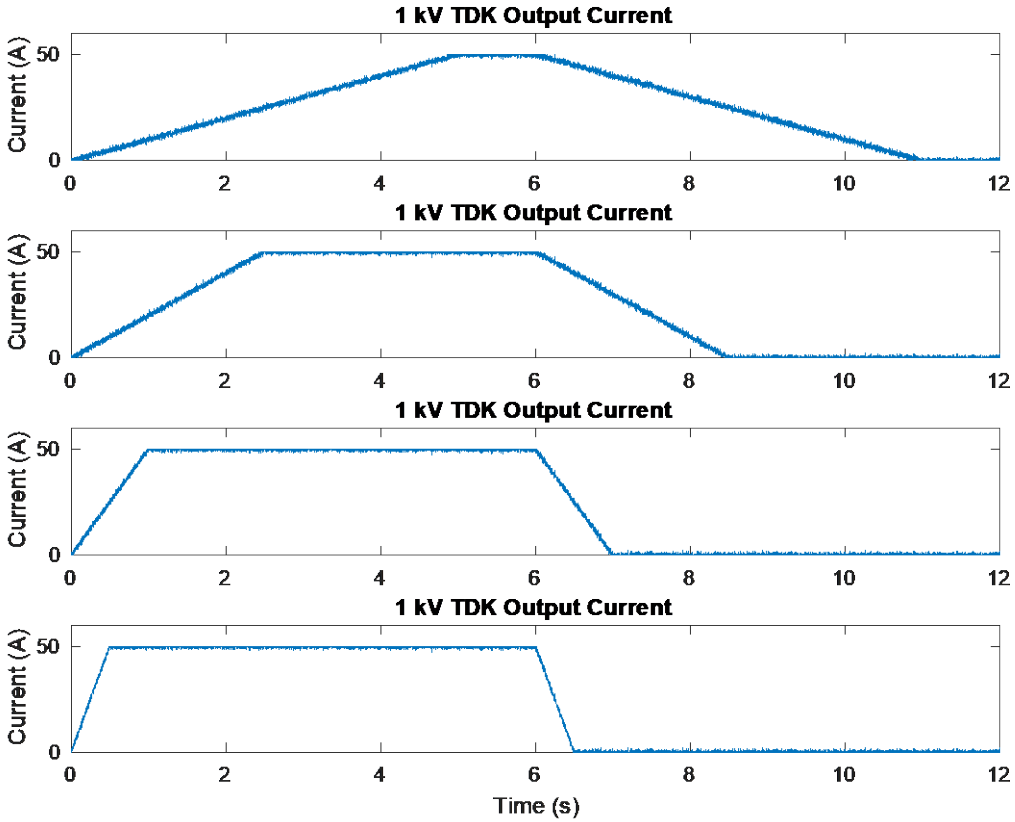

Figure 4.9: Plot showing the 1.2 kV model response to input ramp-rate pulses of 10 A/s, 20 A/S, 50 A/s, and 100 A/s ramp-rates.

4.3.3 Acceptance Testing

The model's performance is evaluated to show the validity of the model shown in Figure 4.10. Table 4.2 shows how the 1 kV model can track the physical hardware data, shown in Figure 4.11 very well. The model far exceeds the required percent error, suggesting the model is achieving its design requirements. These were tests run with the neural and electrical interface connected to other electrical components as they will in the full IDEAL model.

Table 4.2: 1.2 kV TDK AC/DC Converter Results

Parameter	Requirement	Performance
Square-Pulse	Within 1% Error	0.102% Error
Ramp-Rate	Within 1% Error	0.1365% Error
Steady-State	Within 1% Error	0.1187% Error

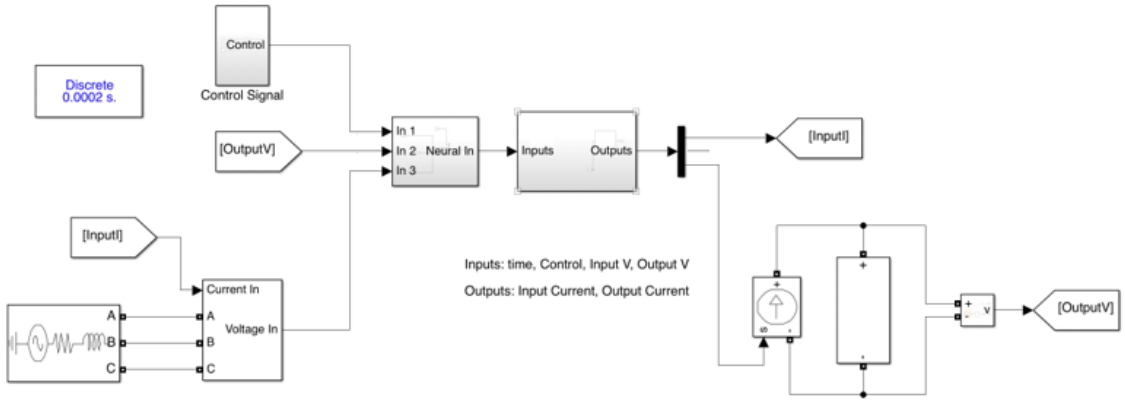

Figure 4.10: 1.2 kV converter model wired up electrically to a representative source and load.

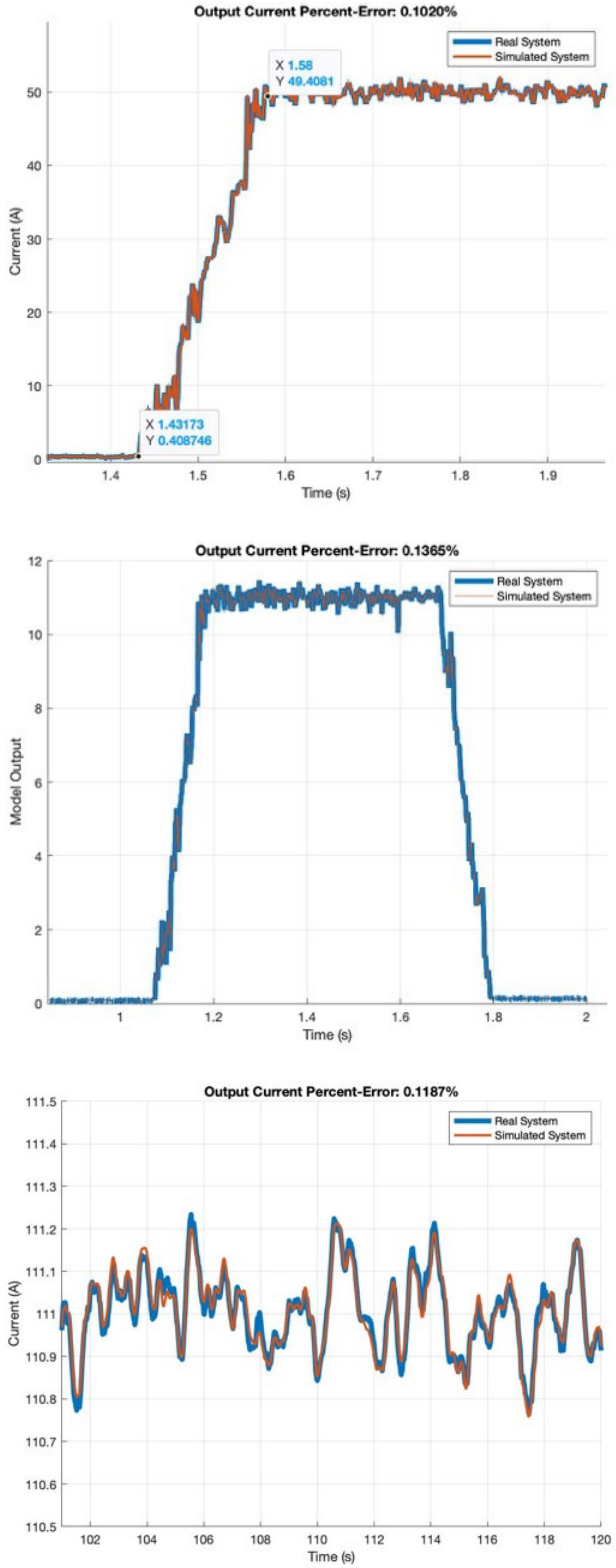

Figure 4.11 Plots of pulse, ramp-rate, and steady-state responses of the 1.2 kV converter model showing the validity of the model.

CHAPTER 5

12 kV TDK AC/DC SYSTEM IDENTIFICATION MODEL

A model of the 480 VAC, three-phase to 12 kVDC TDK converter has been developed in nearly the exact same way as the 1 kVDC TDK converter. The topology between these two converters is nearly identical with the biggest difference being the transformer ratio. The input of these converters is the same 480 VAC generation bus. The 12 kV converter's output is not buffered by a battery like the 1.2 kV converter or fed into a second DC/DC converter. Instead, it is supplied into a high voltage resistive load and as will be shown later, the load profile is largely square in shape with maximum ramp rate. That will change once the Unico inverter is operational since it will be possible for the battery to buffer that load like how it does the 1.2 kV converter. When reading this section, it will read nearly identical to the process used to develop the 1.2 kV converter model.

5.1 Verification of the 12 kV TDK Verification

5.1.1 Requirements Gathering

The 12 kV converter is designed and constructed the same way with the only differences being the transformer ratio and its internal dielectric standoff ratings. The use cases are slightly different for the 12 kV converter. It is used as a pulsed load source into a resistive load within IDEAL. There are limited cases in which this system will need to be ramped at this time. Instead, it is used more as a transient on/off supply. Table 5.1 shows the requirements table for the 12 kV TDK.

Table 5.1: 12 kV Converter Requirements

Parameter	Requirement
Steady-State Following	Within 1% Error
Ramp Rate	Within 1% Error
Square-Pulse	Within 1% Error

The resistive output load determines the output voltage based on the controlled output current and the input voltage that is governed by the generator. Making the choice to use output current as the primary output variable is the most logical. Each output will be evaluated to ensure adequate model behavior. The same 1% error accuracy requirement is enforced here, though the lack of battery buffer makes this converter behave mostly as a load. Because it is used as a transient source, its specific values are less important than its ability to tax the generator and maintain vital load.

5.1.1.1 Functional Test Design

The Functional Test Design is performed the same way it was in the two 1.2 kV converter model's functional tests. The neural network module is connected to Simscape Electrical blocks to evaluate the functional capability of the model. The integrated model is run through several ramp-rate, square-pulse, and steady-state control scenarios to validate the model's ability to communicate with the electrical interface

Pulsed Test

As was performed earlier, rapid rise experiments were performed to characterize the converter's maximum possible rise time. This is achieved by passing on the square pulse control signals presented in Figure 5.1 and observing the converter's own response to them into a resistive load. The resulting slew rate is the maximum achievable by the

hardware's own internal control loop. In this case, the maximum is again roughly 340 A/s. The model will have to show adherence to this maximum slope.

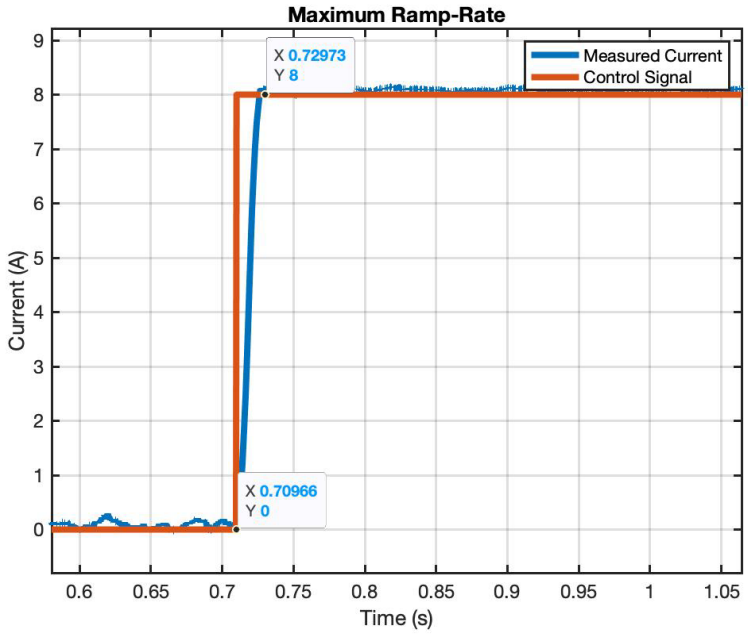

Figure 5.1: Diagram of the pulsed tests run on the 12 kV converter showing the maximum ramp-rate of the converter.

5.1.2 Functional Design

5.1.2.1 System Identification Model Functional Design

As did the 1.2 kV converter model, the 12 kV converter's model needs to connect electrically to any other components in the IDEAL model This is achieved using controlled current and voltage sources that translate the mathematical model into the necessary electrical systems. Because it is the same as described earlier, it will not be discussed further here.

Ramp Rate

Ramp-rate tests experiments evaluate the 12 kV converter's response to different ramp so that experimental data is collected to compare against the model. As in the experiments earlier, data has been collected from a range of ramp rates, listed in Table 5.2.

Table 5.2: Ramp-rate test cases for the 12 kV TDK AC/DC converters.

Ramp-rate	Test 1	Test 2
1 A/s	5 A	8 A
10 A/s	5 A	8 A
20 A/s	5 A	8 A
50 A/s	5 A	8 A
100 A/s	5 A	8 A

Steady State Test

Steady state experiments are designed to prove that the system follows the steady-state behavior of the physical hardware. The hardware was loaded for longer periods of time with the control output held constant. Loading conditions that are 20%, 40%, 60%, 80%, and 100% of its rated capability are performed. The control signals supplied to the model are shown in Figure 5.2.

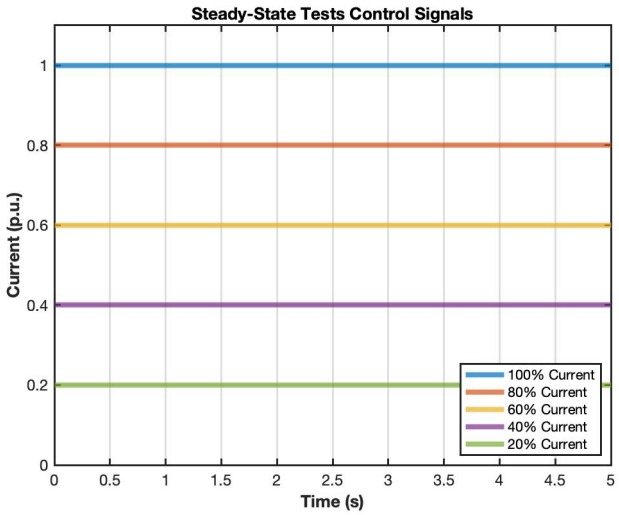

Figure 5.2: Plot of the steady state control signals sourced into the 12 kV TDK converter model.

5.1.3 Detailed Design

5.1.3.1 System Identification Model Detailed Design

The 12 kV converter's system identification model is designed the same way as the 1.2 kV converter's. The mathematical relationship between the input and output power, impedances, and other internal components govern the operation of the converter. Since the main electrical difference between the 12 kV converter and 1.2 kV converter is the transformer's turns ratio, it follows that the mathematical model should be the same as well with a few scaling changes. However, the change of the transformer in the physical domain effects the overall system ratings. The 12 kV converter is rated for 80 kW while the 1.2 kV converter is rated for 150 kW. With the change in ratings, it is not safe to assume that the 1.2 kV converter's system identification model can just be scaled. To that effect, the model is developed from scratch using the same power framework as the 1.2 kV converter model is. The 12 kV converter is a current controlled device so a current reference signal is a model input and the output current is the model output. The 12 kV converter's output voltage is governed by the load and determines the output power. This leads the output voltage to be a model input. The input voltage is not controlled by the 12 kV converter, so the input voltage is also an input to the model. Finally, the input current defines the input power so it is the second model output.

5.1.3.2 Detailed Test Design

Leveraging the same methods used to model the 1.2 kV converter's neural network module, significant data is collected and used to train it. Left-over data sets not used in the model development are compared against the model's performance to determine if the model is a good, poor, or overfit.

5.1.4 Implementation

5.1.4.1 System Identification Implementation

Though the scaling is different between the 12 kV converter and the 1.2 kV converter, the shape and connections to the overall model are the same. The system identification methods take the behavior of the system and work backwards to determine the internal mathematics that connect the model inputs and outputs to each other. The same development programming used to create the 1.2 kV converter was used to create the 12 kV converter model. A sample of the experimental data used to train the model is shown in Figure 5.3. As with the 1.2 kV converter, the algorithm was run, and the best fit model was selected. Utilizing 150 training samples as with the 1.2 kV converter, 15 nodes with a MSE of 0.07.

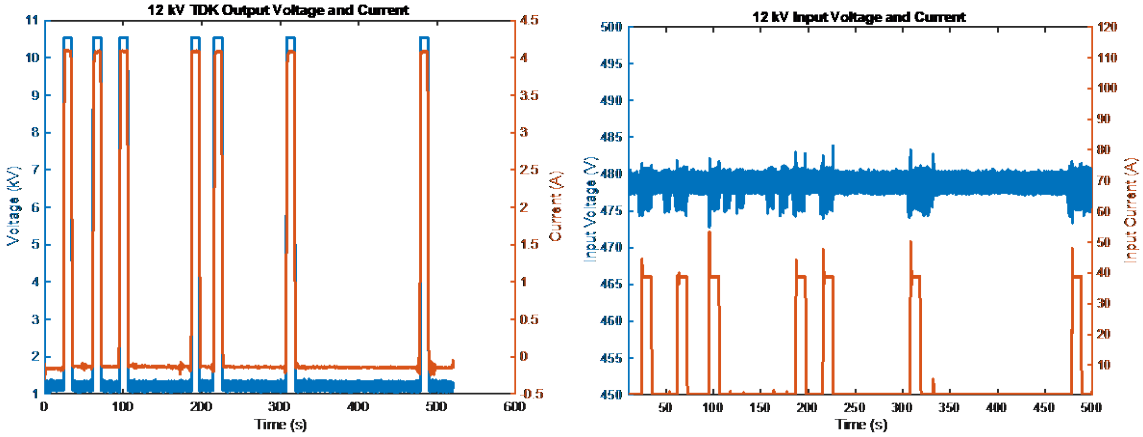

Figure 5.3: Plots showing the input and output electrical responses during a sample pulse train test.

5.2 Validation of the 12 kV TDK Converter

5.2.1 Unit Testing

As already stated, the extra data sets not used in the generation of the neural network module are used to perform detailed evaluation of the converter model. This includes a large amount of data, not all of which will be presented here. Instead, a few different results are shown here in Figure 5.4, to give a general idea of the type of experiments performed and the model result comparison.

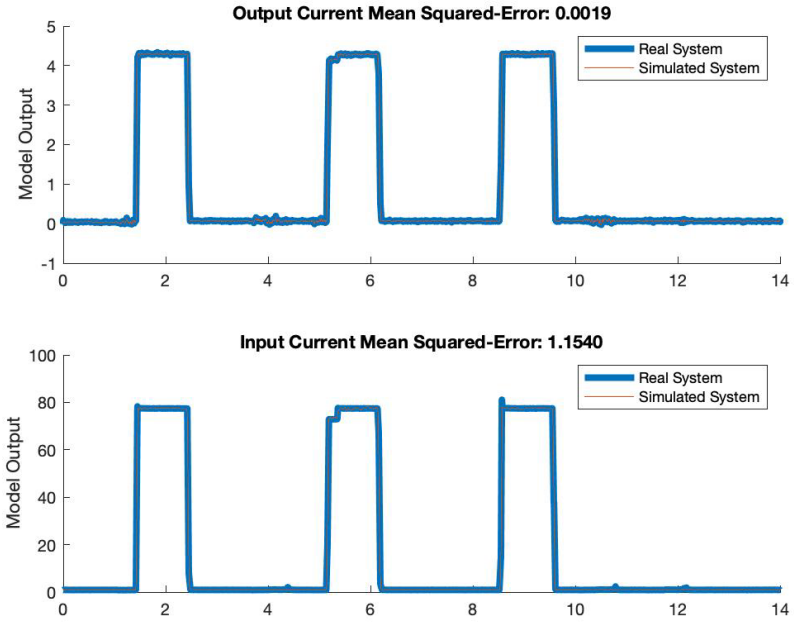

Figure 5.4: Representation of one of the many untrained data sets tested against the 12 kV neural model to determine goodness of fit.

The agreement between the model and experimental data illustrates the capabilities of the 12 kV neural network model to predict data that is not part of the training data set. In the center pulse of Figure 5.4, the resistive load was changed midway through the rise and the figure shows the ability of the model to accurately predict this change when the simulated load is changed accordingly. In the next section, the functional tests will illustrate the ability of the converter to follow control setups that are not from collected data.

5.2.2 Functional Testing

As with the 1.2 kV converter model, the 12 kV converter model is connected to Simscape electrical blocks. This model is evaluated against the profiles described before artificially generated to ensure proper integration with the Simscape Electrical components. In Figure 5.5, the successful responses of the converter model to ramp-rate pulse controls illustrates the ability of the model to accurately follow the control signals when connected to electrical systems.

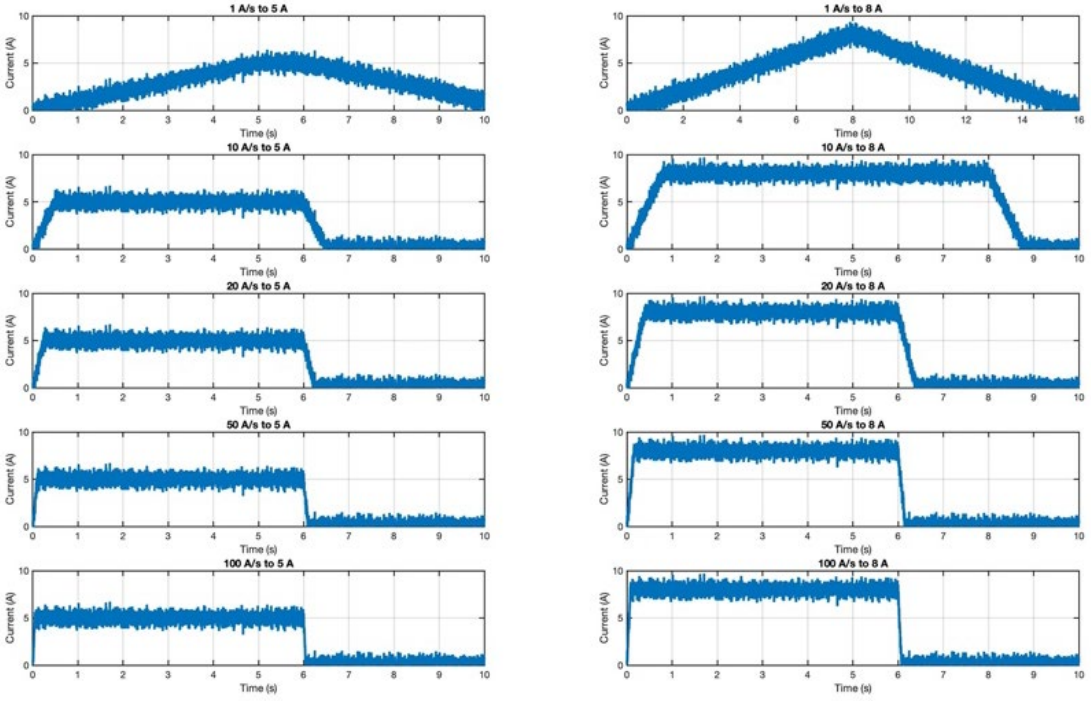

Figure 5.5: Resulting output current waveforms from the 12 kV model when connected to electrical systems and given a ramp-pulse current reference control.

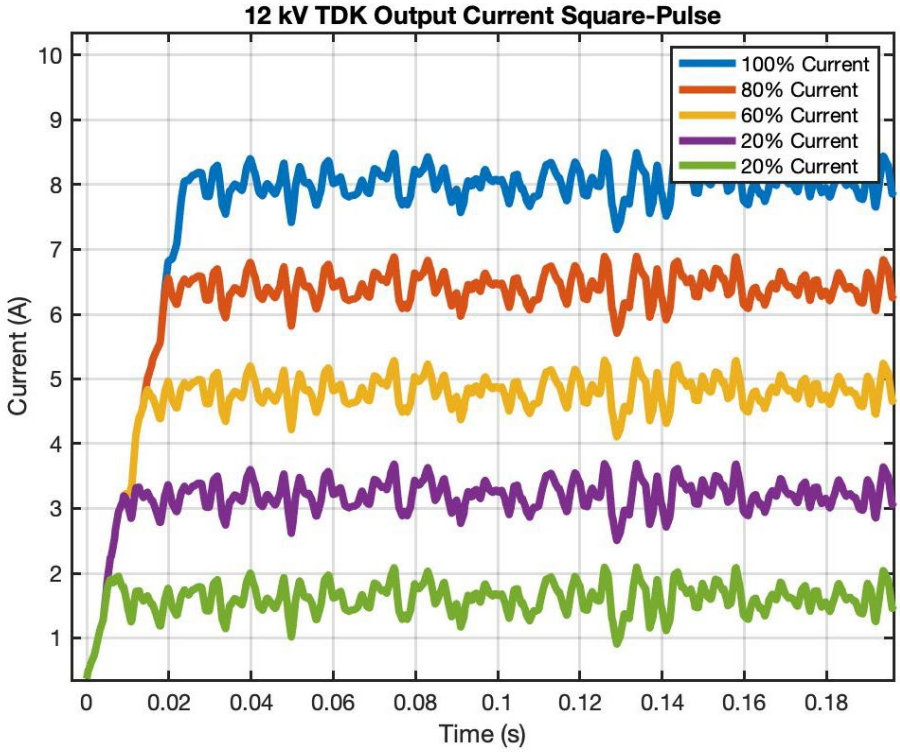

Figure 5.6: 12 kV model output current response to various delta pulse current reference controls showing adherence to the maximum ramp-rate of the 12 kV converter when connected to electrical systems.

5.2.2.1 Acceptance Testing

An overview of the model, that is shown in Figure 5.7, results are seen in Table 5.3. The output current (top) and input current (bottom) both fall within the 1% error requirement for the acceptance of the model. The model results are compared to controlled results from the physical hardware shown in blue. Altogether, this shows the 12 kV converter can accurately represent the physical hardware and it has been verified and validated against the pulsed, ramp, and steady state conditions of interest to the IDEAL testbed.

Table 5.3: 12 kV TDK AC/DC Converter Results

Parameter	Requirement	Performance
Square-pulse	Within 1% Error	0.2135% Error
Ramp Rate	Within 1% Error	0.9446% Error
Steady-State	Within 1% Error	0.2553% Error

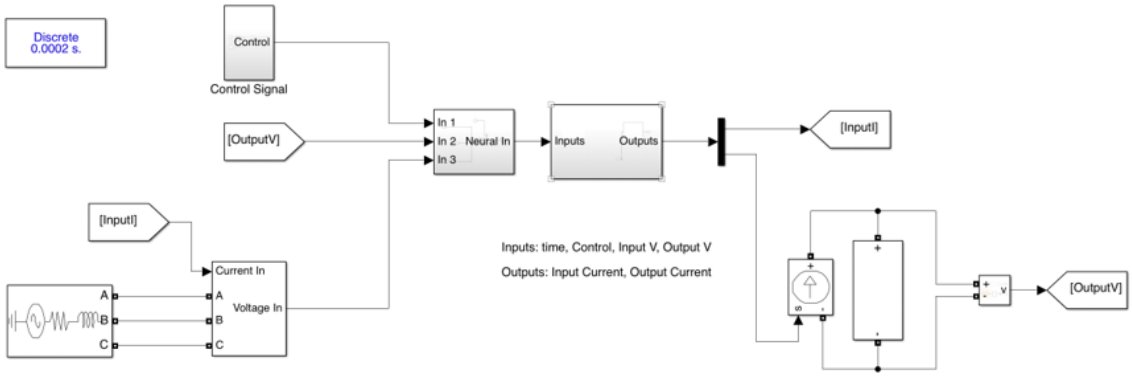

Figure 5.7: 12 kV TDK full model with the neural module and electrical interface connected to external electrical systems.

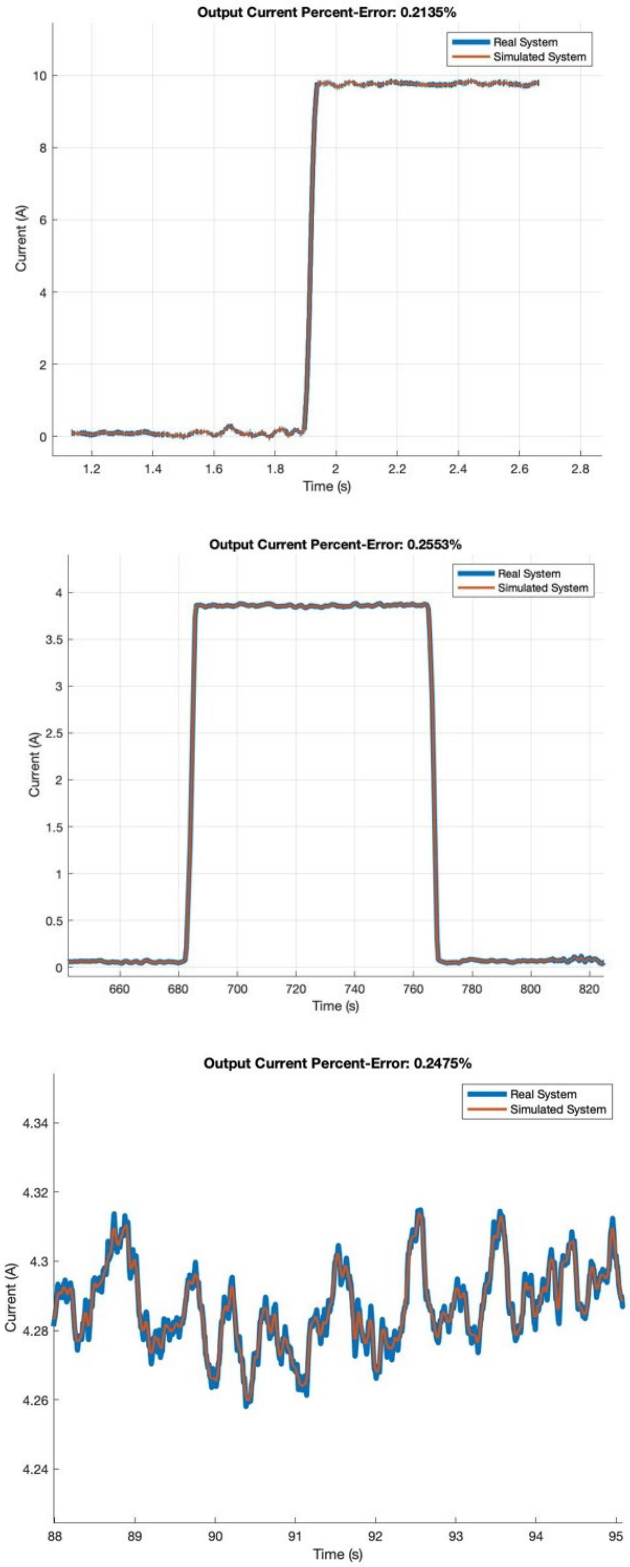

Figure 5.8: 12 kV converter model acceptance test examples. Pulse test (top), ramp-rate (middle), and steady-state (bottom).

CHAPTER 6

MODELING THE 6 kV TDK DC/DC CONVERTER

The final converter studied here is the 1 kVDC to 6 kVDC converter manufactured by TDK Lambda. Like the two converters previously discussed, both full circuit model and the system identification approaches were taken. As with the other converters, roadblocks were hit quickly when going down the circuit modeling approach and it was quickly abandoned. The system identification approach was completed to produce a verified and validated simulation model and it will be discussed here. As implied, the input to this DC/DC converter is not an AC source that is rectified internally. There are still DC input filters, but they are much less significant than the converters discussed previously. H-bridge circuits are used to invert that DC input so it can be stepped up and rectified on the output. Though TDK did again supply some of the circuit schematics, this converter is considered much more proprietary to them and therefore less was provided than in the previous cases. A high-level schematic is shown in Figure 6.1.

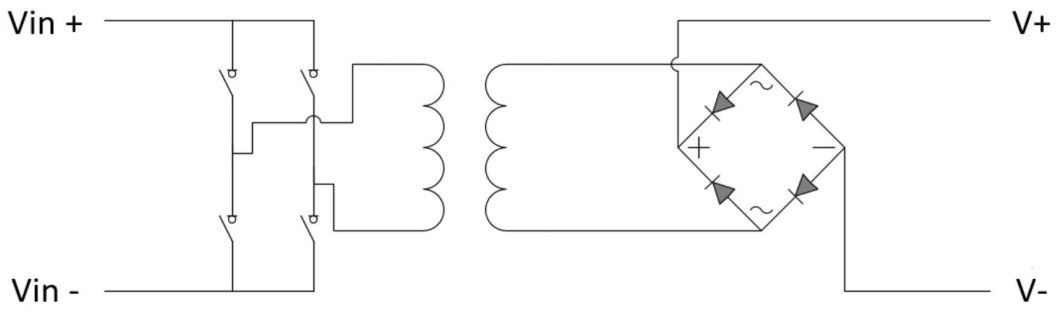

Figure 6.1. 6 kV TDK High-Level Schematic showing the basic components of the 6 kV converter.

6.1 Verification of the 6 kV TDK Converter

6.1.1 Requirement Gathering

As described in the discussion of the IDEAL testbed, this converter is used to condition power from the 1 kVDC bus to supply the resistive 6 kVDC load. The current supplied to the load by this converter is modulated to match the transient load profile that is being emulated in IDEAL. The profile indirectly effects the power quality of the AC generation source. It pulls power off of the 1 kVDC bus and has no control over whether that power comes from the generator or the battery. Correctly regulating power using the 1.2 kV converter discussed much earlier controls that power sharing. The control signal used to emulate the load profile dictates the converter's output current and therefore the model must be able to accurately represent this operation. The converter appears as a load to the 1 kV converter so its input impedance must be properly modeled as they affect each other. In most cases, the transient load supplied by the converter is a near repetitive pulse width modulated signal that is on for 5 seconds and off for 1 second. The transient response of the converter dictates the rise and fall of the converter's output current into the load and therefore capturing this response is critical. While supplying the load, the steady state response must be captured accurately as it is with the previous converters discussed. The requirements are captured in Table 6.1.

Table 6.1: 6 kV TDK AC/DC Converter Requirements

Parameter	Requirement
Steady-State Following	Within 1% Error
Square-Pulse	Within 1% Error

6.1.2 Functional Design

The 6 kV Functional Design step mimics that taken earlier when modeling the 1.2 kV and 12 kV converters, respectively. The neural network model is designed to interface with the Simscape electrical blocks seen earlier in Figure 4.2. These act as the electrical interface for the 6 kV TDK to the rest of the IDEAL power system model.

6.1.2.1 Functional Design Testing

The 6 kV converter will supply ramp, pulsed, and steady state power to the resistive load and therefore these functional scenarios must be accounted for. The system identification model is trained and evaluated using experimentally collected data sets as it was demonstrated previously.

Pulsed Test

The load profile the 6 kV converter supplies is a square pulse that is on for 5 seconds, off for 1 second, and then repeated as needed. The control signal sent to the converter is a pulse width modulated signal, so the converter's output is dictated more by its own internal slew rate then the control signal. As was done with the 1.2 kV and 12 kV converters, that slew rate had to be characterized, seen in Figure 6.2. The data shows a very similar response to the two converters already discussed and that makes because TDK is likely using a similar control logic scheme in all three converters. A current slew rate of roughly 356 A/s is measured.

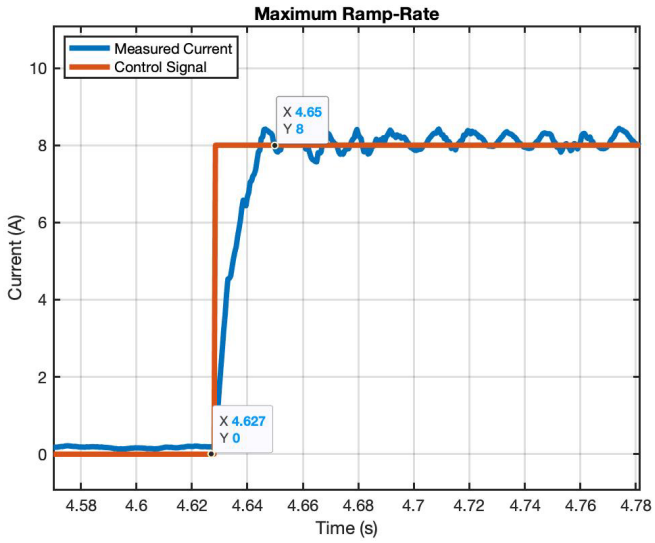

Figure 6.2: Plot showing a maximum ramp-rate test using a delta control signal to evaluate the time it takes to rise to maximum and determining the max rate to be 356 A/s.

Steady State Test

In the same way the steady state response is modeled for the earlier two converters, it must be accurately modeled for this converter. These tests are designed to prove that the system follows the steady-state behavior of the real system within the acceptable margin of error. This is achieved by measuring the converter's output current while the control signal is held constant. Current reference set points of 20%, 40%, 60%, 80%, and 100% of the ratings are tested. The reference control signals are seen in Figure 6.3.

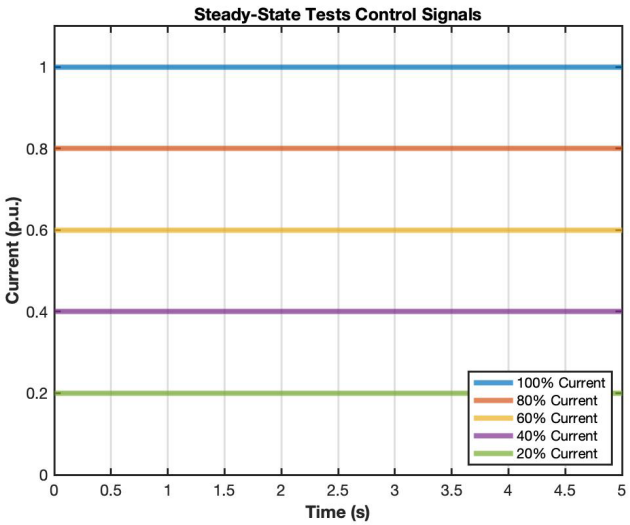

Figure 6.3: Control reference signals to be passed into the 6 kV converter model to evaluate adherence and controllability in steady state.

6.1.3 Detailed Design

The main difference between this converter and the two discussed earlier is the lack of a front-end rectifier, as seen in Figure 6.1. The rest of the building blocks remain the same save the specific component values. This points to the use of the governing equation, Equation (2). The converter is again being used as a current controlled device, and utilizing the law of conservation of energy, the inputs to the model remain as input and output voltage, and the control signal. Then the input and output currents are the outputs of the model.

6.1.3.1 Detailed Test Design

This effort remains the same as with the previous two converters. Data representative of several loading scenarios are fed into the neural network morel to train it and similar data, that is not used to train the model, is used to verify its accuracy in the validation stage.

6.1.4 Implementation

The neural network model development follows the same process as the 1.2 kV and 12 kV converters discussed already. Data collected from the physical hardware is collected and fed into the neural network model generator. The output of the generator resulted in a neural network with 25 hidden nodes and a reported performance of 0.15 MSE. The electrical interface is determined by the inputs and outputs of the neural model. The model outputs are the input and output current, respectively. As such, the model needs to electrically control those parameters. The neural network is connected to an input current source this sets the power draw of the converter. The output is connected to another current source and a sample of the model output current for pulsed, ramp, and steady state conditions is shown in Figure 6.4. Again, the 50 of each each scenario are used, though, since only the pulse and steady-state tests are evaluated, 100 training sets are used. The neural network model chose 25 hidden node layers with 0.15 MSE performance.

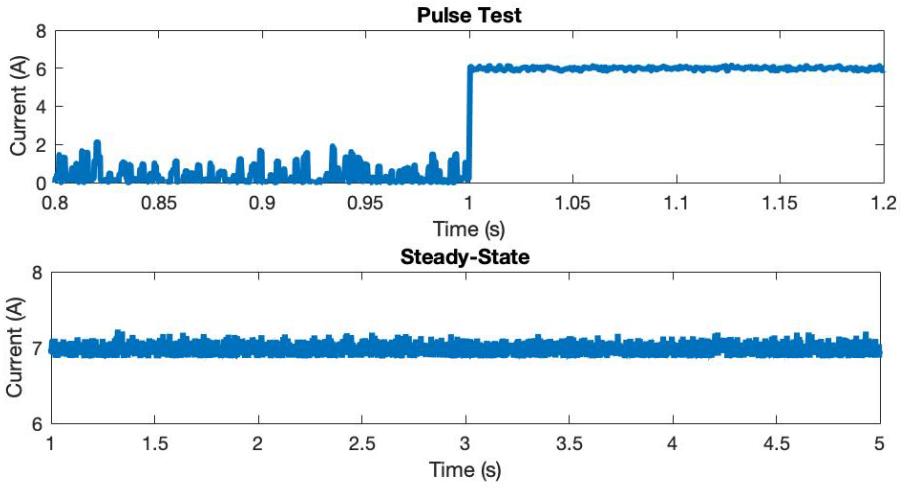

Figure 6.4.: Example of the collected data from the IDEAL test bed from the 6 kV converter to be fed into the neural network model generator.

6.1.5 Detailed Testing

Validating the neural network's performance against untrained data ensures a 'good-fit' rather than an over- or under- fit. In pursuit of this validation, untrained data is fed into the 6 kV converter's neural module. Based on the information provided in Figure 6.5, the model is accurate against untrained data to within 1% error. This points to a 'good' fit of the neural network and not a network that only followed a pattern from the trained data.

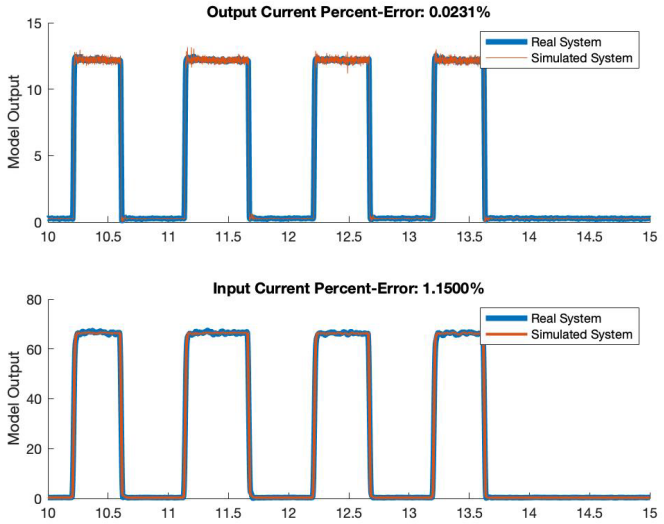

Figure 6.5: Depiction of a test that was used to evaluate the neural network model against untrained data (blue) to confirm goodness of fit.

6.1.6 Functional Testing

The model's response to the ramp-rate and steady state control signals supplied to it are shown in Figure 6.6 and Figure 6.7, respectively. The data shown in Figure 6.6 shows the model's ability to ramp up at the required rate of 356 A/s shown earlier in the experimental ramp rate experiment. As expected, the ramp rate matches for each of the saturation limits supplied to it and it appears to transition well to the steady state condition with minimal overshoot occurring. In the steady state experiments shown in Figure 6.7, there is significant ripple seen in the model output that aligns well with the ripple observed in the physical hardware.

These tests are significant factors in validating the functional behavior of the 6 kV converter model. The controllability of neural model connected to the electrical interface points to an ability for the model to represent the specific control and electrical response when connected to other electrical systems. Essentially, this poses as proof the model is functional in evaluating its response to the behavior of other electronics. This electrical response is pivotal in the desired modeling the IDEAL power system.

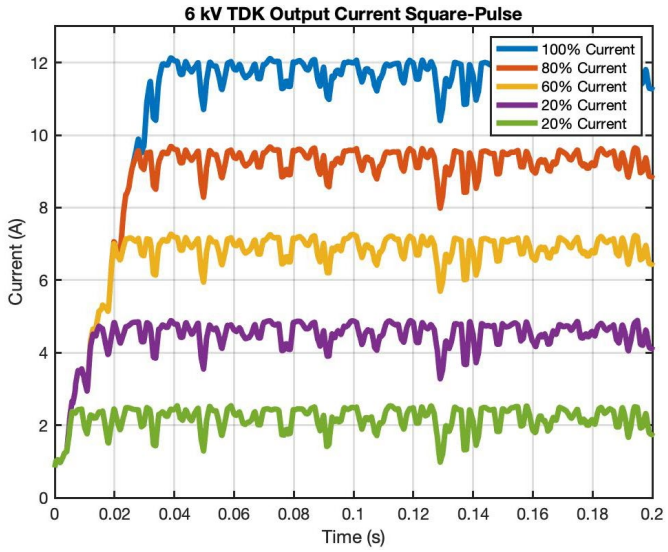

Figure 6.6: 6 kV model response to pulse current reference controls when the neural network is connected to electrical systems showing adherence to the maximum ramp-rate.

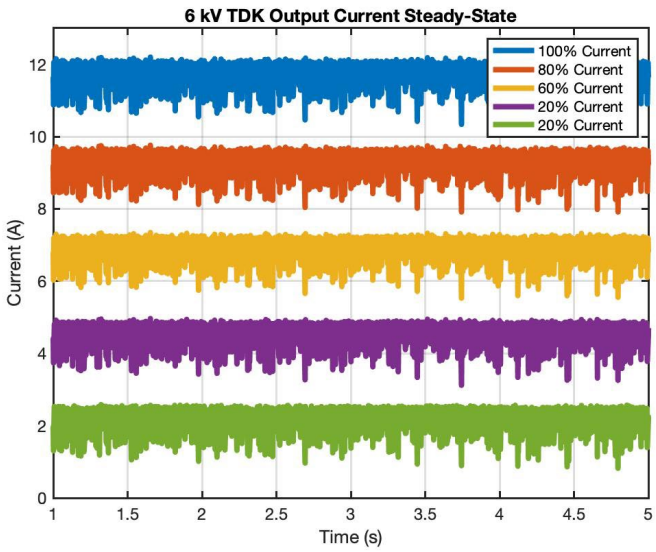

Figure 6.7: 6 kV converter response to steady-state current reference values when connected with other electrical systems.

6.1.7 Acceptance Testing

In the acceptance testing step, a significant amount of untrained data was used to further validate the model's agreement with the experimental data collected from the physical hardware. The model is shown in Figure 6.8 and an example of the model agreement for ramp and steady state conditions are shown in Figure 6.9 and Figure 6.10, respectively. As per Table 6.2, the model falls within the bounds of the originally defined model 1% error requirement and thus the model is verified and validated.

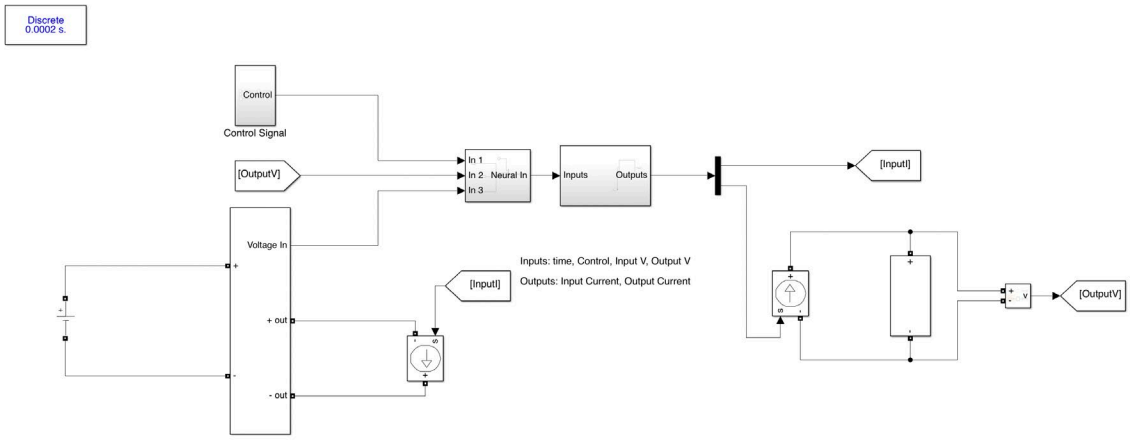

Figure 6.8: Fully connected and implemented model of the 6 kV converter neural module to the electrical interface.

Table 6.2: 6 kV TDK DC/DC Converter Acceptance Evaluation

Parameter	*Requirement*	*Performance*
Square-Pulse	Within 1% Error	0.0368% Error
Steady-State Following	Within 1% Error	0.068% Error

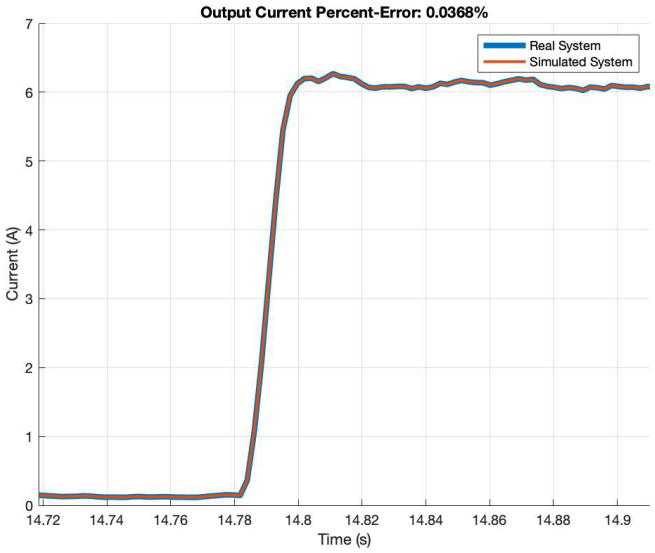

Figure 6.9: Model vs. real response to pulse test illustrating the maximum ramp-rate of the 6 kV converter.

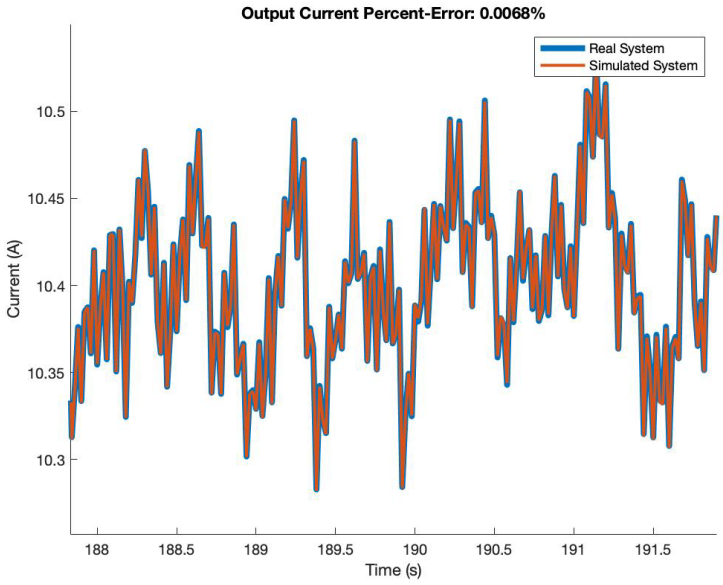

Figure 6.10: Steady-state acceptance testing of the 6 kV converter.

SUMMARY AND CONCLUSION

There is demand in both the private and government sectors to make electrical power systems more intelligent, reliable, and controllable then legacy systems have been. This is achieved by integrating distributed power generation sources, real-time voltage and current sensors, and real-time control that is ready to respond and reconfigure the power system as needed. Though this concept is feasible and quite simple to draw up on paper, it is much harder to implement in practice, especially when the power system needs, and topologies are so unique for each application. Setting up a physical testbed for each scenario is not practical from financial or space aspects. Being able to accurately model the components that make up the power system, and thus the power system, it becomes practical to study multiple use cases quickly. Models must be created and then verified and validated to accurately represent the physical hardware under all the use cases it is expected to operate in or else the models serve no purpose.

Modeling and those components and then verifying and validating those models is easier said than done, especially when physical hardware is commercially procured, and the vendors are not willing or able to share the information needed to create a model. A testbed that has been assembled to study distributed power system control has been discussed here along with the efforts made to model three of the power electronic converters in the testbed. Despite having significant help from the manufacturer, enough information was not provided to make circuit level models that would meet the requirements. Instead, a method of system identification has been used. The system identification model is trained using a neural network that learns how to predict the converter performance. The process used to create the neural network, create the system identification model, and the verification and validation procedure used has been described here.

The result of this work is a demonstration of the effectiveness of utilizing a system identification approach to model power electronics as they are to be fielded in a power system. Utilizing representative tests and gathering large sums of data, the underlying behavior of these systems can be exposed and captured. It has been shown that with the use of neural networks these large data interpolations can be created and connected with other electronic systems and models to accurately represent physical hardware. These processes provide valuable insight to the behaviors of physical hardware and how they will interact with each other. Having models that are verified and validated drastically increases the ability to learn the benefits and operational control requirements of next generation power system employing distributed sources. The V&V paradigm has been shown to be exceptionally useful for the development of models to fit particular use cases. The steps allow a model designer to describe a recipe not only for how a model is developed, but for how to use the model.

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BIOGRAPHICAL INFORMATION

Alexander Johnston began his collegiate career as an Aerospace engineer. He quickly realized his skills and interests lied in the world of electronics and electrical engineering. When he switched degrees, he immediately began interacting with faculty and staff which eventually led to a stint in undergraduate research. This was a direct line to personal edification and interest in research and development. Mr. Johnston began work as a Research Assistant in the University of Texas at Arlington Pulsed Power & Energy Lab.

Mr. Johnston has been studying for his Ph.D. at the University of Texas at Arlington doctoral program where he will study electrical engineering with a focus on control and embedded systems and power. He plans to use the skills and knowledge he gained to work in the area of contracting research and development. Eventually he wishes to begin his own technology development and investment firm.