Sub-10K Cold-Electron Injection to Silicon at Room Temperature

By

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Abstract

The Fermi-Dirac thermal excitation of electrons results in unwanted off-state leakage currents in metal-oxide-semiconductor field-effect transistors (MOSFETs), leading to excessive power consumption in modern electronic devices. The electron thermal excitation results in a theoretical subthreshold slope limit of 60 mV/decade at room temperature, which forces the devices to use a high supply voltage leading to high power consumption. This study investigates a new architecture capable of suppressing electron thermal excitation by using a quantum well (QW) as an energy filter. The QW energy filter is composed of a tunneling barrier 1 (0.5 to 1 nm Al_2O_3 or 0.3-1 nm Si_3N_4 or no tunneling barrier) a quantum well (QW) layer (3-5 nm tin oxide, SnO_2), and a tunneling barrier 2 (native silicon dioxide, SiO_2). The energy filter layers are sandwiched between a chromium electrode and silicon. This energy-filtering structure makes it possible to inject cold electrons into silicon with abrupt current jumps, which correspond to the alignment of the QW levels with the conduction band edge of silicon. Differential conductance (dI/dV) plots show extremely narrow peaks, with their FWHMs (full widths at half maximum) only 0.025mV, corresponding to an effective electron temperature of 0.08 Kelvin at room temperature. This cold electron injection to Si at room temperature has a potential to create transistors that operate with extremely little energy consumption.

Table of Contents

List of figures

Chapter 1: Introduction

The scaling rule allows transistors (MOSFETs) to operate at greater speeds and exponentially larger packing densities[1–4] With the scaling rule, along with many novel MOSFET designs, there have been great enhancements in MOSFET performance over the past few decades. Some examples of these performance enhancers include metal-gate high-k stacks,[5–7] channel strain[8–10], ultra-thin body designs,[11–13] ultra-thin-body silicon-on-insulator substrates[14,15] and FinFETs[16–19]. However, these performance enhancements have recently slowed down. One critical reason is that the voltage scaling [20] cannot be continued due to fundamental thermodynamic limitation. The electron thermal excitation following the Fermi-Dirac distribution imposes a fundamental thermodynamic limitation to the slope of current-voltage (I-V) characteristics (green line in Fig. 1). This prohibits the supply voltage V_{dd} from being arbitrarily reduced as lowering V_{dd} causes a large amount of Off-state current.

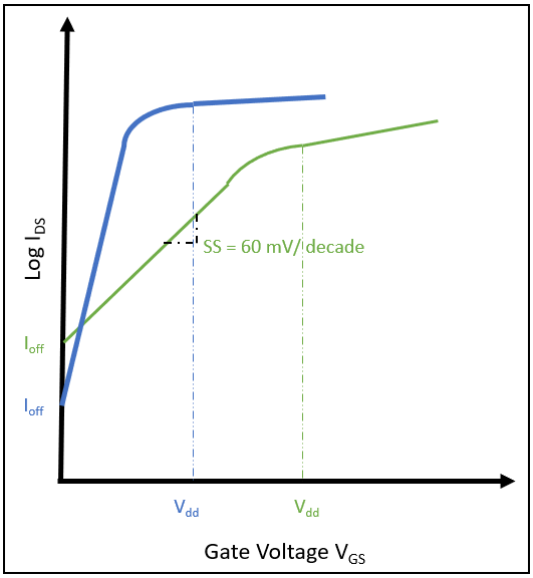


Figure 1: *Subthreshold swing (green) limit at 300K. Blue IV shows desired slope to reduce V_{dd} and Off-state current*

The subthreshold slope (SS) is characteristic of the drain current (I_d) and the gate voltage (V_g) relationship in a metal-oxide-semiconductor field-effect transistor (MOSFET). SS is defined as the amount of gate voltage change to reduce the current by ten times (unit: mV/decade). This subthreshold slop (SS) is a measure of how sharply transistor can turn on or off in the subthreshold region. The smaller the value of the Subthreshold Slop (SS), the steeper the I-V in the subthreshold region.

For a finite subthreshold slope, the MOSFET needs to maintain High enough V_{dd} to ensure high enough I_{on} / I_{off} ratio. However, as we can see in Figure 1, if we can decrease the subthreshold slope value (stepper slope), we can reduce the V_{dd} required to maintain a similar current while making I_{off} small. Therefore, by decreasing the subthreshold slope value (Steeper slope) we can reduce the energy wasted as heat.

The subthreshold slop (SS)[21–23], is given by,

$$SS = \frac{\mathrm{d}V_{GS}}{\mathrm{d}\log(I_D)} = \ln(10).\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right) \quad \text{Eq. (1)}$$

Here V_{GS} is the gate-to-source voltage, I_D is the drain current, C_d is the depletion-layer capacitance, and C_{ox} is the gate-oxide capacitance. We can obtain the theoretical subthreshold if we assume $C_d = 0$ and $C_{ox} = \infty$.

$$SS = \ln(10).\frac{kT}{q} \quad \text{Eq. (2)}$$

From Eq. (1) and Eq. (2), the subthreshold slop (SS) is proportional to the temperature. At room temperature (300K) its theoretical limit is 60 mV/decade.[24] Hence, to reduce the value of the subthreshold slope (steeper slope), it is required that the temperature is lowered.

The root cause of the subthreshold slope limit of 60 mV/decade is the Fermi-Dirac electron thermal excitation. Several strategies have been examined to address this undesired thermal excitation of electrons. Tunneling field-effect transistors[25–27] (TFET), which use band-to-band tunneling[28] to reduce Fermi-Dirac thermal excitation[29,30], are among the most extensively investigated technologies. Here a p-type doped source electrode and n-type doped drain electrode make up most of the TFETs. To reduce the contribution of the Fermi-Dirac thermal excitation, this design uses band-to-band tunneling from the valence band of the p-type source to the conduction band of the n-type drain. Various TFET[31–35] designs with different configurations, such as vertical structures, sidewall gating, planar structures, and nanowires, have been studied. Numerous other material systems, such as InAs-Si[36–38], InAs/GaSb-Si[39–41], AlGaSb-InAs[42–44], and 2D semiconductors, have also been explored (e.g., $MoTe_2$[45,46], WSe_2[47,48], and MoS_2[49,50]). Several types of TFET heterostructures have also been investigated.

This study investigates a new energy-filtering architecture that enables cold electron injection to silicon at room temperature with an effective electron temperature of 0.08 Kelvin. This is done by filtering out thermally excited electrons using a quantum well discrete energy level, allowing only the thermally suppressed cold electrons to tunnel into the silicon upon the application of a voltage bias. This architecture effectively suppresses the thermal excitation of electrons when the Si conduction band edge is aligned with the Quantum well (QW) discrete energy level, enabling cold-electron injection to Si at room temperature.

Chapter 2: Energy Filtering Principle

2.1 Concept

It has been demonstrated that thermally excited electrons can be suppressed without the need for external cooling or cryogenic settings[51]. This was accomplished by filtering high energy electrons using a discrete quantum state; as a result, only cold electrons participate in the electron transport.

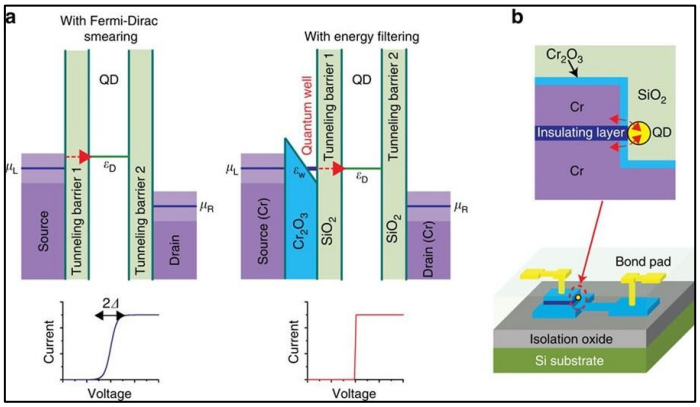


Figure 2: Energy filtering and cold-electron transport in double-barrier tunneling junction (DBTJ) structure [51]

In the previous work [51], as seen in Figure 2, the device architecture consists of source metal, a 2nm Cr_2O_3 layer which forms a quantum well, tunneling barrier 1, a quantum dot as a channel, tunneling barrier 2 and drain metal. In this structure, the thermally excited electrons from the source metal are filtered by the QW energy level of the quantum-well layer before entering the discrete energy levels of the quantum dot and then into the drain electrode. This cold-electron transport has been verified for the 2D (QW) to 0D (quantum dot) system. It would be important to see if the cold-electron transport can be realized for another dimensional system, for example, for 2D to 3D transport. This work investigates the energy-filtered cold-electron transport from 2D (SnO_2 QW) to 3D (Si). Importantly, the investigation of the silicon system will allow the

devices to be fabricated on a large scale as they can be incorporated into existing MOSFET fabrication technologies.

2.2 Principle of Quantum well as Energy filter

When one or more dimensions of a solid shrink to the nanoscale, the confinement of particles leads to discrete quantum states.[52–54] One example of the quantum confinement is a quantum well[55–61], in which the particles are constrained in one dimension but are free to travel in the other two. Confinements typically occur in nanoscale dimensions between 1 and 10 nm. At this size, the dimensions are comparable to the de Broglie wavelength[62–66] of to the electron.

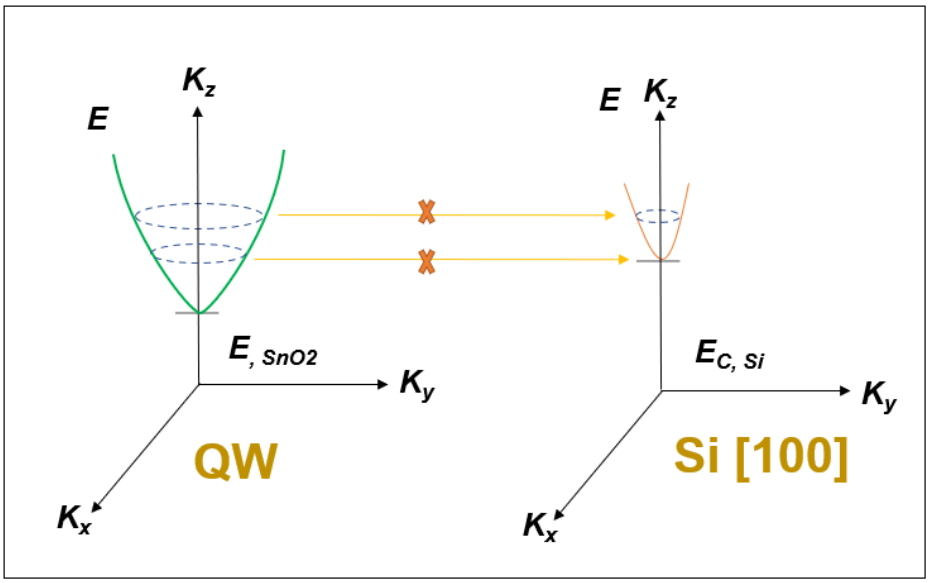


Figure 3: Schematic showing unaligned Quantum well and Silicon [100] bands structure

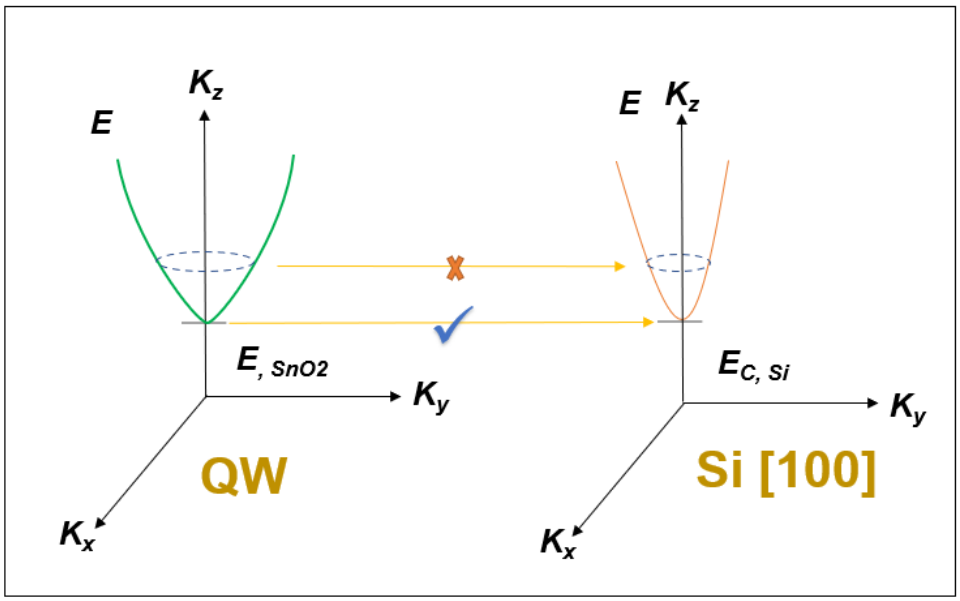


Figure 4: Schematic showing aligned Quantum well and Silicon [100] bands structure

The electron tunneling from a QW to Si needs to satisfy two criteria: 1) energy-Conservation[67–69], and 2) in-plane momentum Conservation.[70–72] The cold-electron injection can be understood from the E-k diagrams in Figures 3 and 4. When a QW state of SnO_2 is below the conduction band edge of Si ($E_{C, Si}$), Figure. 3, there is no configuration that satisfies both energy conservation and in-plane momentum conservation. Accordingly, no electron would tunnel from the QW to Si. When the QW state of SnO_2 is aligned with the conduction band edge of Si ($E_{C, Si}$), there is a tunneling path that satisfies both energy conservation and in-plane momentum conservation, Figure. 4. Here, the electrons at the bottom of the QW sub-level (E_{SnO2}) can tunnel to the Si conduction band edge ($E_{C, Si}$), satisfying both conditions. Since the electrons can only tunnel to the Si conduction band edge from the bottom of the QW sub-level (E_{SnO2}), electrons present in the excited state in the source metal will not be able to tunnel into the silicon conduction band. This results in only the thermally suppressed electrons trapped in the QW sub-level to be able to tunnel through when

the QW sub-level aligns with the Silicon conduction band. Thus, we observe an abrupt current jump in I-V measurements.

Chapter 3: Fabrication Procedure

3.1 Chapter fabrication for QW-Si Device

This chapter describes the fabrication process for a quantum-well-mediated silicon electron transport device. In this chapter, we discuss the problems we faced during the manufacturing of the devices and the steps taken to resolve them, such as moisture accumulation on the source pad owing to the Peltier effect[73–75] and the doping residue on the silicon wafer after doping. Floridization of resist. The devices were fabricated on 4-inch silicon wafers with four different doping concentrations: P-Si, P++Si, N-Si, and N++Si. The wafer was processed using various deposition techniques, thermal growth processes, dry and wet etching processes, and multiple photolithography processes. The entire process was carried out in a class-10/100 cleanroom facility at the Nanofab Research Facility at the University of Texas, Arlington.

3.2 Substrate preparation

Bare test-grade four-inch silicon wafers were cleaned of all organic impurities using a piranha solution. Precaution needs to be taken when utilizing acids by wearing complete PPE equipment when handling acids. The Piranha solution was prepared using H_2SO_4 and H_2O_2 in a ratio of 3:1, So we will take 60mL of sulfuric acid (H_2SO_4) was added to a Pyrex glass Piranha beaker and add 20mL of hydrogen peroxide was added to the same beaker very slowly along the sides of a glass beaker. The wafer was submerged in a freshly prepared piranha solution for 30 minutes, thoroughly rinsed in a DI water bath container for 5 minutes and rinsed in running DI water for a few minutes. Again, it was immersed in a second DI water bath for another 5 minutes.

It was then thoroughly rinsed in running DI water for a few minutes and then slowly blow-dried with nitrogen. After removing the organic impurities, as the wafers are stored in contact with air, a thin layer of silicon dioxide (SiO_2) is formed, and we will need to strip off native silicon dioxide (SiO_2) removed using HF (10:1). Precaution needs to be taken when utilizing acids by wearing complete PPE equipment when handling acids. To begin the process, we removed HF at a 10:1 ratio in a Teflon container, and the quadrant was submerged in the container for 5 minutes to allow sufficient time for HF to react with native silicon dioxide (SiO_2). It was then rinsed in a DI water bath for 5 minutes, followed by rinsing under running DI water for a few minutes. Again, it was immersed in a second DI water bath for another 5 minutes. It was then thoroughly rinsed in running DI water for a few minutes and then slowly blow-dried with nitrogen.

3.3 Thermal Oxide Growth

Once the substrates are thoroughly cleaned, the process of growing oxides on bare Si wafers can be started. To grow the wafers, the cleaned wafers were loaded into a quartz boat. Once the wafers are loaded into the boat, they can be loaded into a thermal oxidation chamber (Tystar Oxidation Furnace) to grow a nominal thickness of 250 nm silicon dioxide for the [100] wafer and 450 nm silicon dioxide for the [111] wafer.

Figure 5: Tystar Oxidation Furnace for Thermal Oxidation and nitride of Silicon

Thermal oxides were grown using the dry oxidation method to ensure high-quality oxide growth. The oxidation parameters for silicon wafers with the [100] orientation are as follows:

Tyster Thermal Oxidation Furnace: KOHD250.001

Ideal Temperature: 450°C

Boat Out: 15 Minutes

Boat In: 15 Minutes

Ramp 700°C: 30 Minutes; N_2: 5000 sccm

Stabilize: 30 Minutes; N_2: 5000 sccm

Ramp 1100°C: 2 Hrs.; N_2: 5000 sccm

Hold: 3 Hrs. 30 Minutes; O_2: 3000 sccm

Anneal: 30 Minutes; N_2: 5000 sccm

Ramp down 700°C: 2 Hrs.; N_2: 5000 sccm

Hold: 700°C; Till alarm Acknowledged

After the oxide was grown, it was measured using Nanospec at the center of all four quadrant regions and the center of the wafer to confirm the film thickness and uniformity. The 250 nm thermal oxide was used as the passivation layer and as a protection to prevent over-etching in the silicon window pattern in the first mask step.

Thermal oxides were grown using the dry oxidation method to ensure high-quality oxide growth. The oxidation parameters for silicon wafers with [111] orientation are as follows:

Tystar Thermal Oxidation Furnace: Dry380nm.001

Ideal Temperature: 450°C

Boat Out: 15 Minutes

Boat In: 15 Minutes

Ramp 700°C: 30 Minutes; N_2: 5000 sccm

Stabilize: 30 Minutes; N_2: 5000 sccm

Ramp 1100°C: 1 Hrs.; N_2: 5000 sccm

Hold: 8 Hrs.; O_2: 3000 sccm

Anneal: 20 Minutes; N_2: 5000 sccm

Ramp down at 700°C: 2 Hrs.; N_2: 5000 sccm

Hold: 700°C; Till alarm Acknowledged

After the oxide was grown, it was measured using Nanospec at the center of all four quadrant regions and the center of the wafer to confirm the film thickness and uniformity. The 450 nm thermal oxide was used as the passivation layer and as a protection to prevent any junk that might accumulate during the dicing of the sample and to prevent over-etching in the silicon window pattern in the first mask step.

3.4 Dicing of Silicon wafers with [111] crystal orientation and cleaning.

After growing a passivation layer on a bare Si wafer, we diced the wafer into 1-inch × 1-inch squares using a DISCO Automatic dicing saw (DAD3220). A dicing machine was used to cut the sample owing to the crystal orientation of the silicon wafer. As expected, a simple scratch may not break the sample in a straight line.

Figure 6: DISCO Automatic dicing saw for dicing the silicon wafers

The dicing equipment uses coolant to keep the blade cool during the dicing operation. Because the coolant contains impurities, it contaminates the silicon wafer. To remove

impurities from the top of the silicon dioxide, we used hydrogen fluoride (HF) to etch away the top layer of the silicon dioxide layer until a nominal thickness of approximately 250 nm was left in order to keep the sample conditions the same for all wafers.

3.5 Pattering of Silicon Island Region

After growing a passivation layer on the bare Si wafer, the next step was to pattern the sample with the first mask. In this study, we used photolithography to expose a particular area to react with further etching.

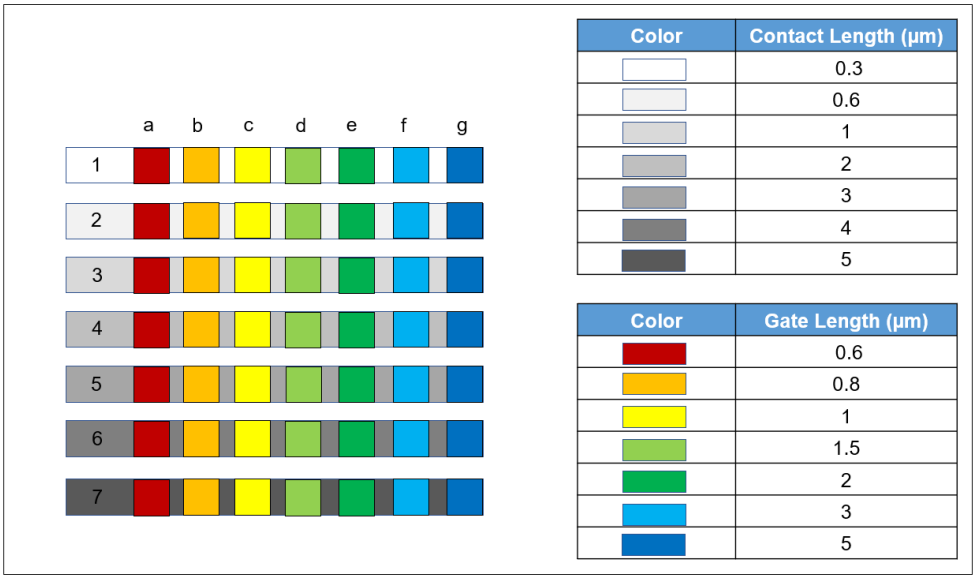


Figure 7: Mask layout showing variation in contact area and gate length

In this process, we created three sample names, A, B, and C, in each quadrant of the silicon wafer, and each sample had four regions, A, B, C, and D. Each region in the sample had seven rows from A to G with variations in the size of the exposed silicon region, and seven columns from 1 to 7 with variations in the distance between the source and drain pads.

3.5.1 Photolithography for silicon window pattern exposure.

Each quadrant was coated with a thin layer of a negative photoresist NR-1000PY of approximately 1 µm using the spin-coating technique. The quadrant was coated with a resist using a dropper to cover approximately 80% of the surface, and then rotated using a Headway Research PWM32 spin coater. The spin coater was initially spun at low rpm to spread the resist across the sample, and then at high speed to ensure a thin, even coat of resist. The spin-coating parameters were as follows:

Step 1:

500 RPM; 100 RPM/s; 5 Seconds

Step 2:

3000 RPM; 1000RPM/s; 60 Seconds

Step3:

0 RPM; 1000RPM/s; 0.1 Seconds

After spin-coating, the sample was preheated at 150°C for 60 seconds on a hotplate. This helps to reduce the residual solvent, which helps in adhesion to the substrate[76] Subsequently, the samples were prepared for photolithography pattern exposure.

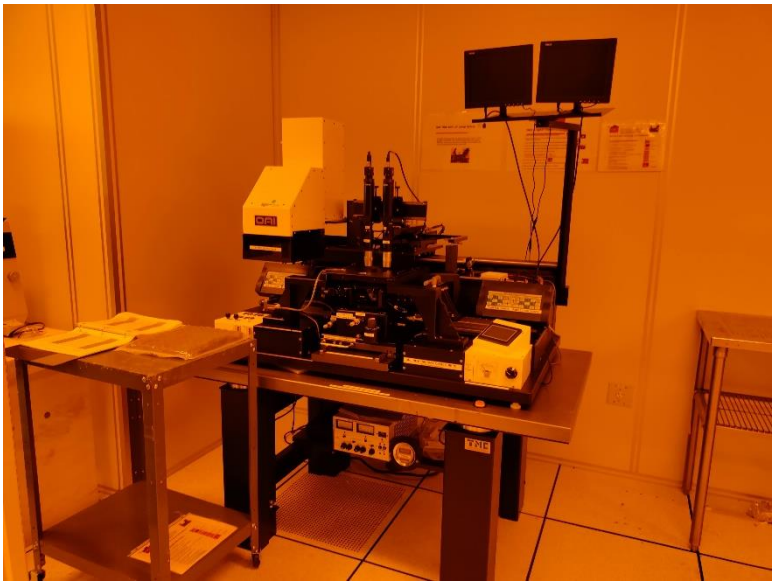


Figure 8: OAI Aligner Equipment for UV Photolithography

The samples were loaded onto an OIA Aligner for the first mask. As this was the first mask, we aligned the samples to ensure that the quadrant was within the mask area. Once properly aligned, it was firmly pressed against the hard mask and exposed to UV light to print the pattern on the sample. The exposure parameters were as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After exposing the samples, we performed a post-bake on a hot plate at 100°C, which helped smooth the concentration profile of the photoreaction product via diffusion.[77] The development process was initiated after the sample was cooled. For this purpose, we used a developer called RD-6 for 25 seconds. Teflon tweezers were used to shake the samples while developing to ensure that all the unexposed resist was removed

from the sample. This was followed by rinsing in a DI water container for 5 minutes with regular stirring to prevent further development. After the first water bath, it was moved to the second DI water bath for 5 minutes with regular stirring. After the development was completed, the sample was removed and slowly blow-dried with dry nitrogen.

3.5.2 Reactive Ion Etching – Dry Etching

The next step was to expose the Si inside the patterned area. To create a Well structure in the silicon dioxide (SiO_2) area, we need an anisotropic etch; we start etching with reactive ion etching. To ensure that we do not etch silicon, we leave an 80 nm silicon dioxide (SiO_2) margin. Ions hitting the silicon during etching can result in a rough silicon surface, which can reduce the device yield by depositing very thin films on the exposed silicon for the energy filter stack. To etch the Silicon dioxide (SiO_2), we use Technics Macro RIE-8800 equipment.

Figure 9: Technics Macro RIE – 8800 equipment for Reactive Ion Etching

Silicon dioxide (SiO_2) is etched with a gas mixture of CF_4 and O_2[78–80]; as the equipment does not have endpoint detection, we used the time to calculate the etched SiO_2. To obtain a stable etch rate, the gas flow, pressure, and power were maintained constant.

During the etching process, there is the possibility of physical sputtering, which can result in impurities accumulating in the window area, resulting in a variation in the etch rate. Therefore, we broke the etching into two parts and cleaned the area with oxygen plasma to remove the impurities and any accumulated photoresist in the window area.

The reactive ion etching parameters were as follows:

Step 1:

Power: 600 W

Pressure: 160 mTorr, CF_4: 30 sccm , O_2: 3.6 sccm

Time: 136 seconds

Step 2:

Power: 350 W

Pressure: 200 mTorr, O_2: 11 sccm

Time: 300 seconds

Step 3:

Power: 600 W

Pressure: 160 mTorr, CF_4: 30 sccm , O_2: 3.6 sccm

Time: 136 seconds

Step 4:

Power: 350 W

Pressure: 200 mTorr, O_2: 11 sccm

Time: 300 seconds

After the etching process was completed, the photoresist was removed from the sample using acetone and isopropyl alcohol (IPA).

3.5.3 Lift-off of the photoresist.

Because the photoresist was soluble in acetone, it was immersed in an acetone bath and sonicated for 5 minutes to expedite its dissolution. After sonication, the samples were removed and rinsed quickly with isopropyl alcohol (IPA). IPA rinsing was performed after acetone to ensure that no acetone residue remained if acetone was dried on the sample surface. After rinsing, the solution was placed in isopropyl alcohol (IPA) and sonicated for 5 minutes. After sonication, the sample was removed and blow-dried slowly using dry nitrogen. However, even after sonication, some redeposited photoresists remained in the silicon window area.

3.5.4 Sample Cleaning and Measurements

To remove the redeposited photoresist, we used oxygen plasma with Macro RIE-8800 equipment. It was observed that the samples treated for 10 minutes or 20 minutes still had some residue remaining. The 30-minute oxygen clean recipe was able to remove all the residues present in and near the window area.

Figure 10: KLA Tencor-P6 profilometer for profile measurement

The thickness profile of the etched area was measured by using a profilometer (KLA Tencor-P6 profilometer). There should be a discrepancy of approximately 60 nm, which is the same as the thickness measured with the reflectometer, the profile height, and the initial measurement of the silicon dioxide thickness. Next, we proceeded to the next phase of the fabrication process.

3.5.5 Wet Etching and Tunnelling Barrier 2

To remove the remaining silicon dioxide (SiO_2) and expose the silicon region, we used a wet-etching technique because of the remarkably high selectivity between silicon

dioxide (SiO_2) and silicon (Si) with hydrogen fluoride (HF). In addition to exposing the Si region, we etched slightly more SiO_2 to reduce the overall vertical profile of the device, and ensured that the nominal thickness was approximately 60 nm. The thickness was slightly higher than required because of the limitations of the OIA Aligner. If the thickness is less than 50 nm, the contrast between the etched and unetched regions is challenging to distinguish, resulting in poor alignment during further processing.

To etch the sample using hydrogen fluoride, caution needs to be taken when utilizing acids by wearing complete PPE equipment when handling acids. To begin the process, we removed HF at a 10:1 ratio in a Teflon container, and the sample was submerged in the container for 5 minutes to allow sufficient time for HF to stabilize the etch rate of silicon dioxide (SiO_2)[81,82]. It was then rinsed in a DI water bath for 5 minutes, followed by rinsing under running DI water for a few minutes. Again, it was immersed in a second DI water bath for another 5 minutes. It was then thoroughly rinsed in running DI water for a few minutes and then slowly blow-dried with nitrogen. To determine the etch rate, the sample is again measured with a reflectometer (Nanometrics Nanospec 4150), and After determining the etch rate, the sample is again placed in the HF Container to remove the remaining silicon dioxide (SiO_2) till the device's nominal thickness is around 60 nm. The thickness profile of the silicon dioxide sample was measured using a reflectometer (Nanometrics Nanospec 4150), and the profile of the etched area was measured using a profilometer (KLA Tencor-P6 Profilometer). There should be a discrepancy of approximately 60 nm, which is the same as the thickness measured with the reflectometer, the profile height, and the initial measurement of the silicon dioxide thickness. After confirming that the silicon

(Si) was exposed, it was left overnight in air to form native silicon dioxide (SiO_2). This thin layer acts as a tunneling barrier 2.

3.6 Patterning of silicon contact pad.

The silicon window was then covered with native silicon dioxide (SiO_2). Layer, we can now create a silicon contact for the quantum-well silicon electron-transport device.

The first step was to pattern the silicon contact-pad area using photolithography.

3.6.1 Photolithography for silicon contact-pad pattern exposure.

The same quadrant was coated with a thin layer of negative photoresist NR-1000PY of approximately 1 µm, using the spin-coating technique. The quadrant was coated with a resist using a dropper to cover approximately 80% of the surface, and then rotated using a Headway Research PWM32 spin coater. The spin coater was initially spun at low rpm to spread the resist across the sample, and then at high speed to ensure a thin, even coat of resist. The spin-coating parameters were as follows:

Step 1:

500 RPM; 100 RPM/s; 5 Seconds

Step 2:

3000 RPM; 1000RPM/s; 60 Seconds

Step3:

0 RPM; 1000RPM/s; 0.1 Seconds

After spin-coating, the sample was preheated at 150°C for 60 s on a hotplate. This helps to reduce the residual solvent, which helps in adhesion to the substrate Subsequently, the samples were prepared for photolithography pattern exposure.

The samples were loaded onto an OIA aligner for the third mask. We used L marks printed from the first mask to ensure that the gate pad was slightly aligned on the top of the silicon window. After it is aligned, it is slightly shifted upward such that the third mask does not overlap the silicon window. Once properly aligned, it was firmly pressed against the hard mask and exposed to UV light to print the pattern on the sample. The exposure parameters were as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After exposing the samples, we performed a post-bake on a hot plate at 100°C, which helped smooth the concentration profile of the photoreaction product via diffusion.[77] The development process was initiated after the sample was cooled. For this purpose, we used a developer called RD-6 for 25 seconds. Teflon tweezers were used to shake the samples while developing to ensure that all the unexposed resist was removed from the sample. This was followed by rinsing in a DI water container for 5 minutes with regular stirring to prevent further development. After the first water bath, it was moved to the second DI water bath for 5 minutes with regular stirring. After the

development was completed, the sample was removed and slowly blow-dried with dry nitrogen.

3.6.2 Reactive Ion Etching – Dry Etching

The next step was to expose the Si inside the patterned area. To create a contact pad in the silicon dioxide (SiO_2) area, because the etch rate of silicon dioxide (SiO_2) to the photoresist is exceedingly high, we start etching with reactive ion etching. To ensure that we do not etch silicon, we leave a 10 nm silicon dioxide (SiO_2) margin. Ions hitting the silicon during etching can result in a rough silicon surface, which can reduce the device yield by depositing very thin films on the exposed silicon for the energy filter stack. To etch the Silicon dioxide (SiO_2), we use Technics Macro RIE-8800 equipment

Silicon dioxide (SiO_2) is etched with a gas mixture of CF_4 and O_2; as the equipment does not have endpoint detection, we used the time to calculate the etched SiO_2. To obtain a stable etch rate, the gas flow, pressure, and power were maintained constant. The reactive ion etching parameters were as follows:

Step 1:

Power: 600 W

Pressure: 160 mTorr, CF_4: 30 sccm , O_2: 3.6 sccm

Time: 86 seconds

Step 2:

Power: 350 W

Pressure: 200 mTorr, O_2: 11 sccm

Time: 60 seconds

After the etching process was completed, the photoresist was removed from the sample using acetone and isopropyl alcohol (IPA).

3.6.3 Lift-off of the photoresist.

Because the photoresist was soluble in acetone, it was immersed in an acetone bath and sonicated for 5 minutes to expedite its dissolution. After sonication, the samples were removed and rinsed quickly with isopropyl alcohol (IPA). IPA rinsing was performed after acetone to ensure that no acetone residue remained if acetone was dried on the sample surface. After rinsing, the solution was placed in isopropyl alcohol (IPA) and sonicated for 5 minutes. After sonication, the sample was removed and blow-dried slowly using dry nitrogen.

3.6.4 Photolithography for overlapping silicon contact pad pattern exposure.

The same quadrant was again coated with a thin layer of negative photoresist NR-1000PY of approximately 1 µm using the spin-coating technique. The quadrant was coated with a resist using a dropper to cover approximately 80% of the surface, and then rotated using a Headway Research PWM32 spin coater. The spin coater was initially spun at low rpm to spread the resist across the sample, and then at high speed to ensure a thin, even coat of resist. The spin-coating parameters were as follows:

Step 1:

500 RPM; 100 RPM/s; 5 Seconds

Step 2:

3000 RPM; 1000RPM/s; 60 Seconds

Step3:

0 RPM; 1000RPM/s; 0.1 Seconds

After spin-coating, the sample was preheated at 150°C for 60 s on a hotplate. This helps to reduce the residual solvent, which helps in adhesion to the substrate1 Subsequently, the samples were prepared for photolithography pattern exposure.

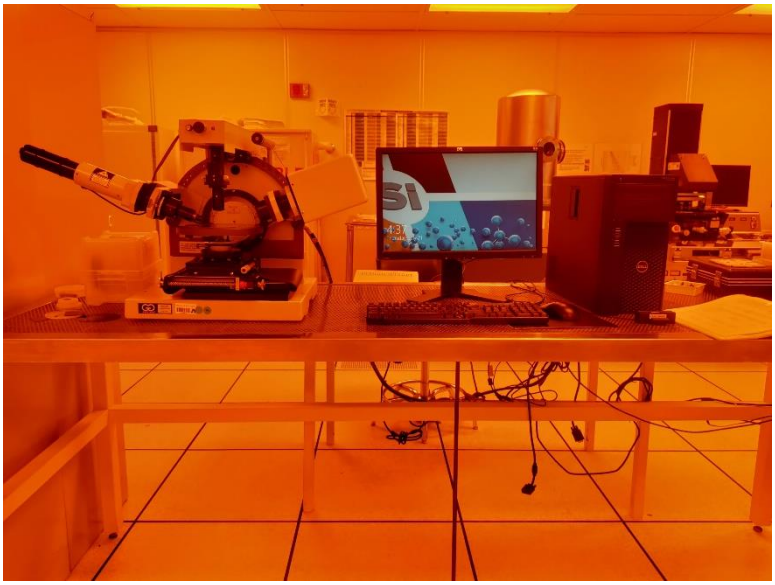


Figure 11: Ellipsometer for measuring thickness of photoresist

The samples were loaded onto an OIA aligner for the third mask. We used alignment marks printed from the third mask to ensure that the gate pad was aligned on the top of the etched area. Once properly aligned, it was firmly pressed against the hard mask and exposed to UV light to print the pattern on the sample. The exposure parameters were as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After exposing the samples, we performed a post-bake on a hot plate at 100°C, which helped smooth the concentration profile of the photoreaction product via diffusion.[77] The development process was initiated after the sample was cooled. For this purpose, we used a developer called RD-6 for 25 seconds. Teflon tweezers were used to shake the samples while developing to ensure that all the unexposed resist was removed from the sample. This was followed by rinsing in a DI water container for 5 minutes with regular stirring to prevent further development. After the first water bath, it was moved to the second DI water bath for 5 minutes with regular stirring. After the development was completed, the sample was removed and slowly blow-dried with dry nitrogen.

3.6.5 Wet Etching of silicon dioxide

To remove the remaining silicon dioxide (SiO_2) and expose the silicon region, we used a wet-etching technique because of the remarkably high selectivity between silicon dioxide (SiO_2) and silicon (Si) with hydrogen fluoride (HF).

To etch the sample using hydrogen fluoride, caution needs to be taken when utilizing acids by wearing complete PPE equipment when handling acids. To begin the process, we removed HF at a 10:1 ratio in a Teflon container, and the sample was submerged in the container for 20 seconds to remove the remaining 10 nm of silicon

dioxide (SiO_2). It was then rinsed in a DI water bath for 5 minutes, followed by rinsing under running DI water for a few minutes. Again, it was immersed in a second DI water bath for another 5 minutes. It was then thoroughly rinsed in running DI water for a few minutes and then slowly blow-dried with nitrogen. Once the silicon was exposed, it was confirmed by measuring the contact current using an I-V probe station and Agilent 4155C. The contact current for 0.01mV should be in the range 0.1 to 0.7 µA range. If the current was not within this range, we repeated lift-off, photolithography, and HF etching. Once we confirm the current, we can move to metal deposition.

3.6.6 Silicon Contact Metal Pad Deposition.

To establish a good contact on the silicon pad, we used a few metals depending on the wafer doping concentration because we did not want to create a Schottky contact but an Ohmic contact, so we could clearly observe the voltage drop across the energy-filter stack. Therefore, we used aluminum (Al) for all p-type wafers. Nickel (Ni) for n-type wafers. The metals were deposited using two different techniques.

a. E-beam deposition: For this technique, we used two types of equipment: nickel (Ni) and aluminum (Al).

    1. AJA E-Beam Deposition
    2. CHA Solution E-Beam Deposition

    In this technique, we loaded our samples into a very high vacuum and used an e-beam to heat them. Evaporated material was deposited on the sample; therefore, the deposition was not conformal. We used this technique to reduce plasma-induced defects[83,84] and gases in the deposition layer; however, it induces defects

due to X-ray radiation[85,86] in a semiconductor material. The main limitation of this method is that the material must have low vapor pressure[87].

In E-beam deposition, we load our samples in the equipment and start the pump-down process with the help of mechanical pumps and Cryogenic pumps to achieve a very high vacuum in the range of 10^{-6} mTorr Range

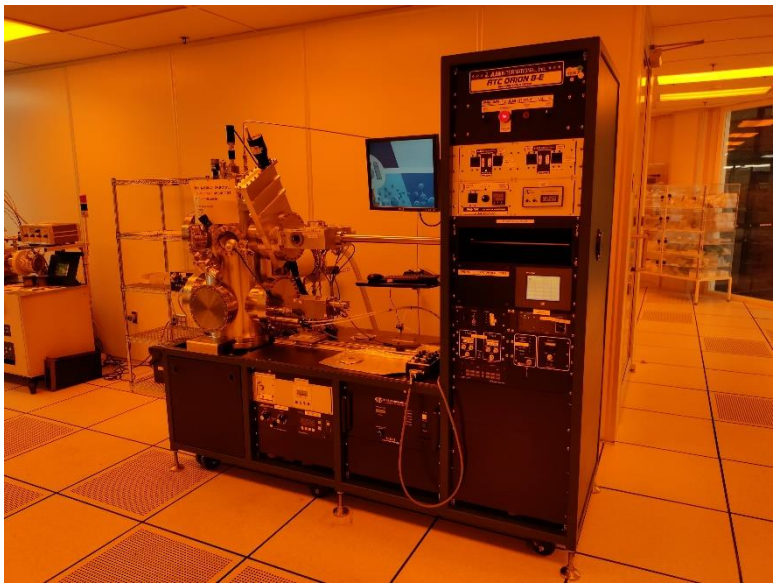


Figure 12: AJA e-beam evaporator equipment for metal deposition

b. Sputter Deposition: For this technique, we used two different types of equipment that are mainly used for aluminum deposition.

    1. AJA Sputter Deposition
    2. Homebuilt Sputter Deposition

In this technique, we loaded our sample into a very high vacuum and used high-energy ions to knock out the material from the source deposited on the sample. To generate high-energy ions, we used the plasma of an inert gas, argon (Ar), to prevent the gas from interacting with the source ions. The deposition of the material is conformal. The benefits of using sputtering over an e-beam are a better range of materials and control

over the stoichiometry of a multi-component system[88,89]. In addition, there was less radiation damage than with e-beam evaporation.

Figure 13: Homebuilt Sputter deposition equipment for DC and RF Sputter deposition

3.6.7 Lift-off of the photoresist.

Because the photoresist was soluble in acetone, it was immersed in an acetone bath and sonicated for 5 minutes to expedite its dissolution. As the layer of resist is dissolved, it also removes the material deposited on top of the resist, but the material that is still deposited on the silicon will still adder to the silicon pad. After sonication, the samples were removed and rinsed quickly with isopropyl alcohol (IPA). IPA rinsing was performed after acetone to ensure that no acetone residue remained if acetone was dried on the sample surface. After rinsing, the solution was placed in isopropyl alcohol (IPA) and sonicated for 5 minutes. After sonication, the sample was removed and blow-dried slowly using dry nitrogen. Therefore, we are now left with metal pads on the silicon.

3.6.8 RTA treatment to establish Ohmic contact

To change the Schottky nature of the Metal and Silicon contacts, we need to heat the samples to diffuse aluminum (Al) in the p-Si substrate to convert the contact area immediately below the metal pad into a p^{++}-Si substrate. As the Fermi energy band decreases[90], the Schottky contact is converted into an ohmic contact. For the n-Si substrate, we used Nickel (Ni) and heated the samples to form a Nickel Silicide (NiSi) at the junction of Nickel (Ni) and Silicon (Si). Because Nickel Silicide (NiSi)[91] has a very low barrier, it acts as an ohmic barrier. By removing the Schottky barrier, we can ensure an exact voltage drop across the energy-filter stack.

To ensure linear contact IV, we experimented with various temperatures and times needed for diffusion for all the various doping levels. We settled on a recipe that would ensure proper ohmic contact IV using an IV probe station and Agilent 4155C Semiconductor Parameter Analyzer.

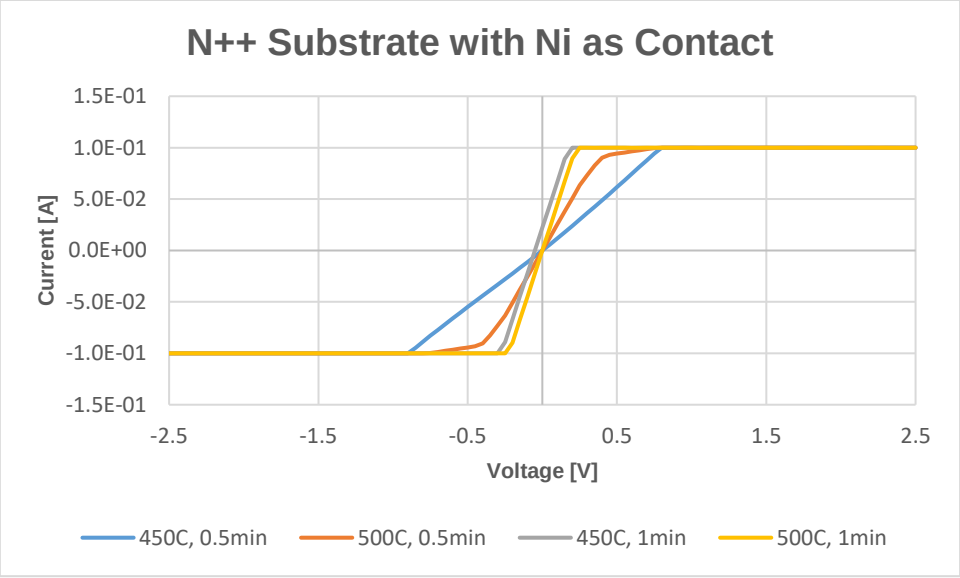


Figure 14: Si - Si IV showing Ohmic contact for N++Si contact with Ni as contact metal

For an N++ substrate, we found that 30 Seconds at both 450°C and 500°C showed an ohmic contact, but a 1 minute treatment at different temperatures showed slightly lower resistance as shown in figure 14.

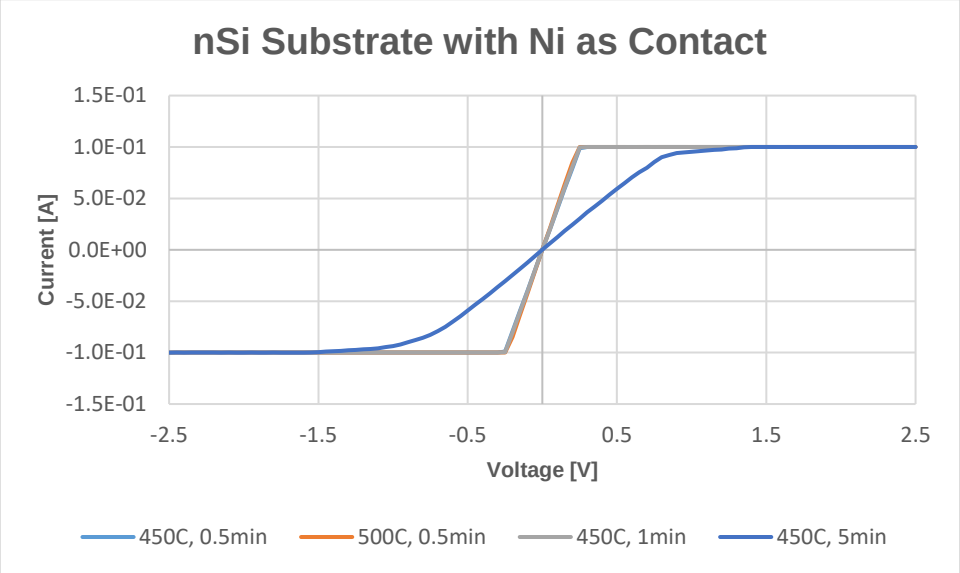


Figure 15: Si - Si IV showing Ohmic contact for n-Si contact with Ni as contact metal

For an N-Si substrate, we found that 30 Seconds at 450°C showed an ohmic contact, but 500°C at 30 Seconds or 1 minute or treatment at different temperatures showed slightly lower resistance as shown in figure 15.

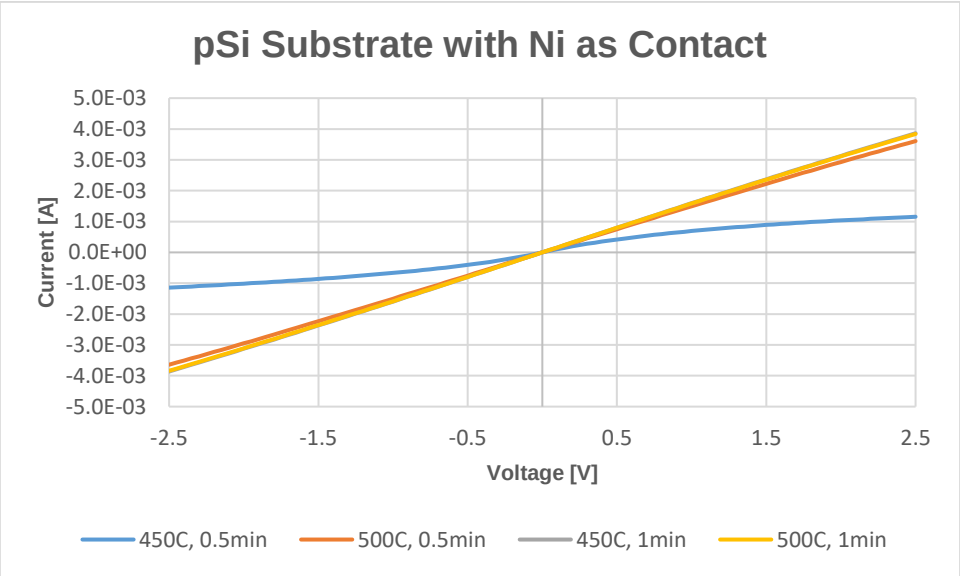


Figure 16: Si - Si IV showing Ohmic contact for p-Si contact with Ni as contact metal

For a P-Si substrate with nickel (Ni), we found that 30 Seconds at 450°C showed an ohmic contact, but at 500°C for 30 Seconds or 1 minute or treatment at different temperatures showed slightly lower resistance as shown in figure 16.

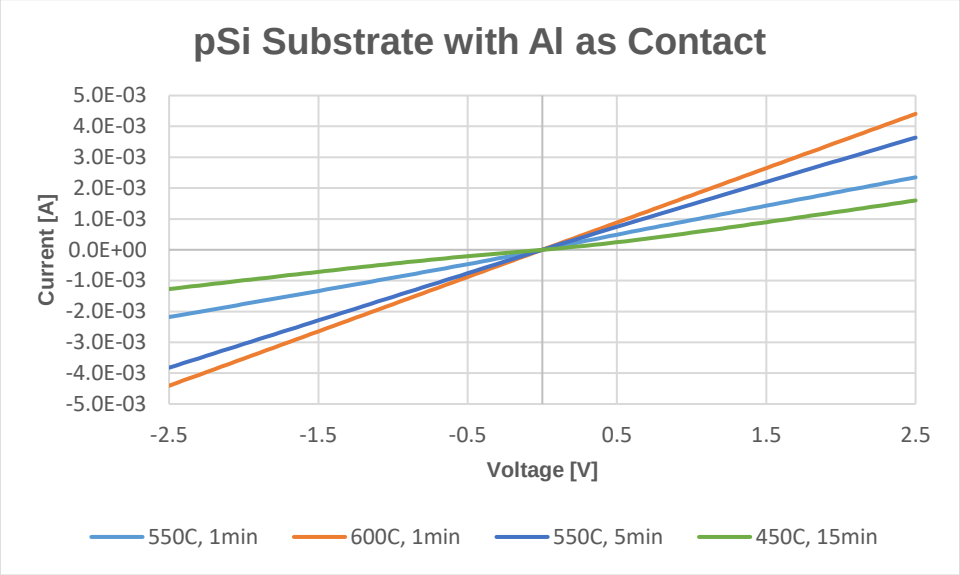


Figure 17: Si - Si IV showing Ohmic contact for p-Si contact with Al as contact metal

For a P-Si substrate with aluminum (Al), we found that 1 min at 550°C or 15 min at 450°C showed an ohmic contact, but 600°C at 1 min lower temperature for a longer treatment time at different temperatures showed a slightly lower resistance as shown in figure 17.

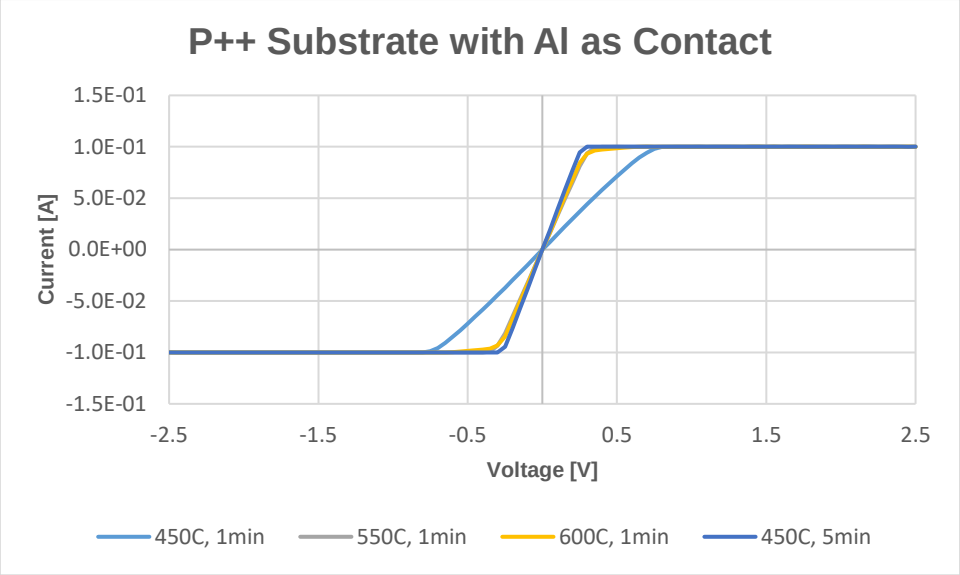


Figure 18: Si - Si IV showing Ohmic contact for P++Si contact with Al as contact metal

For a P++ substrate with aluminum (Al), we found that 1 min at both 450°C and 500°C showed an ohmic contact, but 600°C at 1 min lower temperature for a longer treatment time at different temperatures showed a slightly lower resistance. as shown in figure 18.

After comparing the different temperatures, to simplify the processing, we chose 500°C for 1 min for nickel (Ni) on N-Si and N++ Si substrates and 600°C for 1 min for aluminum (Al) on p-Si and P++ Si substrates.

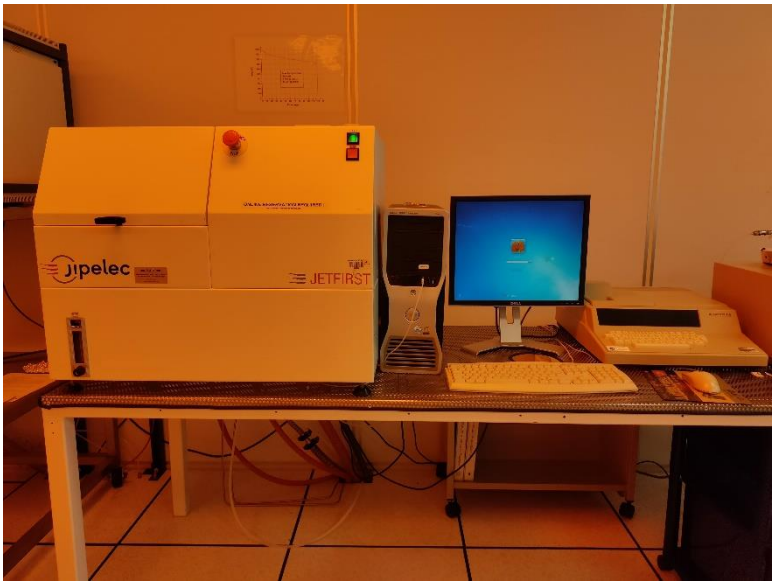


Figure 19: JetFirst Rapid Thermal Annealing for Heating samples

3.7 Building Energy Filter stack.

The energy filter stack was placed on top of the first mask silicon window in the subsequent phase. There are three layers in the energy filter stack:

Tunnelling Barrier 2: Native Silicon Dioxide

Energy Filter: Quantum Well Layer

Tunnelling Barrier 1: Silicon Nitride or Aluminum Oxide

The first mask window region already has the first layer of the energy filter stack, and after exposing the silicon, we allowed a native silicon dioxide film, which was grown in Section 3.5.5 before the third mask step.

3.7.1 Quantum well layer deposition.

The second layer of the energy-filter stack is a quantum well. We selected varied materials for the formation of the quantum well layers, Cr_2O_3 and SnO_2, and found that the tin oxide (SnO_2) quantum well layers showed the best results. Initially, instead of using tin oxide (SnO_2), we used to deposit 1.5 nm tin using the e-beam deposition method as the melting temperature of tin (Sn) is low. The CHA E-beam Solution was used. It was then oxidized on a hot plate at 200°C in open air. However, instead of a 1.5 nm tin oxide film, the tin oxide agglomerated and formed a 5 nm spherical ball shape. Therefore, we decided to move towards thin tin oxide (SnO_2) deposition using the AJA Sputter deposition equipment. The deposition parameters were as follows:

SnO_2 Spark Step 1:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 30 sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

SnO_2 Spark Step 2:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 15 sccm; O_2: 6sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

SnO_2 Deposition

Power: 40 W

Deposition Pressure: 5 mTorr

Ar: 15 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: 217.39 s (3nm), 289.85 s (4nm),362.31 s (5nm)

To determine the deposition rate, we performed deposition on a dummy sample for 600 seconds, and the deposited thickness was measured using an Ocean Optics Reflectometer. The measured thickness was to be 8.28 nm with a 98% fit. The deposition rate is 0.0138 nm/s. This deposition rate was used to deposit different tin oxide thicknesses from 1 nm, 2 nm, 3 nm, 4 nm, 5 nm, 7 nm, and 9 nm for different samples to study the variation within the quantum well thickness and energy level.

Figure 20: Ocean Optics Reflectometer for thickness measurement

3.7.2 Tunneling Barrier 1 deposition.

Once the quantum well layer deposition is completed, we will proceed to deposit Tunneling Barrier layer 1. We used silicon nitride (Si_3N_4) or aluminum oxide (Al_2O_3) as tunneling Barrier 1 material. The silicon nitride tunneling barrier was deposited using AJA Sputter deposition equipment with the following parameters:

Si_3N_4 Spark Step 1:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 15 sccm; N_2: 6sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

Si_3N_4 Deposition

Power: 150 W

Deposition Pressure: 5 mTorr

Ar: 15 sccm;

To determine the deposition rate, we performed a deposition on a dummy sample, and the deposited thickness was measured using a P-6 Profilometer. A deposition rate of 0.0159 nm/s is obtained for the dummy sample.

For aluminum oxide tunneling barrier, the samples were shipped to Northwestern University to Tyler Gish from Dr Hersam's group using Atomic Layer deposition[92–95] equipment.

The thickness deposited was 0.5 nm and 1.0 nm of aluminum oxide or silicon nitride for different samples with similar thicknesses in the quantum well layer. The thickness of the tunnelling barrier was varied to study the effect of the tunnelling barrier thickness on the shift in the voltage distribution across the energy filter stack and to gain control over the voltage at which we observed the jump. Once the energy-filter stack was deposited, we moved to the next stage of patterning the source and drain metal pads.

We also prepared a few samples without any tunnelling barrier 1.

3.8 Source and Drain Contact Metal Pad Deposition.

After completing the energy-filter stack, the sample was patterned using a second mask. We can now create source and drain Pads to test these devices. In the Source

and Darin pads, there is a variation in the distance between the Source and Drain pads with increasing distance from row 1 to row 7.

3.8.1 Photolithography for overlapping silicon contact pad pattern exposure.

The same samples were coated with a thin layer of negative photoresist NR-1000PY of approximately 1 µm, using the spin-coating technique. The quadrant was coated with a resist using a dropper to cover approximately 80% of the surface, and then rotated using a Headway Research PWM32 spin coater. The spin coater was initially spun at low rpm to spread the resist across the sample, and then at high speed to ensure a thin, even coat of resist. The spin-coating parameters were as follows:

Step 1:

500 RPM; 100 RPM/s; 5 Seconds

Step 2:

3000 RPM; 1000RPM/s; 60 Seconds

Step3:

0 RPM; 1000RPM/s; 0.1 Seconds

After spin-coating, the sample was preheated at 150°C for 60 s on a hotplate. This helps to reduce the residual solvent, which helps in adhesion to the substrate1 Subsequently, the samples were prepared for photolithography pattern exposure.

The samples were then loaded onto an OIA aligner for the second mask. Alignment marks printed from the first mask were used to ensure that the source and drain pads were aligned at the top of the silicon window. Once properly aligned, it was firmly

pressed against the hard mask and exposed to UV light to print the pattern on the sample. The exposure parameters were as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 10.2 seconds

Dose: 200 mJ/cm^2

After exposing the samples, we performed a post-bake on a hot plate at 100°C, which helped smooth the concentration profile of the photoreaction product via diffusion.[77] The development process was initiated after the sample was cooled. For this purpose, we used a developer called RD-6 for 25 seconds. Teflon tweezers were used to shake the samples while developing to ensure that all the unexposed resist was removed from the sample. This was followed by rinsing in a DI water container for 5 minutes with regular stirring to prevent further development. After the first water bath, it was moved to the second DI water bath for 5 minutes with regular stirring. After the development was completed, the sample was removed and slowly blow-dried with dry nitrogen.

3.8.2 Source - Drain Contact Metal Pad Deposition.

To make contact with our energy filter stack, we used can use different metals depending on their work function of the metals as shown in Figure 22. In the current configuration, we use chromium (Cr) metal, as its work function[96,97] is 4.5 eV. Because chromium has a low melting temperature, the e-beam deposition technique can be

used. For this technique, we used two different types of equipment that are mainly used for chromium (Cr) deposition.

1. AJA E-Beam Deposition
2. CHA Solution E-Beam Deposition

In this technique, we loaded our samples into a very high vacuum and used an e-beam to heat them. Evaporated material was deposited on the sample; therefore, the deposition was not conformal. We used this technique to reduce plasma-induced defects and gases in the deposition layer; however, it induces defects due to X-ray radiation in a semiconductor material. The main limitation of this method is that the material must have low vapor pressure.

Figure 21: CHA E-Beam Solution for metal deposition

In E-beam deposition, we loaded our samples into the equipment and started the pump-down process with the help of mechanical pumps and cryogenic pumps to achieve a very low vacuum in the range of 10^{-6} mTorr Range.

	Ag	***Al***	***Au***	***Cr***	***Ni***	***Pt***	***W***
ϕ_M(in vacuum)	4.3	4.25	4.8	4.5	4.5	5.3	4.6
n-Ge	0.54	0.48	0.59		0.49		0.48
p-Ge	0.5		0.3				
n-Si	0.78	0.72	0.8	0.61	0.61	0.9	0.67
p-Si	0.54	0.58	0.34	0.5	0.51		0.45
n-GaAs	0.88	0.8	0.9			0.84	0.8
p-GaAs	0.63		0.42				

Figure 22: Table of Various Metal work function[98]

3.8.3 Lift-off of the photoresist.

Because the photoresist was soluble in acetone, it was immersed in an acetone bath and sonicated for 5 minutes to expedite its dissolution. As the layer of resist is dissolved, it also removes the material deposited on top of the resist, but the material that is still deposited on the silicon will still adder to the silicon pad. After sonication, the samples were removed and rinsed quickly with isopropyl alcohol (IPA). IPA rinsing was performed after acetone to ensure that no acetone residue remained if acetone was dried on the sample surface. After rinsing, the solution was placed in isopropyl alcohol (IPA) and sonicated for 5 minutes. After sonication, the sample was removed and blow-dried slowly using dry nitrogen. Therefore, we are now left with metal pads on the silicon.

3.9 RTA for making Quantum well Polycrystalline.

Due to the discrete energy level alignment with the silicon conduction band, it was found that annealing the samples at particular temperatures and lengths caused a rapid fast current spike at particular voltages, demonstrating cold-electron transport. In order to prepare the samples for IV measurements, the RTA chamber heated them. In order to investigate the producing changes of the abrupt, sharp jumps with various annealing conditions, the sample was inserted into the RTA Chamber and heated at various temperatures and periods. The samples may now be processed for electrical characterization because they are ready.

The SnO_2 layer is visible in the TEM picture after Sn was deposited using an e-beam, annealed at 200°C for one hour on a hot plate, and then annealed in an RTA at 500°C for 30 minutes following fabrication. The quantum well created by this method results in an uneven layer thickness of around 5 nm SnO_2, and it also provides very little control over the actual thickness of the quantum well layer.

3.10 Passivation Layer Deposition.

The next step is to deposit the passivation layer to shield the electrodes during subsequent processing once the metal has been deposited. With a thickness of 200 nm, silicon dioxide was used as a passivation layer, and it was deposited using AJA Sputter deposition equipment under the following parameters as follows:

SiO_2 Spark Step 1:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 15 sccm; O_2: 6sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

SiO_2 Deposition

Power: 150 W

Deposition Pressure: 5 mTorr

Ar: 30 sccm; O_2: 6sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: 31,348 seconds

The deposition time for 1 nm silicon dioxide was calculated, from the deposition rate of 0.00637 nm/s obtained for a dummy sample deposition, to be 7837 seconds.

3.11 Gold Contact Metal Pad Deposition.

The fabrication of the device was completed. The next step was to establish a good contact between the source, drain, and gate pads. We used gold to ensure good contact, and nickel (Ni) as a bonding layer between different metals to ensure good

contact with various metals. Instead of covering the entire pad, we deposited a small circle on the pads.

3.11.1 Photolithography for overlapping silicon contact pad pattern exposure.

The same samples were coated with a thin layer of negative photoresist NR-1000PY of approximately 1 µm, using the spin-coating technique. The quadrant was coated with a resist using a dropper to cover approximately 80% of the surface, and then rotated using a Headway Research PWM32 spin coater. The spin coater was initially spun at low rpm to spread the resist across the sample, and then at high speed to ensure a thin, even coat of resist. The spin-coating parameters were as follows:

Step 1:

500 RPM; 100 RPM/s; 5 Seconds

Step 2:

3000 RPM; 1000RPM/s; 60 Seconds

Step3:

0 RPM; 1000RPM/s; 0.1 Seconds

After spin-coating, the sample was preheated at 150°C for 60 s on a hotplate. This helps to reduce the residual solvent, which helps in adhesion to the substrate1 Subsequently, the samples were prepared for photolithography pattern exposure.

The samples were then loaded onto an OIA aligner for the second mask. Alignment marks printed from the first mask were used to ensure that the source and drain pads were aligned at the top of the silicon window. Once properly aligned, it was firmly

pressed against the hard mask and exposed to UV light to print the pattern on the sample. The exposure parameters were as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 10.2 seconds

Dose: 200 mJ/cm^2

After exposing the samples, we performed a post-bake on a hot plate at 100°C, which helped smooth the concentration profile of the photoreaction product via diffusion.[77] The development process was initiated after the sample was cooled. For this purpose, we used a developer called RD-6 for 25 seconds. Teflon tweezers were used to shake the samples while developing to ensure that all the unexposed resist was removed from the sample. This was followed by rinsing in a DI water container for 5 minutes with regular stirring to prevent further development. After the first water bath, it was moved to the second DI water bath for 5 minutes with regular stirring. After the development was completed, the sample was removed and slowly blow-dried with dry nitrogen.

3.11.2 Via holes etching

The electrodes' metal pads in the pattern region must then be exposed. The passivation layer on the rest of the device will safeguard this area while being utilized to probe the device for I-V characteristic measurements. Therefore, it will be necessary

to expose the metal in the pattern region. Reactive ion etching is used in the Technics Macro RIE - 8800 apparatus to remove the silicon dioxide that is present in the design.

By employing the CF_4/O2 etch recipe and varying the etch time, the silicon dioxide etch time is determined by optimizing the etch rate. Plotting the various etch periods and thicknesses, it is determined that Silicon dioxide has an etch rate of 0.7 nm/s. We don't need to preserve any margin in this method since the selectivity for SiO_2 v/s Metal is quite good. The Reactive Ion Etching Parameters were as follows:

Step 1:

Power: 600 W

Pressure: 160 mTorr, CF_4: 30 sccm , O_2: 3.6 sccm

Time: 180 seconds

Step 2:

Power: 350 W

Pressure: 200 mTorr, O_2: 11 sccm

Time: 60 seconds

However, as the samples are processed by small regions. The photoresist also gets etched away in this process and only a vary thin layer of photo resist is present on the samples. We repeat the photolithography step.

3.11.3 Lift-off of the photoresist.

Because the photoresist was soluble in acetone, it was immersed in an acetone bath and sonicated for 5 minutes to expedite its dissolution. As the layer of resist is dissolved, it also removes the material deposited on top of the resist, but the material that is still deposited on the silicon will still adder to the silicon pad. After sonication, the samples were removed and rinsed quickly with isopropyl alcohol (IPA). IPA rinsing was performed after acetone to ensure that no acetone residue remained if acetone was dried on the sample surface. After rinsing, the solution was placed in isopropyl alcohol (IPA) and sonicated for 5 minutes. After sonication, the sample was removed and blow-dried slowly using dry nitrogen. Therefore, we are now left with metal pads on the silicon.

3.11.4 Photolithography for overlapping silicon contact pad pattern exposure.

The same samples were coated with a thin layer of negative photoresist NR-1000PY of approximately 1 µm, using the spin-coating technique. The quadrant was coated with a resist using a dropper to cover approximately 80% of the surface, and then rotated using a Headway Research PWM32 spin coater. The spin coater was initially spun at low rpm to spread the resist across the sample, and then at high speed to ensure a thin, even coat of resist. The spin-coating parameters were as follows:

Step 1:

500 RPM; 100 RPM/s; 5 Seconds

Step 2:

3000 RPM; 1000RPM/s; 60 Seconds

Step3:

0 RPM; 1000RPM/s; 0.1 Seconds

After spin-coating, the sample was preheated at 150°C for 60 s on a hotplate. This helps to reduce the residual solvent, which helps in adhesion to the substrate1 Subsequently, the samples were prepared for photolithography pattern exposure.

The samples were then loaded onto an OIA aligner for the second mask. Alignment marks printed from the first mask were used to ensure that the source and drain pads were aligned at the top of the silicon window. Once properly aligned, it was firmly pressed against the hard mask and exposed to UV light to print the pattern on the sample. The exposure parameters were as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 10.2 seconds

Dose: 200 mJ/cm^2

After exposing the samples, we performed a post-bake on a hot plate at 100°C, which helped smooth the concentration profile of the photoreaction product via diffusion.[77] The development process was initiated after the sample was cooled. For this purpose, we used a developer called RD-6 for 25 seconds. Teflon tweezers were used to shake the samples while developing to ensure that all the unexposed resist was removed from the sample. This was followed by rinsing in a DI water container for 5 minutes with regular stirring to prevent further development. After the first water bath, it was moved to the second DI water bath for 5 minutes with regular stirring. After the

development was completed, the sample was removed and slowly blow-dried with dry nitrogen. After Confirming a good contact with is present on the Etched via holes with the help of IV probe station and Agilent 4155C Semiconductor Parameter analyzer. We start the process for gold pads deposition

3.11.5 Gold Contact Metal Pad Deposition.

Establishing a good contract between the source, drain, and gate pads. We used gold to ensure good contact, and nickel (Ni) as a bonding layer[99–101] between different metals to ensure good contact with various metals. Instead of covering the entire pad, we deposited a small circle on the pads.

For this technique, we used two different types of equipment, mainly used for nickel (Ni) and gold (Au) deposition.

1. AJA E-Beam Deposition
2. CHA Solution E-Beam Deposition

In this technique, we loaded our samples into a very high vacuum and used an e-beam to heat them. Evaporated material was deposited on the sample; therefore, the deposition was not conformal. We used this technique to reduce plasma-induced defects and gases in the deposition layer; however, it induces defects due to X-ray radiation in a semiconductor material. The main limitation of this method is that the material must have low vapor pressure.

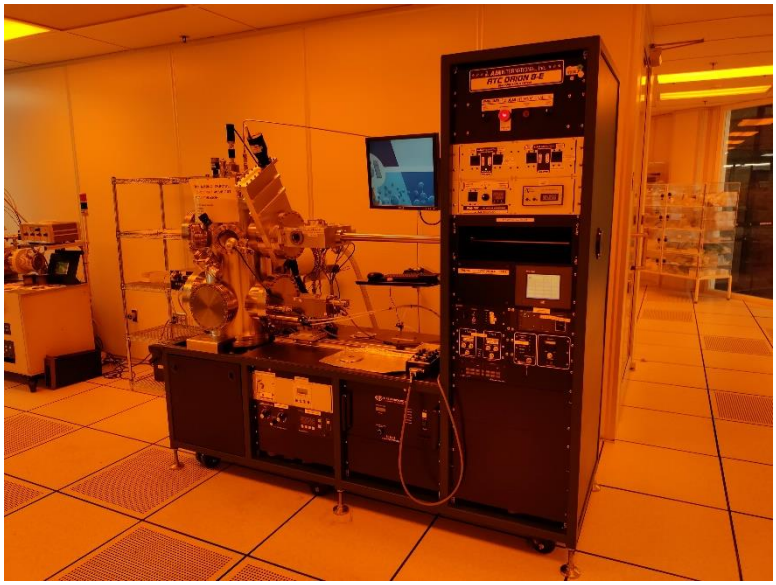


Figure 23: AJA Sputter Deposition equipment for DC and RF Sputtering

In E-beam deposition, we loaded our samples into the equipment and started the pump-down process with the help of mechanical pumps and cryogenic pumps to achieve a very low vacuum in the range of 10^{-6} mTorr Range.

3.11.6 Lift-off of the photoresist.

Because the photoresist was soluble in acetone, it was immersed in an acetone bath and sonicated for 5 minutes to expedite its dissolution. As the layer of resist is dissolved, it also removes the material deposited on top of the resist, but the material that is still deposited on the silicon will still adder to the silicon pad. After sonication, the samples were removed and rinsed quickly with isopropyl alcohol (IPA). IPA rinsing was performed after acetone to ensure that no acetone residue remained if acetone was dried on the sample surface. After rinsing, the solution was placed in isopropyl alcohol (IPA) and sonicated for 5 minutes. After sonication, the sample was removed and blow-dried slowly using dry nitrogen. Therefore, we are now left with metal pads on the silicon.

Chapter 4: Result and discussion

4.1 Electrical Characterization

After completing the device fabrication process, we started with IV measurements using an IV probe station with an Agilent 4155C Semiconductor Parameter analyzer. Three probes were used in the probe-station arrangement inside the cleanroom. The probes were linked to a parameter analyzer using a connection hub. Individual SMU units were attached to the probes and connected to a parameter analyzer.

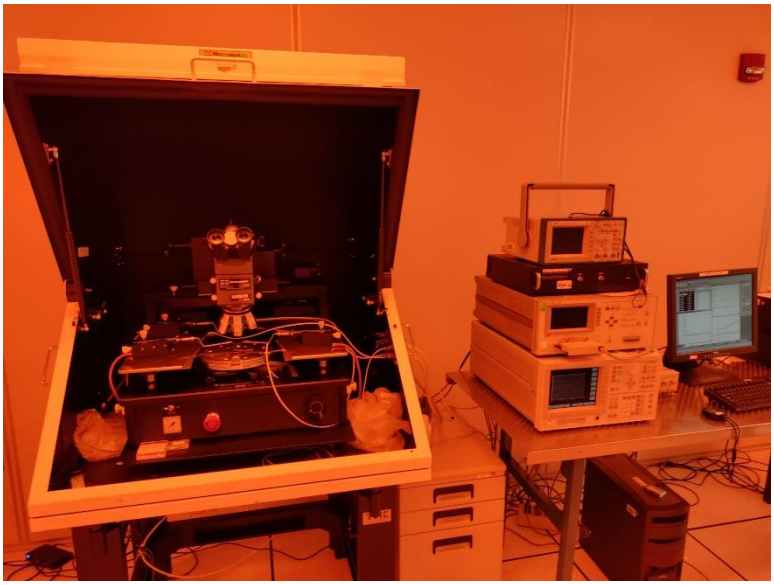


Figure 24: IV Probe station with Agilent 4155C equipment for IV measurement

The majority of the devices were concerned with moisture development during measurement, according to Agilent 4155C current-voltage measurements taken within the cleanroom. As the probe tips come into contact with the source metal surface, moisture begins to develop and spread outward. We believe that the fast heating and cooling of cold electrons as they move from the QW layer to the silicon surface causes moisture to develop owing to the Peltier effect.

Therefore, further measurements were performed under vacuum using the Agilent ES2708 apparatus and the Janis ST-500 Probe station at the Nanofab lab to prevent the formation of moisture on good devices during the measurement process. IV measurements were performed at low temperatures using a liquid nitrogen tank and a LakeShore 331 temperature controller, which uses a heater to maintain the temperature at the set point and controls the ramp rate of cooling and heating to avoid thermal shock to the sample.

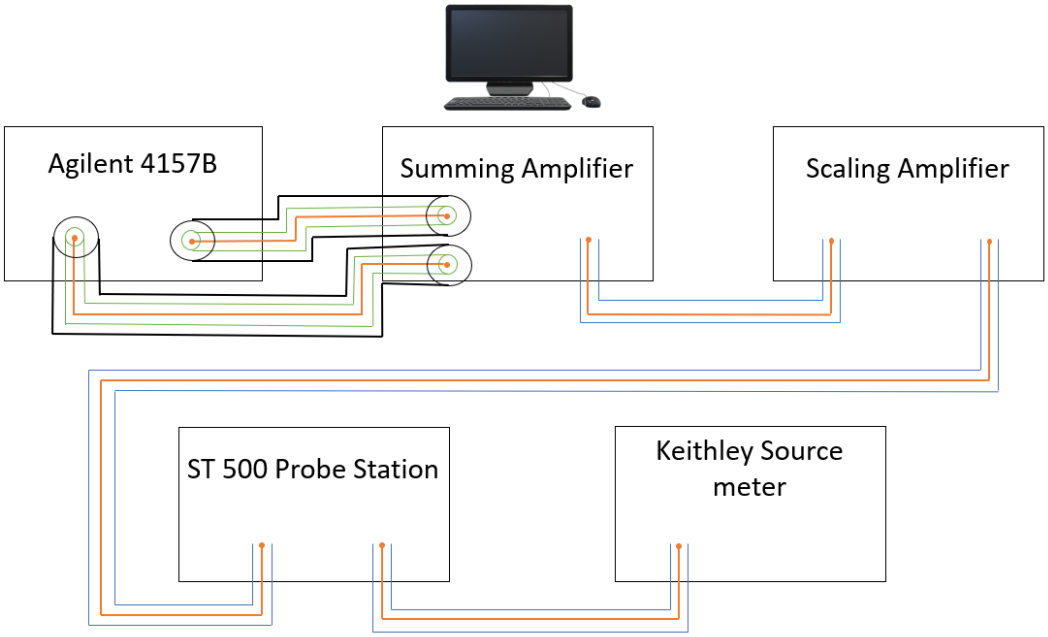


Figure 25: Wiring diagrams of IV measurement equipment

After carefully unscrewing the top lid and inner chamber cover, dry nitrogen was used to evacuate the chamber before placing the sample in the ST-500 probe-station measurement chamber. To avoid contamination of the measuring chamber, sample loading and unloading were performed while wearing a complete face mask, hairnet, and nitrile gloves. Following sample loading, the chamber was purged with dry nitrogen for 10 min to remove as much moisture as possible from the chamber after the lids were returned. During the purging process, we maintained a mild vacuum using a dry mechanical pump and controlled the flow of dry nitrogen to assist in the

removal of moisture from the chamber. Subsequently, the purging process was completed. The dry nitrogen flow was closed, and the turbo-molecular pump was turned on to obtain a high vacuum before proceeding with the low-temperature measurements. Prior to the tests, the Agilent ES2708 Semiconductor parameter analyzer was turned on for 30 min to warm the system up for the best measurements.

We observed poor contact IV in our initial measurements, which meant that there was insufficient contact between the probe tips and contact bond pads. We attempted to clean the probe tips with methanol, using probe tips to scrape the contact surface and changing the probe tips. The cleaned tips provided adequate contact IV for the chromium metal bond pads and were effective. To obtain accurate contact IV readings, methanol was used to clean the probe tips after a few measurements.

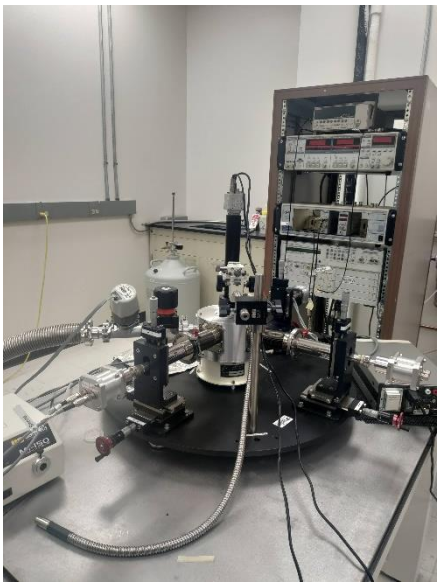


Figure 26: Current-voltage measurement setup for Vacuum measurement of devices

We hypothesized that this was caused by the thin (1–2 nm) chromium oxide layer that developed on top of the chromium metal after it was exposed to air for a while. The pressure applied to the probe tips caused them to penetrate the thin layer of chromium oxide when in contact with it. However, the probes formed a layer of chromium oxide

when they were removed. The tips were completely covered by the chromium oxide coating after a few iterations, which lowered the contact IV current values. The probe tips were cleaned using a methanol squeeze bottle before being rinsed and scrubbed with a lint-free cleanroom paper. To solve this problem, gold was added on top of all the electrodes with 5 nm Nickel as the bonding between gold for different metals and using gold-coated tips.

4.2 Ohmic Contact

After Completing the Silicon pad metal deposition, as the contact was with the metal on the semiconductor, it resulted in Schottky contact. However, because the Schottky contact can cause a voltage drop across the source and the silicon pad, it is difficult to calculate the voltage drop across the energy filter stack. To avoid this, we decided to convert the Schottky contact to an Ohmic contact by heating the sample with the help of a Jetfirst Lamp furnace - rapid thermal processing at a controlled ramp rate. A precise voltage drop across the energy-filter stack can be achieved by eliminating the Schottky barrier.

For the p-type substrate, we heated the samples to diffuse aluminum (Al) in the p-Si substrate, which transformed the contact region just underneath the metal pad into a p++-Si substrate, changing the Schottky nature of the Metal and Silicon connections. Schottky contacts become ohmic when the Fermi energy band narrows.

For the n-type substrate, we heated the samples to form Nickel Silicide (NiSi) at the junction of nickel (Ni) and silicon (n-Si) to create a nickel substrate (Si). Nickel Silicide (NiSi) serves as an ohmic barrier owing to its extremely low barrier.

We tested different diffusion durations and temperatures for all doping levels to ensure linear contact IV. With the use of an IV probe station and an Agilent 4155C Semiconductor Parameter Analyzer, we decided on a formula that would guarantee adequate ohmic contact IV.

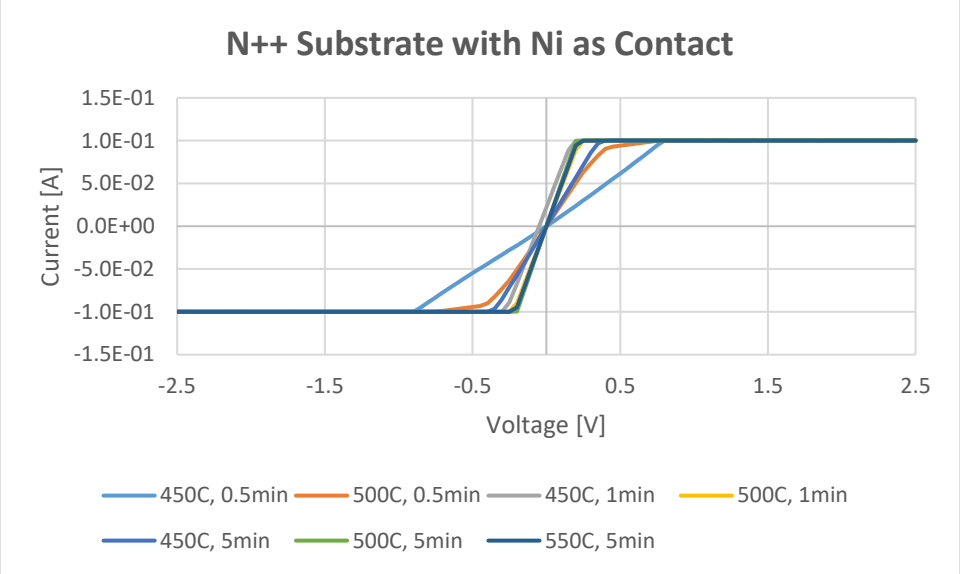


Figure 27: Si - Si IV showing Ohmic contact for N++Si contact with Ni as contact metal

For an N++ substrate, we found that 30 Seconds at both 450°C and 500°C showed an ohmic contact, but a 1-minute treatment at different temperatures showed slightly lower resistance. Increasing the temperature and time did not result in a significant reduction in the resistance as shown in figure 27.

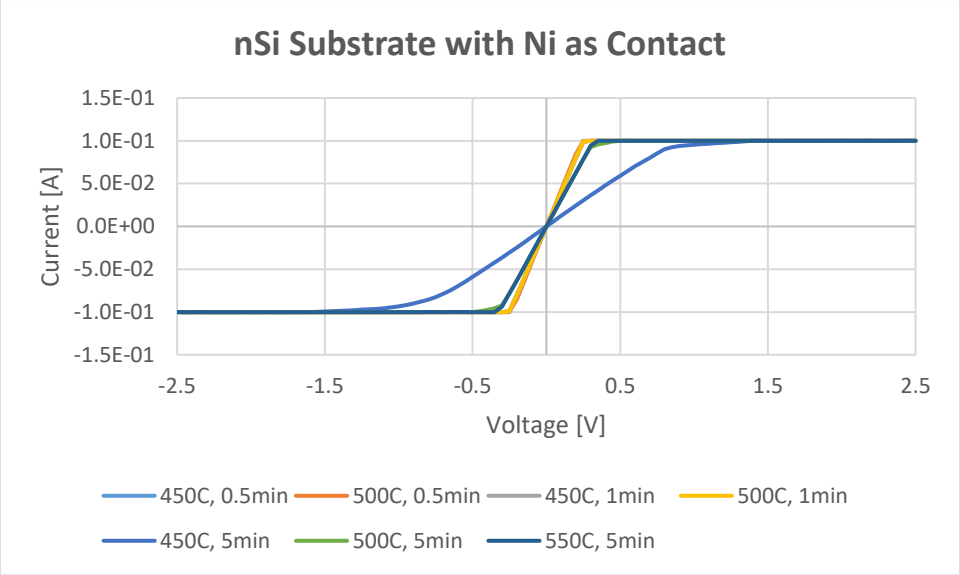
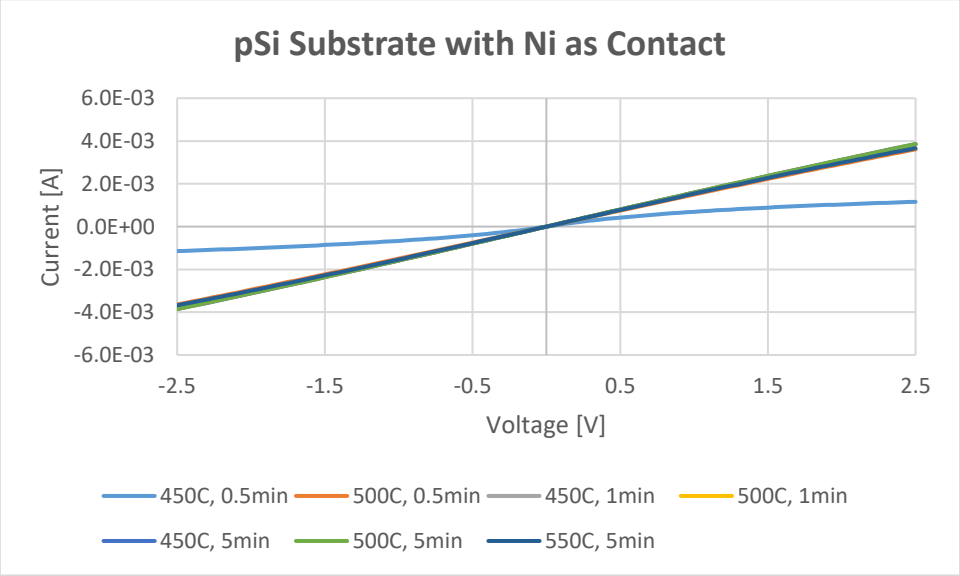


Figure 28: Si - Si IV showing Ohmic contact for n-Si contact with Ni as contact metal

For the N-Si substrate, we found that 30 Seconds at 450°C showed an ohmic contact, but 500°C at 30 Seconds or 1 minute or treatment at different temperatures showed slightly lower resistance. Increasing the temperature and time did not result in a significant reduction in the resistance as shown in figure 28.



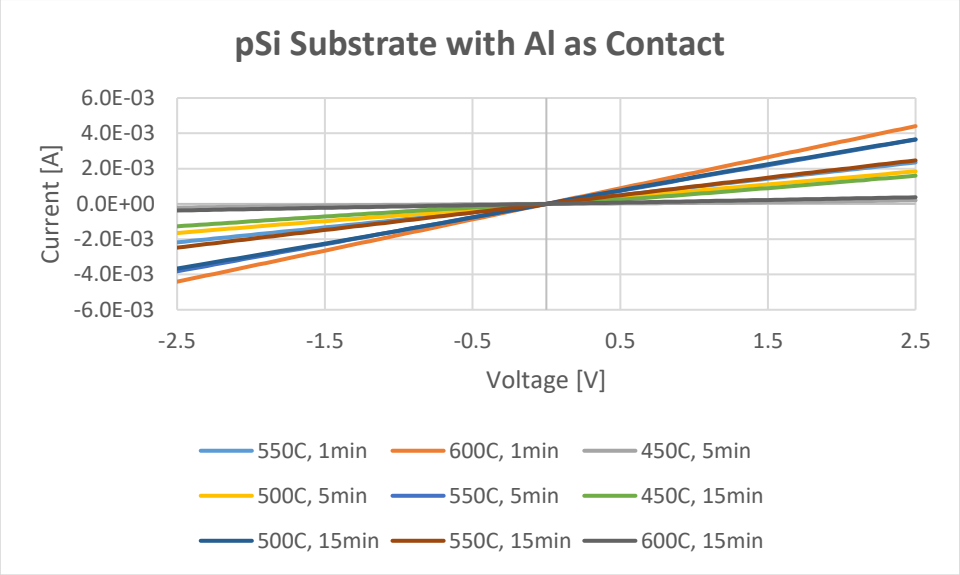


Figure 29: Si - Si IV showing Ohmic contact for p-Si contact with Ni as contact metal (Top) with Al as contact metal (bottom)

For a P-Si substrate with nickel (Ni), we found that 30 Seconds at 450°C showed an ohmic contact, but at 500°C for 30 Seconds or 1 minute or treatment at different temperatures showed slightly lower resistance. Increasing the temperature and time did not result in a significant reduction in the resistance as shown in figure 29.

For a P-Si substrate with aluminum (Al), we found that 1 min at 550°C or 15 min at 450°C showed an ohmic contact, but 600°C at 1 min lower temperature for a longer treatment time at different temperatures showed a slightly lower resistance. We observed some degradation in the ohmic content when the heat treatment time was increased. A shorter time and higher temperature resulted in lower resistance.

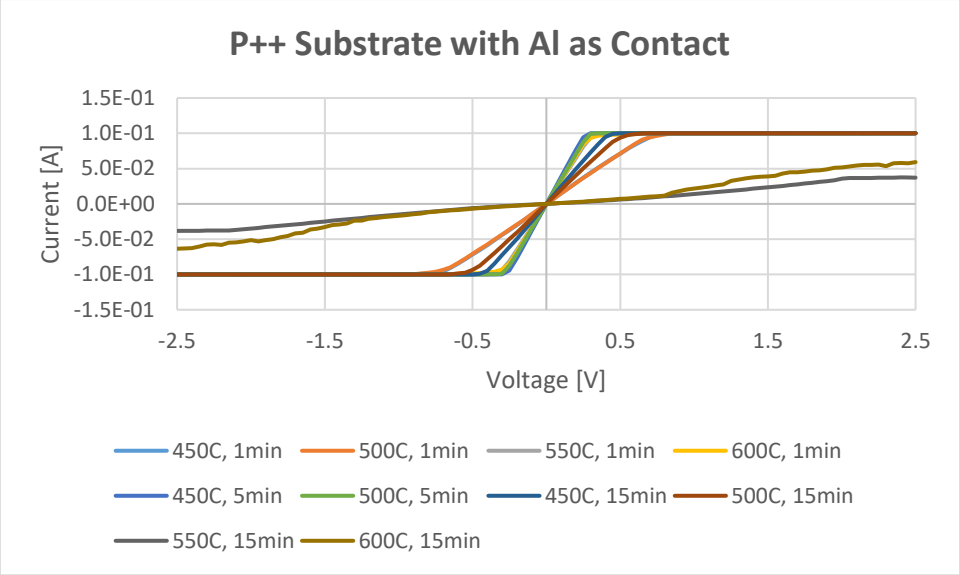


Figure 30: Si - Si IV showing Ohmic contact for P++Si contact with Al as contact metal

For a P++ substrate with aluminum (Al), we found that 1 min at both 450°C and 500°C showed an ohmic contact, but 600°C at 1 min lower temperature for a longer treatment time at different temperatures showed a slightly lower resistance. Increasing the temperature and time did not result in a significant reduction in the resistance, and a long time resulted in degradation in terms of the ohmic contact as shown in figure 30.

After comparing the different temperatures, to simplify the processing, we chose 500°C for 1 min for nickel (Ni) on N-Si and N++ Si substrates and 600°C for 1 min for aluminum (Al) on p-Si and P++ Si substrates.

4.3 First device with promising results

The first devices with successful results were created using an energy-filter stack in the following configurations:

Native SiO_2 (1.5 nm-2 nm) with 1.5 nm Sn deposited by E-beam evaporation and 200°C for 1 hour on a hotplate, and Al_2O_3 deposited by ALD at 0.5 nm. Following manufacturing, the sample was heated in RTA at 450°C for 15 minutes to create an ohmic silicon metal-to-silicon contact.

Silicon bias shows that the conduction band of silicon and the discrete energy level of the quantum well were aligned, causing a sudden rise in the source-silicon current. The differential conductance of this device produced a full-width half-maximum of 5 mV, which is equivalent to an effective electron temperature of 1.667 K. However, the resolution of the measurement was 5 mV. Therefore, to remove this restriction, higher-resolution measurements are required. In addition, as the probe tips make contact with the source metal surface, moisture begins to develop there and spreads outward. We believe that the fast heating and cooling of cold electrons as they move from the QW layer to the silicon surface causes this moisture to develop owing to the Peltier effect. This provided further proof that the cold-electron current jumps were genuine.

Therefore, further measurements were performed under vacuum using the Agilent ES2708 apparatus and the Janis ST-500 Probe station at the Nanofab lab to prevent the formation of moisture on good devices during the measurement process.

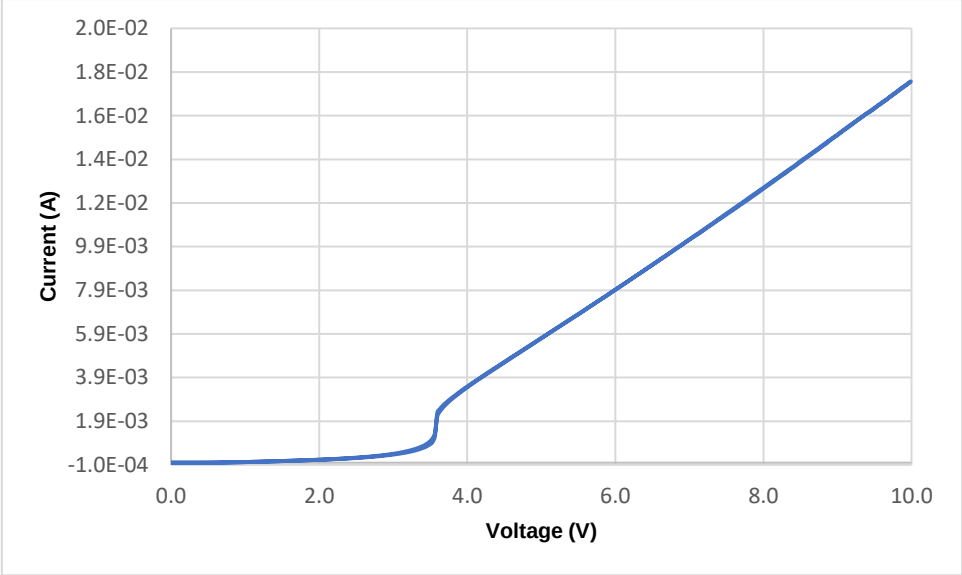


Figure 31: Source-Silicon IV through SnO_2 Quantum Well Energy filter (EF Stack consists of Native SiO_2/ QW: 1.5nm Sn heated at 200°C -1 hr on a hot plate/ 0.5nm ALD deposited Al_2O_3)

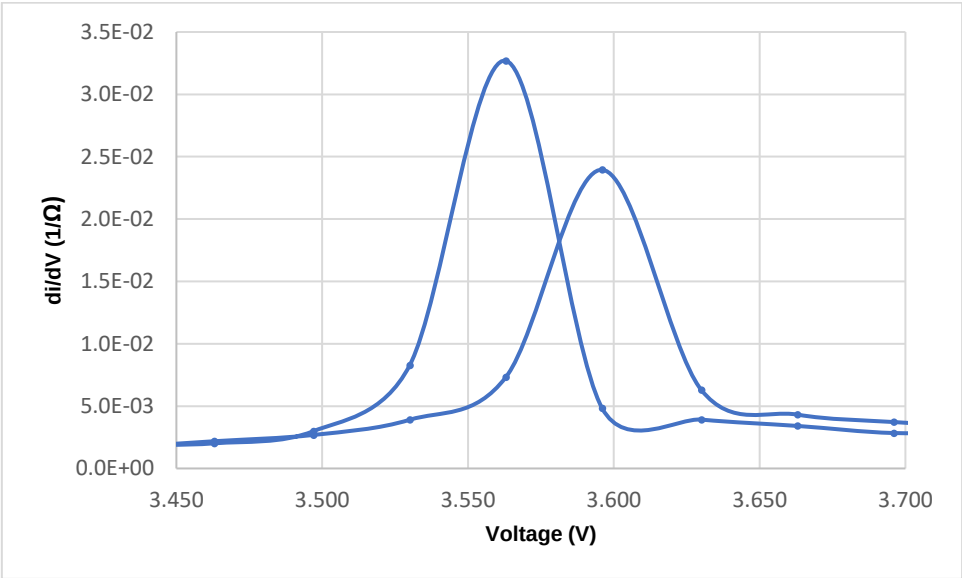


Figure 32: Differential conductance plot for Source-Silicon IV through SnO_2 Quantum Well Energy filter (EF Stack consists of Native SiO2/ QW: 1.5nm Sn heated at 200°C -1 hr on a hot plate/ 0.5nm ALD deposited Al_2O_3) (Forward and reverse measurements show a peak shift of 10mV)

High-resolution measurements were performed using a Keithley Model 6430 Sub-Femtoamp Remote Source Meter and Agilent ES2708 Semiconductor Parameter Analyzer. With this configuration, we were able to measure with 0.25mV. Prior to usage, the Agilent Semiconductor Parameter Analyzer was powered on for 30 minutes to provide the best possible reading. Using low-noise wires, all wiring (coaxial and triaxial) was completed (Keithley, Inc.). As shown in Figure 25. To prevent any additional capacitance or resistance, all cables were built internally utilizing connectors from Keithley Inc.

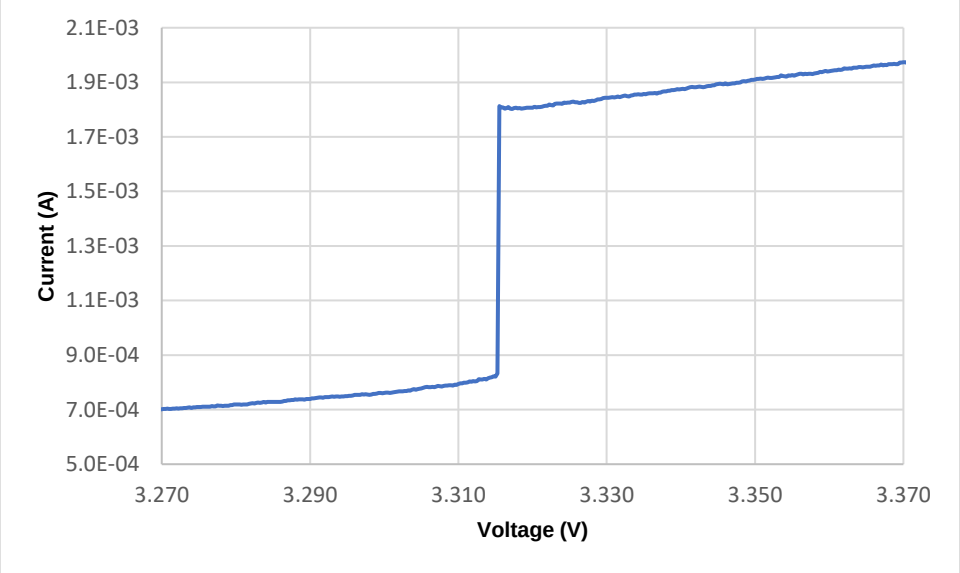


Figure 33: Source-Silicon IV through SnO_2 Quantum Well Energy filter (EF Stack consists of Native SiO_2/ QW: 1.5nm Sn heated at 200°C -1 hr on a hot plate/ 0.5nm ALD deposited Al_2O_3)

The differential conductance of this device produced a full-width half-maximum of 0.25mV, which is equivalent to an effective electron temperature of 0.8 K. However, the resolution of the measurement was 0.25mV.

To directly measure the differential conductance, numerical calculations were performed to determine the differential conductance from a current-voltage staircase

sweep measurement. The difference between the voltages at sites A and B determines the differential voltage (ΔV) for a modest increase in the current (ΔI). We used the Stanford Research SR-570 (Current Pre-amplifier), Stanford Research SIM-980 (Summing amplifier), and Stanford Research SR-830 (Lock-In Amplifier, dual-phase) amplifiers combined into the Stanford Research 830 lock-in amplifier (SR-830) (SIM-983). A direct Current (DC) source was created using the Agilent ES2708 Semiconductor Parameter Analyzer, and a sinusoidal output was produced using the built-in sine generator of the SR-830 (AC). Prior to usage, the Agilent Semiconductor Parameter Analyzer was powered on for 30 minutes to provide the best possible reading. Using low-noise wires, all wiring (coaxial and triaxial) was completed (Keithley, Inc.). To prevent any additional capacitance or resistance, all cables were built internally utilizing connectors from Keithley Inc.

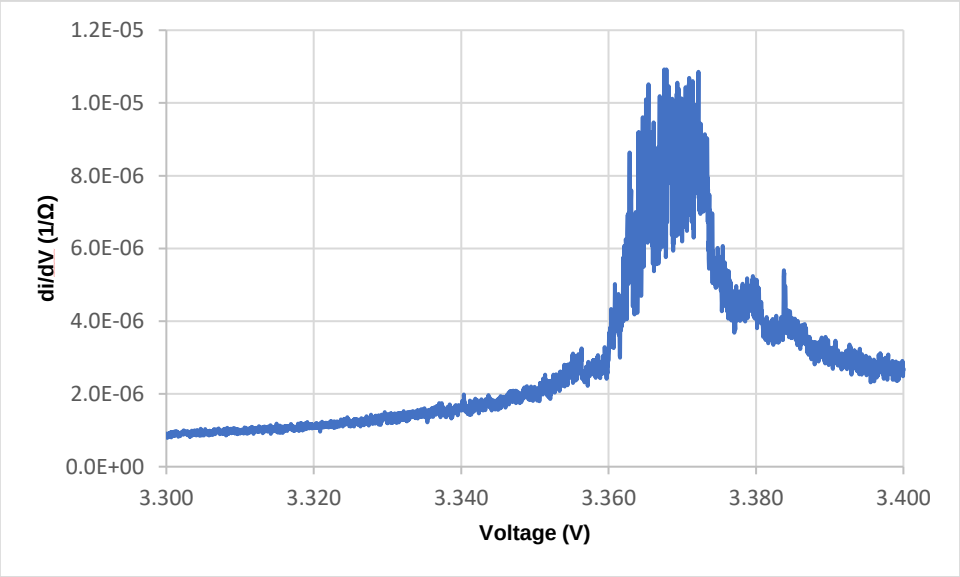


Figure 34: Lock-in Amplifier Differential Conductance vs Voltage measurements showing a FWHM of 10mV

The differential conductance of this device produced a full-width half-maximum of approximately 10mV, equivalent to an effective electron temperature of 32.91 K.

However, the broadening of the lock-in peak was likely due to a shift in the peak position during the long measurement.

Understanding the structural changes in the quantum well structure resulted in a sharp jump in the IV Measurements. Transmission electron microscopy (TEM) was used to obtain a better understanding of the quantum-well structure.

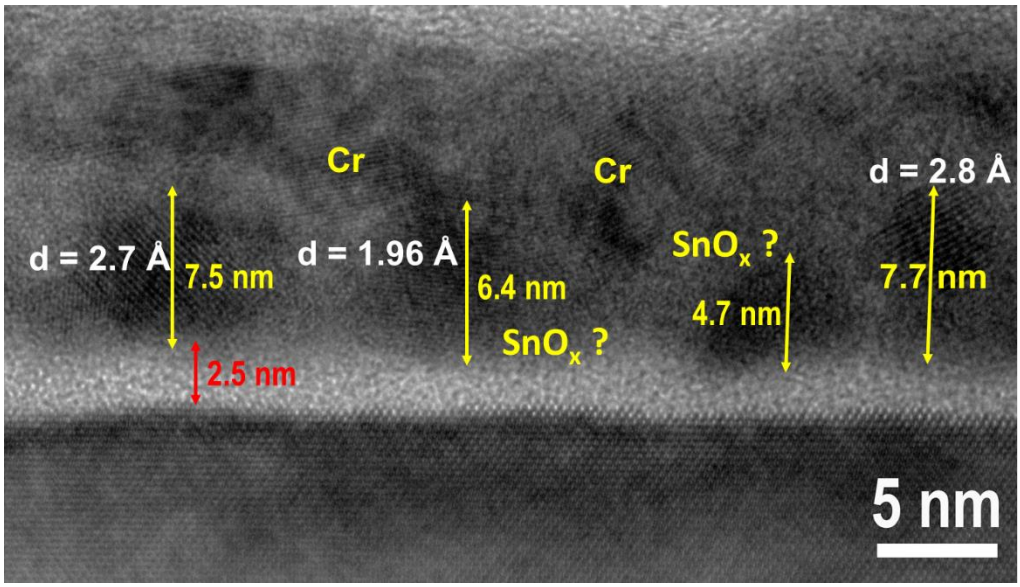


Figure 35: TEM image showing Energy filter layer stack for 50nm Cr/ 0.3nm Si_3N_4 Native SiO_2/ QW: 1.5nm Sn heated at 200°C -1 hr on a hot plate 0.5nm ALD deposited Al_2O_3

This shows that the 1.5 nm Tin (Sn) deposited with the e-beam deposition technique and heated at 200°C on a hotplate was oxidized but formed tin oxide (SnO_2), but instead of a thin layer of the quantum well, we observed a quantum dot with a spherical shape of 5 nm in diameter. Therefore, a consistent thin layer of the quantum well was deposited using sputtered tin oxide (SnO_2).

To investigate the impact of the quantum well layer thickness and variation in annealing duration on the precise voltage for the sudden current jump site, additional measurements were made for a number of other devices with different characteristics.

4.4 Variation In RTA treatment

To investigate the impact of variation in time and temperature on the quantum well layer polycrystallinity. The following conditions were applied to the three samples, and source-silicon IV was measured.

Energy Filter Stack: native SiO_2 / QW:4 nm sputtered SnO_2 / 1 nm sputtered Si_3N_4.

Following fabrication in RTA, the samples were post-annealed at 500°C for 5 minutes, 10 minutes, and 20 minutes.

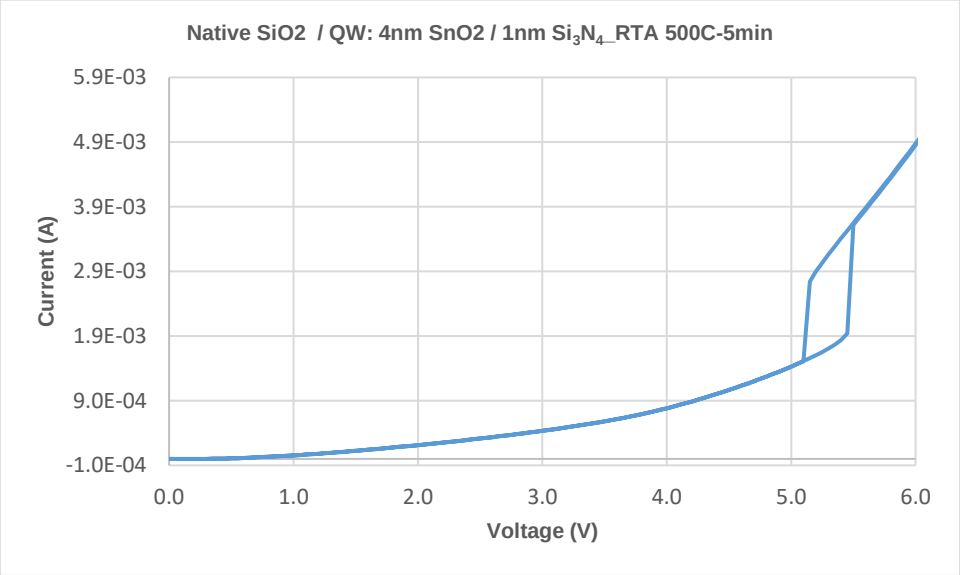


Figure 36: Source-Silicon IV for device with QW: 4nm SnO_2, TB1: 1 nm Si_3N_4 and RTA 500°C -5min

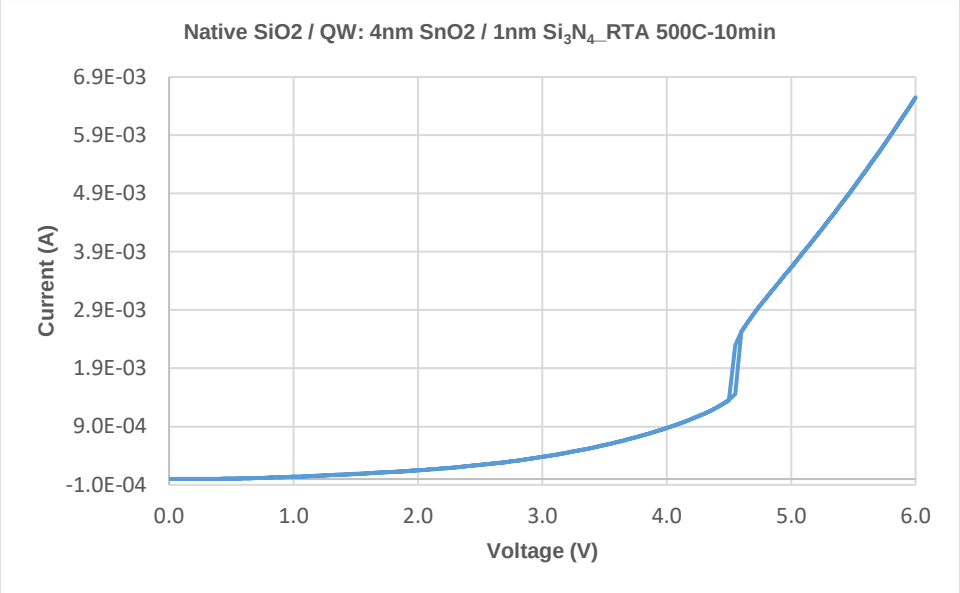


Figure 37: Source-Silicon IV for device with QW: 4nm SnO_2, TB1: 1 nm Si_3N_4 and RTA 500°C -10min

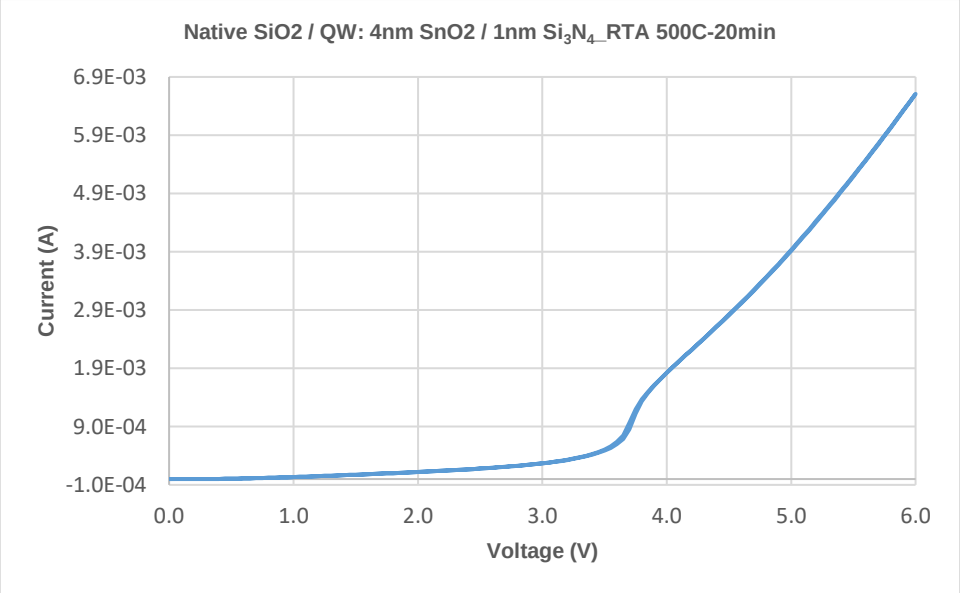


Figure 38: Source-Silicon IV for device with QW: 4nm SnO_2, TB1: 1 nm Si_3N_4 and RTA 500°C -20min

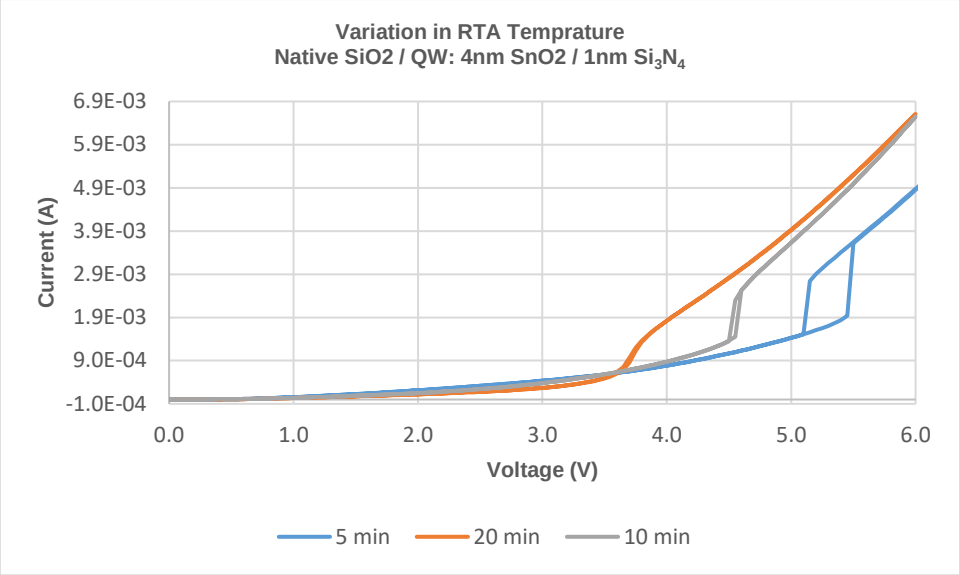


Figure 39: Source-Silicon IV showing variation of abrupt jump voltage with increased RTA annealing time

With an increase in the annealing time, a distinct change in the sharp current jump voltage was observed. We speculate that this may be caused by a modification of the crystal structure of the quantum well layer, which alters the thickness of the quantum well layer. The discrete energy level of the quantum well shifts as a result of the variation in the quantum-well layer thickness. An abrupt jump is visible at a lower voltage bias because of this shift, which lowers the bias needed to line up the discrete energy level with the silicon conduction energy band. However, long exposure to heat treatment resulted in a significant reduction in the jump amplitude, which became smoother, showing degradation.

Understanding the structural changes in the quantum well structure resulted in a sharp jump in the IV Measurements. Transmission electron microscopy (TEM) was used to obtain a better understanding of the quantum-well structure. We see a SnO_2 layer forming a polycrystalline film.

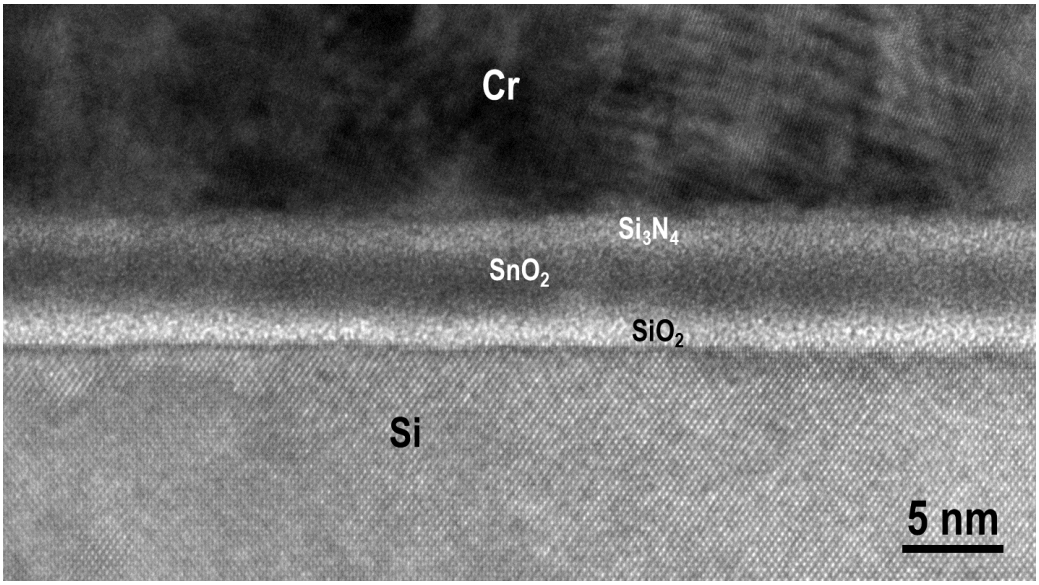


Figure 40: TEM image showing Energy filter layer stack for 50nm Cr/15nm Au/50nm Cr/1nm Si_3N_4/3nm SnOx/1nm SiO_2/Si before RTA annealing

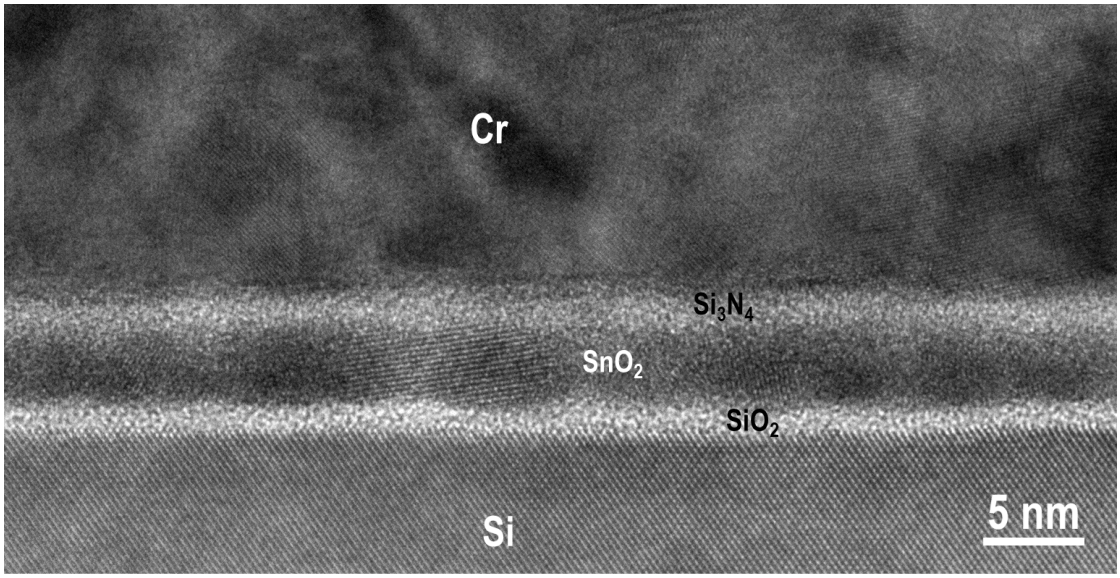


Figure 41: TEM image showing Energy filter layer stack for 50nm Cr/15nm Au/50nm Cr/1nm Si_3N_4/3nm SnOx/1nm SiO_2/Si After RTA annealing at 500°C for 30 minutes

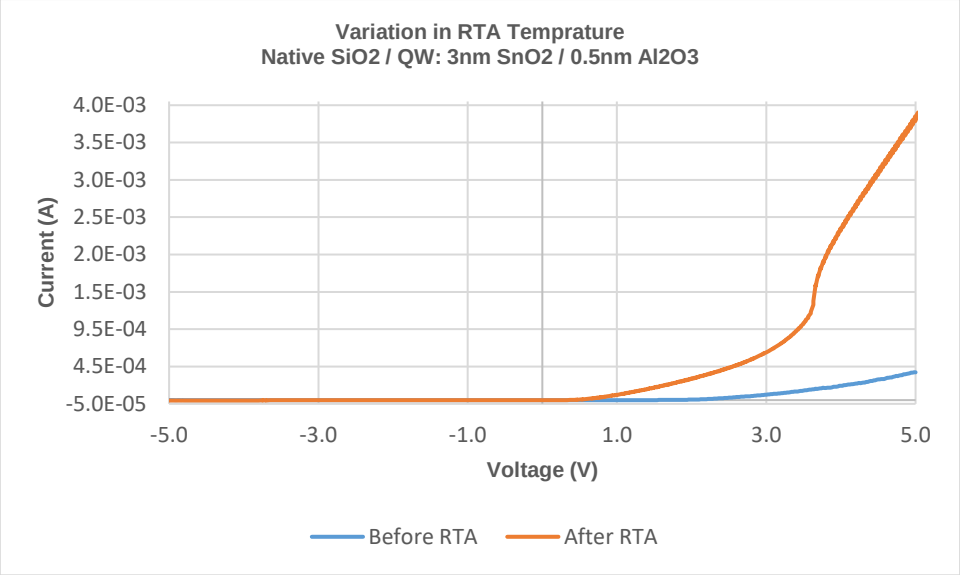


Figure 42: Effect of RTA treatment on Source-Silicon IV for device with QW: 3nm SnO_2, TB1: 0.5nm Al_2O_3 (RTA: 500°C, 15min)

After various experiments, we found that 3 nm, 4 nm, and 5 nm all showed a sharp jump after 500°C for 15 minutes in a vacuum with a ramp-up rate of 100°C per minute. However, even after various temperatures and times, we did not observe a sharp jump between the 1 nm and 2 nm devices.

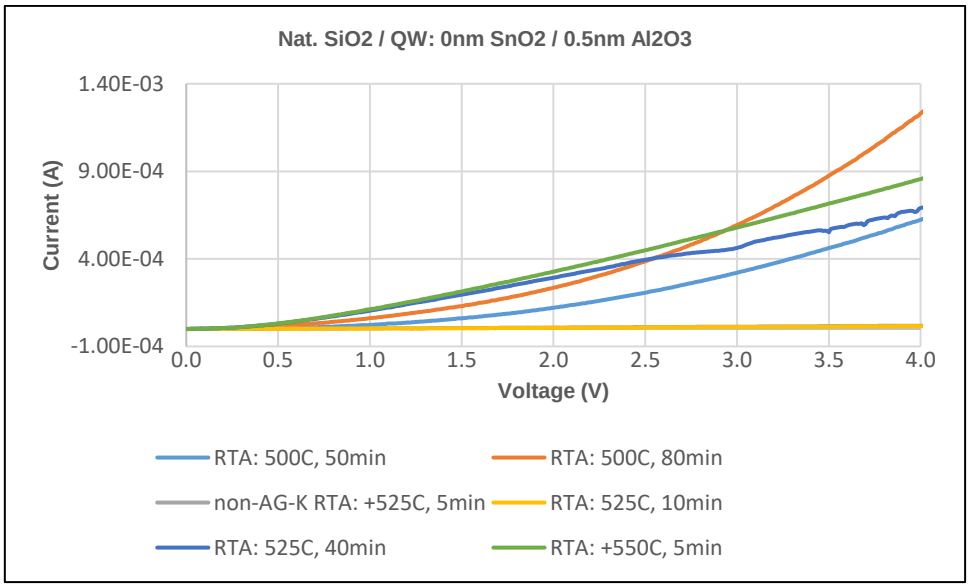


Figure 43: Effect of various RTA treatment on Source-Silicon IV for device with QW: 0nm SnO_2, TB1: 0.5nm Al_2O_3

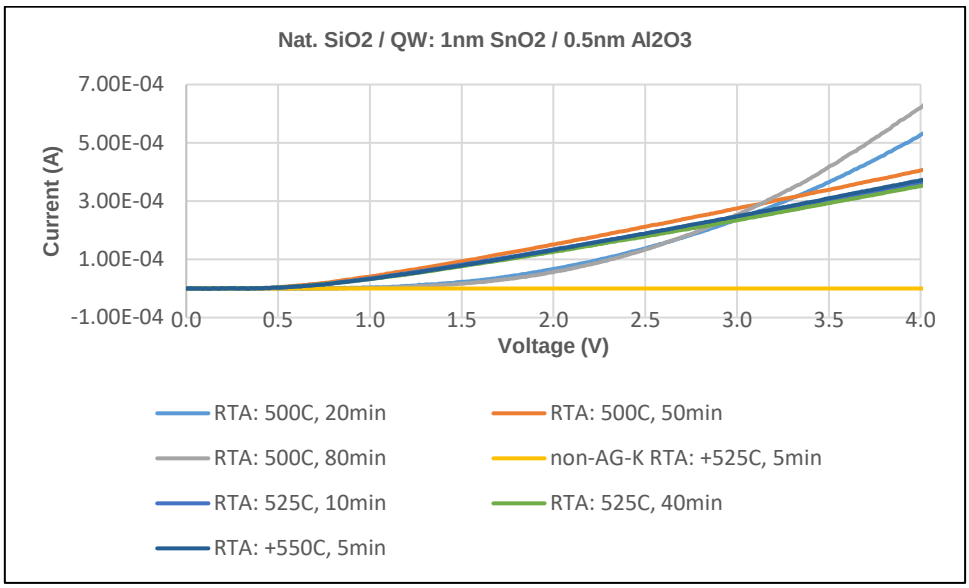


Figure 44: Effect of various RTA treatment on Source-Silicon IV for device with QW: 1nm SnO_2, TB1: 0.5nm Al_2O_3

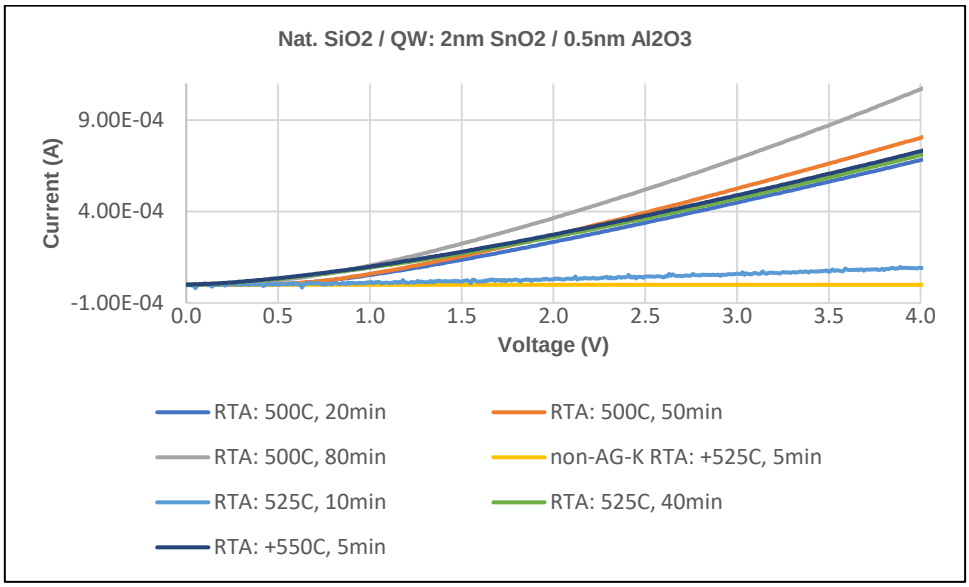


Figure 45: Effect of various RTA treatment on Source-Silicon IV for device with QW: 2nm SnO_2, TB1: 0.5nm Al_2O_3

We discovered that thermal annealing plays a crucial role in the formation of polycrystalline quantum wells in nature. However, as we added 200 nm Sputtered SiO_2 on top of our devices, I changed the temperature between the layers, as the additional SiO_2 helped to trap the heat between the layers.

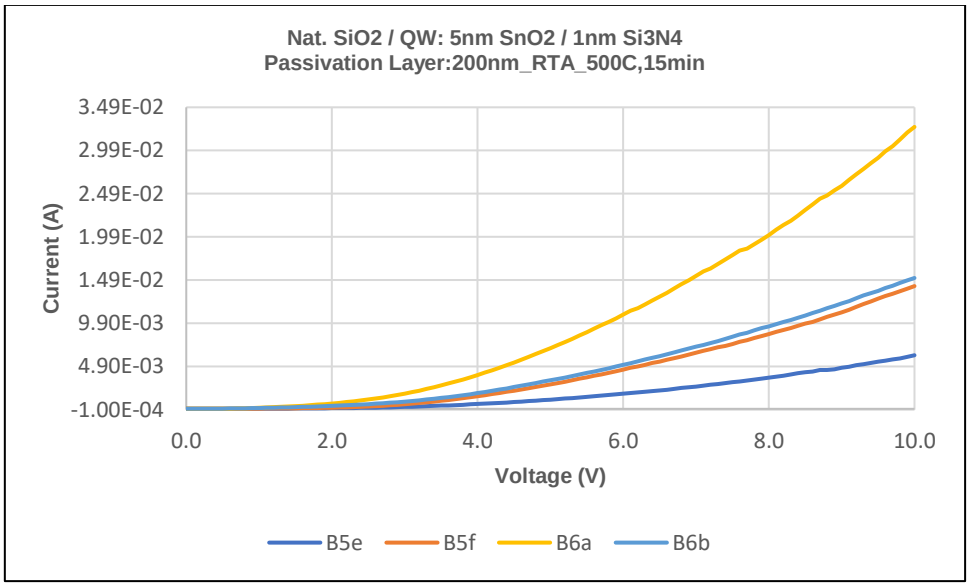


Figure 46: Effect of RTA treatment 500°C for 15 minutes on Source-Silicon IV for device with QW: 5nm SnO_2, TB1: 1nm Si_3N_4 with Passivation layer of 200nm SiO_2

Therefore, after decreasing the temperature and time, we found that 3 nm, 4 nm, and 5 nm all showed a sharp jump after 400°C for 15 minutes in a vacuum with a ramp-up rate of 100°C per minute.

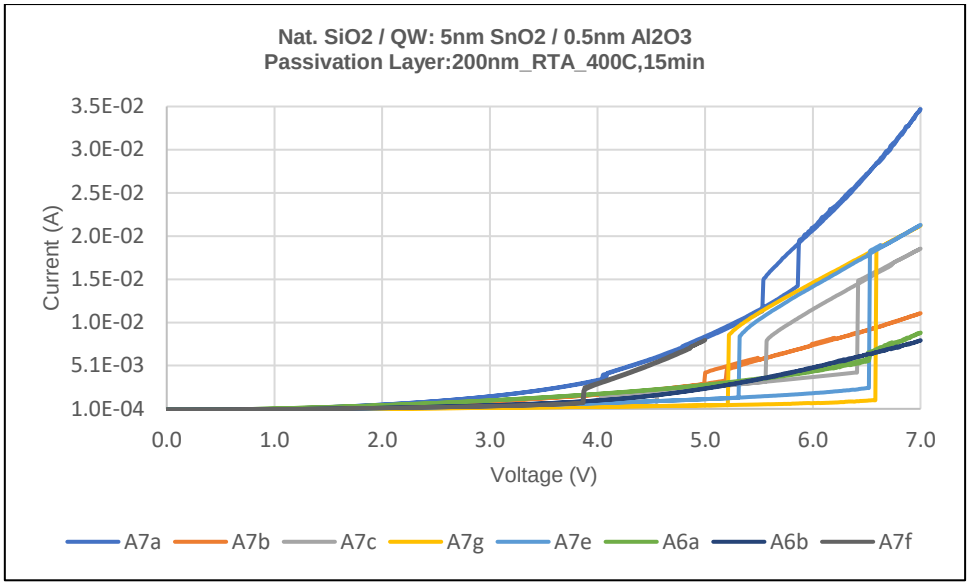


Figure 47: Effect of RTA treatment 400°C for 15 minutes on Source-Silicon IV for device with QW: 5nm SnO_2, TB1: 1nm Si_3N_4 with Passivation layer of 200nm SiO2

However, we observed that the devices exhibited large hysteresis over 1V. Therefore, we suspected that the larger hysteresis could be due to the trapped charges between the passivation layer and the contact electrodes. Hence, we decided to remove the passivation layer while keeping the gold contact pads on the device to reduce the contact problem we faced earlier.

4.5 Variation in QW thickness

To provide greater resolution measurements, the source metal and silicon probes were coupled to an Agilent ES2708 Semiconductor Parameter Analyzer and Stanford Research SIM-980 (Summing amplifier) apparatus via a Keithley Model 6430 sub-femtoamp remote-source meter. Sputtered SnO_2 deposition was used to create new devices such that the thickness of the quantum well layer could be more precisely controlled. A Keithley-Agilent setup was used to measure the gadgets. Three distinct samples with 3 nm, 4 nm, and 5 nm SnO_2 quantum well thickness variations were

created. All samples were annealed for 15 minutes at 500°C under identical RTA conditions.

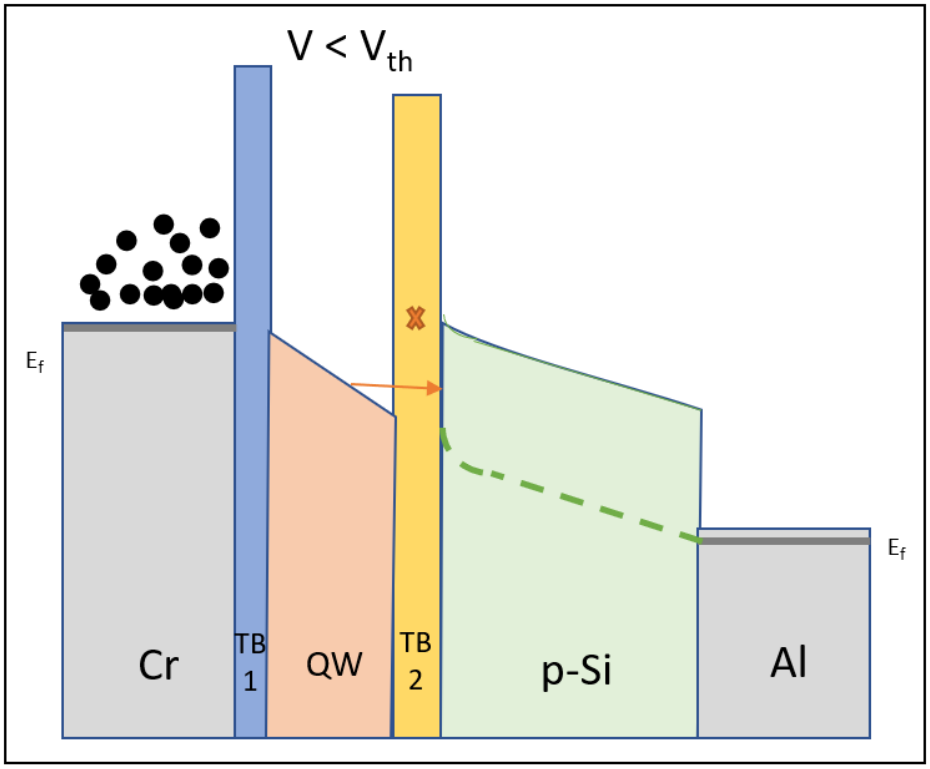


Figure 48: Energy Band diagram showing Electron transport through quantum well energy filter when a positive bias is applied ($V < V_{th}$)

The thermally excited electrons of the source metal enter the discrete energy level of the quantum well and become trapped because there is no way for their excitation because the energy level separation of the quantum well energy levels is significantly greater than the thermal energy at room temperature. A positive bias was used to reduce the conduction energy band of silicon at the silicon metal contact. Electron transmission does not occur as long as the discrete energy level of the quantum well is not aligned with the silicon conduction energy band.

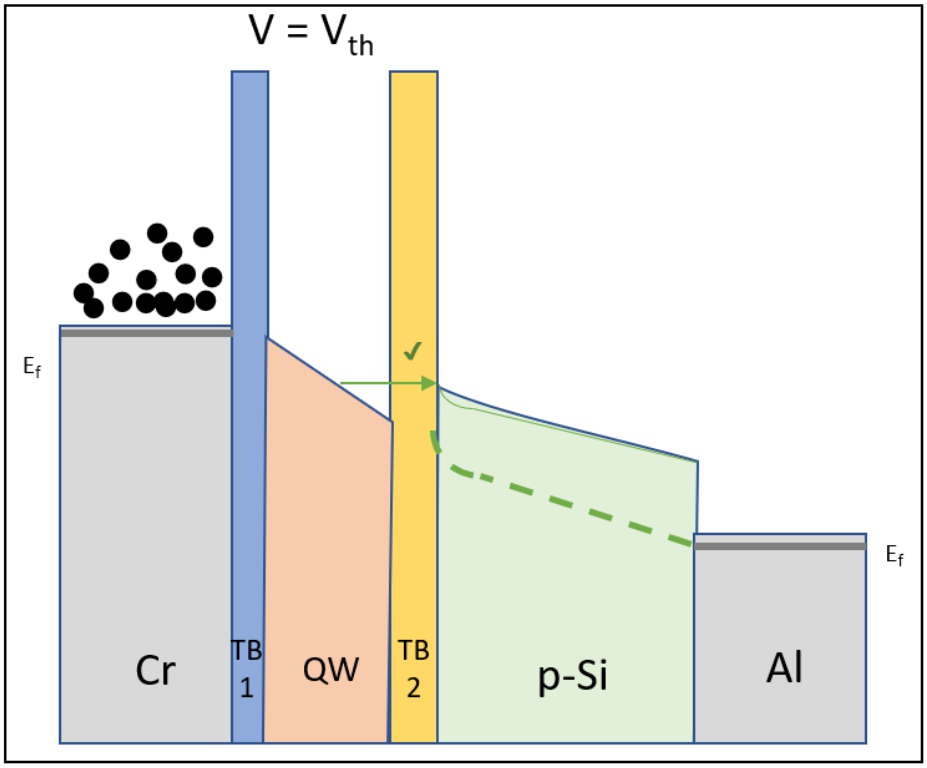


Figure 49: Energy Band diagram showing Electron transport through quantum well energy filter when a positive bias is applied ($V = V_{th}$)

The silicon conduction energy band decreased even further when the positive bias was increased, aligned with the discrete energy level of the SnO_2 quantum well.

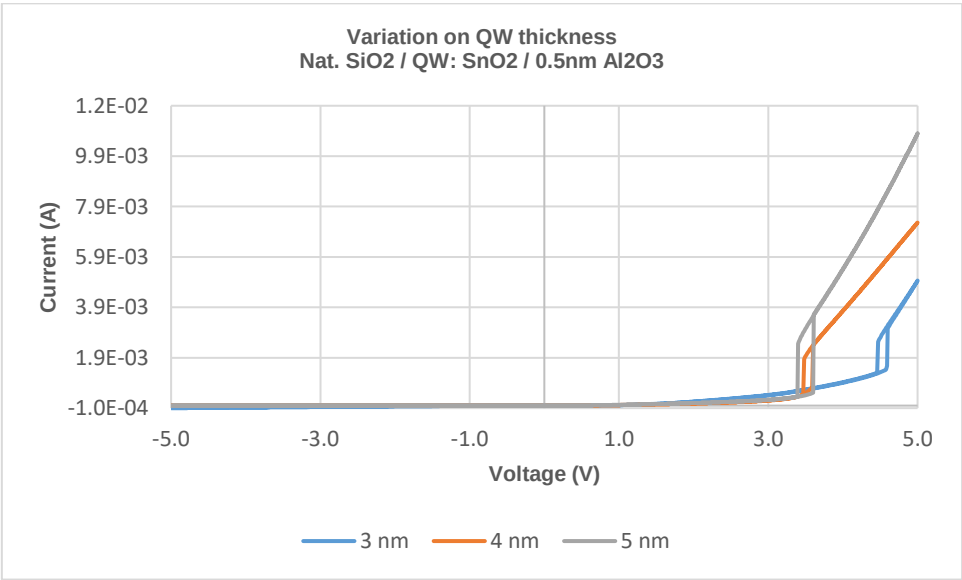
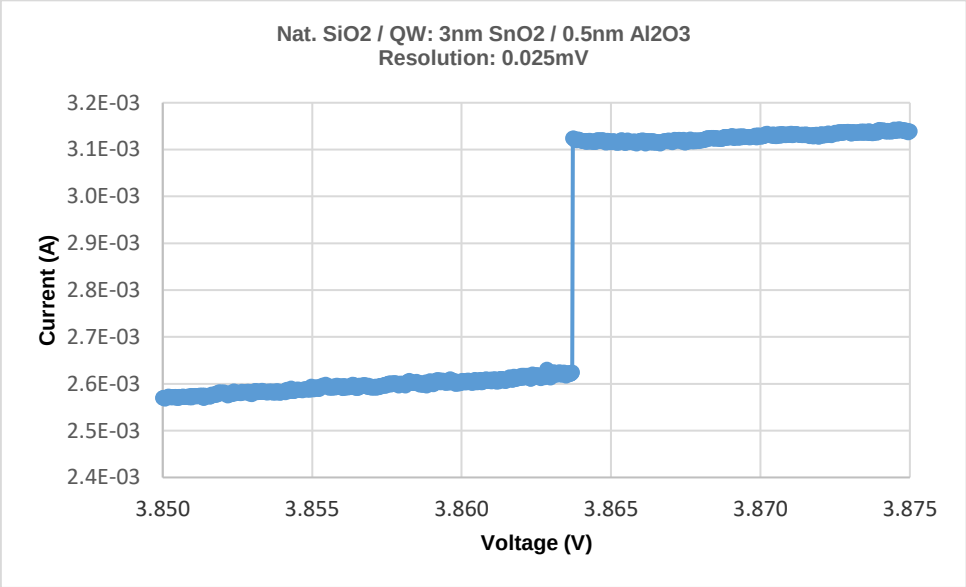


Figure 50: Effect of variation in QW thickness on Source-Silicon IV for device with TB2: Native Oxide SiO_2, TB1: 0.5nm Al_2O_3

The discrete energy levels for the 5 nm SnO_2 quantum well layer were different from those for the 4 nm and 3 nm SnO_2 layers. The silicon conduction band aligns with the discrete energy level of the SnO_2 quantum well layer when the positive bias is increased, triggering a sudden current jump in all the samples.

We observed that a very small amount of current passing through the device could be the result of electron tunneling through the entire energy-filter stack. The 3 nm devices showed a higher leakage current than the 5 nm devices. A thicker energy filter stack helps to reduce the leakage current.



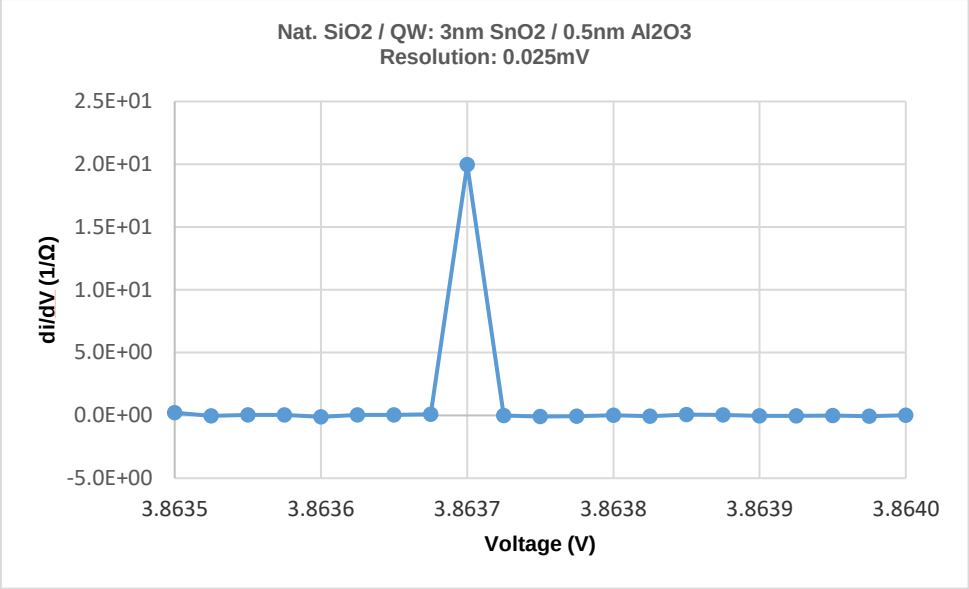
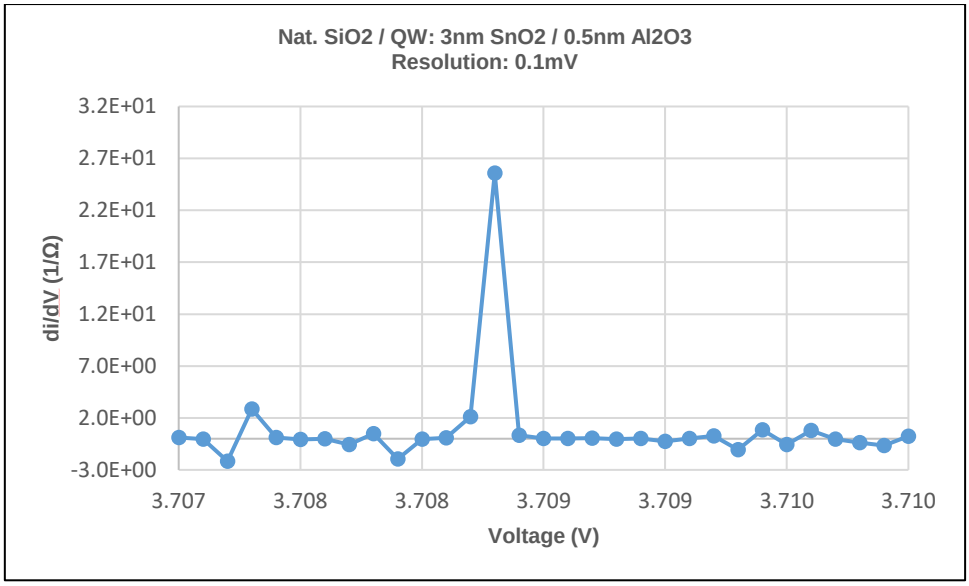


Figure 51: Source-Silicon IV for device (Top) and Differential Conductance vs Voltage (Bottom) for device with Native SiO_2 / QW: 3nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

The zoomed-in plot of the 3 nm device exhibits an extremely abrupt current jump with a resolution of 0.025 mV voltage step size. In the differential conductance vs. voltage graph, a very narrow differential conductance peak can be observed where an abrupt current jump occurs. The differential conductance peak full-width half-maxima for the 3 nm samples was found to be 0.025 mV. The formula FWHM = 3.525 × kT was utilized to obtain the effective electron temperature of the 3 nm sample. The silicon can be injected with cold electrons at room temperature owing to its FWHM of 0.025 mV, which translates to an effective electron temperature of 0.08 Kelvin.



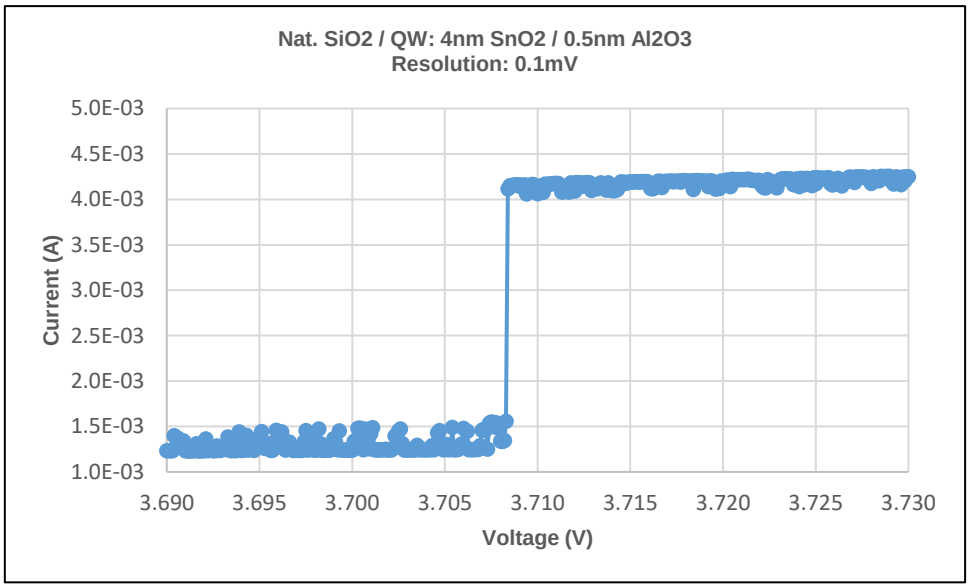


Figure 52: Source-Silicon IV for device (Top) and Differential Conductance vs Voltage (Bottom) for device with Native SiO_2 / QW: 4nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

The 4 nm device's zoomed-in plot exhibits an extremely abrupt current jump with a resolution of 0.1 mV voltage step size. In the differential conductance vs. voltage graph, a very narrow differential conductance peak can be observed where an abrupt current jump occurs. The differential conductance peak full-width half-maxima for the 4 nm samples was found to be 0.1 mV. The formula FWHM = 3.525 × kT was utilized

to obtain the effective electron temperature of the 4 nm sample. The silicon can be injected with cold electrons at room temperature owing to its FWHM of 0.1 mV, which translates to an effective electron temperature of 0.65 Kelvin.

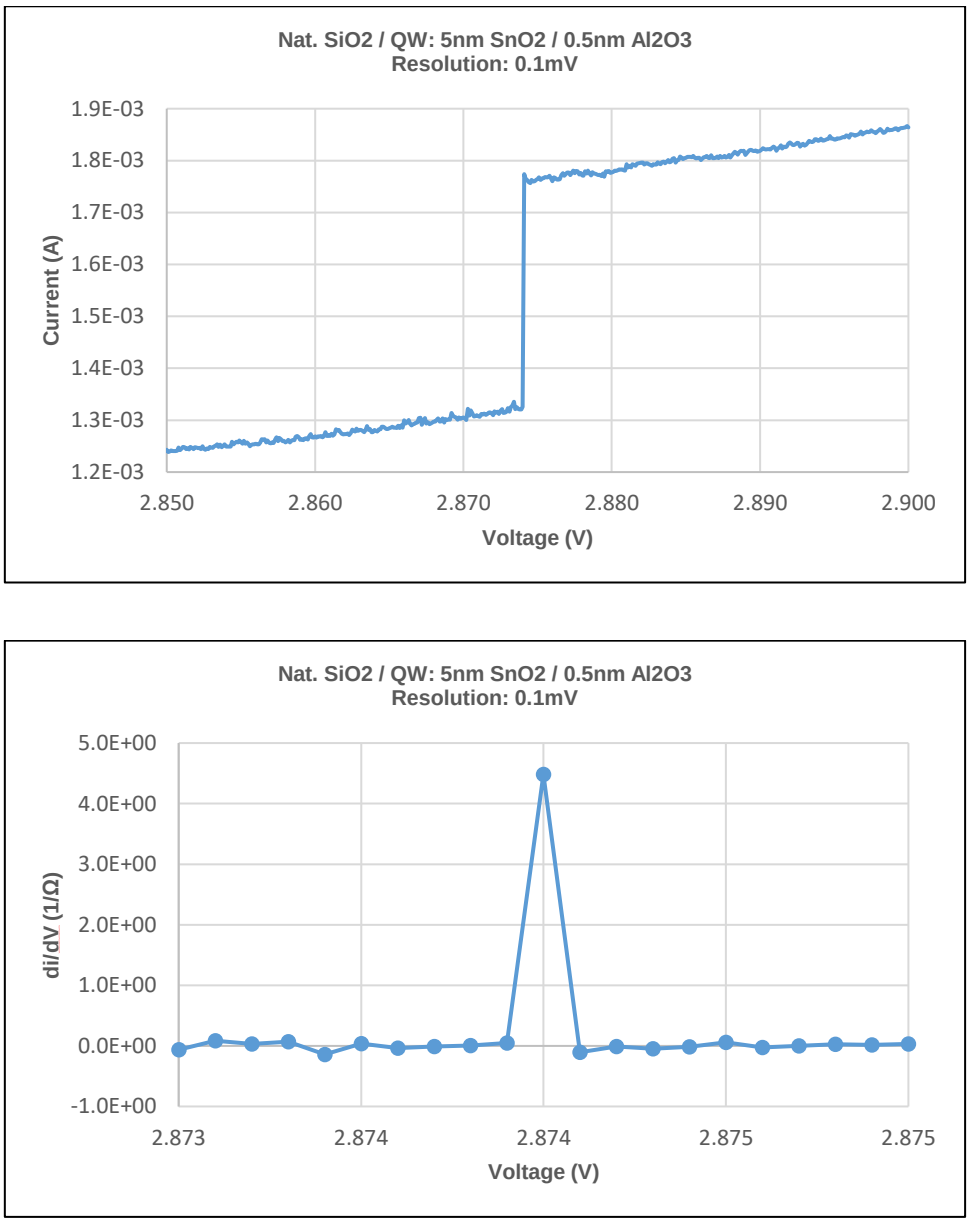


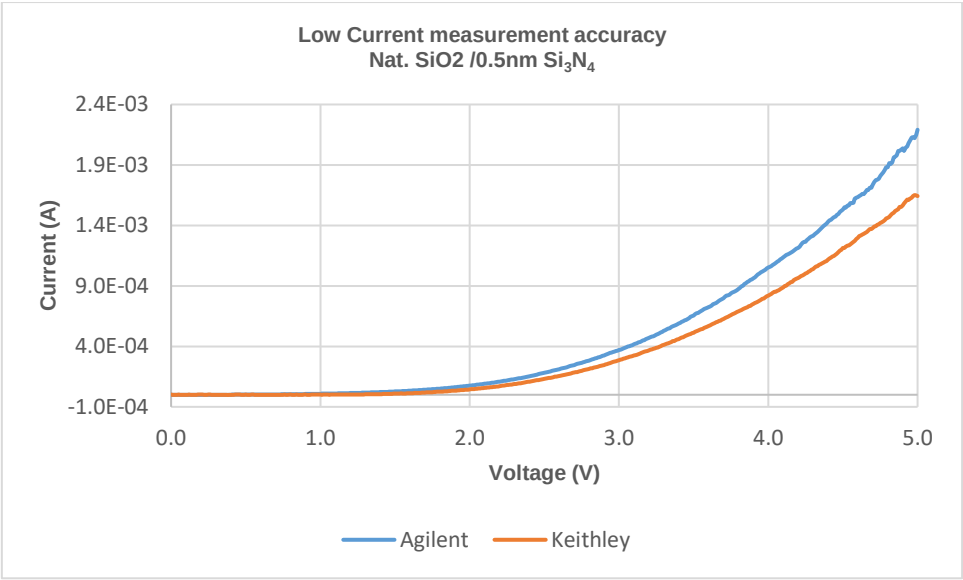
Figure 53: Source-Silicon IV for device (Top) and Differential Conductance vs Voltage (Bottom) for device with Native SiO_2 / QW: 5nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

The 5 nm device's zoomed-in plot exhibits an extremely abrupt current jump with a resolution of 0.1 mV voltage step size. In the differential conductance vs. voltage graph, a very narrow differential conductance peak can be observed where an abrupt current jump occurs. The differential conductance peak full-width half-maxima for the 5 nm samples was found to be 0.1 mV. The formula FWHM = 3.525 × kT was utilized to obtain the effective electron temperature of the 5 nm sample. The silicon can be injected with cold electrons at room temperature owing to its FWHM of 0.1 mV, which translates to an effective electron temperature of 0.65 Kelvin.

An approximate current increase in the mA range was observed in the measured current jump. According to the TEM images, the single-crystal SnO_2 grains were approximately 10 nm^2 in size. When the current density across a single crystalline grain is calculated, the result is 1.0×10^{13} A/m^2. The maximum current density of the Cu wires, which was 5 $A/mm^2 = 5 \times 10^6$ A/m^2, was several times lower than the current density. Therefore, a current density of 1.0×10^{13} A/m^2 for the single crystalline grain of SnO_2 in a semiconducting material is not feasible. As a result, a vast area far greater than $(10m)^2$ must be involved in the current route for cold electron transport across the quantum-well layer.

4.6 Low current measurement

To perform high-resolution measurements, we used an Agilent ES2708 Semiconductor Parameter Analyzer and Stanford Research SIM-980 (Summing amplifier) apparatus via a Keithley Model 6430 sub-femtoamp remote-source meter connected via a coaxial cable.



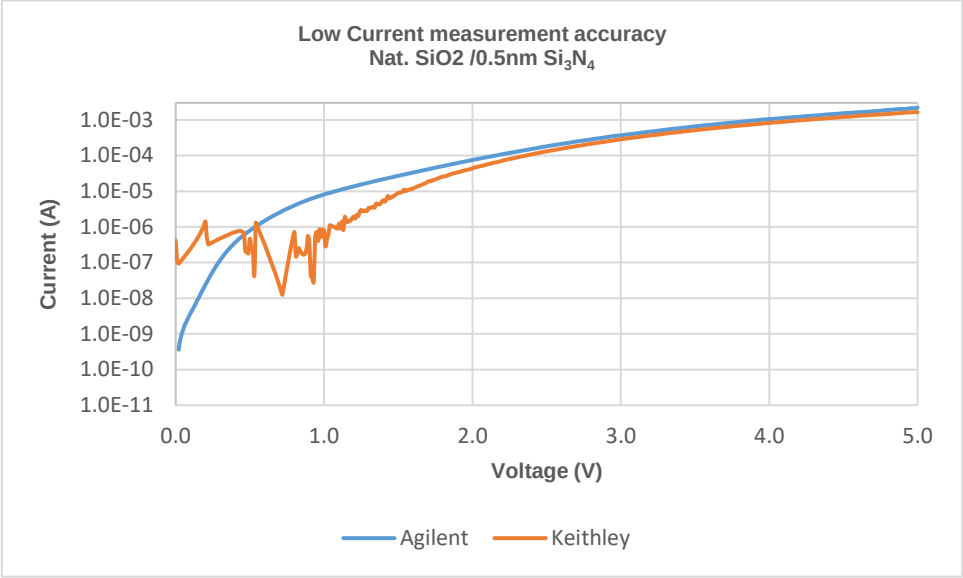


Figure 54: Effect of cables on accuracy in low current measurement (Top: In normal scale, Bottom: In Log scale)

As seen above, on a normal scale, we do not see much noise, but when we take a look at the current on a log scale, we can see noise present at low biases when we use coaxial cables for low currents. To prevent noise from affecting the measurements, we used an Agilent ES2708 Semiconductor Parameter Analyzer with triaxial cables to avoid noise affecting the devices.

4.7 Effect of low temperature

With increasing quantum well layer thickness, the source-silicon current that was measured prior to the sudden current jump decreased. The large current reported in these devices may be due to defect states existing in the thin-film layers during deposition or current flow caused by tunneling. The precise source of the high current can be determined by measuring the components in a low-temperature system. If a high current is generated by defect states in the thin quantum well layer, the low-temperature measurement should have reduced the source silicon current before the sudden surge in current. However, if the high current was caused by tunneling through the thin films, the high current that preceded the sudden surge in the current remained constant.

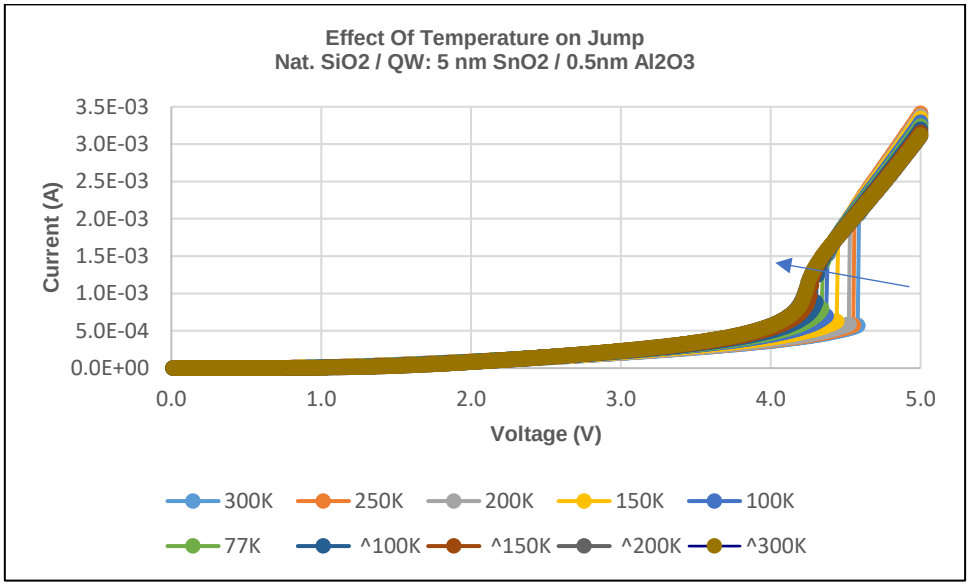


Figure 55: Effect of low temperature on the abrupt jump disappearing of Source-Silicon IV for device with Native SiO_2 / QW: 5nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C - 15min

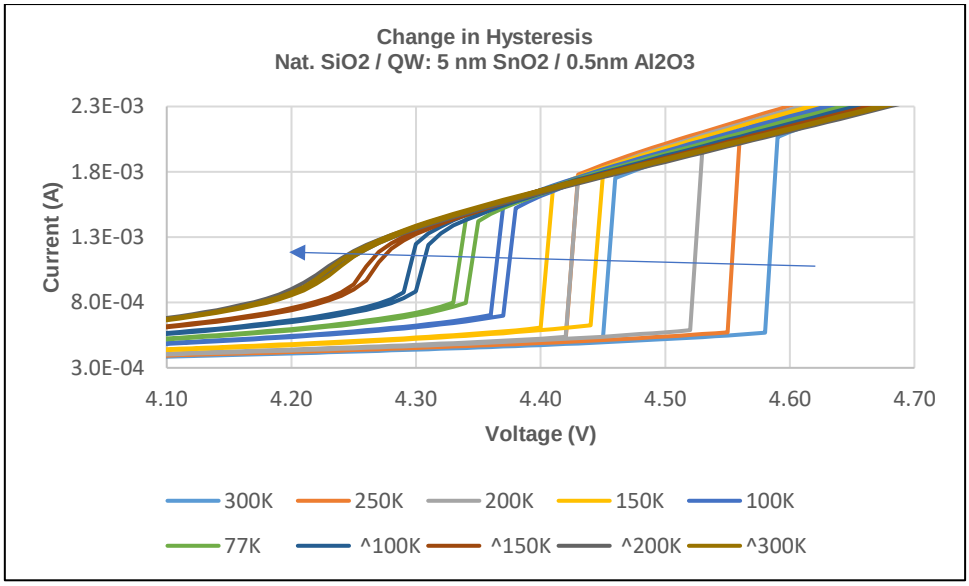


Figure 56: Effect of low temprature on the abrupt jump disappearing zoomed in of Source-Silicon IV for device with Native SiO_2 / QW: 5nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

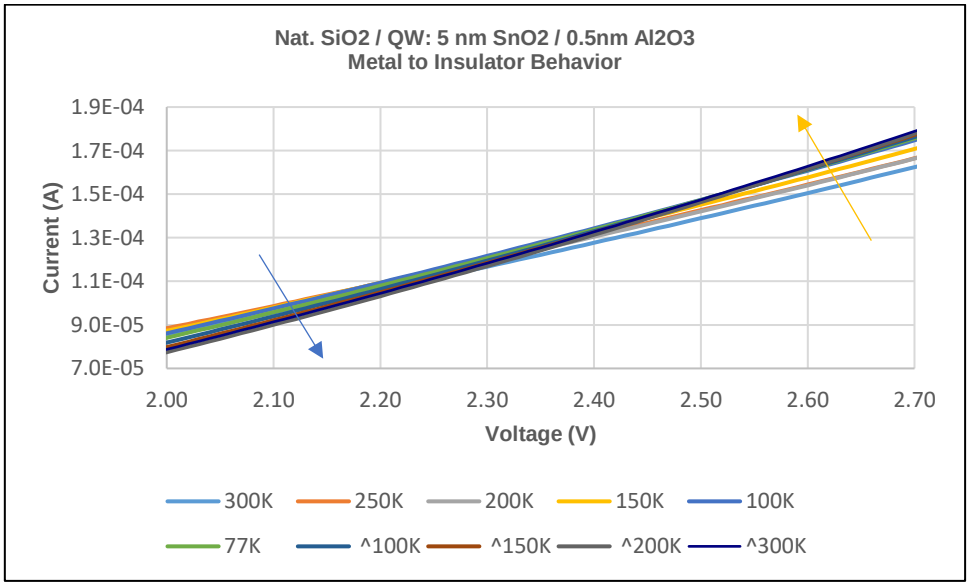


Figure 57: Effect of low temprature on the Source-Silicon Iv showing metal to insulator behavior for device with Native SiO_2 / QW: 5nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

The jump amplitude and voltage both decrease as the temperature drops, as shown in the aforementioned figures, and finally become smoother. However, when the temperature was increased once more, there was no return to the previous state.

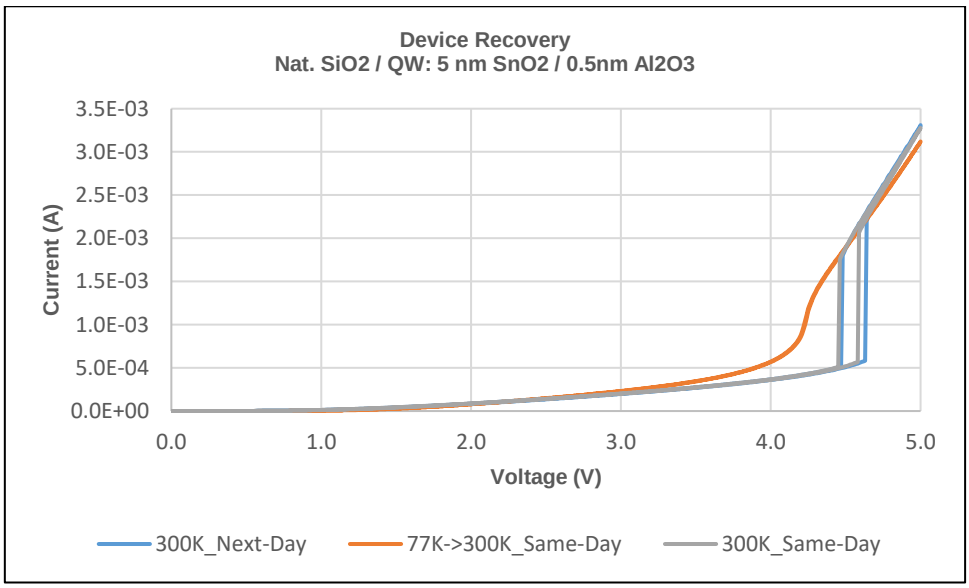


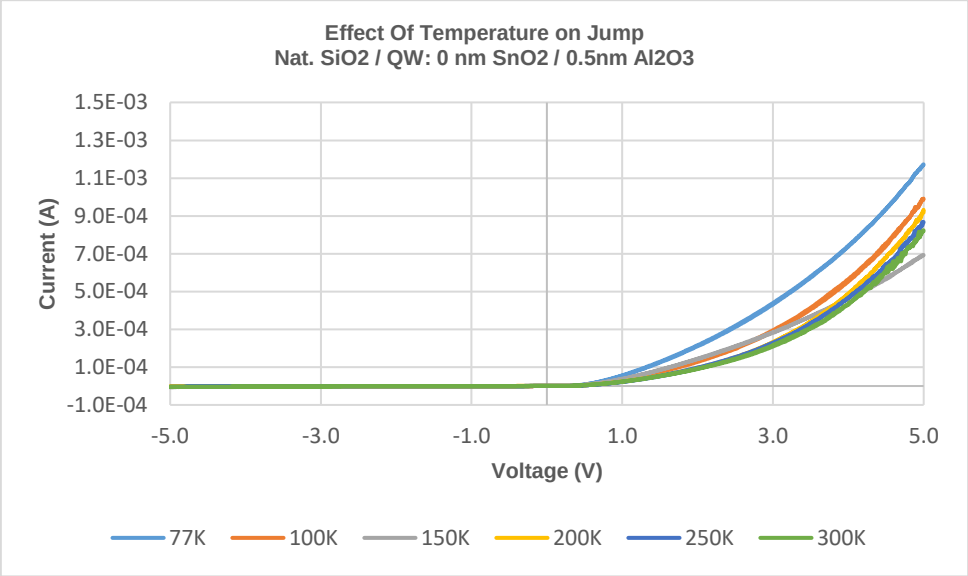
Figure 58: Device recovery effect on the Source-Silicon IV showing recovery of abrupt jump for device with Native SiO_2 / QW: 5nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

However, if we leave the same sample overnight at 300 K, the device recovers to its original state. Hence, it is necessary to measure device behavior at low temperatures. We reduced the temperature and performed the measurements after completing the measurement; at the reduced temperature, we increased the temperature back to 300 K and left it overnight to recover the device.

4.8 Effect of low temperature for various Quantum well thickness

The high current recorded in these devices may be the result of tunneling current flow or defect states that exist in the thin-film layers during the deposition. The components

of a low-temperature system can be measured to identify the actual source of the excessive current. If the defect states in the thin quantum well layer caused a high current, the low-temperature measurement should have lowered the source silicon current before the rapid increase in current. The high current that preceded the rapid increase in the current remained consistent if the high current was brought on by tunneling through the thin layers.



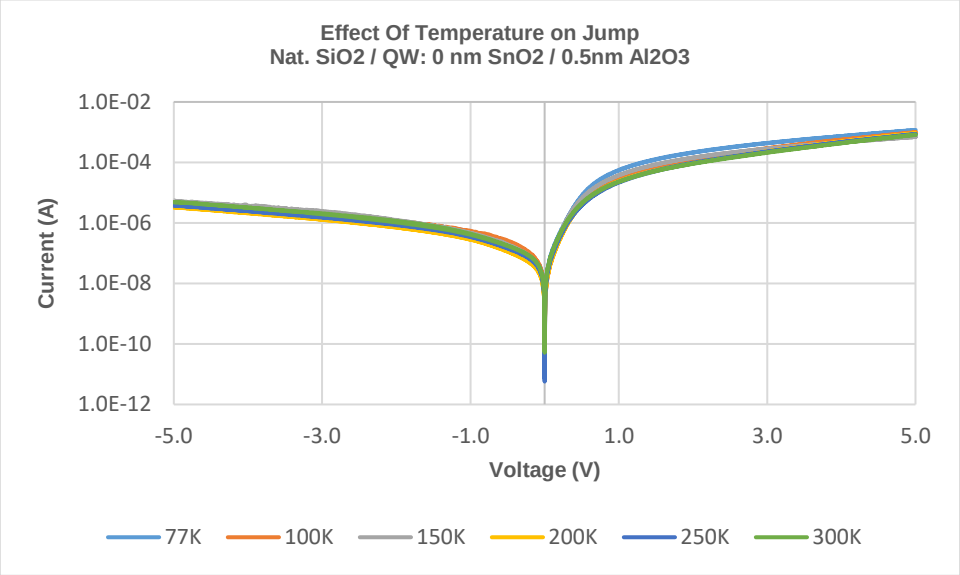
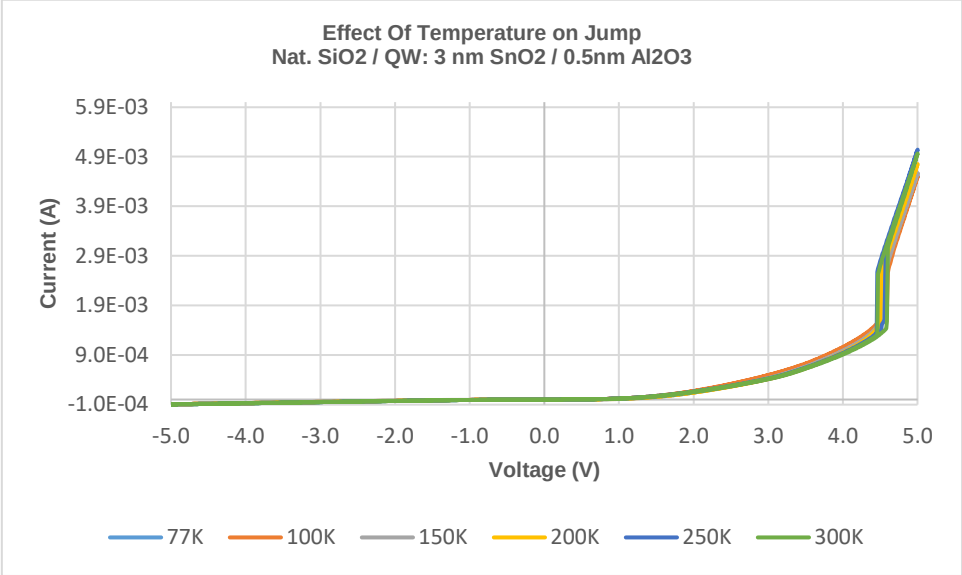


Figure 59: Effect of various low temprature of Source-Silicon IV (Top: In normal scale, Bottom: In Log scale) for device with Native SiO_2 / QW: 0nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

As expected in the 0 nm device, we did not observe any sudden jumps. In addition, as the current passed through only two tunneling barriers, the current amplitude was comparatively lower. In addition, as we can observe, we do not see any dependence on the temperature, which proves that all the current passes through the tunneling barrier only and not because of any defects.



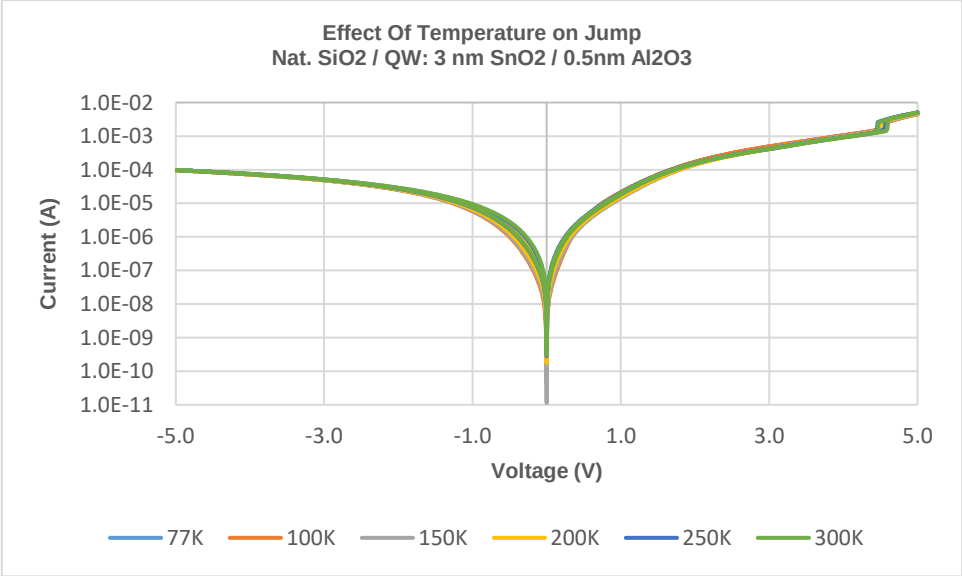
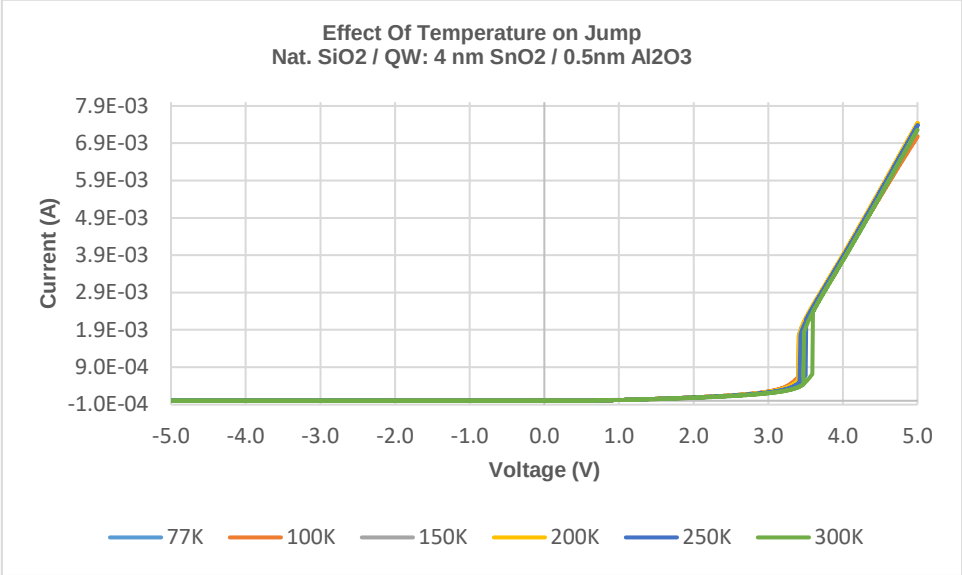


Figure 60: Effect of various low temprature of Source-Silicon IV (Top: In normal scale, Bottom: In Log scale) for device with Native SiO_2 / QW: 3nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

As expected in the 3 nm device, we observed a sudden jump at approximately 4.5 V. In addition, as the current passes through the two tunneling barriers and the quantum well, the current amplitude is comparatively higher than that of the 0 nm device. In addition, as we can observe, we do not see any dependence on the temperature, which proves that all the jumps observed are due to the quantum well alignment.



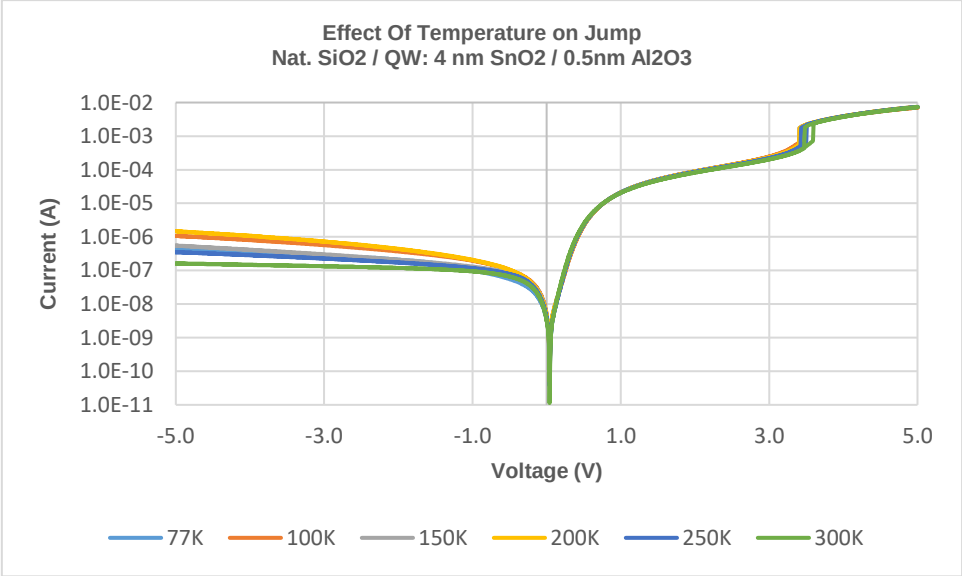
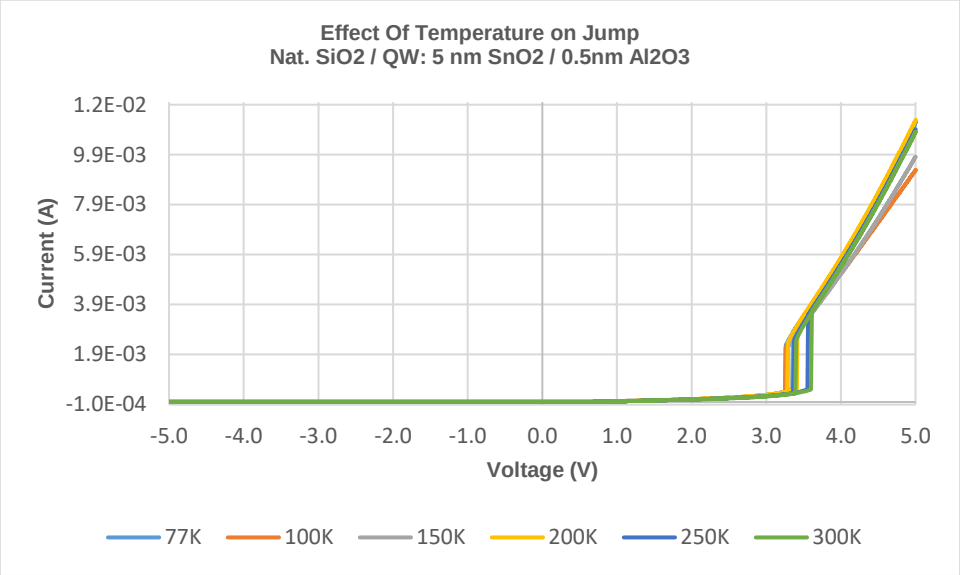


Figure 61: Effect of various low temprature of Source-Silicon IV (Top: In normal scale, Bottom: In Log scale) for device with Native SiO_2 / QW: 4nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

As expected in the 4 nm device, we observed a sudden jump at approximately 3.45 V. In addition, as the current passes through the two tunneling barriers and the quantum well, the current amplitude is comparatively higher than that of the 0 nm device. In addition, as we can observe, we do not see any dependence on the temperature, which proves that all the jumps observed are due to the quantum well alignment.



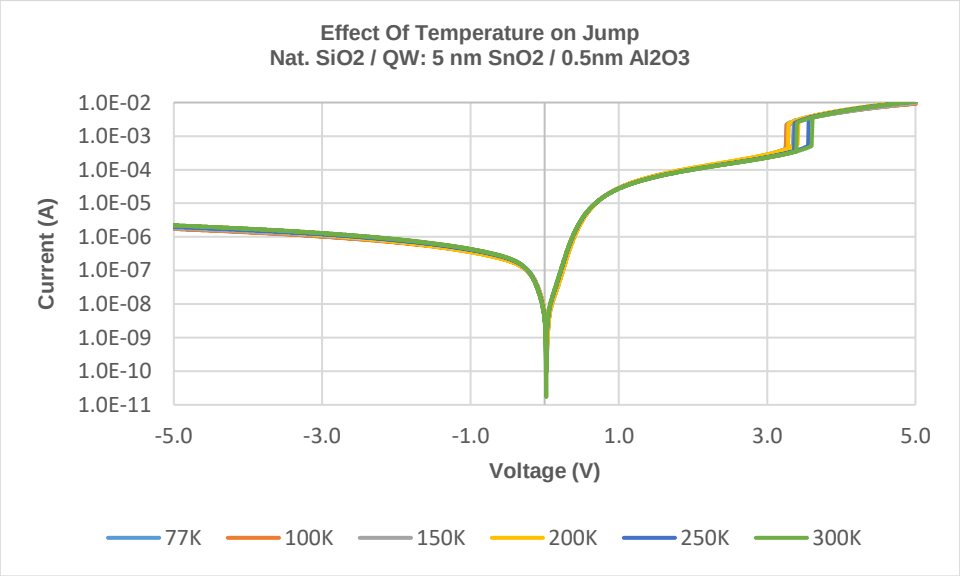


Figure 62: Effect of various low temprature of Source-Silicon IV (Top: In normal scale, Bottom: In Log scale) for device with Native SiO_2 / QW: 5nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

As expected in the 5 nm device, we observed a sudden jump at approximately 3.35 V. In addition, as the current passes through the two tunneling barriers and the quantum well, the current amplitude is comparatively higher than that of the 0 nm device. In addition, as we can observe, we do not see any dependence on the temperature, which proves that all the jumps observed are due to the quantum well alignment.

To observe whether the jump was sudden even at low temperatures, we also measured the devices at a higher resolution of 0.25 mV.

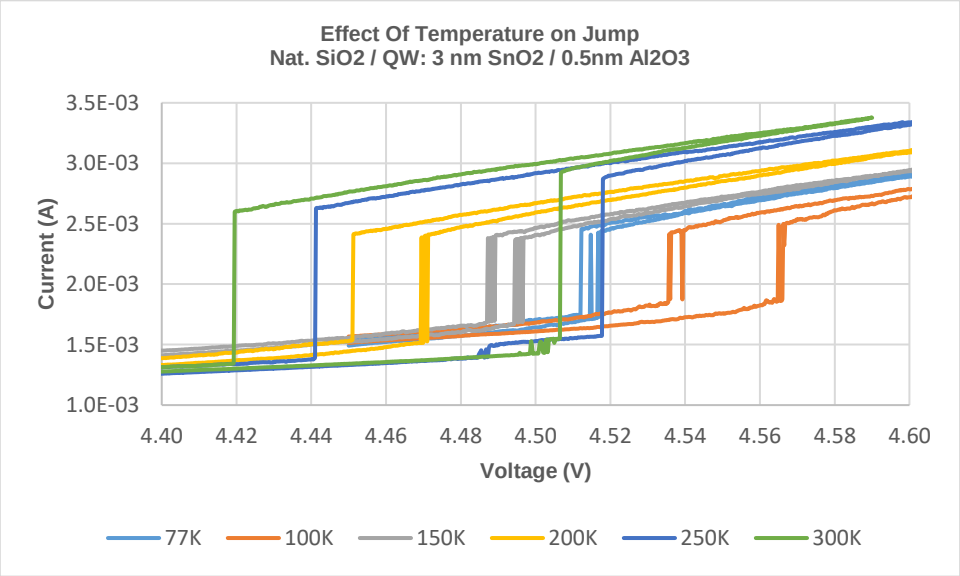


Figure 63: Effect of various low temprature of Source-Silicon IV with high resolution for device with Native SiO_2 / QW: 3 nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

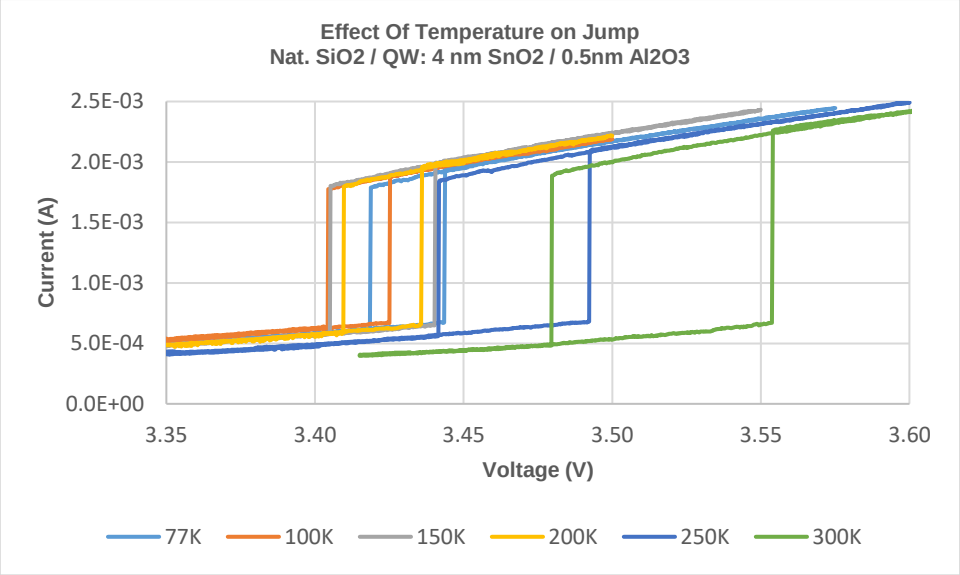


Figure 64: Effect of various low temprature of Source-Silicon IV with high resolution for device with Native SiO_2 / QW: 4 nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

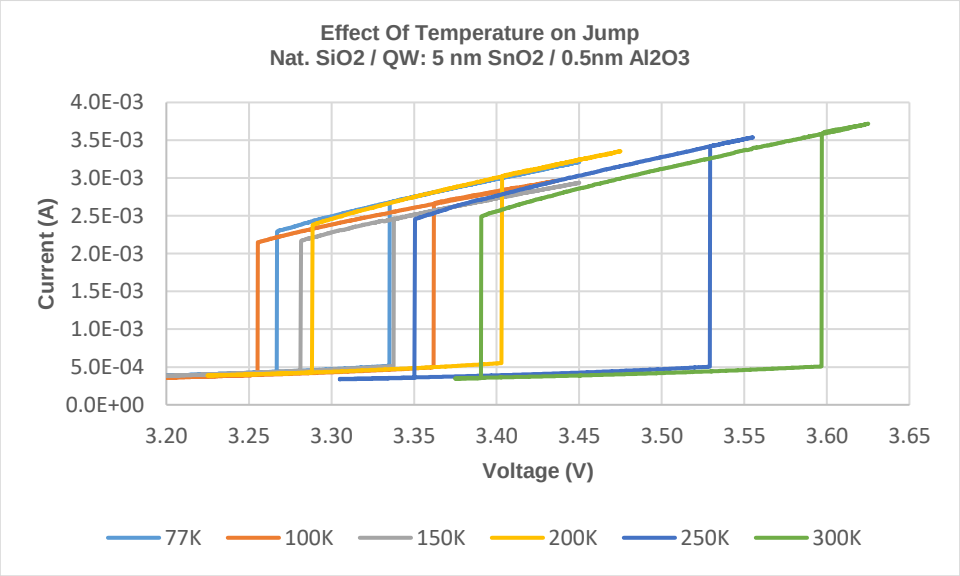


Figure 65: Effect of various low temprature of Source-Silicon IV with high resolution for device with Native SiO_2 / QW: 5 nm SnO_2 / 0.5nm Al_2O_3_RTA 500°C -15min

As we can observe, there is no correlation between the temperature and jump amplitude. Along with it, we can also observe that The device's zoomed-in plot exhibits an extremely abrupt current jump with a resolution of 0.25 mV voltage step size. The differential conductance peak full-width half-maxima of the samples were 0.25 mV.

The formula FWHM = 3.525 × kT was used to obtain the effective electron temperatures of the samples. The silicon can be injected with cold electrons at various temperatures owing to its FWHM of 0.25 mV, which translates to an effective electron temperature of 0.8 Kelvin. This proves that the abrupt jump we observed is due to quantum tunneling and not to any temperature-dependent phenomenon or defects in the energy-filter stack.

Chapter 5: Conclusion

This study has investigated electron transport from 2D QW to 3D semiconductor and its associated electron energy filtering. The fabricated device consisted of a source electrode, tunneling barrier 1 (Al_2O_3, Si_3N_4, or none), quantum well (SnO_2 layer), tunneling barrier 2 (native SiO_2), and a silicon. The QW layer filters out the thermally excited electrons, allowing electrons to tunnel through only when the silicon conduction band edge is aligned with a QW energy level at a certain voltage bias. The TEM analysis showed that the as-deposited tin oxide (SnO_2) layer is an amorphous and the layer becomes polycrystalline when heated at 500°C for 15 minutes. The I-V measurements showed that the electron energy filtering occurs only when the SnO_2 layer is in the polycrystalline structure. The I-V results showed abrupt current jumps, and their differential conductance plots had extremely narrow peaks with an FWHM as small as 0.025 mV, which corresponds to an effective electron temperature of 0.08 Kelvin at room temprature. The I-V measurements at low temperatures (77K -250K) showed that the I-V characteristics are not temperature dependent; the abrupt current jumps are shown at all temperatures investigated (77K-300K). This temperature independence suggests that the observed phenomena are due to electron tunneling, not due to thermally activated processes. The sub-10 K cold-electron injection demonstrated in the silicon system has a potential to create silicon-based transistors that can operate with extremely low energy consumption.

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