Effect of Underfill Material & Gap Height on Reliability of low-k Large-Die Flip Chip Package under thermal Loading

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Abstract

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The reliability assessment of package assembly is important to predict the performance of any microelectronic devices. Formation of fatigue cracks at the interface between the solder joint and component is the common failure occurring in widely used microelectronic devices. Lead-free solders and advanced silicon process nodes with the low-k dielectrics flip chip package are used and are facing significant reliability challenges. The mismatch of coefficient of thermal expansion (CTE) between the chip and substrate affect solder joint reliability. The underfill encapsulant packaging is widely used to improve chip device reliability. In this paper, we are studying the effect of different underfill material and gap height between the die and PCB can improve package reliability. The finite elements method (FEM) have been leveraged for this study. Thermal fatigue takes 80% failure among all the electronic components failure, here Accelerated thermal cycling(ATC) have been used as a load to test stress distribution on package assembly and plastic work in solder joints.

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Chapter 1

INTRODUCTION

Since the birth of digital electronics men have relentlessly perceived the single goal of achieving higher computational power. With the combined strength of higher computational abilities and better power storage capabilities we are more informed and better equipped than ever before. Electronic devices have improved the living standards worldwide. One of major breakthrough in modern day science was the development of integrated circuits. As a result, ICs have become the back bone of our modern civilization. ICs come in different forms and sizes these days as their application varies widely. As a result, more and more materials are being tested and used to improve the performance of these electronic packages. One of such material being widely used in the industry is Low-K materials, Low-K meaning lower coefficient of thermal expansion. These materials are preferred because of its lower cost, a finer pitch and higher performance level. But they have their disadvantages to being poor adhesion and lower modulus. Lower cost of the material is important because the total cost of the electronic package is the major determining factor of the electronic equipment.

Adhesion and modulus are also important qualities of a material, as no package is made of a single material, the interaction of different material under different physical conditions play major roles in electronic industries. Lower adhesion causes delamination of the package as it is a stack up of different materials. A lower modulus makes the material brittle, causing it to break under physical stress.

It is not only the materials that are different, but the models and sizes of packages also vary a lot. This is because of the difference in application and manufacturing processes. One of such variant in packages is the Flip Chip package. The development of flip chips was a breakthrough in itself. It improved the performance of the package and also increased its durability, this enables the package to be connected directly to the circuit using solder bumps. These interconnections play a major role in determining the life of an electronic package as these are the ones first to fail. To improve these interconnections solder balls and copper pads were introduced, but the major improvement to this particular layer in the whole package came with the introduction of underfill materials. Underfill materials were first used in packages by IBM, is was used more of a protective layer for the solder balls from the environment and later on was developed to redistribute thermo mechanical stresses induced in the package upon operation.

Underfill materials basically consist of epoxy resins and silica fillers. By varying the combination of these materials, one is able to control the CTE and young's modulus of the layer. This capability is important as these material properties are the ones which enables the underfill layer to redistribute the stress from its top layer to the bottom in the manner which least affects the solder balls which are located in between, within the underfill layer. Thus, the underfill material plays a major role in increasing the fatigue life of the whole package. Even though this is the case the ability to alter the underfill material is limited. If the layer is too rigid it may preserve the solder balls very well but it could cause delamination between the layers, similarly if it is too flexible then it could fail to redistribute the loads

1.1 Moore's Law

Moore's law is the observation that the number of transistors in a dense integrated circuit doubles approximately every two years. The observation is named after Gordon Moore, the co-founder of Fairchild Semiconductor and Intel, whose 1965 paper described a doubling every year in the number of components per integrated circuit, and projected this rate of growth would continue for at least another decade. Moore's prediction proved accurate for several decades, and has been used in the semiconductor industry to guide long-term planning and to set targets for research and developments.

Figure 1.1: Moore's Law Graph

1.2 Integrated Circuits

Integrated circuits are also known as monolithic integrated circuit which comprises of a set of electronic circuit on one small flat chip or plate of semiconductor material (Silicon). Integrated circuits are usually everywhere as an oscillator, microprocessor, amplifier and many more. With decreasing size of computer, cell phones, electronics the size of the chips or integrated circuits are also reducing. The cost for integrated circuits is reducing too.

There are different types of integrated circuit packages depending on how they

are mounted such as surface mount integrated circuit package, through hole mount integrated circuit package and contactless mount integrated circuit package. The following figure shows a tree chart of different types of integrated circuit packaging techniques used.

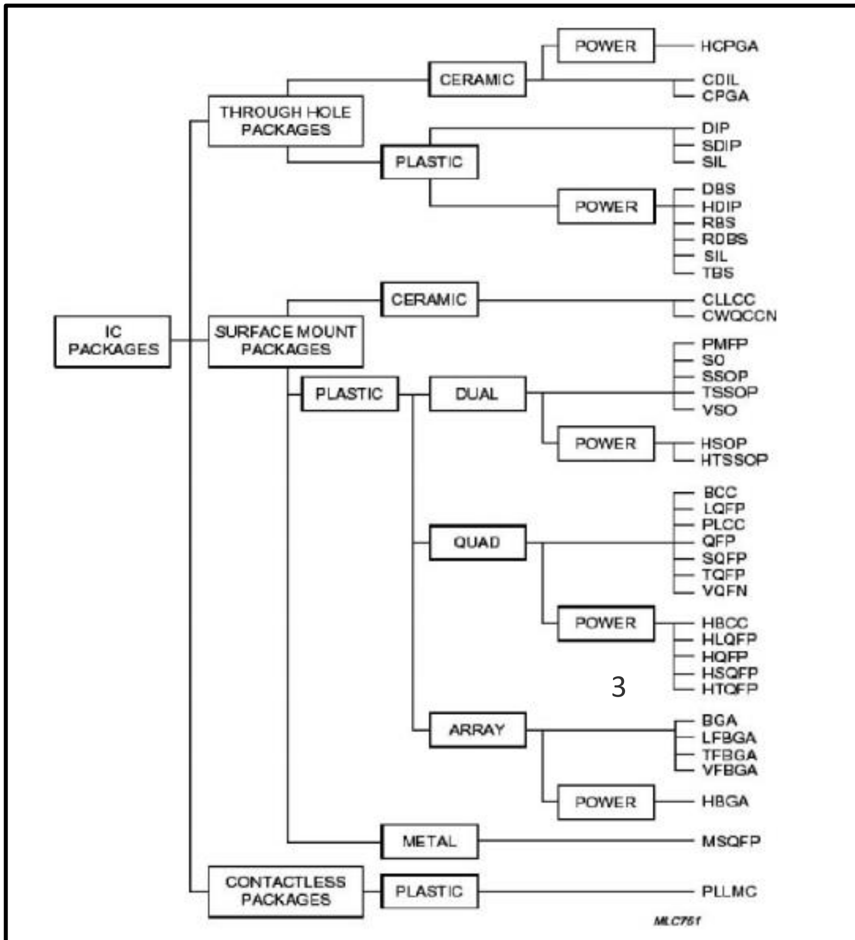


Figure 1.2: Different Types of IC Packaging Techniques

1.3 Flip Chip Package

Flip chip package is a variant in packages. The development of flip chips was a breakthrough in itself. It improved the performance of the package and also increased its durability, this enables the package to be connected directly to the circuit using solder bumps. These interconnections play a major role in determining the life of an electronic package as these are the ones first to fail. To improve these interconnections solder balls and copper pads were introduced, but the major improvement to this particular layer in the whole package came with the introduction of underfill materials. Underfill materials were first used in packages by IBM, is was used more of a protective layer for the solder balls from the environment and later on was developed to redistribute thermo mechanical stresses induced in the package upon operation.

1.4 Motivations and Objective

The main objective of this study is to analyze the role of underfill material and gap height in the fatigue life of the package. Here parametric study has been conducted using different underfill material properties and varying gap heights. The critical solder joint has been found and solder joint reliability was assessed

A model is created per the package dimensions and material properties are assigned. After completing the modeling part, static structure analysis is done using Ansys 18.0. Thermal cycling is applied to the whole model. Ones the simulation is completed material properties and geometry of the underfill layer is assigned as parametric, and different values obtained from literature are assigned. The variations in fatigue life and thermomechanical stresses under different parametric conditions are studied.

Chapter 2

LITERATURE REVIEW

[1] Jimmy M. G. Ong, Andrew A. O. Tay, in his paper different methods to reduce the stress in low- k layer induced under thermal cycling were analyzed. A few different types of underfill material were used for this study and it was observed that a thin substrate and a thin die reduces stresses in low- k layer and the increase in height of cu- post also reduce stress in low-k layer.

[2] Laurene Yip, has demonstrated that cu- pads are more reliable and SnCu0.7 and SAC 305 SOP alloy have better solder bump crack performance than SnAg alloys. Further more lower CTE of the substrate core can reduce die stress.

[3] Ming-Che Hsieh, Chien Chen Lee, and Li Chiun in his paper explains that material properties and thickness of substrate are essential in the impact of warpage response in large die flip chip packages. Also a smaller Cu pad diameter and larger SRO size reduces bump stress and prevent appearance of pre solder crack.

[4] Xiaoyang Liu, Xiaolong Wu, Wenlu Chen, Ran He , Daquan Yu. This paper experimentally selects the best underfill material out of four, with different material properties, that is the most reliable under thermal cycling.

[5] Peng SUN, Vivian ZHANG, Rocky XU.In this paper different underfill material are studied and it is observed that even though underfill materials with lower modulus exhibits less package warpage it fails to pass thermal cycling test due to delamination.

[6] Marie-Claude Paquet, Catherine Dufort ,Thomas E. Lombardi, Tuhin Sinha IBM East Fishkill,

Masahiro Hasegawa, Kodai Okoshi, Kazuyuki Kohara, in this paper different underfill materias were tested under thermal cycling and was observed that the main cause of failure was the underfill to chip side wall delamination.

[7] Jiang Xia, GuoYuan Li, Bin Zhou Analysis, this paper goes through the investigation of different POP structures stress distribution using FEA models. It was concluded from the paper that full-filled is better than edge bonded and edge bonded is better than corner bonded.

[8] Wan Luo, Jun-Jie Liang, Yun Zhang, Rua-Min Zhou, This paper is based on the manufacturing process of the package. It states the role of gap height in the filling of underfill material into the package.

Chapter 3

MATERIAL CHARACTERIAZATION

In this chapter a few of the material properties used in the FEA analysis and the devices used to measure these properties are explained.

3.1.1 Coefficient of Thermal Expansion (CTE):

The rate by which a PCB material expands due to heat is called the Coefficient of Thermal Expansion (CTE). CTE can also be defined as the fractional change in length per degree of temperature change

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE)

ϵ- Strain (mm/mm)

ΔT - Difference in Temperature (^{0}C)

3.1.2 Glass Transition Temperature (Tg):

At this temperature range the polymer chains become more mobile and the PCB substrate transitions from a glassy rigid state to a softened deformable state. The properties are regained once the material cools back to room temperature.

3.1.3 Decomposition Temperature (Td):

At this temperature the PCB material chemically decomposes and it can never regain its original properties upon cooling. It is said that the material losses up to 5% of its mass.

3.2 Thermo Mechanical Analyzer (TMA)

TMA is used to measure the In-plane and Out-plane Co-efficient of Thermal Expansion(CTE), Glass Transition Temperature(Tg) and Decomposition Temperature(Td). Temperature range was -65°C to 260°C with a temperature ramp of 5 C°/min. Sample size for TMA experiments were 6 x 6 mm. Samples were made using a high-speed cutter. The dimensions of the sample are such that it fits correctly under the probe. The Quartz probe of the TMA sets on the sample and the CTE is obtained from the relative movement of the probe.

Figure 3.1: Thermo Mechanical Analyzer (TMA)

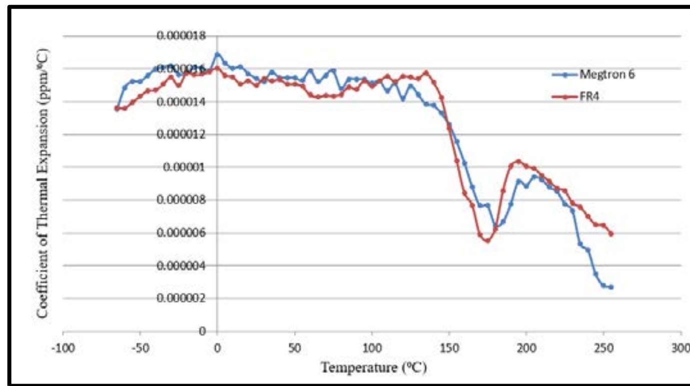


Figure 3.2: Plot for in-plane CTE

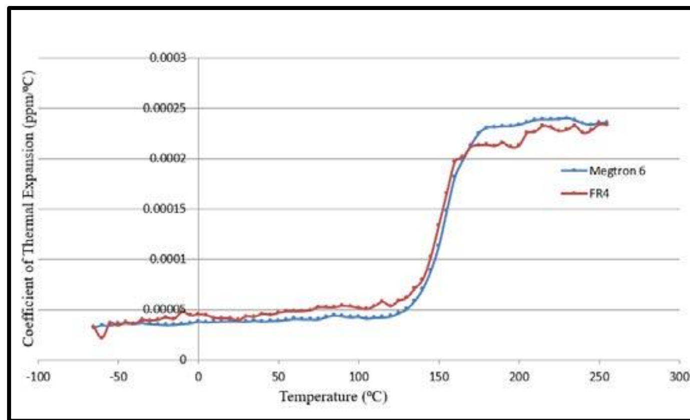


Figure 3.3: Plot for out of plane CTE

The in-plane and out of plane CTE are measured using TMA. Figure 3.5 shows plot for in-plane CTE while figure 3.6 shows plot for out of plane CTE. These coefficients of thermal expansion can be measured by keeping the board sample in three different positions under the quartz probe. A wide variety of thermal loads can be calculated by using a temperature range from -65^{0}C to 260^{0}C. A significant dip can be observed in the in-plane CTE plot after 150^{0}C. This is due to recrystallization and cold crystallization processes occurring in the sample during experiments. Further expansion of sample can be observed above 180^{0}C which at the end melts. The melting process can be seen after about 225^{0}C with decrease in the sample height and viscosity.

3.3 DYNAMIC MECHANICAL ANALYZER (DMA)

DMA is testing machine which helps us to obtain Young's Modulus(E), Storage Modulus(E') and Loss Modulus(E"). A small sinusoidal load generated by a force motor is applied to sample through a drive shaft. The sample dimensions are kept 10 x 50 mm.

Figure 3.4: Dynamic Mechanical Analyzer (DMA)

3.3.1 Young's Modulus (E): Young's Modulus is also known as Tensile Modulus or Modulus of Elasticity. It basically measures the stiffness of a PCB. Young's Modulus can be defined as the ration of stress to strain in a particular direction. Materials that deform less as compared to other under tensile loading are said to be stiffer.

3.3.2 Storage Modulus (E'): Storage Modulus measures the stored energy representing elastic portion of a material.

3.3.3 Loss Modulus (E''): Loss Modulus measures the energy dissipated as heat, representing the viscous portion of the material.

Chapter 4

COMPUTATIONAL ANALYSIS

The Finite Element Method is a computational branch of engineering which discretize a system and reduce it into elements connected by nodes, which enables us to solve various mechanical problems on that particular system. This process provides an approximate method for problem solving. In this study an Octant geometry is used for computational study. Symmetric boundary conditions are applied on the two faces towards the inside were the geometry is split. The front edge of the geometry is assigned as a fixed support in order to restrict movement and to induce stresses while under thermal loading. The two split sides are modeled as frictionless to imply the presence of the whole body. Thermal cycling condition was applied to the whole body. The nature of all the properties were linear elastic, except the solder joints. The critical solder joint was considered as visco-plastic and so Anand's model was used to explain the behavior of the solder joints. SAC405 is a lead-free solder alloy made up of 95.5 % tin, 4% silver and 0.05 % copper. Anand's viscopastic constitutive law is used to describe the inelastic part of the lead-free solder. The Anand's constants are given in the Table. The PCBs were taken as linear orthotropic in nature. Solder is modeled as rate dependent viscopastic material which uses Anand's viscopastic model. It takes both creep and plastic deformation into consideration to represent secondary creep of the solder. Anand's viscopastic constitutive law best describes the inelastic behavior of lead free solder. Anand's law consists of nine material constants A, Q, ξ, m, n, hu, a, su, ŝ.

$$\frac{d\varepsilon_p}{dt} = A\sinh\left(\xi\frac{\sigma}{s}\right)^{\frac{1}{m}}\exp\left(-\frac{Q}{kT}\right)$$

$$\dot{s} = [h_0(|B|)^{\alpha}\frac{B}{|B|}]\frac{d\varepsilon_p}{dt}$$

$$B = 1 - \frac{s}{s^*}$$

$$s' = \hat{s}\left[\frac{1}{A}\frac{d\varepsilon_p}{dt}\exp\left(-\frac{Q}{kT}\right)\right]^n$$

Table 4.1: Anand's material Constants for SAC 405

Constant	Name	Unit	Value
s0	Initial Deformation Resistance	MPa	1.3
Q/R	Activation Energy/ Universal Gas Constant	1/K	9000
A	Pre-exponential Factor	sec-1	500
ξ	Multiplier of Stress	Dimensionless	7.1
m	Strain Rate Sensitivity of Stress	Dimensionless	0.3
h0	Hardening/Sof tening Constant	MPa	5900
ŝ	Coefficient of Deformation Resistance Saturation	MPa	3.9
n	Strain Rate Sensitivity of Saturation	Dimensionless	0.03
a	Strain Rate of Sensitivity of Hardening or Softening	Dimensionless	1.4

Parametric study is conducted by varying geometry, material properties and boundary conditions. But since the ATC is a standard test the boundary conditions cannot be varied, thus these conditions are kept constant throughout the simulation. The material properties of the under fill material are varied in order to determine the influence of its CTE and Modulus on the fatigue life of the whole package. Geometry is also varied, the gap height is varied to determine

its influence in the stresses and deformation caused due to thermal loading.

4.1 PACKAGE MODEL

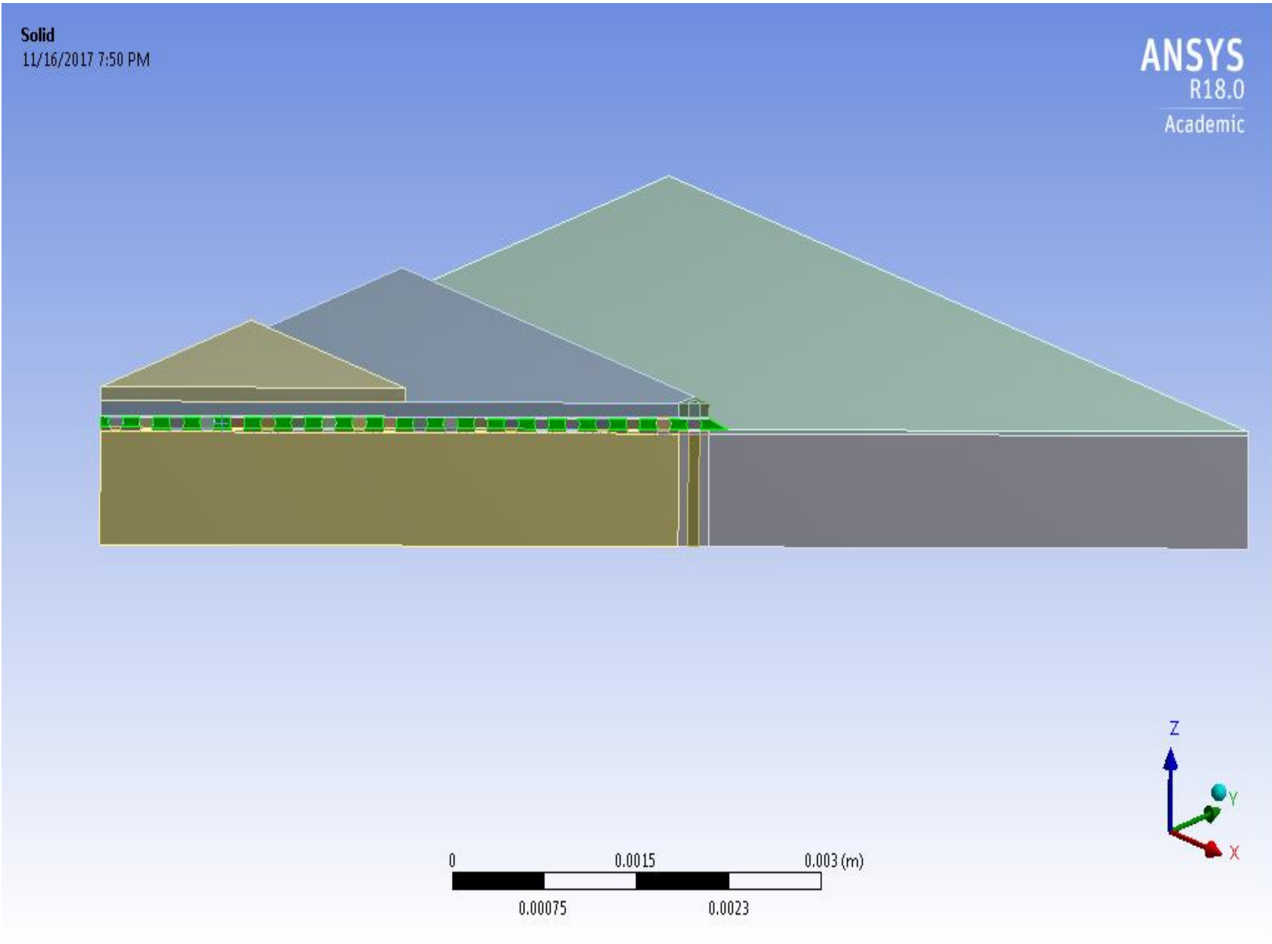


Figure 4.1: Octant model used for FEA simulations

Here an octant model has been used in order to save computational time. Solder ball reliability of this package for the two boards are tested using ATC. A temperature range of -40^{0}C to 125^{0}C with a dwell and ramp time of 15 minutes each is used for the ATC. A solder ball

might fail on both the package and board side, hence it is important to perform failure analysis on these two sides. Analysis will be done depending on the results obtained in further discussions. Figure 4.3 and figure 4.4 shows failure on solder ball on the package and the board side [4].

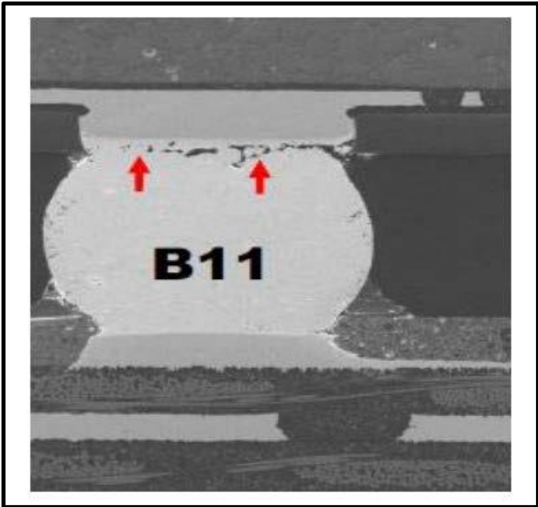


Figure 4.2: Solder ball failure towards package side

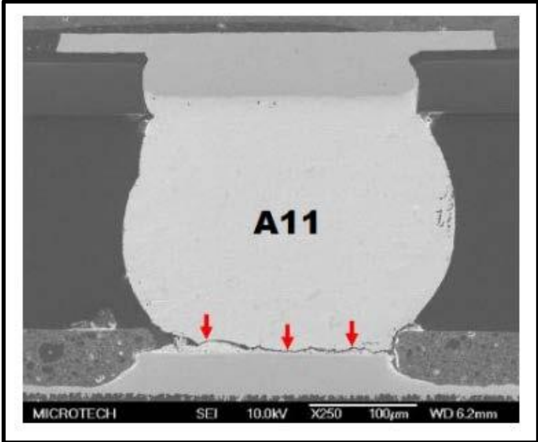


Figure 4.3: Solder ball failure towards board side

The figure below shows how the solder balls are modeled using FEA. The FEA model was developed using images and cross-sectional diagrams of an actual package. Material properties were assigned according to standards. The modeled is developed as such so that the computational results would be close to the actual experimental results.

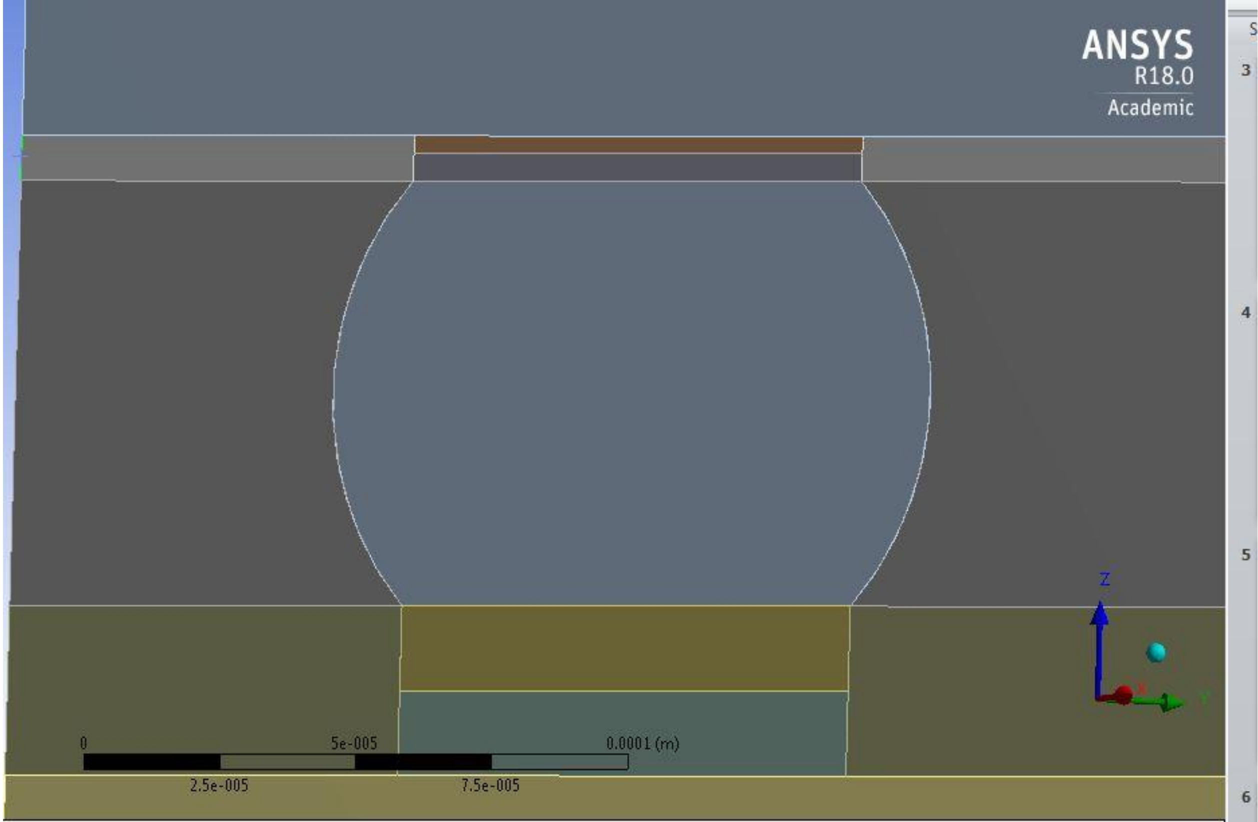


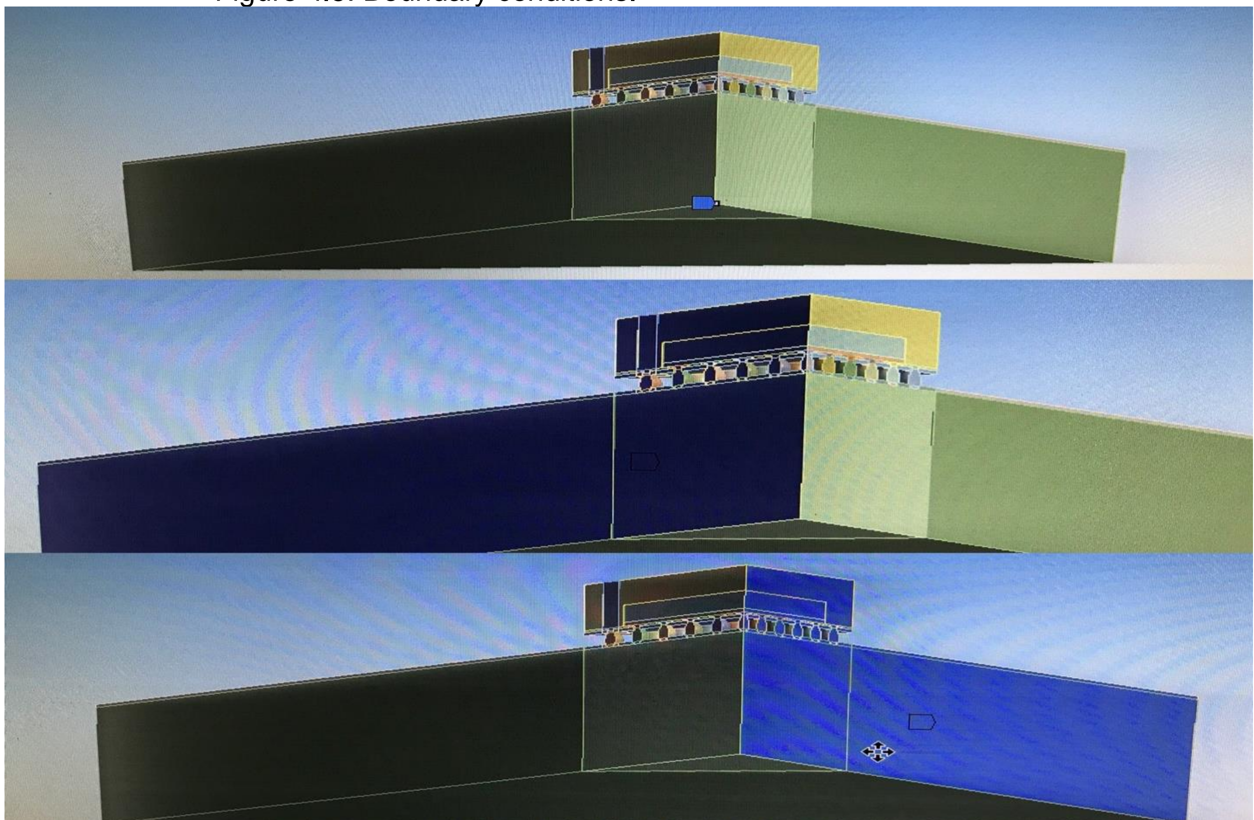
Figure 4.4: FEA diagram of the solder ball.

The solder ball pitch and number of solder balls is obtained from the above figures. All the dimensions are used to construct an octant symmetric model using ANSYS 18. An octant model is used to save the computational time.

4.2 Material Properties and Boundary Condition

Symmetric boundary conditions are applied on the 2 faces towards the inside where the geometry is split. Using octant geometry does not affect the accuracy of the result. The nature of all the properties were linear elastic, except the solder joints, mold compound and the PCB. The solder joints were considered as visco-plastic and so Anand's model was used to explain the behavior of the solder joints. SAC405 is an alloy made of 96.5% tin, 3% silver and 0.5% copper. It is used as the material for solder. Anand's viscoplastic constitutive law is used to describe the inelastic part of the lead-free 7solder. The Anand's constants are given in the Table. The PCBs were taken as linear orthotropic in nature. As mentioned in the assumptions, Solder is modeled as rate dependent viscoplastic material which uses Anand's viscoplastic model. It takes both creep and plastic deformation into consideration to represent secondary creep of the solder. Anand's viscoplastic constitutive law best describes the inelastic behavior of lead- free solder. Anand's law consists of nine material constants A, Q, ξ, m, n, hu, a, su, ŝ.

Figure 4.5: Boundary conditions.



4.3 Given Boundary Conditions

First Symmetry faces were applied on the two sides of the octant model to reduce the number of nodes and then the corner center was fixed to restrain any rigid motion.

Figure 4.6: Critical solder ball.

Table 4.1: Anand's material Constants for SAC 405

Constant	Name	Unit	Value
s0	Initial Deformation Resistance	MPa	1.3
Q/R	Activation Energy/ Universal Gas Constant	1/K	9000
A	Pre-exponential Factor	sec-1	500
ξ	Multiplier of Stress	Dimensionless	7.1

m	Strain Rate Sensitivity of Stress	Dimensionless	0.3
h0	Hardening/Sof tening Constant	MPa	5900
ŝ	Coefficient of Deformation Resistance Saturation	MPa	3.9
n	Strain Rate Sensitivity of Saturation	Dimensionless	0.03
a	Strain Rate of Sensitivity of Hardening or Softening	Dimensionless	1.4

ATC forces a uniform temperature distribution on entire package. It follows the JEDEC Standard No. 22A-10D. The test condition was from the temperature range (-40 to 125°C). The number of cycles per hour is less than 1-2. The ramp rate was taken 15 minutes and the soak time was also kept as 15 minutes.

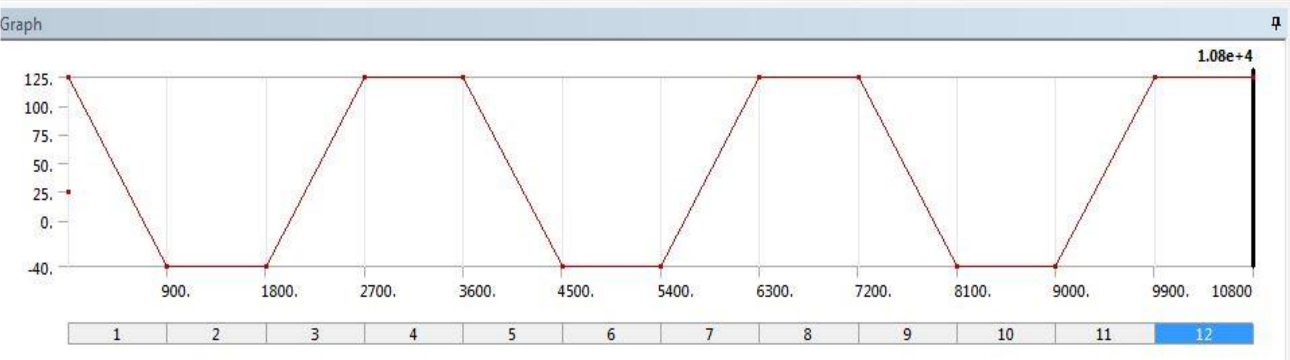


Figure 4.7 Thermal cycle profile

Chapter 5

RESULTS

The whole assembly deform in all direction and show bending effect under thermal loading. This is due to mismatch in CTE the component shows deformation or expansion in different rate causing stresses. The corner solder joint shows a maximum stress, strain and maximum plastic work. In the following parametric study different gap heights and material properties were chosen and the results were observed as follows.

Table 5.1: Different underfill material results

CTE	Modulus	Delta W	stress	strain
1.93E-05	8.91E+09	1.04E+05	9.88E+08	6.39E-02
1.97E-05	1.07E+10	1.10E+05	9.88E+08	6.37E-02
2.00E-05	6.00E+09	99349	9.63E+08	6.42E-02
2.00E-05	6.00E+09	99349	9.63E+08	6.42E-02
2.21E-05	8.71E+09	1.31E+05	9.95E+08	6.43E-02
2.23E-05	6.85E+09	1.26E+05	9.97E+08	6.34E-02
2.25E-05	6.00E+09	1.23E+05	9.97E+08	6.51E-02
2.28E-05	5.47E+09	1.22E+05	9.86E+08	6.73E-02
2.50E-05	6.00E+09	1.52E+05	1.00E+09	6.53E-02
2.50E-05	6.00E+09	1.52E+05	1.00E+09	6.53E-02
2.61E-05	6.03E+09	1.66E+05	1.00E+09	6.51E-02
2.69E-05	6.00E+09	1.77E+05	1.00E+09	6.53E-02
2.75E-05	6.00E+09	1.85E+05	1.01E+09	6.53E-02
3.00E-05	6.00E+09	2.23E+05	1.01E+09	6.54E-02

3.00E-05	3.00E+09	1.65E+05	9.38E+08	9.52E-02
3.00E-05	9.00E+09	2.45E+05	1.01E+09	6.62E-02
3.00E-05	7.00E+09	2.33E+05	1.01E+09	6.37E-02
3.00E-05	6.00E+09	2.23E+05	1.01E+09	6.54E-02
3.00E-05	5.00E+09	2.10E+05	9.95E+08	7.25E-02
3.25E-05	6.00E+09	2.67E+05	1.01E+09	6.55E-02
3.50E-05	6.00E+09	3.14E+05	9.99E+08	6.62E-02
3.75E-05	6.00E+09	3.66E+05	9.99E+08	6.67E-02
4.00E-05	6.00E+09	4.25E+05	9.82E+08	6.80E-02

Figure 2: Comparison of CTE vs Plastic Work

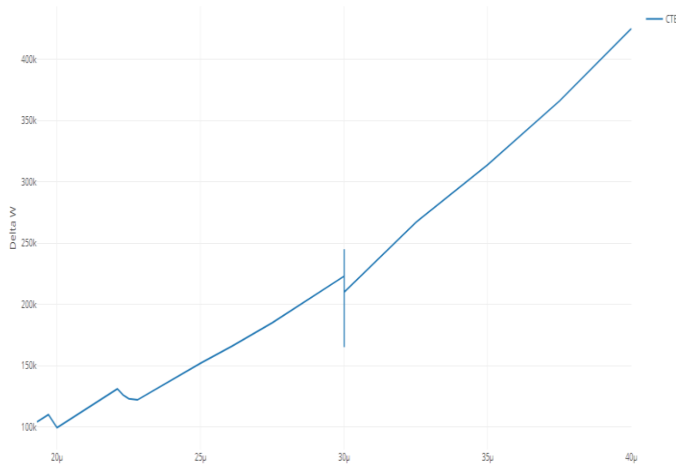


Figure 5.1: CTE vs DW.

As it is evident from the graph and table, the plastic work of the whole package is closely associated with the CTE of the underfill material. From this it could be stated that the lower the CTE of the underfill material the lower would be the plastic work accumulated in each cycle for the package and vice versa. But it should be noted that the CTE of the material is achieved by

varying the combination of the constituent components of the underfill material and their amounts used, and the same components are responsible for varying other material properties of the compound. Therefore, the range to which these properties could be varied are limited in reality.

Table 5.2: Different gap heights used.

gap	stress	Strain
0.2	4.95E+08	0.00318
0.19	4.78E+08	0.003123
0.18	4.70E+08	0.003304
0.17	3.52E+08	0.001767
0.16	3.55E+08	0.001783
0.15	3.50E+08	0.001756
0.14	3.37E+08	0.00169
0.13	3.63E+08	0.001819
0.12	3.50E+08	0.00176
0.11	3.41E+08	0.001962
0.1	3.51E+08	0.001767
0.09	3.45E+08	0.001734
0.08	3.41E+08	0.001715
0.07	3.44E+08	0.001725
0.06	3.61E+08	0.001813
0.05	3.74E+08	0.001884
0.04	3.70E+08	0.001861
0.03	4.10E+08	0.002053
0.02	3.35E+08	0.001743
0.01	4.29E+08	0.002143

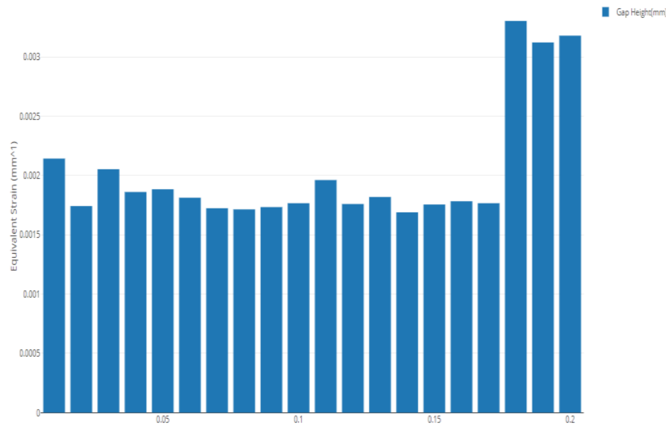


Figure 5.2: Comparison of Gap height vs Equivalent strain

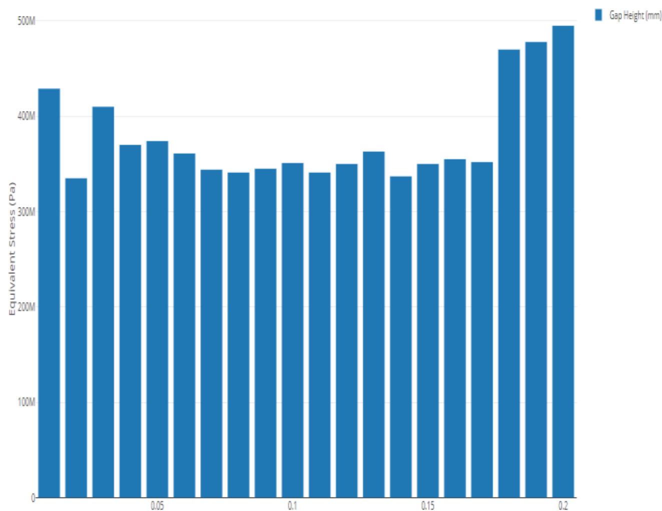


Figure 5.3: Comparison of Gap height vs Equivalent Stress

Varying the gap height by increasing the height of Cu-pads could reduce thee stress and strain levels of the package under CTE but as it could be observed from thee graphs and table of data it tends to pick up after a limit. There fore it is not advisable to increase the gap height more than 40% of the existing gap height.

5.1 Conclusions:

Thermo-Electrical stresses induced in a package during its usage is the major cause of

electronic package failure. The generation of this stresses are inevitable, what can be done is damage control. There are various methods to study these properties of the package, in which FEA is a prominent one. FEA is known to give close enough results so that experimental analysis could be avoided, saving time and cost. In this study the effect of material properties of underfill material and gap height on reliability of the whole package are studied. It was found out that the plastic work (delta W) accumulated during thermal cycling and the CTE of underfill material are closely associated and are directly proportional. The young's modulus of the material does not play a major in accumulation of plastic work but does influence delamination of the package. Lastly it was observed that gap height does not play a big role in induced stress and strain on the package even though a reduction in stress and strain were observed for small increases in gap height.

APPENDIX

APDL SCRIPT USED FOR STRAIN ENERGY DENSITY

! Commands inserted into this file will be executed immediately after the

ANSYS /POST1 command.

! Active UNIT system in Workbench when this object was created: Metric (m, kg, N, s, V, A)

! NOTE: Any data that requires units (such as mass) is assumed to be in the consistent solver unit system.

! See Solving Units in the help system for more information.

```
!APDL SCRIPT TO CALCULATE PLASTIC WORK

/post1 allsel,all

!CALC AVG PLASTIC WORK FOR CYCLE1 set,5,last,1 !LOAD STEP

cmsel,s,botsolder,elem !ELEMENT FOR VOL AVERGAING

etable,vo1table,volu pretab,vo1table

etable,vse1table,nl,plwk !PLASTIC WORK

pretab,vse1table

smult,pw1table,vo1table,vse1table

ssum

*get,splwk,ssum,,item,pw1table

*get,svolu,ssum,,item,vo1table

pw1=splwk/svolu !AVERAGE PLASTIC WORK

!CALC AVG PLASTIC WORK FOR CYCLE2

set,10,last,1 !LOAD STEP

cmsel,s,botsolder,elem

etable,vo2table,volu pretab,vo2table

etable,vse2table,nl,plwk !PLASTIC WORK

pretab,vse2table
```

```
smult,pw2table,vo2table,vse2table
ssum
*get,splwk,ssum,,item,pw2table
*get,svolu,ssum,,item,vo2table
pw2=splwk/svolu !AVERAGE PLASTIC WORK
!CALC DELTA AVG PLASTIC WORK
pwa=pw2-pw1
!CALC AVG PLASTIC WORK FOR CYCLE3

set,15,last,1 !LOAD STEP
cmsel,s,botsolder,elem
etable,vo3table,volu
pretab,vo3table
etable,vse3table,nl,plwk !PLASTIC WORK
pretab,vse3table smult,pw3table,vo3table,vse3table
ssum
*get,splwk,ssum,,item,pw3table
*get,svolu,ssum,,item,vo3table
pw3=splwk/svolu !AVERAGE PLASTIC WORK
!CALC DELTA AVG PLASTIC WORK
pwb=pw3-pw2
```

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BIOGRAPHICAL INFORMATION

Paul Crisanth received his Bachelor's in Engineering (B.E) degree in Mechanical Engineering from Noorul Islam University, India 2013. He pursued his Master's degree in Mechanical Engineering (MS) from the University of Texas at Arlington in fall 2017. He was an active member of EMNSPC Reliability team UTA and Surface Mount Technology Association Student Chapter at the University of Texas at Arlington. His research included experimental material characterizations of printed circuit boards performing various types of critical thermo mechanical analysis using ANSYS workbench, Spaceclaim, etc.

He was also a part of the Texas Instruments (TI) funded projects where he researched on industrial related applications. After graduation, he plans to pursue his career in the field of semiconductor industry and Electronic Packaging.