LOW PHASE NOISE VOLTAGE-CONTROLLED OSCILLATOR DESIGN

by

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ABSTRACT

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Two kinds of voltage-controlled oscillators (VCO) – active inductor based VCO and *LC* cross-coupled VCO – are studied in this work. Although the phase noise performance is not competitive, the proposed active inductor based VCO provide an alternative method to VCO design with very small chip area and large tuning range. The measurement shows a test oscillator based on active inductor topology successfully oscillates near 530MHz band.

The phase noise of the widely used *LC* cross-coupled VCO is extensively investigated in this work. Under the widely used power dissipation and chip area constraints, a novel optimization procedure in *LC* oscillator design centered on a new inductance selection criterion is proposed. This optimization procedure is based on a physical phase noise model. From it, several closed-form expressions are derived to describe the phase noise generated in the *LC* oscillators, which indicate that the phase noise is proportional to the $L^2 \cdot g_L^3$ factor. The minimum value of this factor for an area-limited spiral inductor is proven to monotonically decrease with increasing inductance, suggesting a larger inductance is helpful to reduce the phase noise in LC VCO design. The validity of the optimization procedure is proven by simulations. Two test chips are designed and measured.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

The explosive growth of today's telecommunication market has brought an increasing demand for high performance, low cost, low power consumption radio-frequency integrated circuits (RFICs). Tremendous effort has been reported to integrate all radio-frequency (RF) blocks, including the low-noise amplifier (LNA), mixer, intermediate frequency (IF) filter, local oscillator (LO) and power amplifier (PA) into a single chip [1]-[8]. Among all these RF blocks, the design on voltage-controlled oscillators (VCOs), which generate the LO carrier signal, is a major challenge and thus has received the most attention in recent years, as evidenced by the large number of publications [9]-[15]. The LOs are usually a frequency-synthesizer based on a phase-locked loop (PLL) as depicted in the Fig 1.1, in which the output oscillation signal is provided by a VCO. Due to the ever-increasing demand for bandwidth in communications, very stringent requirements are placed on the spectral purity of LOs, making the VCO design a critical sub-circuit to the overall system performance.

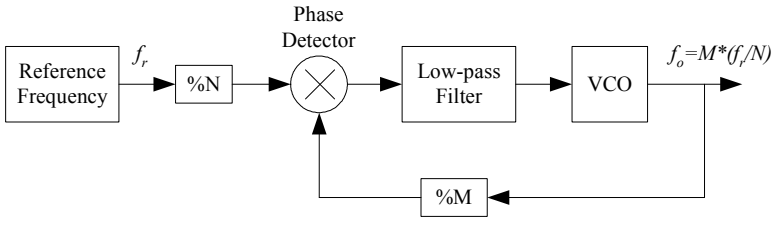


Figure 1.1 Block diagram of PLL-based frequency synthesizers

The phase noise is widely used to characterize the spectral purity (or frequency stability) of an oscillator. Although ring oscillators are more compact, the inductance-capacitance cross-coupled oscillators (*LC* oscillators) provide better phase noise performance at radio frequencies. This work focuses on the phase noise performance of *LC* oscillators.

In *LC* oscillators, the on-chip passive inductors are critical components. It is well known that a high quality factor (*Q* factor) tank can effectively improve the noise performance of the oscillators. However, due to several energy loss mechanisms of the on-chip passive inductor, the *Q* factors of the on-chip inductors as well as the overall *Q* factor of the tank are primarily limited by the given processing technology. Hence, many *Q* improvement methods require additional process steps, which may be impractical for circuit designers. Besides directly increasing the *Q* of the inductors, it will be shown the inductance selection also has significant impact on the phase noise performance. In this work, a new inductance selection criterion is proposed based on the investigation of the area-limited spiral inductors. According to this new inductance selection criterion, a novel optimization design procedure is presented for both bipolar and CMOS *LC* oscillators.

1.1 Organization

Chapter 2 gives a brief introduction to the oscillator and phase noise. It presents two models to explain the oscillation start-up mechanism. Basic noise sources in the active and passive elements are introduced and the phase noise of the oscillators is

defined. The negative consequences of the phase noise are illustrated in both the receiver and transmit paths.

Chapter 3 investigates the oscillator designs based on active inductors. The implementation of the active inductors using the gyrator topology is first introduced, followed by several oscillators designed by using active inductors. Although these circuits oscillate successfully, the study shows that their phase noise performance is relatively poor, making them inadequate for low-noise applications.

Chapter 4 focuses on the on-chip passive inductor design. The layout and structure of the inductors are introduced. Since the parasitic effects are critical to the inductors, their physical mechanisms are presented. Two modeling approaches, segmented model and compact model, are discussed in detail. To increase the accuracy, the parameters of the compact model are also extracted from simulation data by an extraction procedure. Very good consistency has been observed between the simulation and the models.

Chapter 5 reviews several phase noise models in detail, including the empirical Leeson's model, linear time-invariant model, linear time-variant model, non-linear time-invariant model and numerical model. These models explain the phase noise generation mechanism and provide helpful design insights to reduce the phase noise. The benefits and disadvantages of each phase model are compared.

For the *LC* oscillators, several phase noise improvement techniques are summarized in Chapter 6. The phase noise generation mechanisms, especially the

flicker noise up-conversion mechanisms, are presented. The topologies and trade-offs of these techniques are studied in detail.

Chapter 7 presents a new optimization procedure in low-noise *LC* oscillator design. A simplified, physical phase noise model is introduced first. Then the phase noise generated by the *LC* oscillators is expressed by several closed-form equations. These equations indicate that the phase noise is proportional to $L^2 \cdot g_L^3$, where g_L is the effective parallel conductance of the inductor. The simulation shows that the $L^2 \cdot g_L^3$ factor is reduced monotonically with the increase of the inductance, suggesting a larger inductance may result in better phase noise performance. Based on this inductance selection criterion, a new optimization procedure is proposed for both bipolar and CMOS *LC* oscillators.

In chapter 8, the layout and measurement of two oscillators – one active inductor based oscillator and one *LC* oscillator designed using the optimization procedure – are presented.

A summary of the results and suggestions of future work are given in Chapter 9.

CHAPTER 2

OSCILLATOR AND PHASE NOISE FUNDAMENTALS

Any practical oscillator has fluctuations in both the amplitude and the phase. Such fluctuations are caused by both the internal noise generated by passive and active devices and the external interference coupled from the power supply or substrate. The amplitude noise is usually less important in comparison with the phase noise for oscillators, since it is suppressed by the intrinsic nonlinear nature of oscillators. Hence, the amplitude fluctuations will die away after a period of time in oscillators. On the other hand, the phase noise will be accumulated, resulting in the severe performance degradation of the system where the oscillator is used. Therefore, wireless communication systems usually impose strict specifications on the phase noise performance.

Internal noise will be the focus of this dissertation. In this chapter, the fundaments of the oscillator and the phase noise are presented.

2.1 Oscillator Fundamentals

As an integral part of many electronic systems, oscillators are widely used in many applications ranging form clock generation in microprocessors to frequency synthesis in cellular phones. Note that even if the required working frequency is

constant, the oscillation frequency usually has to be tunable to overcome the imperfections in the fabrication process.

2.1.1 Categorization of VCOs

The voltage signal is widely used as the frequency control signal of the oscillators. Such a circuit is called the voltage-controlled oscillator (VCO). VCOs can be categorized by method of oscillation into resonator-based oscillators and waveform-based oscillators [16], as illustrated in Fig. 2.1. The output signal of resonator-based oscillators is sinusoidal while the waveform-based oscillators usually generate square or triangular wave. Primary examples of two categories are the *LC* oscillator and the ring oscillator, respectively. Each type has different ways of performing frequency tuning. For example, the current steering technique is used in ring oscillators and the variable capacitors (or varactors) are used for *LC* oscillators. According to the difference in the tuning circuits, the resonator-based oscillators can be further classified into *RC* circuits, switched-capacitor (*SC*) circuits, *LC* circuits and crystal oscillators.

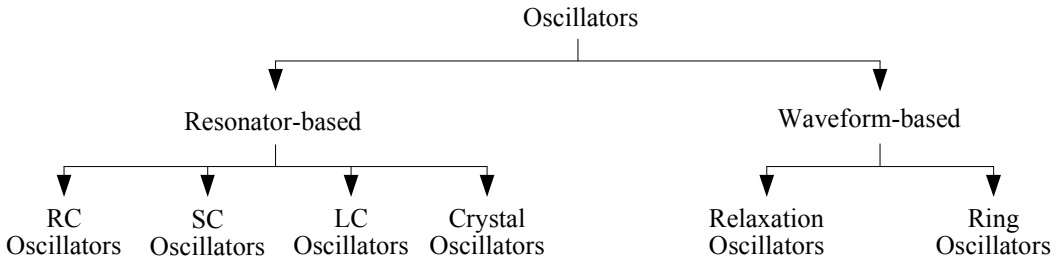


Figure 2.1 Classification of VCOs

In terms of integrability, ring oscillators are desirable in a VLSI environment. However, the *LC* oscillators usually provide better phase noise performance in

comparison with the ring oscillators at radio frequencies. In some application, their performance is even comparable with the crystal oscillators, which has the best phase noise quality. Relaxation VCOs are usually not a good choice for high frequency application due to the huge amount of phase noise introduced as a result of positive feedback. Since the *LC* oscillators provide very attractive low-noise performance, *LC* oscillators are the major topic in this dissertation.

2.1.2 Feedback Model of Oscillators

Although oscillators are nonlinear in nature, they are usually viewed as a linear time-invariant feedback system as shown in Fig 2.2. In the *s*-domain, the transfer function of this negative feedback system is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + A(s)F(s)}. \tag{2.1}$$

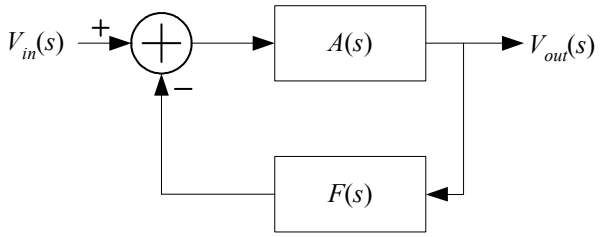


Figure 2.2 Block diagram of negative feedback systems

If the loop gain $A(s)F(s)$ is equal to –1 at a specific frequency ω_0, the closed-loop gain of (2.1) approaches infinity. Under this condition, the feedback becomes positive and the system trends to be unstable. Separating the magnitude and the phase of $A(s)F(s)$, the well-known "Barkhausen criteria" are obtained for the oscillation start-up

$$\left|A(j\omega_0)F(j\omega_0)\right| \geq 1, \tag{2.2}$$

$$\angle A(j\omega_0)F(j\omega_0) = 180°. \tag{2.3}$$

To guarantee the effective "regeneration" of the input signal, the magnitude of the loop gain has to be greater than unity (usually choose 2~3 in practical oscillators). The "input signal" here may be generated by any noise or fluctuation in oscillators. Note that Barkhausen criteria are necessary but not sufficient for oscillation [17].

2.1.3 Negative Resistance Model of Oscillators

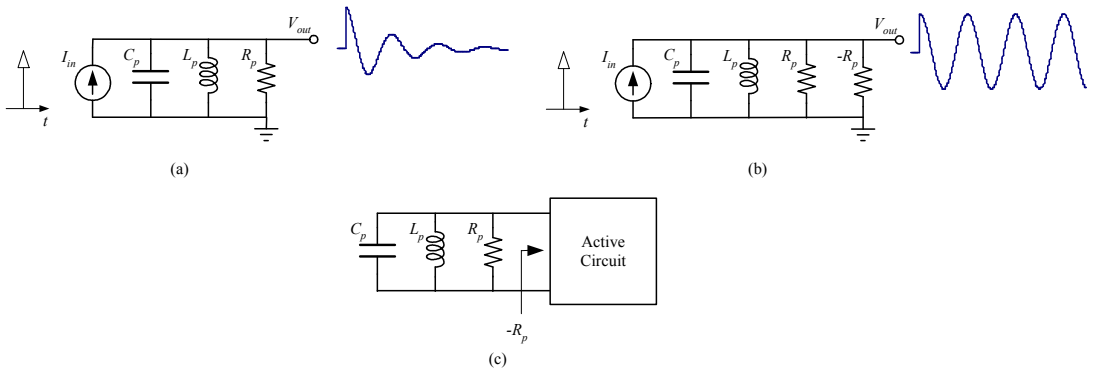


Figure 2.3 Negative resistance model (a) oscillation decays in a RLC tank (b) negative resistance compensates the energy loss and (c) negative resistance model

It is convenient to apply the feedback model to some types of oscillators such as ring oscillators. However, for resonator-based oscillators, an alternative view providing more insight into the oscillation phenomenon employs the concept of "negative resistance". The resonator can be equivalent to a parallel *RLC* tank circuit as shown in Fig 2.3 (a), where R_p captures the energy loss inevitable in any practical system. If the tank is stimulated by a current impulse, the tank responds with a decaying oscillatory behavior due to R_p. Now suppose a resistor equal to $-R_p$ is placed in parallel with R_p and the experiment is repeated (Fig. 2.3(b)). Since R_p // $(-R_p) = \infty$, the tank oscillates at

ω_0 indefinitely. Thus, if a one-port circuit exhibiting a negative resistance is placed in parallel with a tank, the combination may oscillate. Such a topology is called as negative resistance model (Fig. 2.3(c)).

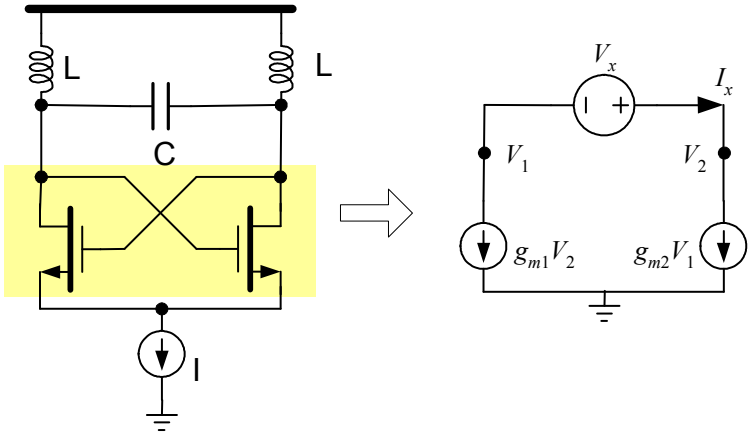


Figure 2.4 Negative resistance provided by cross-coupled transistors in *LC* oscillators

Active circuit can provide the negative resistance required in the negative resistance model. In the *LC* oscillator, the cross-couple transistors can be modeled as the small signal equivalent circuit depicted in Fig 2.4, where the 2nd order effects are neglected. If a voltage source is applied to the input, the following voltage and current equations can be derived

$$V_x = V_2 - V_1, \tag{2.4}$$

$$I_x = g_{m2} \cdot V_1 = -g_{m1} \cdot V_2. \tag{2.5}$$

Therefore, V_x is given by

$$V_x = V_2 - V_1 = -I_x \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}} \right). \tag{2.6}$$

If two transistors are identical, then the negative resistance is

$$\frac{V_x}{I_x} = \frac{-2}{g_m}. \tag{2.7}$$

This negative resistance will compensate the energy loss in the tank if $R_p \leq 2/g_m$ and the oscillation can sustain in the *LC* oscillator.

2.2 Phase Noise Fundamentals

2.2.1 Noise Sources in Passive and Active Devices

2.2.1.1 Thermal Noise

Thermal noise is generated by the random thermal motion of the electrons and is unaffected by the presence or absence of DC current, since typical electron drift velocities in a conductor are much less than electron thermal velocities. In a resistor *R*, thermal noise can be represented by a series noise voltage with the spectral density of

$$\frac{\overline{V^2}}{\Delta f} = 4kTR \tag{2.8}$$

where *T* is the absolute temperature. Thermal noise is present in any linear passive resistor. In bipolar devices, the parasitic spreading resistors such as R_b can generate the thermal noise. For MOSFETs, the resistance of the channel also generates thermal noise with the spectral density given by

$$\frac{\overline{V^2}}{\Delta f} = \frac{2}{3} \cdot 4kT / g_m \tag{2.9}$$

where g_m is the conductance of the channel. Note that the term 2/3 is accurate only for the long channel device and should be replaced by a larger value for submicron MOSFETs [18].

2.2.1.2 Shot Noise

Shot noise is associated with a DC current and is presented in diodes, CMOS and bipolar devices. It is the fluctuation of the DC current and usually is modeled as a noise current source with the spectral density of

$$\frac{\overline{I^2}}{\Delta f} = 2qI \,. \tag{2.10}$$

For example, the spectral density of the shot noise associated with the collector DC current in a bipolar transistor is given by

$$\frac{\overline{I^2}}{\Delta f} = 2qI_C \,. \tag{2.11}$$

2.2.1.3 Flicker Noise

Flicker noise is found in all active devices as well as in some discrete passive elements such as carbon resisters. It is mainly caused by traps associated with contamination and crystal defects. The flicker noise is also called as $1/f$ noise because it displays a spectral density of the form

$$\frac{\overline{I^2}}{\Delta f} = K_1 \frac{I^a}{f^b} \tag{2.12}$$

where I is the DC current, K_1, a and b are constants. If b = 1 in (2.12), the spectral density has a $1/f$ frequency dependence as shown in Fig. 2.5. Obviously, the flicker noise is most significant at low frequency. Note that MOSFETs usually generate more flicker noise in comparison with the bipolar counterpart.

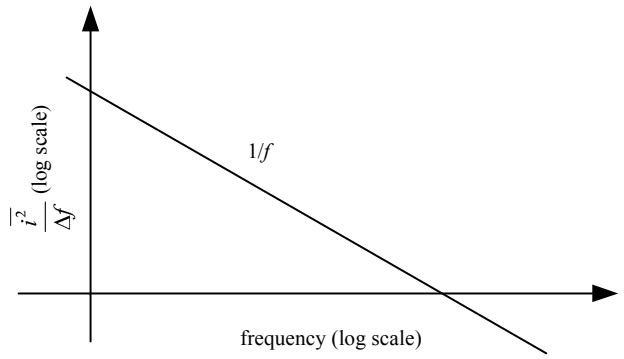


Figure 2.5 Spectral density of flicker noise versus frequency

Two other types of noise sources, the burst noise (also called as popcorn noise) and avalanche noise are also found the electronic systems. However, their effects on the phase noise of oscillators are neglected in this dissertation.

2.2.2 Definition of Phase Noise

For an ideal oscillator, the output can be expressed as $V_{out}(t) = V_0 \cos[\omega_0 t + \phi_0]$, where amplitude V_0, the frequency ω_0, and the phase reference ϕ_0 are constants. In the frequency domain, the one-side spectrum of such an oscillation signal is an impulse at ω_0 as shown in Fig 2.6 (a). As a comparison, the typical spectrum of the practical oscillators is illustrated in Fig 2.6 (b). It has power around harmonics of ω_0 if the oscillation waveform is not sinusoidal. More important, due to the existence of the noise generated by active and passive elements, the spectrum of a practical oscillator has sidebands close to and its harmonics, resulting in the fluctuation in oscillation frequency. These sidebands are generally referred as phase noise sidebands.

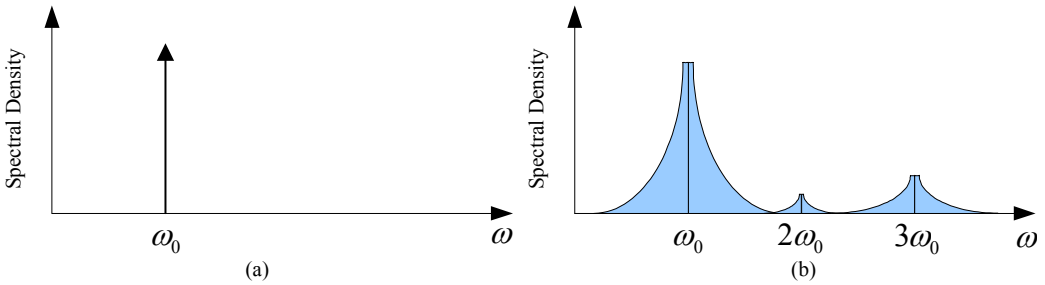


Figure 2.6 Spectrum of an ideal (a) and a practical oscillator (b)

The phase noise describes the fluctuation of the oscillation frequency. Many ways of quantifying a signal's frequency instabilities have been put forward [19], but it is usually characterized in terms of the single sideband noise spectral density. It has units of decibels below the carrier per hertz (dBc/Hz) and it is defined as

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega,\quad 1Hz)}{P_{carrier}}\right] \tag{2.13}$$

where $P_{sideband}(\omega_0+\Delta\omega,\ 1\text{Hz})$ represents the single side-band power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1Hz as visualized in Fig 2.7. Note that the above definition includes the effect of both amplitude and phase fluctuations.

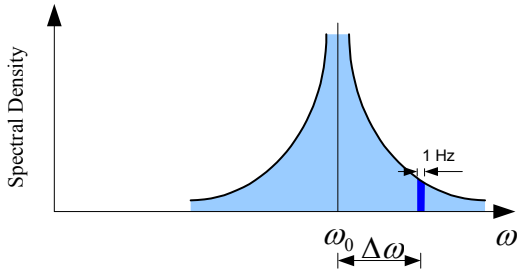


Figure 2.7 Definition of phase noise

The advantage of this parameter is its ease of measurement. Its disadvantage is that it shows the sum of both amplitude and phase variations. However, it is important to know the amplitude and phase noise separately because they behave differently in the circuit. For instance, the effect of amplitude noise is reduced by the intrinsic amplitude limiting mechanism in oscillators and can be practically eliminated by the application of a limiter to the output signal, while the phase noise cannot be reduced in the same manner. Therefore, in most applications, the phase noise of the oscillators is dominated by the phase noise, which will be investigated in the following chapters.

2.2.3 Destructive Effects of Phase Noise

The destructive effect of phase noise can be best seen in the front-end of a super-heterodyne radio transceiver. Fig. 2.8 (a) illustrates a typical front-end block diagram, in which the receiver consists of a LNA, a band-pass filter and a down-conversion mixer and the transmitter comprises an up-conversion mixer, a band-pass filter and a power amplifier. The LO that provides the carrier signal for both mixers is embedded in a frequency synthesizer (see Fig 1.). If the LO is noisy, both the down-converted and up-converted signals are corrupted, as depicted in Fig. 2.8 (b) and (c). Note that a large interferer in an adjacent channel may accompany the wanted signal according to Fig. 2.8 (b). When two signals are mixed with the LO output exhibiting finite phase noise, the down-converted band consists of two overlapping spectra, with the want signal suffering from significant noise due to tail of the interferer. This effect is called “reciprocal mixing”[20].

Shown in Fig. 2.8 (c), the effect of phase noise on the transmit path is slightly different. Suppose a noiseless receiver is to detect a weak signal at ω_2 while a powerful, nearby transmitter generates a signal at ω_1 with substantial phase noise. Then, the wanted signal is corrupted by the phase noise tail of the transmitter.

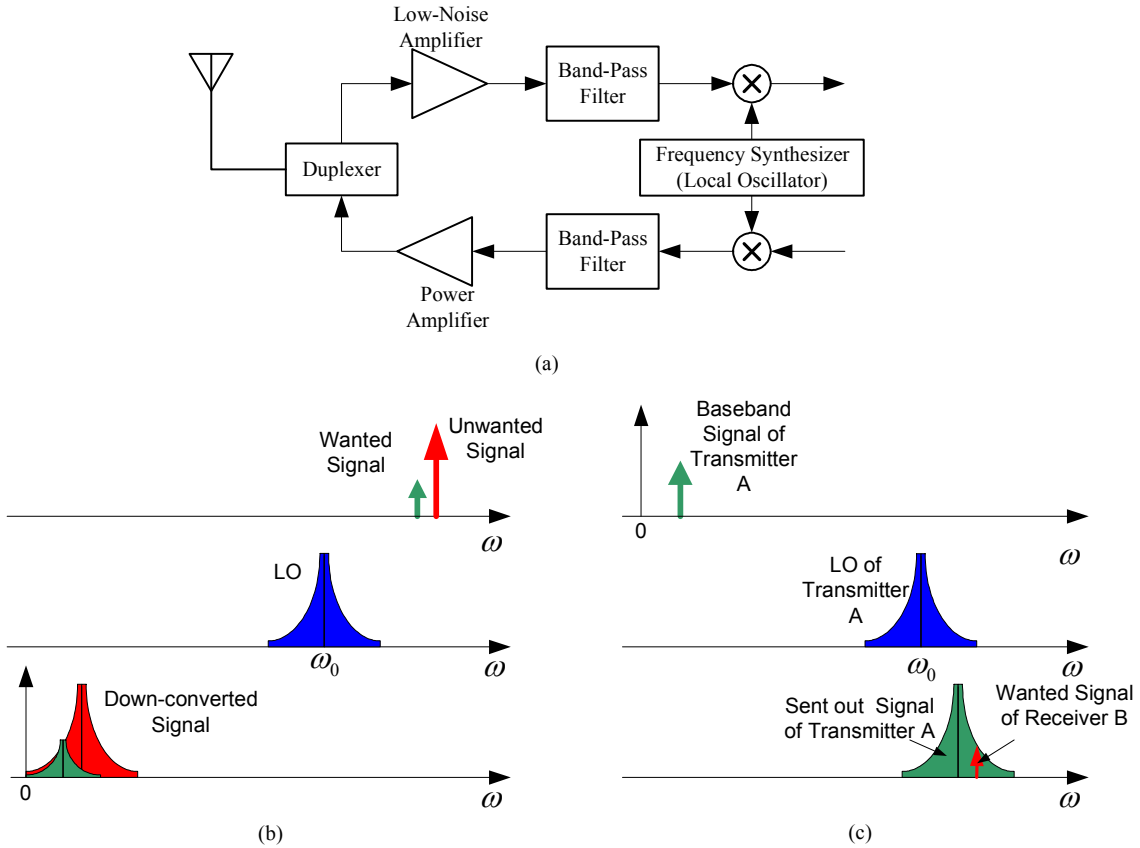


Figure 2.8 Destructive effect of phase noise on typical wireless transceivers (a) Block diagram of wireless transceivers (b) Effect of phase noise on receive path and (c) Effect of phase noise on transmit path

Note the channel spacing in modern wireless communication systems can be as small as a few tens of kilohertz while the carrier frequency may be several hundreds megahertz or even several gigahertz. Therefore, the output spectrum of the LO must be

extremely sharp. For example, in a GSM system, the phase noise power per unit bandwidth must be about 118dB below the carrier power (-138dBc/Hz) at an offset of 200kHz [21]. Such stringent requirements impose a great challenge in low-noise oscillator design.

2.3 Summary

Fundamental knowledge of oscillators and phase noise was presented in this chapter. The physical mechanism of oscillation was investigated from two oscillator models – the feedback model and the negative resistance model. Several types of noise in both active and passive devices were introduced. The phase noise definition and its destructive effects on wireless communication systems were briefly discussed.

CHAPTER 3

ACTIVE INDUCTOR BASED OSCILLATORS

It will be shown in the next chapter that the integrated passive inductor usually has poor Q factor and occupies large chip area. The reliability is also questionable especially if the extra process steps are used to increase the Q factor. On the other hand, the functionality of the passive inductors can be emulated by the active component to obtain a more reliable and cost-effective design. In the chapter, the active inductor based oscillators will be investigated.

3.1 Gyrators

A gyrator [22] provides the most direct means of simulating a passive inductor. As depicted in Fig 3.1, it consists of an anti-parallel connection of two transconductances. If a capacitor, C_1, is connected to one port of the gyrator, the input impedance seen from the other port is given by

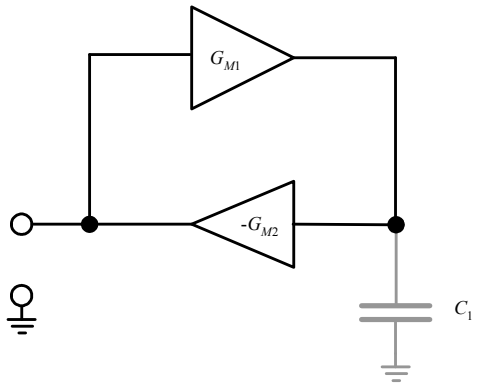


Figure 3.1 Gyrator topology

$$Z_{in} = j\omega \frac{C_1}{G_{m1} G_{m2}}. \tag{3.1}$$

Therefore, the topology in Fig 3.1 is equivalent to an inductor with inductance of $C_1/(G_{m1} \cdot G_{m2})$.

The simplest active inductor based on a gyrator topology is shown in Fig 3.2 [23]. In this circuit, the anti-parallel connection of two transconductances is realized by two MOSFETs configured as the common-source (M_1) amplifier and the source follower (M_2). The parasitic capacitance attached on the node A forms the corresponding C_1 in Fig 3.1. Using TSMC0.25μm model file (see appendix 1), the equivalent inductance defined as $\mathrm{Im}[Z_{in}]/\omega$ is simulated and plotted in Fig 3.3 (a). This result suggests that the circuit successfully emulates a 5.34nH inductor if the frequency is lower than 3GHz. At higher frequency, however, the circuit becomes capacitive due to the parasitics.

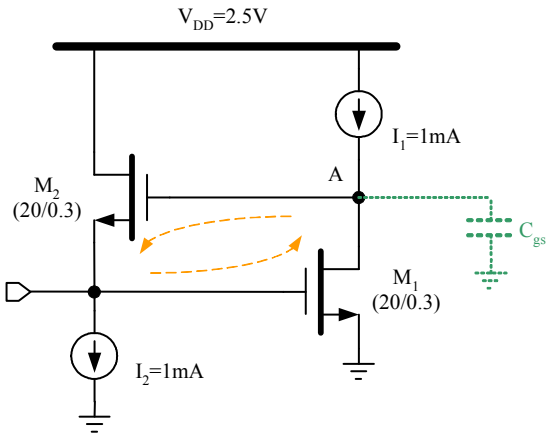
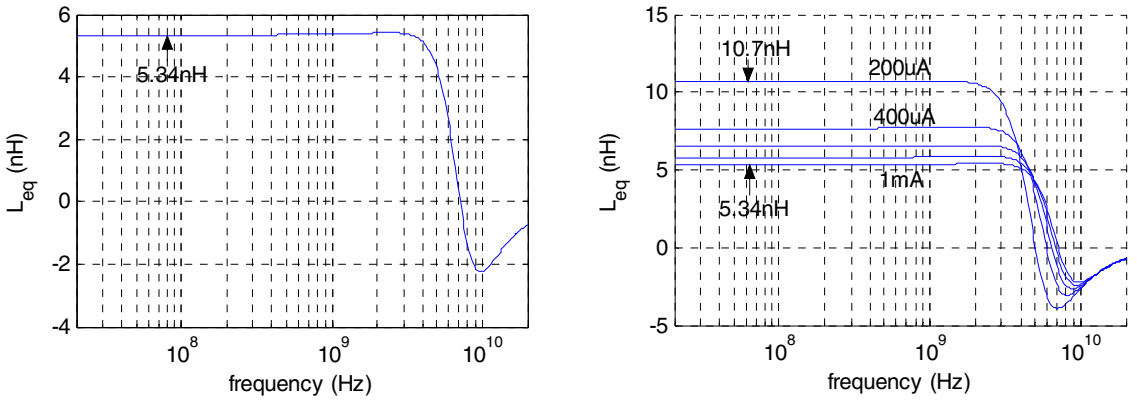


Figure 3.2 A simple gyrator in MOS implementation

One of the benefits of the active inductors is their tuning capability. As shown in Fig. 3.3 (b), the inductance of the circuit is tuned form 5.34nH to 10.7nH simply by decreasing the bias current I_1 from 1mA to 200μA. Hence, the oscillators based on the active inductors can achieve wide tuning range with simple tuning circuitry.



(a) (b)

Figure 3.3 Equivalent inductance of the circuit in Fig. 3.2 (a) with 1mA bias current and (b) with 200μA, 400μA, …, 1mA bias current

The quality factor is one of the most critical parameters to characterize inductors and it will be frequently used in this dissertation. The most fundamental definition of the Q factor is

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}} \tag{3.2}$$

The above definition does not specify what stores or dissipates the energy. For an inductor, only the energy stored in the magnetic field is of interest. Therefore, the nominator is equal to the difference between peak magnetic and electric energy. In the LC oscillators, the LC tank is usually represented by a parallel RLC circuit. In this case, it can be shown that the Q factor can be expressed as [24]

$$Q = 2\pi \cdot \frac{\text{peak magnetic energy - peak magnetic energy}}{\text{energy loss in one oscillation cycle}}$$

$$= \frac{R_p}{L\omega} \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right] = \frac{\text{Im}(Z)}{\text{Re}(Z)} \tag{3.3}$$

where R_p and L are the equivalent parallel resistance and inductance, respectively, ω_0 is the resonance frequency, and Z is the impedance seen at one terminal of the inductor while the other is grounded. This definition will be followed in the dissertation for both active and passive inductors. However, although it is extensively used, this definition is only applicable at low frequency where the circuit or device is inductive. In addition, for active inductor, there is no magnetic energy stored.

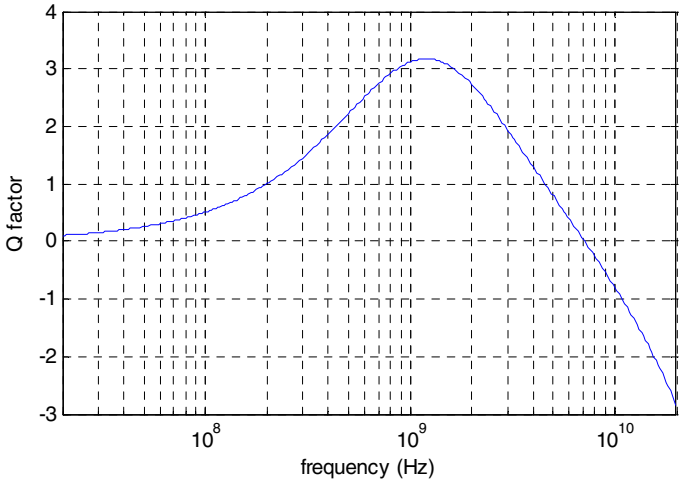


Figure 3.4 Q factor of the circuit in Fig. 3.2 with 1mA bias current

According to the definition of (3.3), the Q factor of the simplest active inductor is plotted in figure 3.4. Note that although the Q factor in this case is only slight larger than 3, very large Q factor (several hundred or even higher [25]) are achievable for the

active inductors. This feature makes the active inductors an attractive solution in active filter design [23], [26]-[28].

3.2 Oscillators Based on Active Inductors

Two oscillators based on the active inductor topology are investigated. In the first oscillator, the active inductor replaces the inductor in a *LC* oscillator. The second oscillator is implemented by the active inductor directly. The bipolar transistors are used in both designs.

3.2.1 Embedded Active Inductor into LC Oscillator

The active inductor depicted in Fig 3.2 is single-ended. However, floating inductors are desirable in both oscillator and filter designs. Such a floating active inductor is shown in Fig 3.5 (a) [28]. In this active inductor implementation, two active inductors consisting of Q_1, Q_2, Q_3 and Q_4, Q_5, Q_6 are combined together to form a floating active inductor. For each active inductor, the anti-parallel connection of two transconductances is implemented by combining a common-collector common-base configuration (Q_1, Q_2) with a common-emitter stage (Q_3). For a quick understanding of the circuit operation, assume the bipolar transistors are modeled by g_m and c_π only. By applying a test voltage v_1 at the input port, a feedback current $i_f = g_m \cdot v_1/2$ is generated which charges up $c_{\pi 3}$. This in turn creates an input current, $i_1 = v_1 \cdot g_m^2/(s \cdot 2c_{\pi 3})$, where all transistors are assumed to have the same transconductance, $g_{m1} = g_{m2} = g_{m3} = g_m$. From this expression of i_1, the input impedance can be calculated as

$$Z_{in} \approx s \cdot 2 \cdot c_{\pi 3} / g_m^2 . \tag{3.4}$$

Note that the idealized input impedance is purely inductive. It is similar to the ideal gyrator's input impedance given by (3.1).

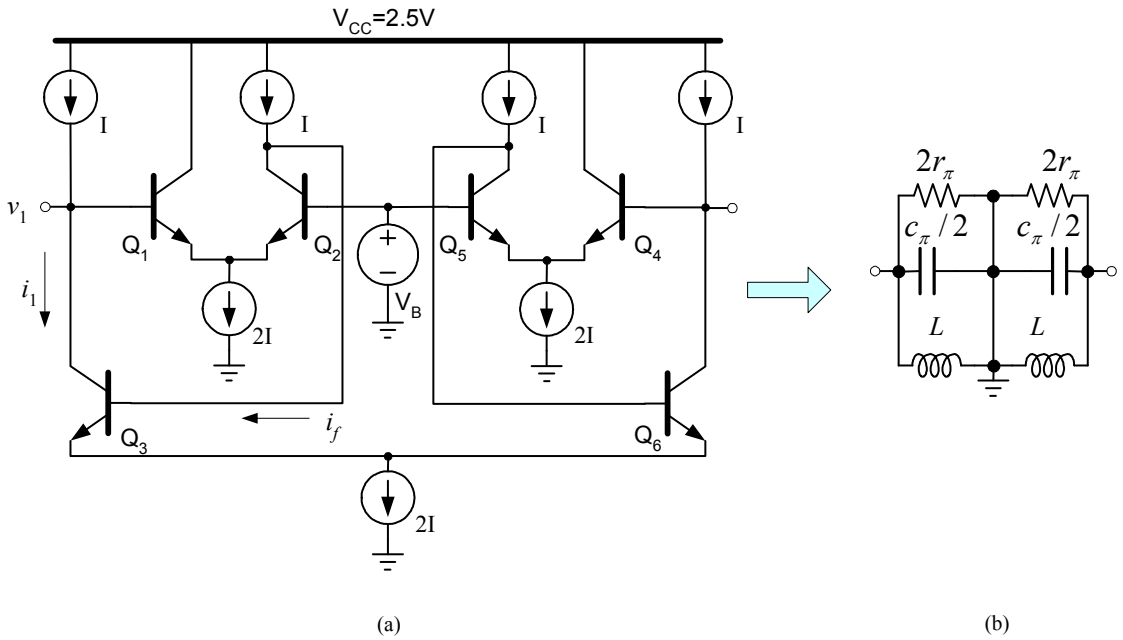


Figure 3.5 A floating active inductor (a) and its passive counterpart (b)

If r_π is also taken into account, the more detail analysis reveals that the input impedance is give by

$$Z_{in} = \frac{s \cdot 2 \cdot c_{\pi 3}}{s \cdot c_{\pi 3} / r_\pi + s^2 \cdot 2 \cdot c_\pi \cdot c_{\pi 3} + g_m^2}, \tag{3.5}$$

where $g_{m1} = g_{m2} = g_{m3} = g_m$, c_π is the base-charging capacitance for Q_1 and Q_2, $c_{\pi 3}$ is the base-charging capacitance of Q_3, r_π is the input resistance of Q_1 and Q_2. The first term beginning from the left-hand side of the denominator contributes an equivalent resistance and the second term indicates a very high frequency self-resonance resulted by capacitive components, while the last term corresponds to an inductor. Hence, (3.5)

suggests the active inductor in Fig. 3.5 (a) can be modeled by a parallel *RLC* circuit as shown in Fig. 3.5 (b).

The above analysis is proven by the small signal simulation results provided in Fig 3.6. The resistance and reactance of the input impedance of the active inductor in Fig 3.5 (a) are plotted in Fig 3.6 (left and right, respectively). A generic bipolar model file is used in this simulation (see appendix 2). The power supply is 3V and the bias voltage at the base of Q_2 and Q_5 is V_B = 1.6V. All current sources in Fig. 3.5 are realized by the simple current mirrors with I = 1.3mA (not shown in Fig. 3.5). As a comparison, the resistance and reactance of the passive counterpart as depicted in Fig 3.7 are plotted in Fig. 3.6. In the equivalent passive circuit, two small resistors capturing the base spreading resistance are added. Very good consistencies are observed in the simulation results. Note that the resistance becomes negative near the frequency of 800MHz, suggesting that the active inductor becomes unstable.

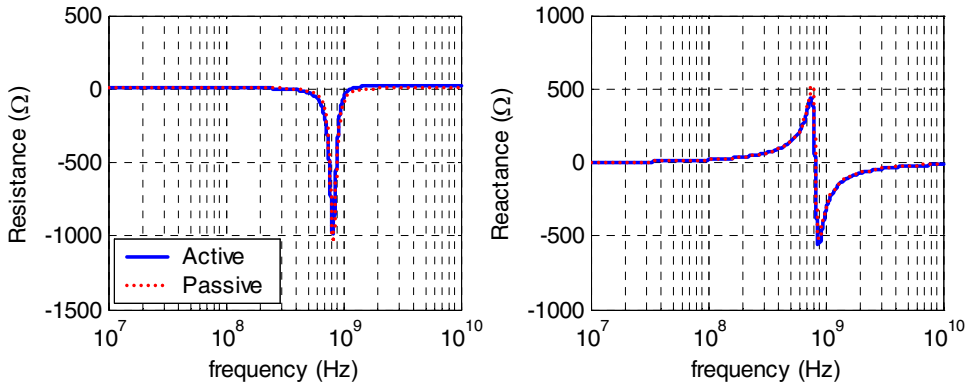


Figure 3.6 Resistance (left) and reactance (right) of the input impedance of the active inductor in Fig. 3.15 (a)

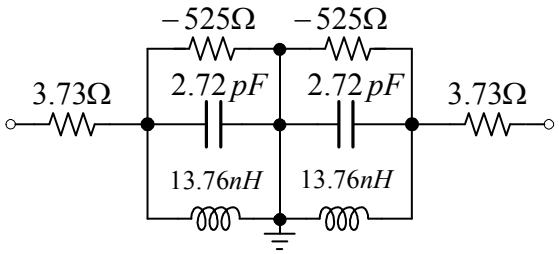


Figure 3.7 The equivalent *RLC* circuit for active inductor in Fig. 3.5 (a)

This active inductor is then embedded into an *LC* oscillator as shown in Fig. 3.8 (a) [29]. Since the active inductor is equivalent to a *RLC* circuit, it is used as a resonator directly in order to achieve the maximum oscillation frequency. Two resistors, R_C (=3.3kΩ), act as the load of the cross-coupled transistors and provide the DC operation point for the devices. The power supply is 3V and the tail current is 0.85mA which is realized by a simple current mirror (not shown in the figure). The completed schematic of the active inductor is illustrated in Fig 3.8 (b). Note that the bias current of the active inductor is tunable by controlling the voltage of input node, f_{ctrl}. According to the previous analysis, the bias currents change the g_m of the transistors. Accordingly, the inductance is changed and the oscillation frequency is tunable.

Such an active-inductor-based *LC* oscillator is successfully oscillates at frequency of 465MHz, as evidenced by the transient simulation result depicted in Fig. 3.9 (a). The amplitude of the differential output signal is about 180mV. Note that although the equivalent *RLC* tank circuit has a resonating frequency about 822MHz, the actual oscillation frequency is much lower due to the parasitic capacitance at the node *V*1 and *V*2 and the nonlinear large signal characteristic of the oscillator.

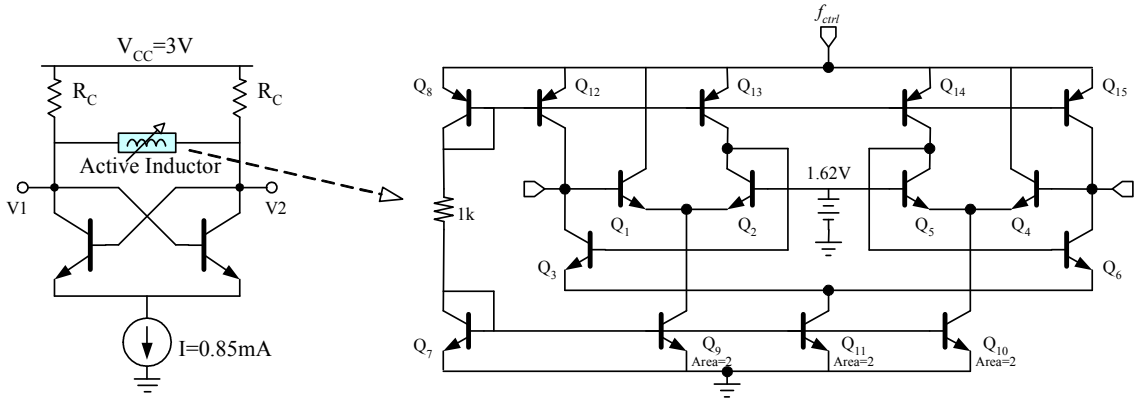


Figure 3.8 A *LC* VCO based on active inductor in Fig 3.5 (a)

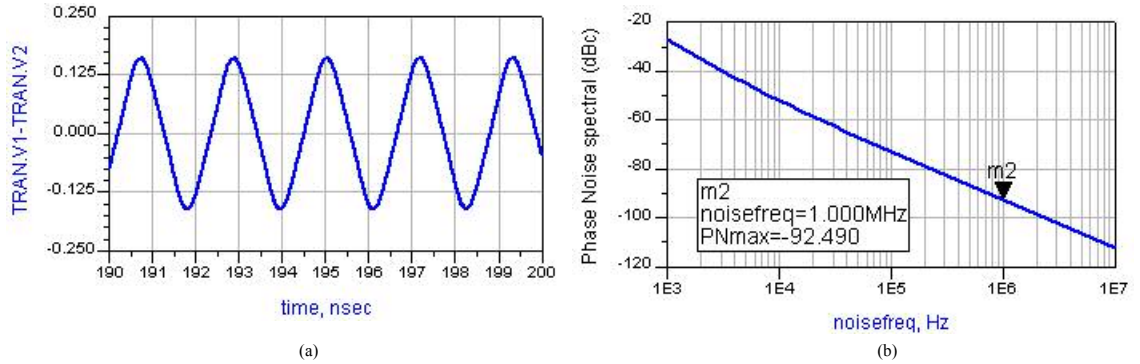


Figure 3.9 The waveform (a) and phase noise (b) of the oscillator in Fig 3.8

The oscillator's phase noise is obtained by the Advanced Design System (ADS) Harmonic Balance simulation, and the result is shown in Fig. 3.8 (b). The oscillator exhibits a –92.49dBc phase noise at the offset frequency of 1MHz. This noise performance is relatively poor in comparison with the *LC* oscillator realized by the passive inductors. Note that the phase noise also depends on the selection of R_C and f_{ctrl} voltage. Such dependence is illustrated in Fig. 3.10. However, for certain bias currents, the minimum phase noise at 1MHz offset is limited to about –92~–91dBc for this active inductor based oscillator.

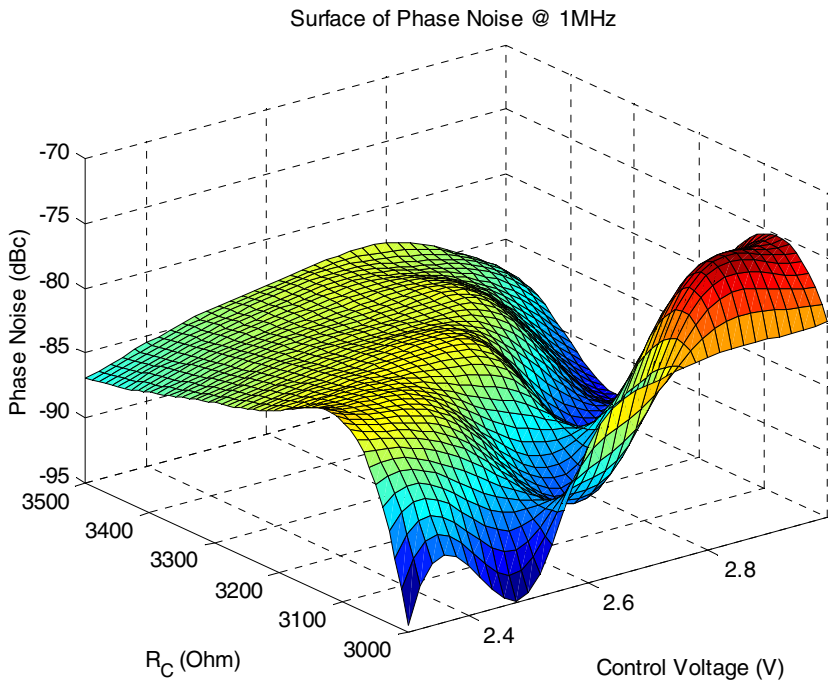


Figure 3.10 The phase noise at 1MHz offset as a function of R_C and f_{ctrl} voltage

Finally, the oscillation frequency and the phase noise (at 1MHz offset) as a function of the control voltage are plotted in the Fig. 3.11 (R_C = 3.3kΩ). This oscillator exhibits 157% tuning range when control voltage sweeps from 2.1V to 3V, which is very wide. The gain of the VCO is $K_v \approx$ 540MHz/V. On the other hand, a relatively large phase noise variation (near 10dB) in the tuning range is observed.

Another drawback of this oscillator is the power dissipation. For instance, the overall power dissipation is 36mW if the control voltage is chosen as 3V. However, the active inductor consumes 28.2mW, which is nearly 78.3% of the total power dissipation.

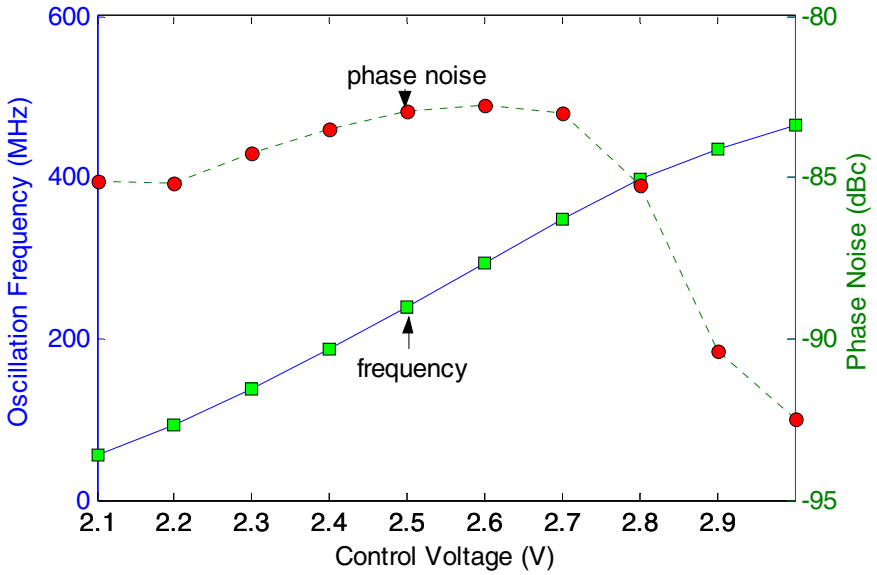


Figure 3.11 Oscillation frequency and phase noise as a function of the control voltage

3.2.2 Active Inductor Acts as an Oscillator

The simulation result in Fig. 3.6 shows that the input resistance of the active inductor is negative. This result seems to be opposite the conclusion in equation (3.5), where the resistance in the *RLC* circuit is equal to r_π. The contradiction can be explained by taking the base spreading resistance r_b into account. If the bipolar transistor is modeled by both c_π, r_π, g_m and r_b, the small signal equivalent circuit of the active inductor can be obtained as shown in Fig. 3.12, where only the single-ended inductor that consists of Q_1, Q_2 and Q_3 is included.

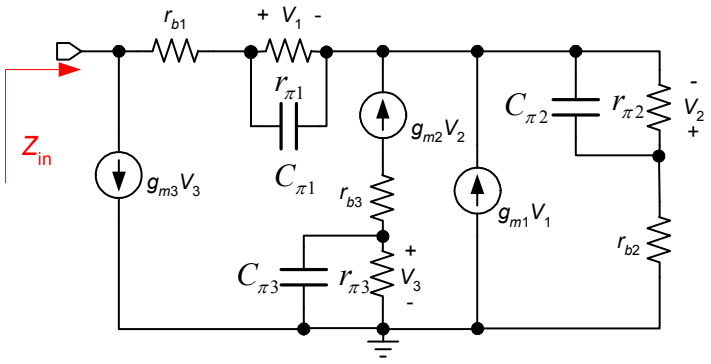


Figure 3.12 Small signal model of the active inductor in Fig 3.5 (a)

With the help of the small signal model, the input impedance Z_{in} is given by

$$Z_{in} = \frac{(g_{m2} + sZ_{\pi 2})(1 + sZ_{\pi 1} r_{b1}) + (g_{m1} + sZ_{\pi 1})(1 + sZ_{\pi 2} r_{b2})}{sZ_{\pi 1}(g_{m2} + sZ_{\pi 2}) + \frac{g_{m2} g_{m3}(g_{m1} + sZ_{\pi 1})}{sZ_{\pi 3}}} \tag{3.6}$$

where $Z_{\pi i} = r_{\pi i} // C_{\pi i}$ (i =1, 2 and 3). If the transistors are identical and are biased by the same current, $g_m = g_{mi}$ and $Z_\pi = Z_{\pi i}$ are valid. Hence, (3.6) is simplified to

$$Z_{in} = \frac{-2\omega^2 Z_\pi^2 r_b + 2j\omega Z_\pi}{g_m^2 - \omega^2 Z_\pi^2}. \tag{3.7}$$

Obviously, the real part of the input impedance is negative if g_m is large enough. Therefore, according to the negative resistance model discussed in Chapter 2, such a circuit can "generates" energy and thus may oscillate, suggesting the active inductor can act as an oscillator directly with the proper bias.

Based on this idea, a single-ended oscillator is designed as depicted in Fig 3.13. The simulated output signal and its phase noise are plotted in Fig 3.14 (a) and (b), respectively. As it has been expected, the oscillation successfully started up. The circuit consumes less power (29.5mW), but oscillates at higher frequency (538.9MHz) due to

the simpler design. However, the phase noise performance has no significant improvement in comparison with the previous one. A VCO based on this topology was fabricated and the measurement results are provide in Chapter 8.

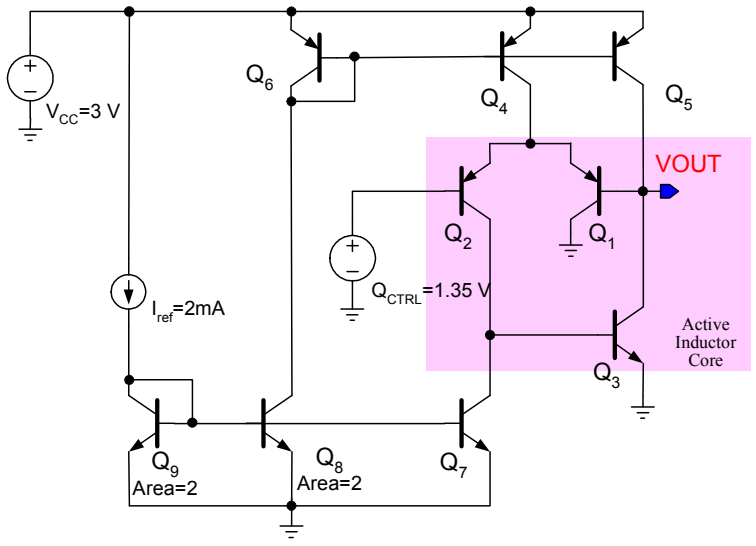
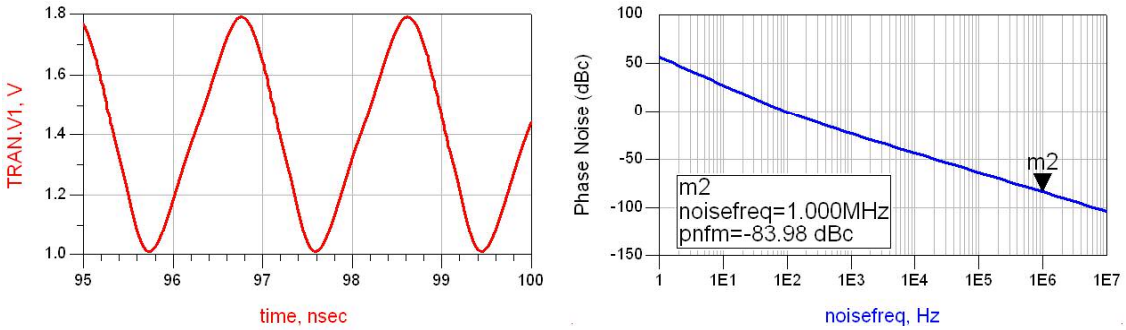


Figure 3.13 Make the active inductor as an oscillator directly



(a) (b)

Figure 3.14 Waveform (a) and phase noise (b) of the oscillator in Fig 3.13

3.3 Pros and Cons of the Active Inductor Based Oscillators

As demonstrated in the previous design, the active inductor based oscillators usually have very large tuning range due to the tuning capability of the active inductors.

Since the inductance is controlled by bias current, the tuning circuitry is easy to be implemented, making the active inductor suitable to VCOs design. On the other hand, the inductance of the integrated passive inductors is constant.

The active inductor based oscillators is realized only by the transistors and capacitors (if necessary). Hence, it is possible to achieve very compact designs in term of the chip area. On the contrary, the passive inductors are usually very large, significantly increasing the cost of the chip. In addition, the active inductors are insensitive to fabrication process. Therefore, they provide better reliability especially if the extra process steps are utilized in the passive inductor fabrication.

However, the phase noise performance of the active inductor based oscillators is relatively poor due to the lack of the narrow band tank circuit. Note that noise generated by the active devices in the active inductors significantly deteriorates the phase noise even if the inductor has a very high Q factor. The transistors in the active inductor also increase the power dissipation of the oscillator. According to (3.1), the inductance is in reversely proportional to g_m, resulting in higher power dissipation at higher frequency. In some cases, the power consumed by the active inductors is even dominating.

In summary, although the active inductors provide some benefits such as tuning capability and compact chip area, the excessive noise and power dissipation limit its application in oscillator design especially at radio frequencies.

CHAPTER 4

ON-CHIP PASSIVE INDUCTORS

The passive devices such as inductors, capacitors, resistors and transformers are traditionally considered playing a minor role in comparison with active devices. However, they are actually very critical parts in today's RFICs. At low frequency, designers usually emulate the functionality of passive devices with active components to make their design more reliable and cost-effective as demonstrated in the last chapter. This method is generally not applicable at radio frequency. For example, the oscillators based on the active inductors generate unacceptable phase noise.

The passive capacitors and resistors are relatively easy to integrate in comparison with the passive planar inductors. However, the inductors are widely used in almost all fundamental building blocks of RF circuits, including oscillators, LNA, filters, transforms and matching circuitry. Their quality significantly affects the performance of the overall system. For the integrated inductors, the capacitive and the electromagnetic coupling between individual passive component and the low resistivity substrate used for latch-up suppression degrade their Q factor. For example, given the commonly used metal thicknesses in the typical CMOS technology, the Q for inductors <10nH inductor on a low resistivity substrate is limited to below six [30].

The rest of the dissertation will focus on the *LC* oscillator based on the passive integrated inductors and its phase noise performance. This kind of oscillator provides a very competitive phase noise performance when working at the radio frequency due to the narrow band tank. The passive inductor plays a decisive role in the *LC* oscillator performance, especially the phase noise performance. Hence, its characteristics will be investigated in this chapter in detail.

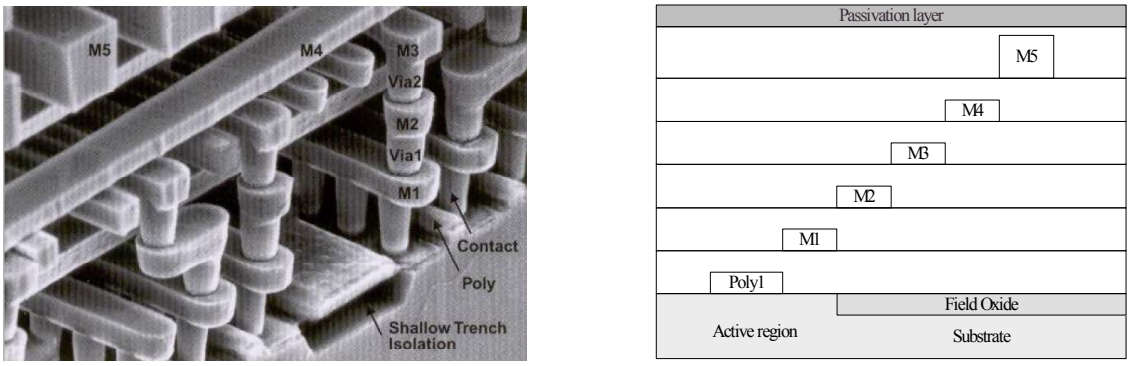
4.1 Introduction of On-chip Inductors

4.1.1 Structure and Layout

The on-chip passive inductors are implemented by a series of transmission lines with the spiral layout. Since they are extensively used in today's RFICs, their fabrication, characteristic, simulation and optimization gain tremendous research interest in the past twenty years [31]-[34].

A 3-D view of a typical model CMOS technology chip obtained by the scanning electron microscope technology is shown in Fig. 4.1 (a) [35], and its cross-section view is illustrated in Fig. 4.1 (b). For the typical CMOS technologies, there are usually 4~5 (or even more) metal layers made by aluminum, copper or metal alloys. Note that the highest metal layer is usually thicker in comparison with other metal layer, which is suitable to fabricate the passive devices, especially the spiral inductors, since it provides higher conductivity. Besides the metal layers, one or two polysilicon layers may be include as the conducting layers. Between two conducting layers, the oxide layers are utilized to isolate them electrically. The substrate is fabricated by doped silicon

material. Finally, a “glass” or “passivation” layer, protecting the surface against damages caused by mechanical handling and dicing, covers the chips.



(a) (b)

Figure 4.1 Typical modern CMOS process (a) 3D view and (b) cross-section

The layout of the spiral inductors can be square, polygon or circular as illustrated in Fig. 4.2 (a) to (c), respectively. Among them, the square spiral inductors are most widely used due to its simplicity. The processing technology limits the usage of the circular inductors. However, the characteristic difference is negligible between the circular inductors and the polygon inductors if the number of the polygon sides is large enough (i.e. ≥16). The planar layouts are usually described by the following parameters: (i) number of turns, n, (ii) width of metal line, w, (iii) space of metal line, s, (iv) external, internal and average diameter, d_{out}, d_{in} and $d_{avg} = 0.5 \cdot (d_{out} + d_{in})$, respectively and (v) number of sides, N, for the polygon inductors. Note that the two ports of these inductors are not symmetrical. Therefore, if the fully differential inductor is required in the circuit, two inductors are used (Fig. 4.2 (d)). Another method is to adopt the fully symmetrical layout as shown in Fig. 4.2 (e).

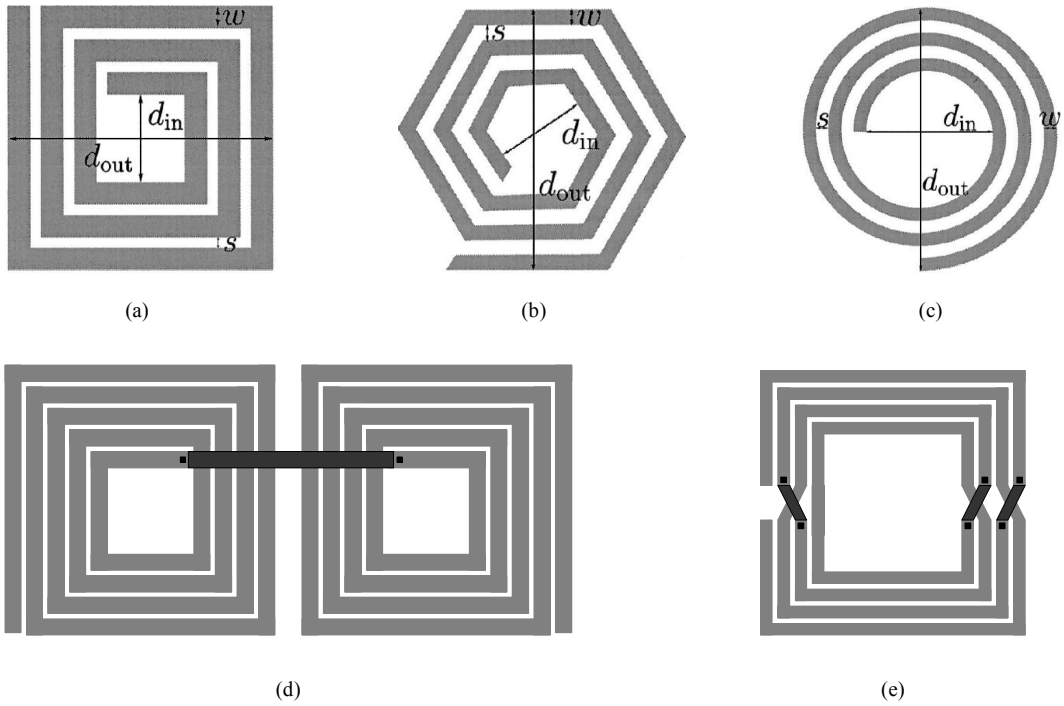


Figure 4.2 Typical layouts of the spiral inductors (a) square spiral inductor (b) hexagon spiral inductor (c) circular spiral inductor (d) symmetrical inductor by using two square spiral inductors and (e) symmetrical square spiral inductor

The inductance of the spiral inductors is primarily determined by the planar layout. On the other hand, the parasitic capacitors and resistors that are critical to the quality of the inductors are determined by both the planar layout and the vertical structure. To implement the spiral inductors on chip, at least two metal layers are required. Hence, the vertical structure for commonly used spiral inductors can be simplified as shown in Fig. 4.3, where the underpass metal line is connected with the external circuitry. Since increasing the distance between the spiral and substrate is propitious to minimize the parasitic capacitance, the spirals are always fabricated by the top metal layer, which is also thicker than others in almost all processes. If the conductivity of the top layer is not large enough to reduce the metal loss, several metal

layers can be stacked together as shown in Fig. 4.4 (a) [34]. However, this solution increases the parasitic capacitance between metal lines and thus degrades the maximum operation frequency of the inductors. On the contrary, if the inductance is not sufficient by using only one metal layer, the metal layers below it can be utilized to fabricate the spirals and several spiral layouts can be connected in series to save the chip area as illustrated in Fig. 4.4 (b) [36]-[37]. Obviously, the parasitic capacitance is also increased in this design.

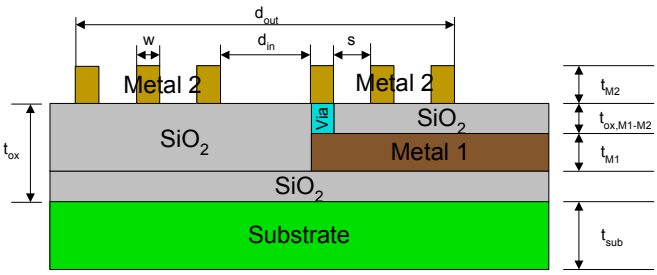


Figure 4.3 Cross-section of the two layer spiral inductors

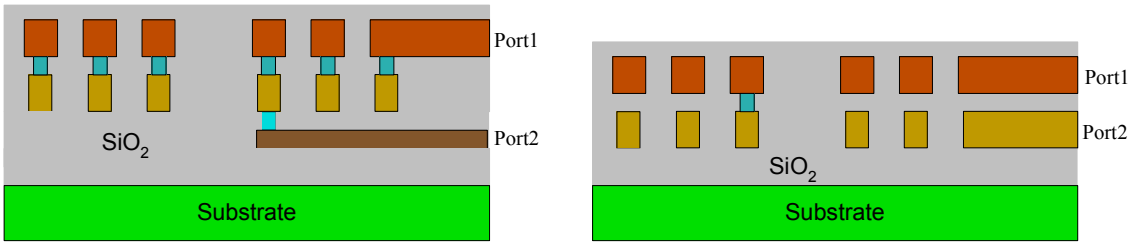


Figure 4.4 Cross-section of two stacked spiral inductors with two metal layers in parallel (a) and in series (b)

4.1.2 Inductance and Resonance Frequency

The inductance is the principle quantity that measures performance of an inductor. While an ideal inductor exhibits a constant inductance value for all

frequencies, a spiral inductor usually exhibits an inductance value resemble to the function of frequency depicted in Fig. 4.5. There are three distinct regions in this plot. Region A comprises the useful band of operation of an integrated inductor. Inside this region, the inductance value remains relatively constant and the passive element can be securely used. Region B is the transition region in which inductance value becomes negative with a zero crossing, which is called the self-resonance frequency of the inductor. Beyond this critical frequency point, the passive element starts performing as a capacitor. In region C, the integrated element exhibits capacitive behavior and the quality-factor value is almost zero, making it practically useless.

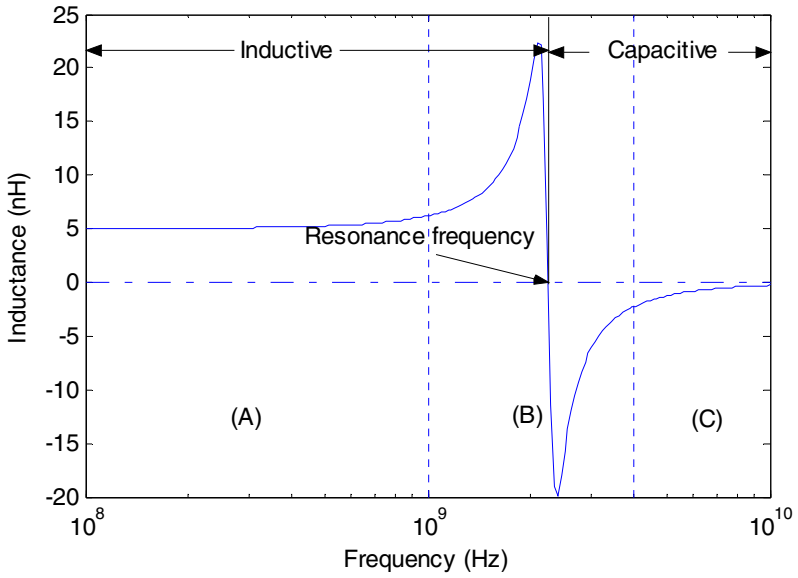


Figure 4.5 Distinct operational regions of a typical spiral inductor

4.2 Spiral Inductor Modeling

Accurately modeling a spiral inductor is still a challenging problem and attracts a lot of research work [38]-[42]. There are two ways to model the spiral inductors. In

the first way, the spiral inductor is divided into several segments and each segment is modeled separately. Then, by taking into account the coupling effects among the segments, the overall inductors' characteristics are obtained. This method is accurate but complicated and hard to embed into a SPICE-like simulator. On the other hand, the spiral inductors can be approximated by the compact models such as the π circuit. These simple models are easy to integrate into the circuit simulator.

4.2.1 Parasitic Effects

The key to accurate modeling is the ability to identify the relevant parasitics and their effects. Since an inductor is intended for storing magnetic energy only, the inevitable resistance and capacitance in a real inductor are considered as parasitics and thus resulting in energy loss. For the on-chip inductor, the parasitic effects include:

(i) Energy loss inside the nonzero-resistivity metal lines, which is from current flowing through the spiral inductor itself and includes both ohmic and eddy-current loss. For a single metal line, the DC current is uniformly distributed inside the conductor and the ohmic loss is independent to frequency. However, as the frequency goes up, the skin effect limits the depth of the current penetrating into the metal, making the depth comparable to or even smaller than the cross-section dimensions of metal lines. Therefore, the ohmic loss of metal line is a function of frequency. In addition to the skin effect, the magnetic field generated by neighboring lines further changes the current distribution and results in a higher current density at the edges of the metal lines (the eddy-current loss). This effect is depicted in Fig. 4.6 and is called as proximity

effect. It has a greater impact than the skin effect on the increase of the resistance and degradation of Q in today's spiral inductor design.

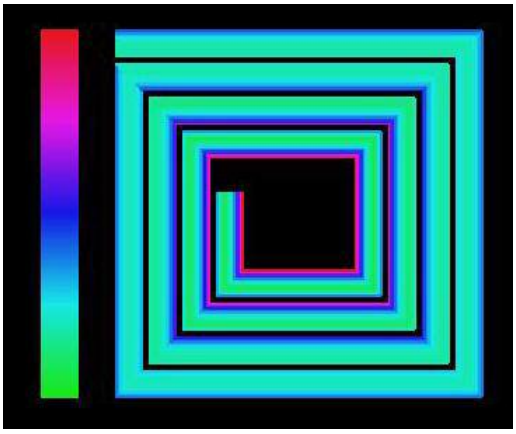


Figure 4.6 Current distribution in a spiral inductor caused by the proximity effect [43]

(ii) Ohmic loss in the conductive substrate, which is due to the displacement current conducted through the metal-to-substrate capacitance.

(iii) Loss due to the eddy current in the underlying substrate, induced by the penetration of the magnetic field into the conductive silicon. For typical CMOS technology, the resistivity of the substrate is small in order to prevent the latch-up. Hence, this loss may be significant if the substrate resistivity is small (<10Ω·cm).

4.2.2 Segmented Models

In a segmented model, the spiral inductor is divided into a set of sections. Such an approach was originated by Greenhouse [44] and then refined by others [45]. For example, each side of a square inductor can be modeled by an equivalent π circuit as depicted in Fig. 4.7 [46]. The analytical expressions of the elements in this equivalent circuit are summarized in table 4.1. For instance, the self-inductance of a given metal

line can be computed by (1), where l, w and h are the length, width and thickness. The metal loss of this line is calculated by (2), where R_{sh} is the sheet resistance. The capacitance between the metal line and the substrate is obtained by (3). The mutual inductance contributes the primary inductance of the spiral inductance. Equations (4) to (10) describe the method to calculate the mutual inductance between two metal lines with arbitrary position. Equations (11), (12) and (13) are the expressions to calculate the parasitic resistance of capacitance formed by the substrate loss.

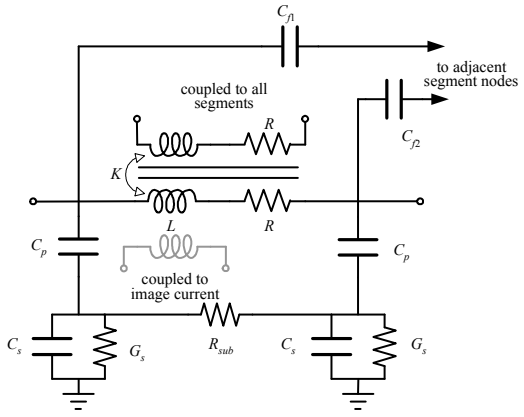


Figure 4.7 Equivalent two-port circuit for one side of the square spiral inductor

The circular inductors can be modeled by the similar way. In this case, a circular inductor is considered as several metal line rings connected in series as depicted in Fig. 4.8 (a) [34]. Each ring can be viewed as a two-port network with a specific impedance matrix. The overall 2×2 impedance matrix of the spiral inductor is found by connecting the outputs 1, …, $N-1$ to the inputs 2, …, N, respectively. The coupling effect between rings can be expressed by a matrix, Z, which can be solved by the field equations in the disconnected system of rings.

Table 4.1 Equations of the elements in Fig. 4.7

	Equation
$L = 2l\{ln[2l/(w+t)]+0.50049+(w+t)/3l\}$	(1)
$R = R_{sh}l/w$	(2)
$C_p = \varepsilon_0\varepsilon_r w/h$	(3)
$M = 2lU$	(4)
$K_m = M_{1,2}/\sqrt{L_1L_2}$	(5)
$2M = (M_{l+m\pm\delta}+M_{\delta})-(M_{l\pm\delta}+M_{m\pm\delta})$	(6)
$2M = (M_{m+p}+M_{m+q})-(M_p+M_q)$	(7)
$M_{lm} = 2\cos\phi\left[l\tanh^{-1}\left(\frac{m}{l+y}\right)+m\tanh^{-1}\left(\frac{l}{m+y}\right)\right]$	(8)
$M_{lm} = 2\cos\phi\left[(M_{\mu+l,\nu+m}+M_{\mu\nu})-(M_{\mu+l,\nu}+M_{\nu+m,\mu})-\Omega d_z/\sin\phi\right]$	(9)
$\Omega = \frac{\pi}{2}+\tan^{-1}\left[\frac{d_z^2\cos\phi+lm\sin^2\phi}{d_z R_l\sin\phi}\right]-\tan^{-1}\left(\frac{d_z\cos\phi}{l\sin\phi}\right)-\tan^{-1}\left(\frac{d_z\cos\phi}{m\sin\phi}\right)$	(10)
$R_{sub} = \rho_{Si}l/(wh_{Si})$	(11)
$C_s = \frac{(w+\Delta w')}{h}\varepsilon_0\varepsilon_{r,Si}$, $\Delta w' = \left(1+\frac{1}{\varepsilon_{r,Si}}\right)\frac{\Delta w}{2}$, $\Delta w = \frac{t}{\pi}ln\left[4e\Big/\sqrt{\left(\frac{t}{h}\right)^2+\left(\frac{1/\pi}{w/t+1.1}\right)^2}\right]$	(12)
$G_s = \hat{\sigma}\frac{w}{\hat{h}}$, $\hat{\sigma} = \sigma\left(\frac{1}{2}+\frac{1}{2\sqrt{1+10h/w}}\right)$, $\hat{h} = \frac{w}{2\pi}log\left(\frac{8h}{w}+\frac{4w}{h}\right)$	(13)

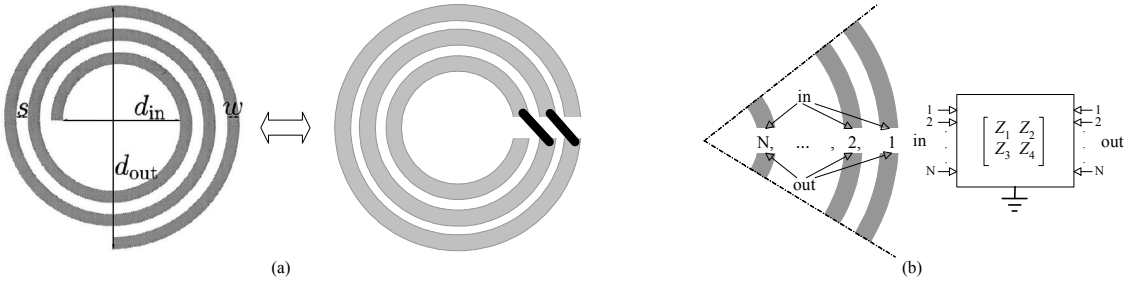


Figure 4.8 Concentric-ring model of a circular spiral inductor (a) Approximate a spiral by a set of rings and (b) Concentric-ring model

Although the segmented approach leads to more accurate results, its complexity limits its application in the circuit simulators. In fact, the compact models discussed in the following section are more widely used.

4.2.3 Compact Models

4.2.3.1 Nine Elements Lumped π Model

If the total metal line length is smaller than the operational waveform, it is convenient to model the whole inductor by a lumped, compact model. The basic compact model of the spiral inductors consists of nine elements as illustrated in Fig. 4.9 [41]. The inductance and resistance of the spiral and underpass are represented by the series inductance, L_s, and the series resistance, R_s, respectively. The overlap between the spiral and the underpass allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is modeled by the series capacitance, C_s. The oxide capacitance between the spiral and the silicon substrate is modeled by C_{ox}. The capacitance and resistance of the silicon substrate are modeled by C_{sub} and R_{sub}. The characteristics of the elements are investigated in the rest of the section.

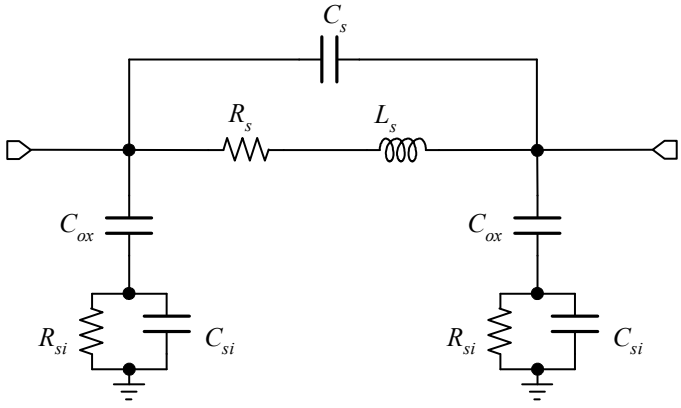


Figure 4.9 Nine elements lumped π model

(i). *Series Inductance L_s*

As the primary parameter, the inductance of the spiral inductor received extensively study. Jenei proposed a physics-based, close-formed expression [47]. According to his theory, the inductance of a square inductor can be written as

$$L = \frac{\mu_0 l}{2\pi}\left\{\ln\frac{l}{n(w+t)} - 0.2 - 0.47n + n(n-1)\cdot\left[\ln\left(\sqrt{1+\left(\frac{l}{4nd^+}\right)^2}+\frac{l}{4nd^+}\right)\right.\right.$$

$$\left.\left. - \sqrt{1+\left(\frac{l}{4nd^+}\right)^2}+\frac{l}{4nd^+}\right]\right\} \tag{4.1}$$

where w, t are the line width and thickness respectively, n is the number of turns, d^+ and l are the average distance and total length of metal lines that are given by

$$d^+ = (w+s)\frac{(3n-2N_i-1)(N_i+1)}{3(2n-N_i-1)} \tag{4.2}$$

$$l = (4n+1)d_{in}+(4N_i+1)N_i(w+s) \tag{4.3}$$

respectively, where s is the space of metal lines, N_i is the integer part of n and d_{in} is the inner diameter of the spiral inductor. However, the validity of these equations is still in question.

Nowadays, the most widely used method for inductance calculation is still based on segmentation, in which the self-inductance of a segment is first computed and then the overall inductance is calculated by summing both the self-inductance and the mutual inductance between all segments. This approach is followed in many publications [40] [48] [49]. Generally speaking, the inductance is difficult to write as an analytical, close-formed expression.

On the other hand, the empirical equations based on curve-fitting techniques are usually used in practical inductor designs due to their simplicity. For example, Wheeler presented an empirical expression as follows [50]

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{4.4}$$

where ρ is the fill ratio defined as $(d_{out} - d_{in})/(d_{out} + d_{in})$, n is the number of turns, K_1 and K_2 are two empirical constants. For different inductor shapes, the values of K_1 and K_2 are listed in Table 4.2

Mohan also proposed an empirical, monomial expression for the spiral inductance [51], which is given by

$$L_s = \gamma d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}, \tag{4.5}$$

where γ, α_1, α_2, α_3, α_4 and α_5 are constants obtained by fitting the simulation and measurement data (see Table 4.2). By comparing the inductance obtained from ADS Momentum simulation and this expression, it was found the typical error is only a few percent over a very broad design space (see Table 4.3).

Table 4.2 Coefficients for Wheeler and Mohan expressions

	Wheeler		Mohan					
Layout	K_1	K_2	γ	α_1	α_2	α_3	α_4	α_5
Square	2.34	2.75	1.62×10^{-3}	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	2.33	3.82	1.28×10^{-3}	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	2.25	3.55	1.33×10^{-3}	-1.21	-0.163	2.43	1.75	-0.049

Variations in processing may cause more errors in the inductances. Hence, these curve-fitting models are accurate enough for the practical spiral inductor design. The

monomial expression is especially useful in the inductor optimization problem discussed in Chapter 7.

(ii). *Series Resistance* R_s

By taking into account the skin effect, the series resistance R_s can be expressed as a frequency dependent function as follows

$$R_s = \frac{l}{\sigma w \delta (1 - e^{-t/\delta})} \tag{4.6}$$

where σ is the metal conductivity, t is the metal line thickness, l is the total length of metal lines and δ is the skin depth given by

$$\delta = \sqrt{\frac{2}{\mu_0 \omega \sigma}} . \tag{4.7}$$

(iii). *Series Capacitance* C_s

The capacitance, C_s, models the parasitic capacitive coupling between input and output ports of the inductors. This capacitance allows the signal to flow directly from the input to output without passing through the spiral inductor. Based on the structure of the inductors, both the crosstalk between adjacent turns and the overlap between the spiral and underpass contribute to C_s. However, since the adjacent turns are almost equi-potential, the effect of the crosstalk capacitance is negligible. The effect of overlap capacitance is dominant in C_s. Therefore, for most practical inductors, it is sufficient to model C_s as the sum of all overlap capacitances, which is given by

$$C_s = nw^2 \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{4.8}$$

where n is number of overlaps, w is the spiral line width and $t_{oxM1\text{-}M2}$ is the oxide thickness between the spiral and the underpass (see Fig 4.3).

(iv). *Oxide Capacitance C_{ox}*

The capacitance, C_{ox}, models the capacitance between the spiral and the substrate, which is the most important parasitic capacitance in the spiral inductors. Since the lateral dimension of the spiral inductor is much larger than the thickness of the oxide layer, C_{ox} can be approximated by a parallel plate capacitor. Thus the capacitance is evenly separated by two capacitors in the π model, which is given by

$$C_{ox} = 0.5 \cdot lw \cdot \frac{\varepsilon_{ox}}{t_{ox}}. \tag{4.9}$$

There is a more accurate way to estimate C_{ox} obtained from microstrip theory [52]. According to this theory, C_{ox} can be calculated by

$$C_{ox} = 0.5 \cdot l \frac{\varepsilon_0 \varepsilon_{eff}}{F(t_{ox}, w)} \tag{4.10}$$

where the effective permittivity ε_{eff} is given by

$$\varepsilon' = \frac{\varepsilon_{ox} + 1}{2} + \frac{\varepsilon_{ox} - 1}{2(1 + 10t_{ox} / w)^{1/2}} \tag{4.11}$$

and function $F(t_{ox},w)$ is given by

$$F(t_{ox}, w) = \frac{1}{w / t_{ox} + 2.42 - 0.44 t_{ox} / w + (1 - t_{ox} / w)^6}, \quad t_{ox} < w. \tag{4.12}$$

The second method is used to calculate C_{ox} in this work.

(v). *Substrate Resistance R_{si}*

The physical origin of R_{si} is the loss caused by the silicon conductivity which is predominately determined by the majority carrier concentration. It can be expressed as

$$R_{si} = \frac{2}{G_{sub} lw} \tag{4.13}$$

where G_{sub} it the conductance per unit area of the silicon substrate. This parameter can be obtained by measurement. On the other hand, R_{si} also can be computed by the following expression [53]

$$R_{si} = \frac{2t_{si}}{\sigma_{si} lw K_C} \tag{4.14}$$

where K_C is a constant obtained by curve-fitting, which is

$$K_C = \begin{cases} 5.1675 + 0.6342/\xi, & 0.01 \le \xi < 0.15 \\ 1.2538 + 1.1783/\xi, & 0.15 \le \xi < 1.5 \\ 1.1658 + 1.0604/\xi, & 1.5 \le \xi \le 10 \end{cases} \tag{4.15}$$

the value, ξ, is determined by the vertical structure of the inductor given by

$$\xi = \sqrt{A}/t_{si} = \sqrt{lw}/t_{si} \tag{4.16}$$

where t_{si} is the thickness of the silicon substrate. This method is adopted in this work.

(vi). *Substrate Resistance* C_{si}

The parameter, C_{si}, models the high-frequency capacitive effects occurring in the semiconductor. Similar to the oxide capacitance C_{ox}, C_{si} can be written as

$$C_{si} = 0.5 \cdot lw \cdot C_{sub} \tag{4.17}$$

where C_{sub} is the capacitance per unit area of the silicon substrate which can be obtained by measurement. The value for C_{si} can also be computed from the structure of the spiral inductors. According to [54], C_{si} can be calculated by

$$C_{si} = 0.5 \cdot \varepsilon_o \varepsilon_{eff} \cdot l / F(w, t_{si}) \tag{4.18}$$

where ε_{eff} is the effective permittivity given by

$$\varepsilon_{eff}(f) = \varepsilon - \frac{\varepsilon - \varepsilon'}{1 + (f / f_c)^2} \tag{4.19}$$

ε' and f_c (the critical frequency) in (4.19) is given by

$$\varepsilon' = \frac{\varepsilon + 1}{2} + \frac{\varepsilon - 1}{2(1 + 10 t_{si} / w)^{1/2}} . \tag{4.20}$$

$$f_c = \frac{c^2 \varepsilon_0 Z_0}{2 t_{si}} \sqrt{\frac{\varepsilon}{\varepsilon'}} \tag{4.21}$$

respectively, with

$$Z_0 = \frac{120 \pi F(w, t_{si})}{\sqrt{\varepsilon'}} \tag{4.22}$$

and the speed of light c. $F(w,t_{si})$ in (4.18) and (4.22) is a function determined by the vertical structure of the spiral inductors

$$F(w, t_{si}) = \frac{1}{2\pi} \ln\left[\frac{8 t_{si}}{w} + \frac{w}{4 t_{si}}\right], \quad t_{si} > w . \tag{4.23}$$

The equations from (4.18) to (4.23) are used to calculated C_{si} in this work.

Although all components have clear physical meaning in this nine-element model, and their values can be obtained from analytical expressions determined by the lateral layout and vertical structure of the spiral inductors, this compact model neglects the proximate effect and the eddy current, resulting in overly optimistic performance predictions.

4.2.3.2 Improved π Models

Because of the limitation of the simple π model, many improved π circuits are proposed. Figure 4.10 (a) is one of the improved π model in which the eddy current in the substrate is taken into account by adding several mutual inductors [55].

A more complicated double-π model proposed by Cao is illustrated in Fig 4.10 (b) [56]. In this model, the skin effect is modeled by one additional *RL* branch paralleled to the DC resistance R_0. The *RL* branch captures the effect of different current densities in metal lines. The single-π model is extended to the double-π topology to account for the capacitive coupling between metal lines, which is modeled by C_c and is neglected in the simple π model. The proximity effect between metal lines is modeled by the mutual inductance as depicted. Finally, the eddy current loss in the substrate is captured by the resistors R_{sc}. By these arrangements, all major parasitic effects in typical spiral inductors are taken into account.

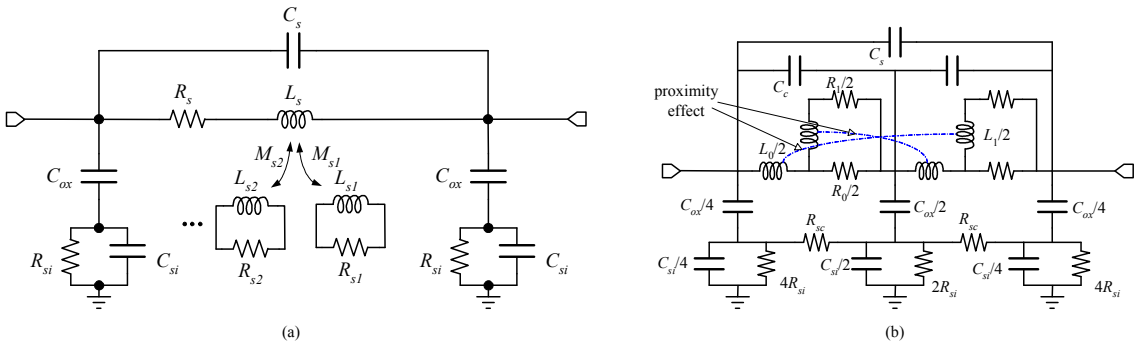


Figure 4.10 Two improved π models (a) taking the substrate eddy current into account and (b) taking both the substrate eddy current and proximity effect into account

In *LC* VCO design, the tuning frequency is relatively small. The transition region and the capacitive region as illustrated in Fig 4.5 are useless in this case. Therefore, a simple nine elements π model is sufficient.

4.3 Spiral Inductor Simulation and π Model Parameters Extraction

4.3.1 Spiral Inductor Simulation

There are many software tools that support the simulation of the on-chip spiral inductors. They can be categorized to two types. The first is an electromagnetic field solver such as Maxwell. These tools are usually called full-wave 3D solvers. The second is a partial-element-equivalent-circuit-based solver such as ASITIC [43] and ADS Momentum [57]. These simulators are called as 2.5D solvers sometimes. The former solvers are more accurate but time consuming while the latter are faster. The ADS Momentum program was used in this research to characterize the spiral inductors.

A typical square spiral inductor depicted in Fig. 4.11 is simulated by ADS Momentum. The spiral is a three-turn, 200μm×200μm square inductor. The metal line width is 18μm with a conductor spacing of 2μm. A 108μm underpass metal line is used to connect the center to the external circuit. A 13μm×13μm via connects the spiral to the underpass. The conductivity of the metal is 2.67×10^{7}S/m.

For simplicity, the top "glass" layer is neglected and the metal2 layer is exposed to open air directly. The conductivity of the substrate is 20 S/m. The bottom of the substrate is grounded. In simulation, the Port1 and Port2 (connect with underpass and spiral respectively) are terminated by two 50 Ω loads.

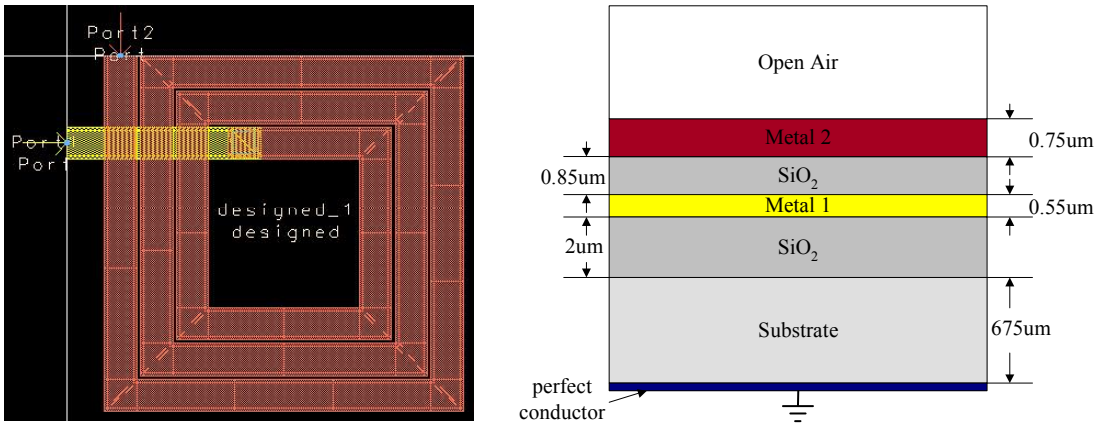


Figure 4.11 Lateral layout (left) and vertical structure (right) of the spiral inductor

The inductance and the quality factor as a function of the frequency of this spiral inductor are plotted in the Fig. 4.12 (left and right respectively), where the inductance is defined as

$$L_s = \frac{\mathrm{Im}(-1/Y_{12})}{2\pi f} \tag{4.24}$$

and the quality factor is defined by (3.3), i.e.

$$Q_{11} = \frac{\mathrm{Im}(1/Y_{11})}{\mathrm{Re}(1/Y_{11})} \tag{4.25}$$

where, Y_{11} and Y_{12} are Y-parameters of the spiral inductor. The simulation shows that the inductance at low frequency is 1.74nH. As expected, the inductance at high frequency becomes negative, representing a capacitive region as depicted in Fig. 4.5. For this specific inductor, the self-resonate frequency is close to 20GHz. Also the maximum Q factor in the inductive region is limited to 4 because of the losses occurring in the metal lines and substrate.

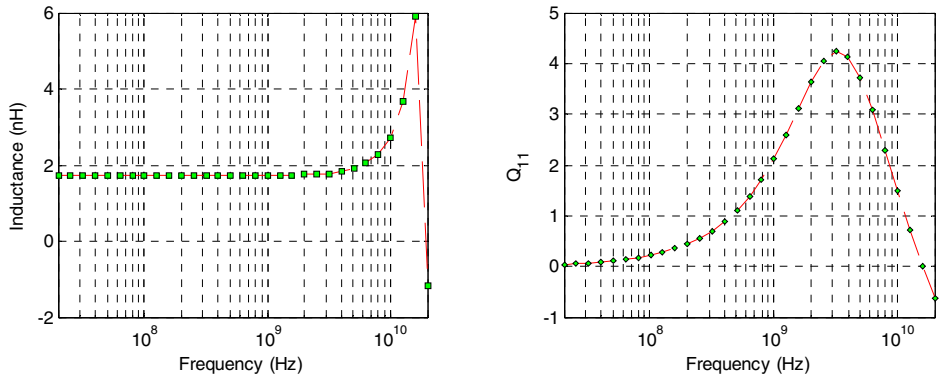


Figure 4.12 Inductance (left) and quality factor (right) of the simulated inductor

4.3.2 Model Parameters Extraction

The parameters in the simple π model can be extracted from the simulation or measurement results to improve the modeling accuracy. In the nine elements π model, the conductance of two shunt branches, $Y_{shunt1}(\omega)$ and $Y_{shunt2}(\omega)$, and the impedance of the series branch, $Z_{series}(\omega)$, satisfy the following expressions

$$Y_{shunt1}(\omega) = Y_{11}(\omega) + Y_{12}(\omega) \tag{4.26}$$

$$Y_{shunt2}(\omega) = Y_{22}(\omega) + Y_{12}(\omega) \tag{4.27}$$

$$Z_{series}(\omega) = -\frac{1}{Y_{12}(\omega)}. \tag{4.28}$$

For the series branch in the π model, $Z_{series}(\omega)$ is given by

$$Z_{series}(\omega) = -\frac{1}{Y_{12}(\omega)} = [R_s + j\omega L_s] // \frac{1}{j\omega C_s}. \tag{4.29}$$

Since the low frequency characteristics is determined only by R_s and L_s while the high frequency characteristics is dominated by C_s, R_s, L_s and C_s can be extracted using the following expressions

$$R_s = \mathrm{Re}\left[-\frac{1}{Y_{12}(\omega)}\right]\Bigg|_{low\quad frequency} \tag{4.30}$$

$$L_s = \mathrm{Im}\left[-\frac{1}{Y_{12}(\omega)}\right]\Big/\omega\Bigg|_{low\quad frequency} \tag{4.31}$$

$$C_s = \mathrm{Im}\left[-Y_{12}(\omega)\right]/\omega\Big|_{high\quad frequency}. \tag{4.32}$$

For the shunt branch in the π model, the conductance, $Y_{shunt1}(\omega)$, is given by

$$\frac{1}{Y_{shunt1}(\omega)} = \frac{1}{j\omega C_{ox1}} + \frac{1}{G_{si1} + j\omega C_{si1}}. \tag{4.33}$$

If ω is small enough ($G_{si1} >> \omega C_{si1}$), the image part of $1/Y_{shunt1}(\omega)$ is primarily determined by the first term at the right side of (4.33). Hence, C_{ox1} can be obtained by

$$C_{ox1} = \mathrm{Im}\left[Y_{shunt1}(\omega)\right]/\omega\Big|_{low\quad frequency}. \tag{4.34}$$

The rest two parameters, C_{si1} and R_{si1}, cannot be directly extracted from low frequency or high frequency data. However, the Cauchy's method reported in [58] can be applied to (4.33) to obtain the best-fitted C_{si1} and R_{si1}. C_{ox2} and C_{si2} and R_{si2} in another shunt branch can be extracted by the same method.

4.3.3 Compare Model with Simulation Results

To simulate the spiral inductors, a mesh will be generated according to the smallest wavelength in ADS Momentum. If the wavelength is small (high frequency), the density of the mesh is high, resulting in a very long simulation time. To avoid this problem, C_s is directly estimated by (4.8), which is 39.5fF in this case. Note that C_s has little effect at low frequency. This inductance value will be used in both the extracted model and the calculated model.

The parameters in the model are first calculated by the analytical methods introduced previously. Mohan's empirical model (4.5) is applied to estimate L_s. The other parameters, R_s, C_s, C_{ox}, R_{si} and C_{si}, are computed by (4.6), (4.8), (4.10), (4.14) and (4.18), respectively. Note that the underpass line is neglected in the calculation. The component values are listed in Table 4.3. The extraction procedure is also applied to the simulation data. The corresponding values are listed in the same table. Comparing the inductance value obtained by the two methods, the error is found to be very small (1.6%). This result also validates Mohan's empirical model.

Table 4.3 Components' value obtained from analytical calculation and extraction

Component	L_s (nH)	R_s (Ω)	C_s (fF)	C_{ox1} (fF)	C_{si1} (fF)	R_{si1} (Ω)	C_{ox2} (fF)	C_{si2} (fF)	R_{si2} (Ω)
Analytical	1.764	4.778	39.47	226.6	55.55	381.2	226.6	55.55	381.2
Extraction	1.736	4.912	39.47	220.1	71.03	261.4	209.3	73.18	291.5

In Fig 4.13, four functions, L_{11}, R_{11}, L_{12} and R_{12}, are compared to evaluate the consistency between the model (analytical and extracted) and the simulation results. These four functions are defined by:

$$\frac{1}{Y_{11}(\omega)} = R_{11}(\omega) + j\omega L_{11}(\omega) \tag{4.35}$$

$$\frac{1}{Y_{12}(\omega)} = R_{12}(\omega) + j\omega L_{12}(\omega). \tag{4.36}$$

In Fig 4.13, the functions obtained from the simulation are illustrated as discontinuous markers while the functions achieved from the extraction parameters and analytical expressions are plotted by the solid and dotted lines, respectively. At high

frequency, both the analytical model and the extracted model become inaccurate since the eddy current loss and the proximity effect are not included in this model. In addition, the dimension of the inductor is comparable to the wavelength (i.e. the total length is about 1.8mm while the wavelength is 1.5cm for 20GHz), making the lump model lose its accuracy. However, it can be concluded that the data obtained from two models matches the simulation results very well in the inductive region (less than 8GHz). Therefore, the spiral inductors in the *LC* oscillator can be represented by this simple π model accurately.

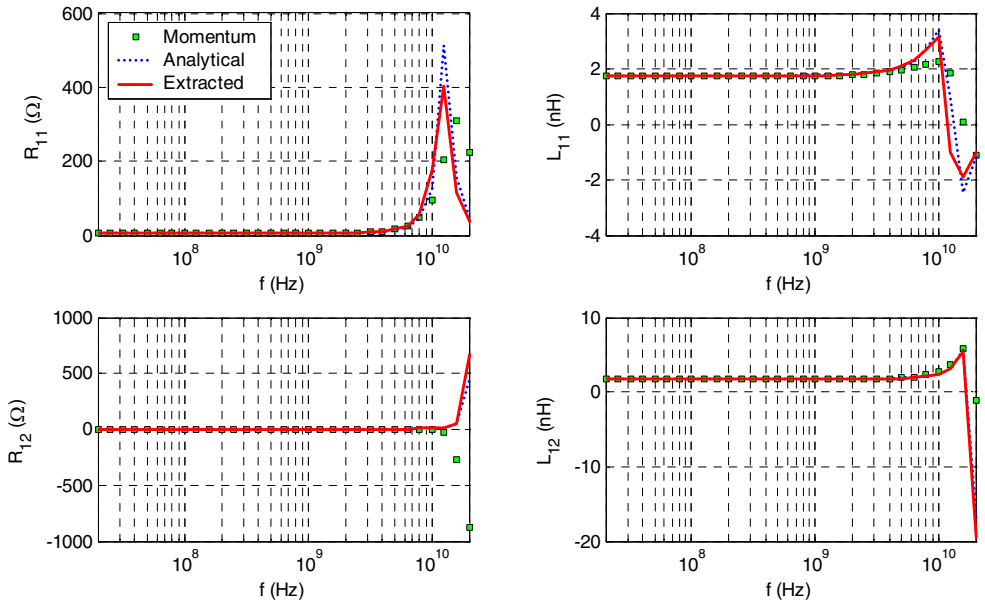


Figure 4.13 Comparison the analytical and extracted model with the simulation results

The *Q* factors defined by (4.25) are plotted in Fig 4.14. Very good consistency is achieved between both cases in the inductive region. However, the *Q* obtained from extracted model, the analytical model is more optimistic by 32% maximum.

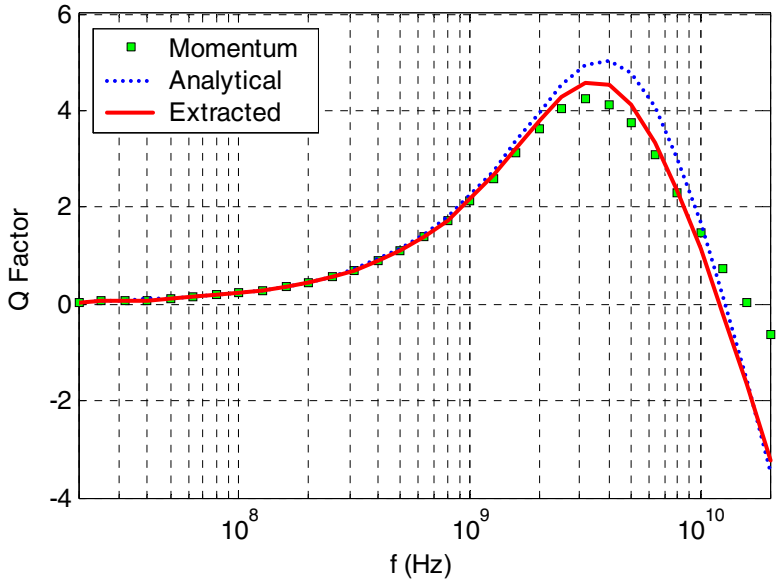


Figure 4.14 Q factors obtained from simulation data, extracted and analytical model

4.4 Techniques to Improve Q Factor

The Q factor is the critical parameter to the on-chip spiral inductors. Since the Q factor of the varactors is usually much larger than the spiral inductors' Q in typical processes, the overall Q factor of an LC tank circuit is primarily determined by the spiral inductor. Therefore, improving its Q factor can effectively reduce the phase noise in oscillators.

The techniques to improve the Q factor can be divided into two categories: (1) process dependent methods and (2) process independent methods. In the first approach, the standard processes are modified to achieve higher Q factors. For example, to suppress the eddy current in the substrate, the conductivity of the substrate is reduced in [59] to increase the Q factor. Similarly, a thick isolation layer formed by the porous

silicon is inserted between the spiral inductor and the substrate in [30], decreasing the parasitic capacitance and reducing the loss caused by the substrate. Recently, by using Micro-Electro-Mechanical (MEM) technology, a spiral inductor can be suspended to achieve very competitive Q factors [60]. For circuit designers, however, these methods are impractical because they need additional processing steps supported by the foundries.

The patterned ground shields (PGS) technique is now widely used to improve the performance of the spiral inductor without extra processing steps [24]. In this technique, a patterned ground layer is inserted between the spiral inductor and the substrate. The pattern of this layer is radialized as illustrated in Fig 4.15 (a). The ground strips are made by polysilicon layer or metal layer while the slots are used to isolate the adjacent strips. Obviously, the slots act as an open circuit to cut off the path of the induced eddy current since they are orthogonal to the metal lines of the spiral. Hence, the eddy current loss in the substrate is suppressed and a 33% Q improvement is achieved in [24]. Besides this function, the shield also prevents both the noise coupling from the substrate and the crosstalk between the inductor and the adjacent devices.

To suppress the proximity effect, a single metal line can be separated to several thinner metal lines in parallel as shown in Fig 4.15 (b). As illustrated in Fig. 4.6, the proximity effect increases the current density near the edges of metal lines, boosting the resistivity of the metal lines and thus decreasing the Q factor. However, by using the multi-paths arrangement, the current is more evenly distributed in metal lines and Q value is preserved.

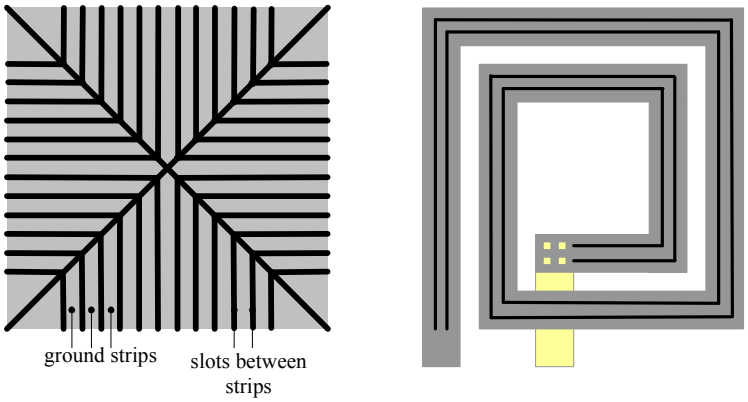


Figure 4.15 Two methods to improve Q factor (a) patterned ground shield and (b) multi-path metal lines

4.5 Summary

The design, modeling and simulation of the spiral inductors were investigated in this chapter in detail. Their typical lateral layout and vertical structure of integrated inductors were first introduced. Then, the parasitic effects were summarized. Based on these parasitic effects, two modeling approaches – segmented model and compact model – were introduced. For the widely used compact π model, the analytical expressions for each component were given. A spiral inductor with typical layout and structure was simulated by ADS Momentum. Its π model was obtained by both the analytical expressions and the extraction procedure. Very good consistency was found between the models and the simulation results in the inductive region, indicating the effectiveness of the π model. Finally, several techniques to improve the Q factor of the spiral inductors were discussed.

CHAPTER 5

PHASE NOISE MODELS

Phase noise performance is a critical specification for VCOs. The phase noise models describe the phase noise generation mechanism in oscillators. With the help of these models, the phase noise can be estimated before the oscillators are fabricated. The models also provide the design trade-offs and insights, which are very valuable for circuit designers.

Several phase noise models, including the Leeson's empirical model, classical linear time-invariant model, Hajimiri's linear time-variant model, Samori's non-linear time-invariant model, and Kaertner and Demir's numerical model, will be presented and investigated in this chapter in detail.

5.1 Empirical Phase Noise Model – Leeson's Model

Figure 5.1 approximately illustrates a typical measurement result of the phase noise generated by an oscillator. At a small offset frequency, the phase noise decreases with the increase of the cube of the offset frequency (i.e. the slope is –30dB/dec). The slope changes to –20dB/dec above a corner-frequency, $\Delta\omega_{1/f^3}$. The phase noise plot finally becomes flat at a large offset frequency. This noise floor is determined by the active devices noise floor or the instrumentation used in measurement.

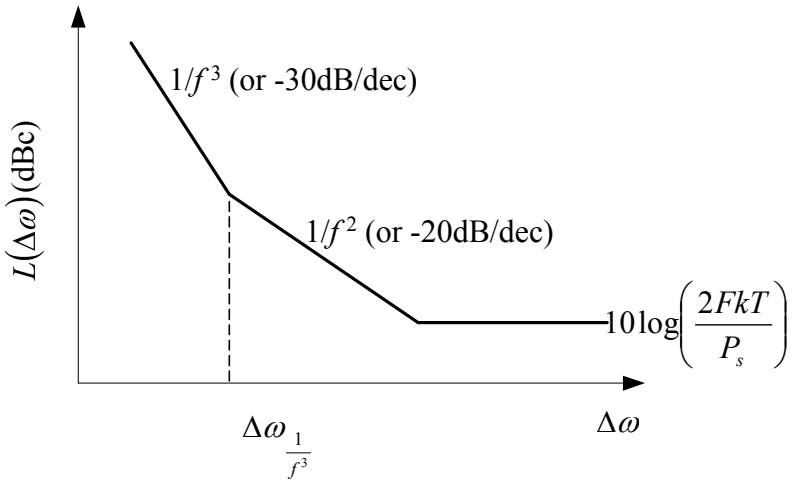


Figure 5.1 Typical plot of the phase noise of an oscillator versus offset from carrier

D. B. Leeson [61] proposed an empirical phase noise model to describe the phase noise plot depicted in Fig. 5.1. According to this model, the phase noise generated by an oscillator can be expressed as:

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{2FkT}{P_S} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{5.1}$$

where ω_0 is the oscillation frequency, $\Delta\omega$ is the frequency offset at which the phase noise is defined, T is the absolute temperature, k is the Boltzmann's constant, P_s is carrier power, Q_L is the loaded Q factor of the tank. The parameter F (often called the excess noise number) is an empirical parameter which can only be found from fitting the measurement data. Also, this model asserts that the corner frequency between the $1/f^3$ and $1/f^2$ region is precisely equal to the $1/f$ corner frequency of the device noise. However, measurements frequently show this equality does not exist. Therefore, this parameter is usually a fitting parameter too.

In summary, the Leeson's model cannot be used to predict the phase noise generated by an oscillator because it has two empirical parameters which have to be obtained from measurement. Also, it does not describe the mechanism of the phase noise generation and thus provides little design insight. More accurate phase models are necessary to investigate the phase noise. In this chapter, four other phase noise models will be introduced and the advantages and disadvantages of each will be summarized.

5.2 Linear Tine-Invariant (LTI) Model

An oscillator can usually be approximately modeled as a linear system. Two linear models, one based on the negative feedback system and the other one based on the one-port negative resistance network, have been introduced in Chapter 2. It is convenient to model an *LC* cross-coupled oscillator as a one-port negative resistance model as shown in Fig. 5.2. In this model, the transconductance of the active circuit, G_m, must compensate for the loss caused by parasitic resistance R_p in the tank. If the loop is broken at the cross point and the circuit is considered as a linear feedback system, it is easy to show that the open-loop transfer function for this basic oscillator is:

$$T_{loop}(s) = G_m \frac{sL}{1 + sL/R_p + s^2 LC}. \tag{5.2}$$

The imaginary part of the loop transfer function is equal to

$$\mathrm{Im}\left[T_{loop}(\omega)\right] = G_m \frac{\omega L\left(1-\omega^2 LC\right)}{(1-\omega^2 LC)^2 + \omega^2\left(L/R_p\right)^2}. \tag{5.3}$$

If the imaginary part of the loop transfer function is zero and the open-loop gain is greater than one, the system will oscillate at the frequency given by

$$\omega_0 = \frac{1}{\sqrt{LC}}, \tag{5.4}$$

and G_m will compensate the energy loss in the tank, which means

$$G_m \le 1/R_p. \tag{5.5}$$

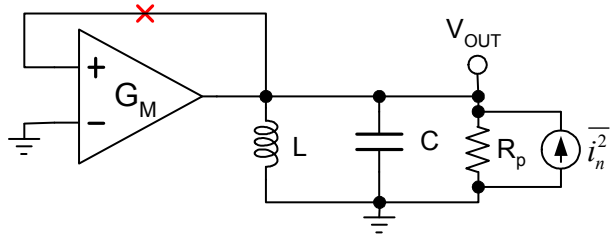


Figure 5.2 One-port negative resistance oscillator with noise current in the tank

5.2.1 Tank Noise

The parasitic of the tank is simply modeled as a parallel resistor in Fig. 5.2. The thermal noise it generates is modeled as a noise current, $\overline{i_n^2}$, paralleled with the tank as shown in the same figure. The thermal noise introduces the phase noise at the output of the oscillator. In the LTI model, oscillators are viewed as LTI systems. To investigate phase noise of the basic oscillator in Fig. 5.2, the transfer function from the noise current to the output voltage in closed-loop operation is derived, which is

$$T^2_{noise,Rp}(s) = \frac{\overline{V_n^2}}{\overline{i_n^2}} = \left[\frac{sL}{1 - sL\left(G_m - 1/R_p\right) + s^2 LC}\right]^2. \tag{5.6}$$

Assume G_m=1/R_p, it can be shown that the transfer function at small offset frequency $\Delta\omega$ approximately equals [62]

$$T^2_{noise,Rp}(\Delta\omega) = \left[\frac{1}{2j}\cdot\sqrt{\frac{L}{C}}\cdot\frac{\omega_0}{\Delta\omega}\right]^2. \tag{5.7}$$

Note that $T_{noise,Rp}$ is the equivalent impedance of the tank at the frequency $\omega_0 \pm \Delta\omega$. Accordingly, the one-side spectral density of the output noise voltage is

$$\overline{V_{on,gp}^2(\Delta\omega)} = 4kTg_p \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2 \cdot \omega_0^2 L^2 \tag{5.8}$$

where g_p is the conductance, i.e. $g_p=1/R_p$. The noise voltage described here actually includes both the amplitude noise (AM noise) and the phase noise (PM noise). If the oscillator employs an automatic gain control (AGC) circuit, the AM noise will be removed for frequency offset less than the AGC bandwidth. In addition, the nonlinearity of the oscillators determines the oscillation amplitude and it can be viewed as an internal AGC mechanism in oscillators. Therefore, even when there exists AM noise, it will die away with time and thus has little effect on output phase noise. According to the energy equi-partition theorem, neglecting the AM noise results in a factor 0.5 multiplied to (5.8). So, the spectral density of the noise voltage is

$$\overline{V_{on,gp}^2(\Delta\omega)} = 2kTg_p \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2 \cdot \omega_0^2 L^2 . \tag{5.9}$$

Note that in practical circuits this phase noise reduction factor will be somewhere between 0.5 to 1. In the frequency domain, (5.9) means that the noise power spectral density will be shaped by the noise transfer function of (5.7) as shown in Fig. 5.3.

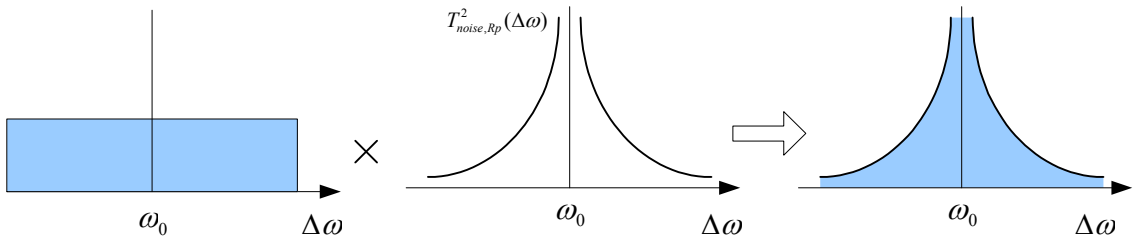


Figure 5.3 Noise shaping in oscillators

Practical tanks may have more parasitic elements as shown in Fig. 5.4, where the parasitic series resistance of the inductor and capacitor, R_l and R_c, are taken into account respectively. In this case, if an effective series resistance, R_{eff}, is defined as

$$R_{eff} = R_l + R_c + \frac{1}{R_p \omega_0^2 C^2}, \tag{5.10}$$

it can be shown that the spectral density of the output noise voltage is [62]

$$\overline{V^2_{on,gp}(\Delta\omega)} = 2kTR_{eff} \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2. \tag{5.11}$$

Accordingly, to compensate for the loss of this tank, G_m of the active element has been changed to

$$G_m = R_{eff} \cdot (\omega_0 C)^2. \tag{5.12}$$

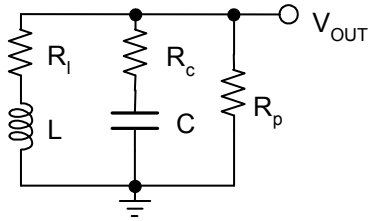


Figure 5.4 Tank circuit includes the series parasitic resistance R_l and R_c

5.2.2 Active Element Noise

The active elements in the oscillator also introduce noise. This noise can be modeled by an output noise current, $\overline{i_{n,Gm}^2}$, as

$$\overline{i_{n,Gm}^2} = 4kT \cdot F_{Gm} \cdot G_m, \tag{5.13}$$

where F_{Gm} is the noise factor of the amplifier. Using (5.12) and applying the same procedure, the spectral density of the output noise voltage generated by G_m is given by

$$\overline{V_{on,Gm}^2(\Delta\omega)} = 2kTR_{eff} \cdot F_{Gm} \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2. \tag{5.14}$$

Nonlinear oscillators usually have a different noise factor compared with the linear noise factor F_{Gm}. Therefore, a factor α is multiplied to F_{Gm} to represent the amount of noise the actual noisy amplifier generates in excess of an ideal noisy amplifier. By defining A as $\alpha \cdot F_{Gm}$, the (5.14) becomes

$$\overline{V_{on,Gm}^2(\Delta\omega)} = 2kTR_{eff} \cdot A \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2. \tag{5.15}$$

The overall one-side spectral density of the noise is given by

$$\overline{V_{on}^2(\Delta\omega)} = 2kTR_{eff} \cdot (1+A) \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2. \tag{5.16}$$

For a sine-wave oscillation with the amplitude of V_0, the phase noise of the oscillator at the offset of $\Delta\omega$ is given by

$$L(\Delta\omega) = \frac{4kTR_{eff}}{V_0^2} \cdot (1+A) \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2. \tag{5.17}$$

This equation represents the phase noise of *LC* oscillators predicted by the LTI model. Note that a similar method can also be applied to other types of oscillators such as ring oscillators [20].

5.2.3 Limitation of the LTI Phase Noise Model

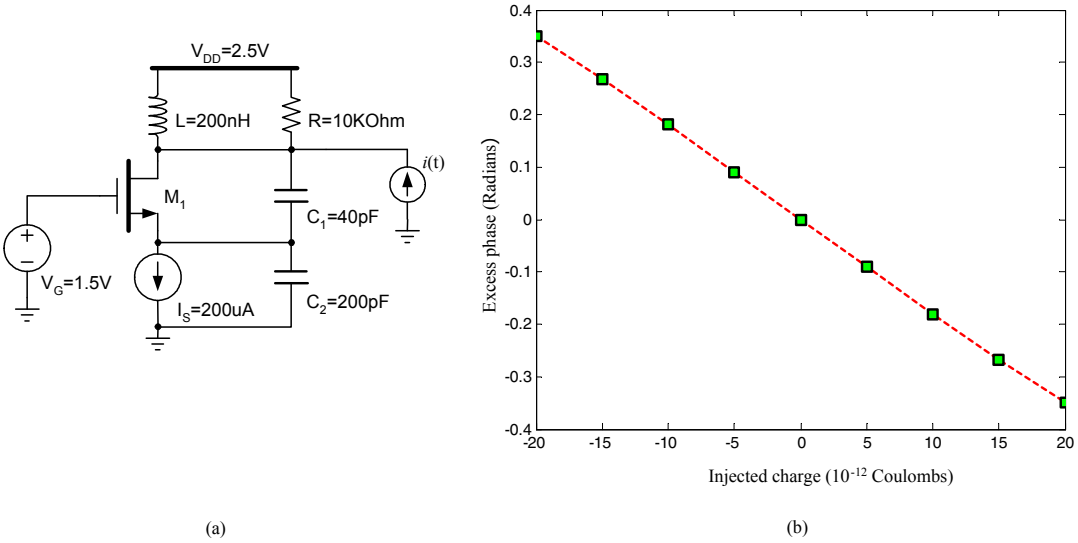
The LTI phase noise model successfully explains why the phase noise decreases with a slope of –20dB/dec for the additive noise. This classical, simple theory can be applied to different kinds of oscillators and provides an acceptable estimation in some designs. For example, only 4dB error between the theoretical calculation and measurement of a ring oscillator is reported in [20]. It also points out two ways to reduce the phase noise according to equation (5.17) – to reduce the effective resistance R_{eff} and to increase the oscillation amplitude. However, due to the nonlinear nature of the oscillators, the LTI model is not able to explain many effects in oscillators' phase noise. For example, it cannot explain the $1/f^3$ region resulting from by the flicker noise. Experiments also reveal that the device noise at high frequencies can be folded into the carrier band and contributes to output phase noise (also called multiplicative noise). The LTI model cannot explain this phenomenon either. Furthermore, there is no analytical equation for the parameter A in (5.17) and therefore it is still an empirical parameter. In summary, this approach represents no fundamental improvement compared with the Leeson's model.

5.3 Linear Time-Variant Phase Noise Model – Hajimiri's Model

In the LTI phase noise model, the responses of the oscillator to noise sources are approximated by LTI systems. However, all oscillators are essentially time-variant

systems. The voltage and current in an oscillator have to be changed periodically to produce the oscillation. Therefore, the LTI approximation is dubitable. Starting from the time-variant nature of the oscillators, Hajimiri proposed a novel, linear time-variant (LTV) phase noise model [63]-[64].

5.3.1 Linearity Assumption



(a) (b)

Figure 5.5 Phase shift versus injected charge (b) for a Colpitts oscillator (a)

The linearity assumption is still valid for oscillators if the noise is much smaller than the oscillation signal. Note that the linearity refers to the noise-to-phase transfer characteristics in oscillators. For example, if a current impulse is injected into a 60MHz Colpitts oscillator as shown in Fig. 5.5 (a) to mimic a noise source in the oscillator, the resulted phase shift obtain from HSPICE simulation is plotted in Fig. 5.5 (b). It can be concluded that the relationship is linear even for a relatively large phase shift (0.35 radian or 20°). In practical oscillators, the noise is usually much smaller and the linear

noise-to-phase transfer characteristic is valid for almost all kinds of oscillators. Note that the injection timing is chosen at the zero crossing for all simulations. However, injecting the same current impulse at different times will cause different excess phase. This phenomenon is the basis of the Hajimiri's LTV phase noise model.

5.3.2 Impulse Sensitivity Function (ISF)

The same perturbation occurring at different times will result in different phase shifts due to the time-variant nature of oscillators. Supposing a perturbation charge is injected into an ideal *LC* tank as shown in Fig. 5.6 (a), the oscillation amplitude will increase ΔV if the injection occurred at the peak (Fig. 5.6 (b)). Note that the zero crossing time is not changed in this case. In practical oscillators, this amplitude variation will disappear quickly due to their loss. So, the perturbation at the peak introduces little phase noise. On the contrary, if the same perturbation is injected at the zero crossing, it has no effect on the oscillation amplitude but generates a phase shift as shown in Fig. 5.6 (c). Although the time-dependence depicted in Fig. 5.6 is only demonstrated by an ideal *LC* circuit, a similar phenomenon happens in all oscillators.

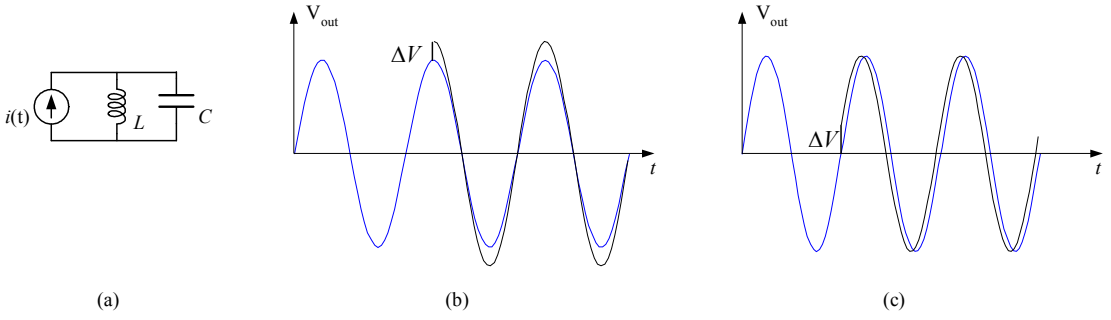


Figure 5.6 Impulse injected into an ideal *LC* tank (a) at the peak (b) and the zero crossing (c)

Based on this time-variant characteristic and the linear assumption, the unit impulse response for excess phase of an oscillator can be expressed as

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t-\tau) \tag{5.18}$$

where q_{max} is the maximum charge displacement on the node, and $u(t)$ is the unit step function. The function $\Gamma(x)$ is called the *impulse sensitivity function* (ISF). It is a dimensionless, frequency- and amplitude-independent periodic function with period of 2π which describes how much phase shift results from applying a unit impulse at time $t = \tau$. The ISF is a function of the waveform, which in turn is governed by the nonlinearity and the topology of the oscillator.

For a given the ISF, the output excess phase, $\phi(t)$, can be calculated using the superposition integral

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau) d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma(\omega_0\tau) i(\tau) d\tau \tag{5.19}$$

where $i(t)$ is the input noise current injected into the node. The periodic ISF can be expanded into a Fourier series

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n) \tag{5.20}$$

where θ_n is not important for random input noise and thus can be neglected. Substituting (5.20) into (5.19), the excess phase, $\phi(t)$, is given by

$$\phi(t) = \frac{1}{q_{\max}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_o\tau) d\tau \right] \tag{5.21}$$

Using this equation, the excess phase $\phi(t)$ resulting from an arbitrary input current, $i(t)$, can be computed if the Fourier coefficients of the ISF have been found. If the current is sinusoid ($i(t) = I_n \cos[(n\omega_0 + \Delta\omega)t]$ with $\Delta\omega << \omega_0$), the arguments of all the integrals in (5.21) are at frequencies higher than ω_0 and are significantly attenuated by the averaging nature of the integration, except the term arising from the n-th integral. It can be shown that the excess phase generated by the integral can be approximated by

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{\max}\Delta\omega}. \tag{5.22}$$

5.3.3 Phase-to-Voltage Transformation

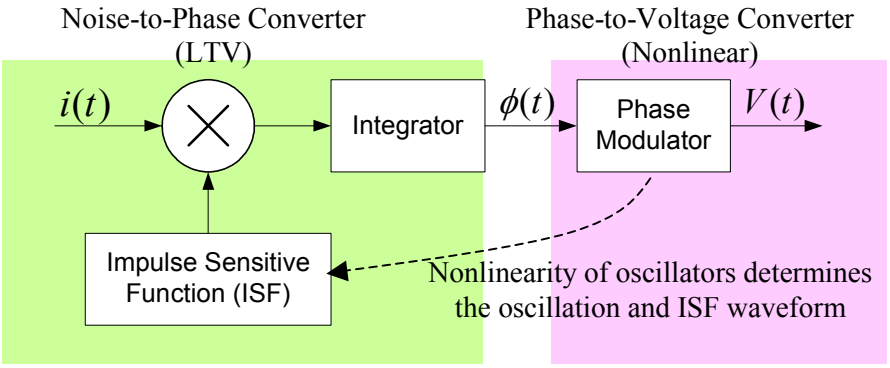


Figure 5.7 Block diagram of the LTV phase noise model

To calculate the phase noise, the power spectral density (PSD) of the oscillator output voltage needs to be computed, which requires knowledge of how the output voltage relates to the excess phase variations. As shown in Fig. 5.7, the conversion of the device noise current to the output voltage is treated as the result of a cascade of two processes. The first LTV current-to-phase process has been discussed in section 5.3.2,

while the second system is a nonlinear phase modulation (PM) system which transforms the excess phase to output voltage. A PM cosine signal can be written as

$$V_{\text{out}}(t) = V_0 \cos(\omega_0 t + V_{\text{m}} \sin\Delta\omega t). \tag{5.23}$$

It is well known that such a PM procedure results in two extra sidebands at the frequencies of $\omega_0 \pm \Delta\omega$ (if V_{m} is small). Mathematically, V_{out} is given by

$$V_{out}(t) = V_0 \cos\omega_0 t - \frac{V_m V_0}{2}[\cos(\omega_0 - \Delta\omega)t - \cos(\omega_0 + \Delta\omega)t]. \tag{5.24}$$

Therefore, for the excess phase generated by an injected current at $n\omega_0 + \Delta\omega$, the resulting two equal sidebands at $\omega_0 \pm \Delta\omega$ have the sideband power relative to carrier given by

$$P_{SBC}(\Delta\omega) = \left(\frac{I_n c_n}{4q_{\max}\Delta\omega}\right)^2. \tag{5.25}$$

Now the injected single-tone current will be replaced by a noise current with a white power spectral density $\overline{i_n^2}/\Delta f$. Note that I_n represents the peak amplitude, hence, $I_n^2/2 = \overline{i_n^2}/\Delta f$ for a unit bandwidth. Also, an injected current at $n\omega_0 - \Delta\omega$ will result in the same two equal sidebands. Thus, (5.25) should be multiplied by a factor 2. Finally, the bandwidth of the injected white noise current is very wide, and the superposition for different n has to be applied. Based on this analysis, the output phase noise in dBc/Hz resulted by the white noise current is given by

$$L\{\Delta\omega\} = 10 \cdot \log\left(\frac{i_n^2/\Delta f \cdot \sum_{n=0}^{\infty} c_n^2}{4q_{\max}^2\Delta\omega^2}\right). \tag{5.26}$$

According to Parseval's relation, the summation term in (5.26) is given by

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi} \left|\Gamma(x)\right|^2 dx = 2\Gamma_{rms}^2 \tag{5.27}$$

where Γ_{rms} is the RMS value of the ISF. As a result, the phase noise is

$$L\{\Delta\omega\} = 10 \cdot \log\left(\frac{\Gamma_{rms}^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \Delta\omega^2}\right). \tag{5.28}$$

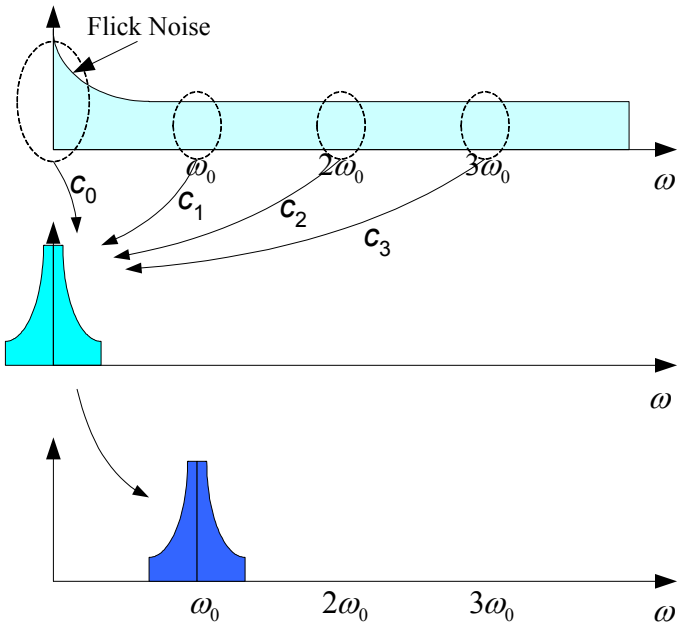


Figure 5.8 Conversion of noise to phase fluctuations and phase-noise sidebands

This equation represents the phase noise spectrum of an arbitrary oscillator in $1/f^2$ region of the phase noise spectrum. In the frequency domain, this LTV model can be illustrated by Fig. 5.8. In the first LTV system, the white noise near the frequency is folded down to the near-DC frequency according to the Fourier coefficients. In the second phase-to-power transformation procedure, the low frequency noise is up

converted to the carrier band. Note that there exist significant differences between Fig. 5.8 and Fig. 5.3.

5.3.4 Corner Frequency and Cyclostationary Noise Sources

5.3.4.1 Corner Frequency

By using the LTV model, the relationship between the device 1/*f* corner and the phase noise 1/f^3 corner can be found. Note that these two corner frequencies are usually assumed to be the same. However, the measurements frequently disaffirm such equality. The device noise spectrum in the flicker noise dominated portion can be denoted as

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}. \tag{5.29}$$

Following the same derivation, the phase noise resulting from the flicker noise is

$$L\{\Delta\omega\} = 10 \cdot \log\left(\frac{c_0^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right). \tag{5.30}$$

Let (5.30) be equal to (5.26). The corner frequency can be solved as

$$\omega_{1/f^3} = \omega_{1/f} \cdot \frac{c_0^2}{2\Gamma_{rms}^2}. \tag{5.31}$$

This equation suggests that the 1/f^3 phase noise corner depends not only on the device 1/*f* noise corner but also the Fourier coefficients of the ISF. Since the ISF is determined by the waveform, the first coefficient, c_0, can be significantly reduced if certain symmetry properties exist in the waveform. Therefore, (5.31) points out that poor 1/*f* device noise need not imply poor close-in phase noise performance.

5.3.4.2 Cyclostationary Noise Sources

Due to the periodic nature of the oscillations, the statistical properties of some random noise sources in oscillators may change with time. These sources are referred as cyclostationary noise sources. For example, if a MOS device is used in oscillators, its channel noise is cyclostationary because the noise power is modulated by the gate source overdrive voltage which varies with time periodically. There are other noise sources in the circuit whose statistical properties do not depend on time and the operation point of the circuit, and are therefore called as stationary noise sources. For instance, the thermal noise of a resistor is a stationary noise source. The LTV model provides a simple way to deal with cyclostationary noise sources. A white cyclostationary noise current, $i_n(t)$, can be decomposed by

$$i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t) \tag{5.32}$$

where $i_{n0}(t)$ is a white stationary noise current and $\alpha(\omega_0 t)$ is a deterministic periodic function describing the noise amplitude modulation. It has been normalized to 1 and can be derived easily from device noise characteristics and operation point. By this decomposition, an effective ISF can be expressed as

$$\Gamma_{eff}(x) = \Gamma(x) \cdot \alpha(x). \tag{5.33}$$

Replacing the original ISF by this effective ISF in the previous derivation, the phase noise contributed by the cyclostationary noise sources in oscillators can be computed by (5.30) easily.

5.3.5 Comparison between Model Predictions and Simulations

Two oscillators are studied to verify the effectiveness of the Hajimiri's model. The first example is the CMOS Colpitts oscillator shown in Fig. 5.5 (a). The NMOS transistor is TSMC 0.25μm device whose model file was obtained from MOSIS website and is listed in Appendix 1. The channel thermal noise current is estimated by $\overline{i_n^2}/\Delta f = 4kT\gamma g_m$ with γ=2.5 for a short channel device [18]. In the SPICE simulator, the flicker noise of the MOS device is calculated by

$$\overline{i_{n,1/f}^2}/\Delta f = \frac{KF \cdot I_{ds}^{AF}}{C_{ox} L_{eff}^2 \cdot f^{EF}}. \tag{5.34}$$

In this model, FK_N=1E-27, KF_P=1E-28 and AF=EF=1. According to these parameters, the device 1/f corner frequency is computed and the result is 3.167MHz.

The phase noise of this 60MHz MOS Colpitts oscillator was then calculated. The result is shown in Fig. 5.9. The oscillator was simulated by both SpectreRF and ADS. The phase noise as a function of the offset frequency from both programs was plotted in the same figure. The significant error in the $1/f^3$ region is observed. On the other hand, the phase noise in the $1/f^2$ region obtained from either SpectreRF or ADS matches theoretical computation well, especially between the theoretical prediction and the SpectreRF simulation result. Note that the simulations obtained from SpectreRF and ADS are not consistent either. For example, ADS simulation gave smaller phase noise in the $1/f^2$ region compared with the SpectreRF's result. Actually, though some simulators have provided the functionality of phase noise simulation, obtaining accurate

prediction is still a challenging topic currently. The reliable phase noise usually has to be obtained by direct measurement.

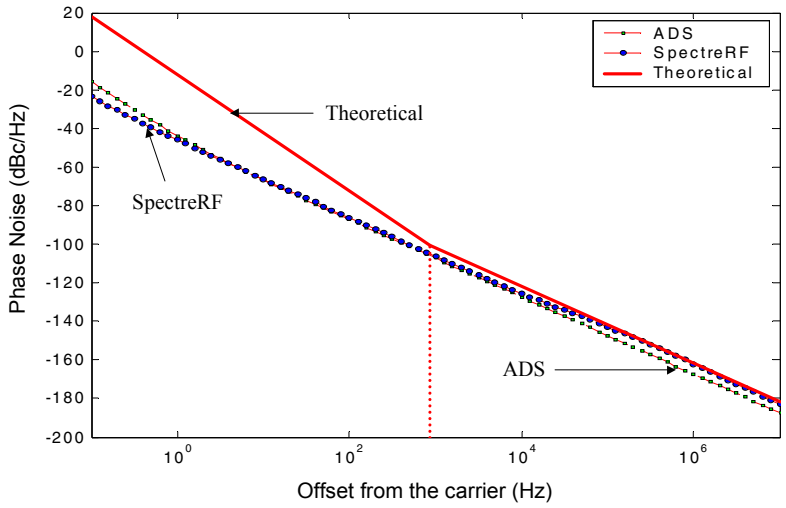


Figure 5.9 Comparison of the phase noise of the 60MHz MOS Colpitts oscillator

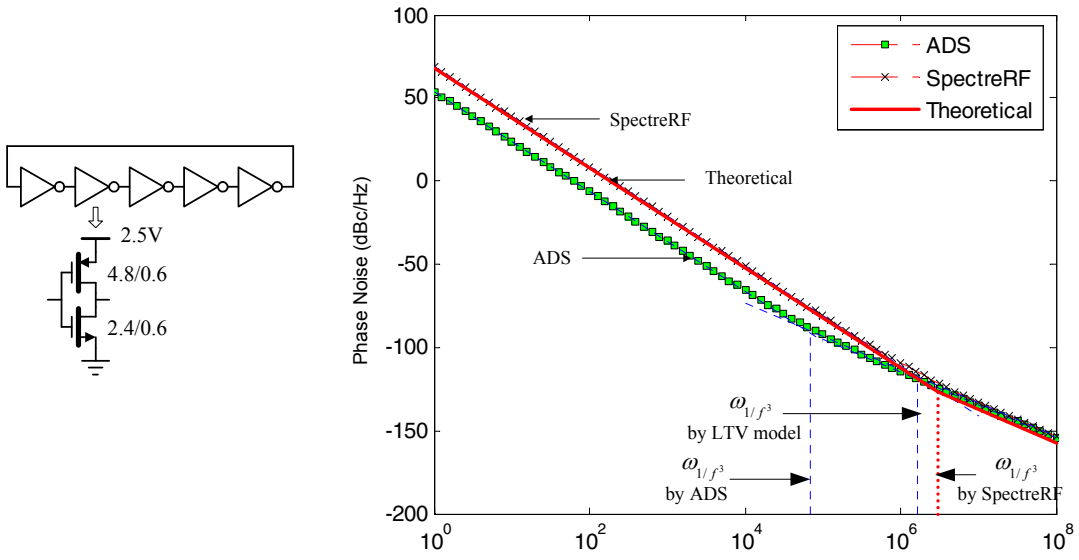


Figure 5.10 A 5-stage CMOS ring oscillator (left) and its phase noise versus offset frequency plot (right)

The ring oscillator was studied too. The ring oscillator under consideration consists of 5 inverters, and its oscillation frequency is 528MHz. The same TSMC 0.25μm model file is used for transistors. In this case, it is found that the theoretical prediction is consistent with the SpectreRF simulation at both the $1/f^2$ and $1/f^3$ region as shown in Fig. 5.10. The $1/f^3$ corner frequency obtained by calculation and simulation are 1.26MHz and 1.67MHz, respectively. However, the ADS and SpectreRF simulation differs in the $1/f^3$ region, suggesting that accurate phase noise generated by oscillators has to be determined by measurement.

5.3.6 Advantages and Disadvantages of the LTV Model

The Hajimiri's LTV phase model is a general model which can be applied to all kinds of oscillators. It even can be extended to estimate the phase noise of other circuits in which the operation point varies with time. By the definition of the ISF, the model closely relates the phase noise with the time-variant nature of the oscillator and provides a clear physical mechanism of phase noise generation. It also points out some design insight to improve the phase noise performance. For example, to reduce the close-in phase noise in oscillators, the oscillation waveform and thus the ISF waveform must be symmetric about a vertical axis to minimize the c_0 according to (5.31). The measured phase noise and the model prediction were also consistent with each other according to reference [63].

The major difficulty of this model is obtaining the ISF, which is obviously the core of the model. Although three methods were mentioned in [63], the most reliable and accurate method is to inject a perturbation current and observe the phase response

of the oscillators as was done already in the previous two examples. However, to get an ISF with decent accuracy, many time domain simulations have to be performed. For instance, the same perturbation currents are injected into the Colpitts oscillator at 296 different times in one period in the previous simulation. The simulation can automatically be done by most of the simulators by using a sweep function, but the required simulation time is relatively long. Furthermore, to observe their effect on excess phase, several oscillation periods after the injections have to be simulated to let the AM variation disappear. This requirement prolongs the simulation time. Finally, if these is no dominant noise source and the phase noise of the oscillators are excited by several noise sources at different nodes, several different ISFs need to be found using time domain simulation. These difficulties in finding ISF limit the application of the LTV model in practical oscillator phase noise analysis.

5.4 Nonlinear Time-Invariant (NTI) Phase Noise Model – Samori's Model

The assumption that the transistors of oscillators work in their linear region is usually not tenable. As mentioned before, the LTI phase model cannot explain the many nonlinear effects such as noise folding. Therefore, the nonlinearity in the oscillators should be taken into account in the phase noise model.

Along with the maturity of the on-chip inductors, *LC* oscillators are widely used in RFIC designs due to their good phase noise performance, simple implementation and differential output. The phase noise of this type of oscillator became a very popular research topic. Samori proposed a nonlinear time-invariant (NTI) phase noise model for the *LC* oscillators [65]. This model explained how the device noise produces phase

noise by analyzing the nonlinearity of the conductance of the differential pair in *LC* oscillators. The model also provides a lot of very useful design insights and optimization rules to reduce the phase noise.

5.4.1 Harmonic Transfer in Nonlinear System

The output noise generated by a tank was calculated in the derivation of the LTI model (equation 5.8). It is well known that the *Q* factor of the tank is $Q=\omega_0 C/g_{ot}$ where g_{ot} is the equivalent parallel conductance of the tank given by

$$g_{ot} \approx g_{pC} + g_{pL} + \frac{\omega_0^2 C^2}{g_{sC}} + \frac{1}{\omega_0^2 L^2 g_{sL}}, \tag{5.35}$$

where the term g_{sC} and g_{sL} are the parasitic conductance in series with *C* and *L*, respectively, g_{pC} and g_{pL} are the conductance in parallel to the same reactive elements, and ω_0 is the oscillation frequency. By these definitions, the one-side spectral density of the output noise voltage can also be expressed as:

$$\overline{V_{on,got}^2(\Delta\omega)} = \frac{kT}{C}\frac{\omega_0}{Q}\frac{1}{\Delta\omega^2}. \tag{5.36}$$

Similar to the factor *A* in the LTI model of (5.15), all other noise voltages generated by active devices are taken into account by multiplying $\overline{V_{on,got}^2(\Delta\omega)}$ by a factor, *F*. Therefore, the phase noise at offset $\Delta\omega$ is given by:

$$L(\Delta\omega) = \frac{2}{A_0^2}\frac{kT}{C}\frac{\omega_0}{Q}\frac{1}{\Delta\omega^2}(1+F), \tag{5.37}$$

where A_0 is the amplitude of oscillation. Unlike the LTI model, the Samori's model figures out a way to compute the factor *F* by taken into account the nonlinearity

of the differential pair in *LC* oscillators. Denoting the output current of the differential pair as $I = I(V)$ and assuming a small single tone signal, $V_l(t)$, at the frequency of $\omega_0 - \Delta\omega$ is superimposed on the carrier, $V_o(t)$, with amplitude of A_0, the output signal of the differential pair can be approximated as

$$I\left(V_o(t) + V_l(t)\right) \approx I\left(V_o(t)\right) + \left.\frac{dI}{dV}\right|_{V_o(t)} V_l(t)\,. \tag{5.38}$$

The dI/dV is the transconductance of the differential pair, i.e. $g(V) = dI / dV$. For *LC* oscillators, the $g(V_o(t))$ is an even function of the time with a fundamental frequency of $2\omega_0$ as shown in Fig. 5.11. Thus, it can be expressed by the Fourier expansion

$$g\left(V_o(t)\right) = \sum_{n=-\infty}^{+\infty} g^{(2n)} e^{j2n\omega_o t} \tag{5.39}$$

where the coefficients $g^{(2n)}$ are real.

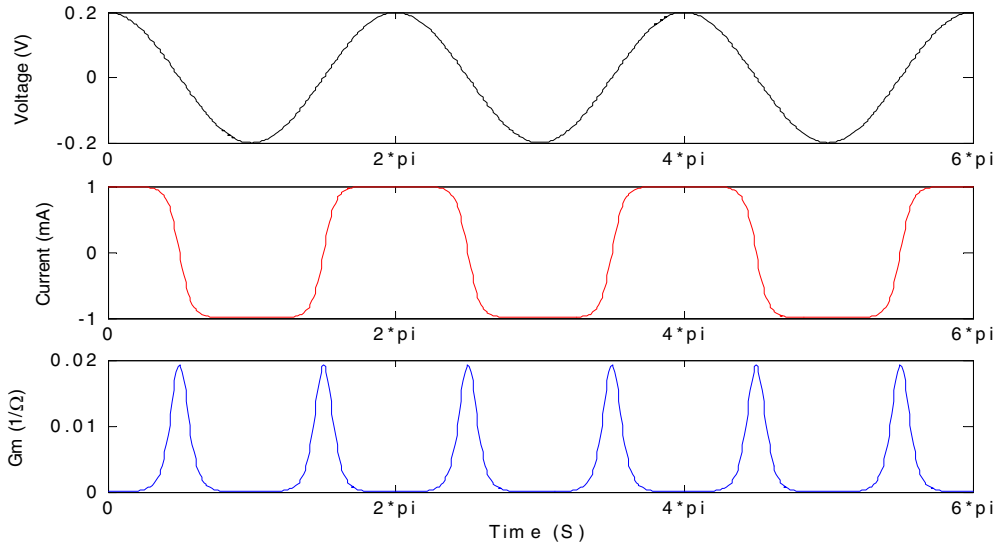


Figure 5.11 Input voltage (top), output current (middle) and transconductance (bottom) of a bipolar different pair biased by 1mA tail current

The first term in (5.38) gives the output harmonics at ω_0. It can be computed as

$$\frac{dI}{dt} = \frac{dI}{dV}\frac{dV}{dt} = g(V)\frac{dV}{dt}, \tag{5.40}$$

$$I_o(t) = I\big(V_o(t)\big) = \int g\big(V_o(t)\big)\frac{dV_o}{dt}dt\,. \tag{5.41}$$

Substituting (5.39) into (5.41) and assuming a cosine oscillation waveform, V_o=A_0·cos($\omega_0 t$), (5.41) leads to the current component at frequency ω_0

$$I_o(t) = (g^{(0)} - g^{(2)})V_o(t)\,. \tag{5.42}$$

Since both $I_o(t)$ and $V_o(t)$ are signal with frequency of ω_0, it is useful to adopt a phasor notation in derivation. Thus, (5.42) can be written as

$$\overline{I_o} = (g^{(0)} - g^{(2)})\overline{V_o} = g_{meff}\overline{V_o}\,, \tag{5.43}$$

where g_{meff} is the effective transconductance which is precisely the ratio of $\overline{I_o}/\overline{V_o}$. The second term in the right-hand side of (5.38) gives the intermodulation tones at frequency $n\omega_0 \pm \Delta\omega$. They can be expressed as [66]:

$$\left(\frac{\overline{V_l}}{2}e^{j(\omega_0-\Delta\omega)t} + \frac{\overline{V_l}^*}{2}e^{-j(\omega_0-\Delta\omega)t}\right)\cdot\sum_{n=-\infty}^{+\infty} g^{(2n)}e^{j2n\omega_o t}\,. \tag{5.44}$$

This equation shows that the harmonic tone $\overline{V_l}$ at $\omega_0-\Delta\omega$ generates two intermodulation terms: $\overline{I_l}$ at $\omega_0-\Delta\omega$, given by $g^{(0)}\overline{V_l}$, and $\overline{I_u}$ at $\omega_0+\Delta\omega$, given by $g^{(2)}\overline{V_l}^*$. Similar terms will be generated by an input harmonic tone $\overline{V_u}$ at $\omega_0+\Delta\omega$. By using a matrix representation, the intermodulation terms can be written as

$$2\begin{bmatrix} \overline{I}_l^*/2 \\ \overline{I}_u^*/2 \end{bmatrix} = \begin{bmatrix} g^{(0)} & g^{(2)} \\ g^{(2)} & g^{(0)} \end{bmatrix} \begin{bmatrix} \overline{V}_l^*/2 \\ \overline{V}_u^*/2 \end{bmatrix}. \tag{5.45}$$

It is well know in communication theory that a small tone superimposed on a carrier will create amplitude modulation (AM) and phase modulation (PM). If the a single tone, $\overline{V_l}$, is superimposed on a carrier, the resulting voltage signal, $V(t)$, is given by

$$V(t) = A_0 \cos(\omega_0 t) + \left|\overline{V_l}\right| \cos\left[(\omega_0 - \Delta\omega)t + \phi_l\right]. \tag{5.46}$$

Applying the phasor decomposition technique, this equation can be written approximately as

$$V(t) = A_0\left[1 + m_V(t)\right]\cos(\omega_0 t + \beta_V(t)), \tag{5.47}$$

where $A_0 m_V(t) = \mathrm{Re}\left\{\overline{V_l}^* e^{j\Delta\omega t}\right\}$ and $A_0\beta_V(t) = \mathrm{Im}\left\{-\overline{V_l}^* e^{j\Delta\omega t}\right\}$. By introducing the phasor representation, the AM and PM modulation indices, $\overline{m_V}$ and $\overline{\beta_V}$, are defined by $m_V(t) = \mathrm{Re}\left\{\overline{m_V} e^{j\Delta\omega t}\right\}$ and $\beta_V(t) = \mathrm{Im}\left\{\overline{\beta_V} e^{j\Delta\omega t}\right\}$. For the tone, $\overline{V_u}$, at the frequency of $\omega_0+\Delta\omega$, a similar relationship holds. The modulation indices can be expressed as

$$\begin{bmatrix} \overline{m_V} \\ \overline{\beta_V} \end{bmatrix} = \frac{1}{A_0}\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_l}^* \\ \overline{V_u} \end{bmatrix}. \tag{5.48}$$

The intermodulation voltages are found by inverting the matrix.

$$\begin{bmatrix} \overline{V_l}^* \\ \overline{V_u} \end{bmatrix} = \frac{A_0}{2}\begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} \overline{m_V} \\ \overline{\beta_V} \end{bmatrix}. \tag{5.49}$$

Similarly, the output current can be expressed as

$$\begin{bmatrix} \overline{I_l^*} \\ \overline{I_u} \end{bmatrix} = \frac{\left|\overline{I_0}\right|}{2} \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} \overline{m_I} \\ \overline{\beta_I} \end{bmatrix}. \tag{5.50}$$

Form (5.45), (5.49) and (5.50), the following equation is obtained.

$$\left|\overline{I_0}\right| \begin{bmatrix} \overline{m_I} \\ \overline{\beta_I} \end{bmatrix} = \begin{bmatrix} g_{am} & 0 \\ 0 & g_{pm} \end{bmatrix} \begin{bmatrix} \overline{m_V} \\ \overline{\beta_V} \end{bmatrix} \left|\overline{V_0}\right|, \tag{5.51}$$

where $g_{am}=g^{(0)}+g^{(2)}$ and $g_{pm}=g^{(0)}-g^{(2)}=g_{eff}$. Note that these g_{am} and g_{pm} of a bipolar or a CMOS differential pair can be easily obtained. Fig. 5.12 shows g_{am} and g_{pm} computed numerically from the hyperbolic tangent and square trans-characteristics of bipolar devices and CMOS devices, respectively. The tail current is chosen as 1mA in both cases. For the CMOS pair, $\mu_n C_{ox}$ is 1.345×10^{-4} A/V^2 and W/L is 10.

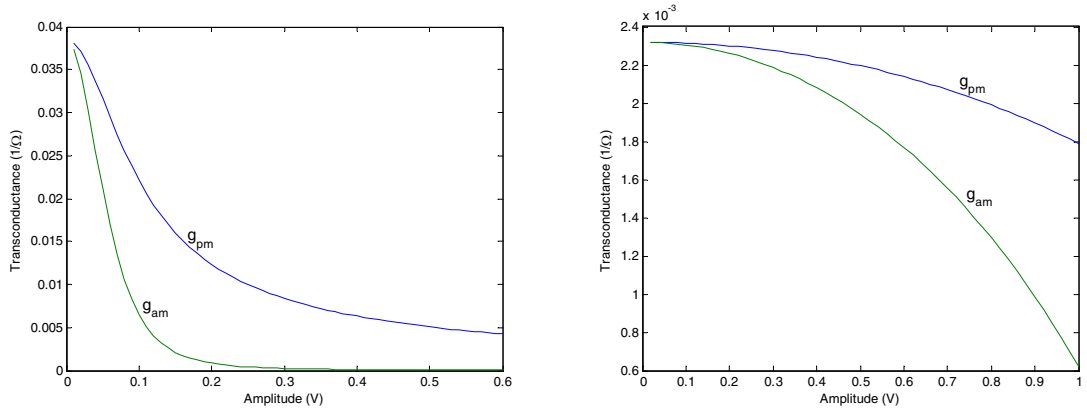


Figure 5.12 Dependence of AM and PM transconductance of a bipolar (left) and NMOS (right) pairs as a function of the amplitude of the input signal

From this figure, it can be concluded that the noise is equally partitioned between amplitude noise and phase noise when the amplitude is small. However, when the oscillators enter the nonlinear region, the g_{am} drops more quickly than g_{pm} does.

Therefore, the noise sources generate more phase noise than amplitude noise in the nonlinear region. If an ideal hard limiter can approximate the pair, the current will be an ideal square and there is no AM noise. On the other hand, any change in the phase of the input waveform causes a time shift of the output transitions and generates the phase noise at the output.

5.4.2 Phase Noise due to Differential Pair

As mentioned in Chapter 2, the major device noise of a bipolar device includes the shot noise associated with collector and base currents, the thermal noise from the base spreading resistor and the flicker noise. For a MOSFET, the noise sources are the channel thermal noise and flicker noise. If the phase noise is measured in the $1/f^2$ region, the flicker noise is neglected. The noise which is modeled by the noise current parallel to device, such as the collector shot noise in BJTs and the channel thermal noise in MOSFETs, can be transformed to the input of the differential pair as noise voltages governed by $\overline{I_n^2}/G_m^2$ [18]. The resulting double side noise voltage spectrum can be written as $2kTR_{b,eff}$, where $R_{b,eff}$ is the effective base (or gate) spreading resistance that generates the equivalent noise voltage. Obviously, this noise is a wide-band white noise. The single-tone harmonic transfer theory discussed in 5.4.1 can be applied to it. Based on the same derivation, the matrix expression similar to (5.45) is obtained

$$\begin{bmatrix} \overline{I}_l^*/2 \\ \overline{I}_u^*/2 \end{bmatrix} = \begin{bmatrix} g^{(-2n)} & g^{(2n+2)} \\ g^{(2n+2)} & g^{(-2n)} \end{bmatrix} \begin{bmatrix} \overline{V}_{2n+1,l}^*/2 \\ \overline{V}_{2n+1,u}^*/2 \end{bmatrix}. \tag{5.52}$$

This equation shows that only the noise voltages near the frequency of $\pm(2n+1)\omega_0$ will generate the noise current at $\pm(\omega_0 \pm \Delta\omega)$. The relative contribution to the

noise voltage is weighted by the Fourier coefficients, $g^{(2n)}$, of $g(V_o(t))$. Note that if the white noise has an equivalent bandwidth of $N\omega_0$ where n is successive numbers from 1 to $N/2$, the overall output noise current will be the summation of all contributed noise voltages at different frequencies.

A special case is to consider the pair as a hard limiter. The output current in this case is a square wave and the $g(V_o(t))$ is a train of δ functions at a frequency of 2 ω_0. The Fourier spectrum of $g(V_o(t))$ has an infinite number of terms given by $(-1)^n \delta(\omega - 2n\omega_0) \cdot g_{ot} / 2$. Since noise voltage is multiplied in the time domain, the output noise current spectrum is obtained from the convolution between these functions and the wideband noise. Fig. 5.13 schematically shows the white noise spectrum with a bandwidth $N\omega_0$. The noise close to the frequency $\pm(2n+1)\omega_0$, denoted by the dashed areas, will be folded within the tank bandwidth. Each folded replica is weighted by the corresponding $g^{(2n)}$ factor governed by (5.52). For example, the contribution to $\overline{I_u}$ from $\overline{V_{3l}^*}$ and $\overline{V_{3u}}$ is determined by $g^{(4)}$ and $g^{(-2)}$ respectively. The overall output noise current spectrum is the summation of all the corresponding folded noise terms as shown in Fig. 5.13. For the hard limiter approximation, Samori showed that the F factor in (5.37) can be expressed as

$$F = 2R_{b,eff} g_{ot} \frac{N}{2}, \tag{5.53}$$

where g_{ot} is calculated by (5.35). N defines the bandwidth of the noise by $N\omega_0$.

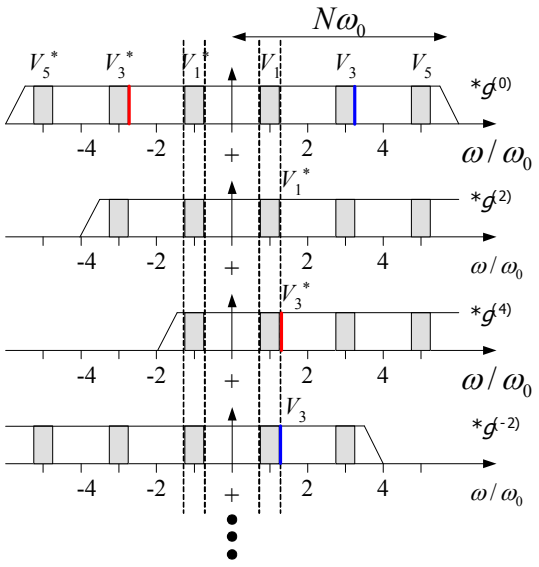


Figure 5.13 Folding of the white noise spectrum at the input of the differential pair

For practical differential pairs, (5.52) still holds. However, the F factor cannot be computed by the simple analytical expression like (5.53). As demonstrated in Fig. 5.12, a numerical solution for $g^{(2n)}$ is easy to obtain based on the hyperbolic tangent and square law trans-characteristics for bipolar and CMOS differential pairs. Therefore, unlike the LTI phase noise model, the F factor can be numerically obtained in the Samori phase noise model.

5.4.3 Phase Noise due to Tail Current Source

When the oscillation amplitude is large (for example, 300-500mV for bipolar pairs), the pair is completely switched during most of the carrier period. In this case, the conducting transistor acts as a cascode device to the tail current source. In a linear circuit, it is well known that the cascode transistor contributes little noise. So, the phase noise generated by the differential pair is negligible during these times. On the other

hand, the phase noise generated by the tail current source progressively gains importance.

If the hard limiter approximation is valid, the phase noise generated by the tail current source can again be calculated analytically. The tail current source noise, modeled as a noise current I_n, is delivered to the tank via an ideal switch. It is equivalent to multiplying the noise current by a square wave $T(t)$ with a frequency ω_0. An expression similar to (5.44) can be obtained

$$\left(\frac{\overline{I_n}}{2}e^{j\omega t}+\frac{\overline{I_n}^*}{2}e^{-j\omega t}\right)\cdot\sum_{n=-\infty}^{+\infty}T^{(2n+1)}e^{j(2n+1)\omega_o t}, \tag{5.54}$$

where $T^{(2n+1)}$ is the Fourier coefficients of the square wave. This equation governs the convolution in the spectral domain between the noise in the tail current source and the spectrum of $T(t)$. The noise current tone $\overline{I_u}$ and $\overline{I_l}$, at frequencies of $\omega_0\pm\Delta\omega$, can be calculated as

$$\begin{bmatrix}\overline{I}_l^*/2\\ \overline{I}_u^*/2\end{bmatrix}=\begin{bmatrix}T^{(-1)} & T^{(1)} & T^{(-3)} & \cdots\\ T^{(1)} & T^{(3)} & T^{(-1)} & \cdots\end{bmatrix}\begin{bmatrix}\overline{I_n}(\Delta\omega)/2\\ \overline{I_n^*}(2\omega-\Delta\omega)/2\\ \overline{I_n}(2\omega+\Delta\omega)/2\\ \overline{I_n^*}(4\omega-\Delta\omega)/2\\ \vdots\end{bmatrix}. \tag{5.55}$$

Note that this equation shows that the output noise currents are due to the noise components around the even harmonics of ω_0 in the tail current source. Using (5.55) and (5.50), AM and PM current current at $\omega_0-\Delta\omega$ can be expressed as

$$\overline{I_{l,am}}(\omega_0-\Delta\omega)=\frac{1}{\pi}\overline{I_n}(\Delta\omega)+\frac{1}{\pi}\sum_{n=1}^{\infty}\frac{\overline{I_n^*}(2n\omega_0-\Delta\omega)+\overline{I_n}(2n\omega_0+\Delta\omega)}{4n^2-1}e^{j(n-1)\pi}, \tag{5.56}$$

$$\overline{I_{l,pm}}(\omega_0-\Delta\omega)=\frac{1}{\pi}\sum_{n=1}^{\infty}(2n)\frac{\overline{I_n^*}(2n\omega_0-\Delta\omega)+\overline{I_n}(2n\omega_0+\Delta\omega)}{4n^2-1}e^{jn\pi}\,, \tag{5.57}$$

The equations (5.55) to (5.57) suggest: (i): the noise at $(2n+1)\omega_0\pm\Delta\omega$ are not folded within the bandwidth of the tank (5.55); (ii) the noise at $\Delta\omega$ only contributes to AM noise (the first term in (5.56)) and (iii) the PM noise is contributed by the noise current at $2n\omega_0\pm\Delta\omega$ with $n>0$ (5.57).

If the noise in the tail current source is white with the double-sided power spectral density S_{nt}, then it satisfies $\overline{I_n^2}=4S_{nt}$. The total phase noise spectral density results is

$$S_{pm}(\omega_0-\Delta\omega)=\frac{S_{nt}}{\pi^2}\sum_{n=1}^{\infty}4n^2\,\frac{2}{(4n^2-1)^2}=\frac{S_{nt}}{8}\,. \tag{5.58}$$

The resulting F factor in (5.37) is given by

$$F=\frac{S_{nt}}{8kTg_{ot}}\,. \tag{5.59}$$

For practical differential pairs, $T(t)$ is not a strict square waveform. Although (5.54) and (5.55) are still valid, there is no analytical expression for $\overline{I_{l,am}}$ and $\overline{I_{l,pm}}$ as well as for the F factor. However, the convolution procedure is similar to Fig. 5.13 and thus the F factor can be numerically solved. Combining (5.53) and (5.59), the F factor for practical LC oscillators can be written as

$$F=2R_{b,eff}g_{ot}\eta+\frac{\sigma S_{nt}}{kTg_{ot}}\,, \tag{5.60}$$

where the upper values for η and σ are $N/2$ and 1/8 as given by the hard limiter approximation. They may be used as a first order estimate of the F factor. An accurate F factor for practical circuits has to be computed numerically.

5.4.4 Advantages and Disadvantages of NTI Phase Noise Model

Samori's NTI phase noise model systematically illustrates the noise generation mechanisms in *LC* oscillators from a spectral domain point of view. These mechanisms provide useful design insight into *LC* oscillators. For example, the phase noise generated by a biasing circuit, usually neglected, must be taken into account if the oscillation amplitude is relatively large.

However, Samori's model can only be applied to the differential pair based *LC* oscillators. Although the similar noise folding mechanism exists in all kinds of oscillators, there is no mathematical approach to estimate the phase noise based on this NTI model. Extending this theory to other oscillators may be an interesting research topic. Also, obtaining the F factor numerically for a practical differential pair is tedious.

5.5 Kaertner and Demir's Phase Noise Model

Kaertner [67] and Demir [68]-[70] developed two phase noise models for oscillators. Although their theories are different in definitions and derivations, they produce consistent results because two models are both based on perturbation theory and the stochastic process. These two models are more rigorous when compared with the previous four models. For example, the phase noise at the carrier frequency in Demir's model is finite while it is infinite in Hajimiri's LTV model. The completed

mathematical derivation of this model is out of the scope of this dissertation. The basic idea and the conclusion of the Demir's phase noise model will be introduced briefly.

For a given oscillator with a *LC* tank, if two independent state variables, voltage $v(t)$ across the capacitor versus the current $i(t)$ through the inductor are plotted, a closed trajectory with a period of T similar to the trajectory as shown in Fig. 5.14 is obtained. In general, the dynamics of an oscillator can be described by a system of different equations

$$\dot{x} = f(x), \tag{5.61}$$

where x is an n-dimensional state vector. If there is no noise sources (i.e. no perturbations) in oscillators, the system has a periodic solution $x_s(t)$, which forms a stable-limit cycle in the n-dimensional solution space as illustrated in Fig. 5.14. When the oscillator is perturbed, this periodicity is lost. For stable oscillators, however, the perturbed trajectory remains within a small band around the unperturbed trajectory as shown in the same figure. If there are p random noise sources, a small state-dependent perturbation term $B(x)b(t)$ can be added to (5.61) where $b(t)$ is a p-dimensional vector and $B(x)$ is a $n \times p$ matrix. Hence, the perturbed system is described by

$$\dot{x} = f(x) + B(x)b(t). \tag{5.62}$$

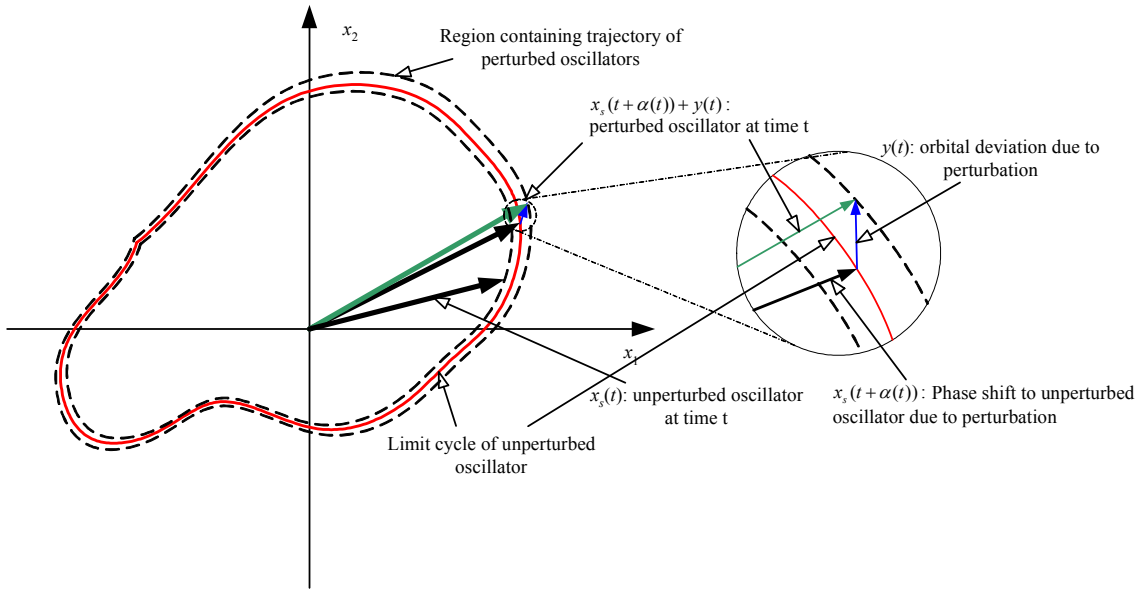


Figure 5.14 Oscillator trajectories

Demir proved that the solution, $x_s(t)$, for a perturbed system can be expressed by $x_s(t+\alpha(t))+y(t)$, where (i) $\alpha(t)$ is a changing time shift, or *phase deviation*, in the periodic output of the unperturbed oscillator; (ii) $y(t)$ is an additive component, which is called an *orbital deviation*, to the phase-shifted oscillator waveform. By this decomposition, a nonlinear differential equation for phase deviation, $\alpha(t)$, is derived. It can be expressed as

$$\frac{d\alpha(t)}{dt} = v_1^T\left(t+\alpha(t)\right)B\left(x_s\left(t+\alpha(t)\right)\right)b(t), \quad \alpha(0)=0\,. \tag{5.63}$$

where $v_1(t)$ is a periodically time-varying vector called the *Floquet vector* [71]. If $b(t)$ are white, solving this equation and computing the noise spectrum by autocorrelation, the spectrum of the oscillator output with white noise sources is given by

$$S_V(f) = \sum_{n=-\infty}^{\infty} X_n X_n^* \frac{f_0^2 n^2 c}{\pi^2 f_0^4 n^4 c^2 + (f + nf_0)^2}, \tag{5.64}$$

where X_n is the Fourier coefficients of the solution $x_s(t)$ for the unperturbed system. X_n satisfies

$$x_s(t) = \sum_{n=-\infty}^{\infty} X_n \exp(jn2\pi f_0 t). \tag{5.65}$$

c in (5.64) is a single scalar constant which is defined as

$$c = \frac{1}{T}\int_0^T v_1^T(\tau) B(x_s(\tau)) B^T(x_s(\tau)) v_1(\tau) d\tau. \tag{5.66}$$

From the output spectrum, phase noise can be found easily. The same procedure can also be extended to colored noise sources in oscillators, and similar results are obtained [70]. The author also developed a mathematical method to solve equation (5.63) and hence find the final phase noise of oscillators.

Demir's phase noise model is a unifying model which can be applied to any nonlinear oscillator (i.e. electrical, optical, mechanical and so on). It is very rigorous, but its results are difficult to use in the phase noise estimation by hand-calculations. It does not provide useful design insight either. On the other hand, this model, as well as the mathematical method the author proposed, are very useful in simulations. For example, the SpectreRF simulator uses a similar method in its PSS and PNoise simulation to find the phase noise of oscillators [72].

5.6 Summary

Five phase noise models –Leeson's model, LTI model, LTV model, NTI model and Kaertner and Demir's model – were discussed in this chapter. Leeson'd model is an

empirical model which cannot be used in predicting phase noise. The empirical constants in this model have to be obtained from measurements. By applying classical linear circuit theory, the LTI model gives an explanation of the –20dB slope in the phase noise plot. It also provides some design insight for suppressing phase noise. However, because of neglecting the nonlinearity in oscillators, the model represents no fundamental improvement comparing with the Leeson's model.

Both the LTV model and the NTI model view the oscillator as a nonlinear system. But they start out from different points of view. In the NTI model for *LC* oscillators, the transconductance of differential pair is considered as nonlinear directly. This nonlinearity folds the noise at different frequencies into the carrier band – a very similar procedure occurs in every mixer. On the other hand, the LTV model views the oscillator as a linear but time variant system to noise sources. If a linear system is time-variant, it also can generate frequency components that do not exists in the input signal (the noise frequencies) [73] – noise-folding effect occurs in the NTI systems too. In other words, in the LTV model, the oscillator acts as a VCO and changing its operating frequency due to FM modulation caused by noise generated in the oscillator. In the NTI model, the phase noise comes from the small-signal mixing of noise due to the nonlinear behavior of the oscillator, where noise mixes with the oscillation signal and harmonics to generate sideband frequencies on either side of the oscillator signal. From this point of view, it can be concluded that these two models are two different ways of looking as the same problem. Note that the LTV model is a general model but the NTI

model discussed here is only for *LC* oscillators. However, the NTI model provides a lot of very useful design insights which lead to many phase noise suppression techniques.

In the end, a unifying and more rigorous phase noise model – Kaertner and Demir's model – was introduced briefly. This model is particularly suitable to simulators to compute the phase noise in oscillators.

CHAPTER 6

TECHNIQUES FOR SUPPRESSING PHASE NOISE OF LC OSCILLATORS

Although relaxation and ring oscillators are attractive from the standpoint of circuit integration, *LC* tuned oscillators are still the only reliable way to meet the very tight phase noise requirements imposed by today's wireless communication systems. Thereofore, in the last years the interest for this solution has increased.

A very useful phase noise model proposed by Samori has been introduced in chapter 5. In his model, the noise sources are assumed to be white. However, the flicker noise of the devices has significant contribution to the phase noise by the up-conversion mechanism. This effect is especially important to the CMOS oscillator and when the band spacing is small. Therefore, it received a lot of research recently [74]-[77]. In this chapter, the phase noise generation mechanisms for different noise sources will be summarized. Then several techniques to suppress the phase noise will be introduced.

6.1 Phase Noise Generation in *LC* Oscillators

According to Samori's phase noise model, the phase noise of *LC* oscillators can be expressed as

$$L(\Delta\omega) = \frac{2}{A_0^2}\frac{kT}{C}\frac{\omega_0}{Q}\frac{1}{\Delta\omega^2}(1+F), \tag{6.1}$$

where A_0 is the amplitude of oscillation. The first term of (6.1) describes the noise generated by the tank parasitic resistance while F is the noise-folding factor that

describes the phase noise generated by the nonlinear active devices. If the differential pair can be considered as a hard limiter and the noise can be assumed white, then the F factor is given by

$$F = 2R_{b,eff} g_{ot} \frac{N}{2}, \tag{6.2}$$

where g_{ot} is the effective parallel conductance of the tank, N defines the band width of the noise by $N\omega_0$ and $R_{b,eff}$ is the effective noise resistance. Besides these two kinds of noise, there are three other noise sources in typical LC oscillators: (i) the flicker noise of the differential pair, (ii) the white noise generated by the tail current source and (iii) the flicker noise provide by the tail current source device. In this chapter, several techniques will be introduced to suppress these noise sources. However, equations (6.1) and (6.2) actually describe the intrinsic minimum phase noise that can be reached by the LC oscillator.

The mechanism on how these noise sources cause the output phase noise will be summarized as follows.

First, the thermal noise generated by the parasitic resistance of the tank will appear as predicted by the classical linear phase noise model. To reduce this noise, the parasitic resistance should be minimized. Hence, the Q factors need to be maximized for both the spiral inductors and varactors. However, as pointed out in Chapter 4, their values are primarily determined by the process technology.

Second, the phase noise contributed by the white noise of the differential pair is described by Samori's model. According to his theory, the noise voltages near the

frequency of $\pm(2n+1)\omega_0$ will generate the noise current at $\pm(\omega_0\pm\Delta\omega)$ and thus create the output phase noise by injecting the noise current into the tank.

Third, the flicker noise of the differential pair contributes to the phase noise by a special up-conversion process [77]. If this flicker noise is only modeled as a near-DC noise voltage at the input of the transistor, it cannot account for the close-in phase noise because only the noise voltage near the frequency of $\pm(2n+1)\omega_0$ contributes to the phase noise according to the Samori's phase noise model. However, the flicker noise also modulates the second-order harmonic voltage waveform at the tail every half period, inducing a noisy current in the capacitor, C_{tail}, attached at the coupled sources (or the emitters for bipolar case) of the differential pair. It is equivalent to a noise current in the tail at the frequency of $2\omega_0$. Therefore, after commutation through the differential pair, this noise current mixes down to the oscillation frequency as predicted by Samori's model. Note that if the near-DC white noise cannot be ignored, it contributes to the phase noise by the same way.

Fourth, the white noise in the tail current source leads to phase noise too. According to Samori's model, the noise at $(2n+1)\omega_0\pm\Delta\omega$ has no effect on the phase noise but the noise at $\Delta\omega$ contributes to AM noise and the noise at $2n\omega_0\pm\Delta\omega$ ($n>0$) directly generates the phase noise. Although the near-DC noise only results in AM noise at the output, this AM noise will modulate the effective capacitance of the varactors, converting AM to PM and generating phase noise [75] [76]. This procedure is called as AM-to-PM (or AM-to-FM) up-conversion.

Finally, the flicker noise in the tail current source also produces output phase noise. The tail current governs the amplitude in the current-limited regime. Therefore, the flicker noise in the tail current source will produce a low frequency random AM signal. Then the AM-to-PM up-conversion occurs and the flicker noise appears as the close-in phase noise. Note that this flicker noise is usually dominant compared with the low frequency white noise in the tail current source and thus very troublesome.

The qualitative analysis listed above is helpful to explain the phase noise suppression techniques summarized in the next section.

6.2 Phase Noise Suppressing Techniques

The white noise of the tank and the differential pair are intrinsic noise sources, and they cannot be removed or suppressed. On the other hand, the flicker noise form the differential pair and tail current source as well as the white noise of the tail current source may be effectively reduced by some techniques. These techniques include: (i) remove tail current source (ii) capacitive noise filtering in the tail current source, (iii) *LC* noise filtering, (iv) inductive control line, (v) inductive degeneration, (vi) decouple the common node by a capacitor, (vii) reduce VCO gain by switched capacitors (viii) differential control line.

6.2.1 Remove Tail Current Source

As pointed out by the Samori's model, the tail current source contributes more phase noise when the oscillation amplitude is large. Therefore, removing the tail current source is helpful to get rid of the phase noise from the tail current source [76] [78]. A

possible topology without the tail current source is shown in Fig. 6.1 (a) and it does produce steady-state oscillation.

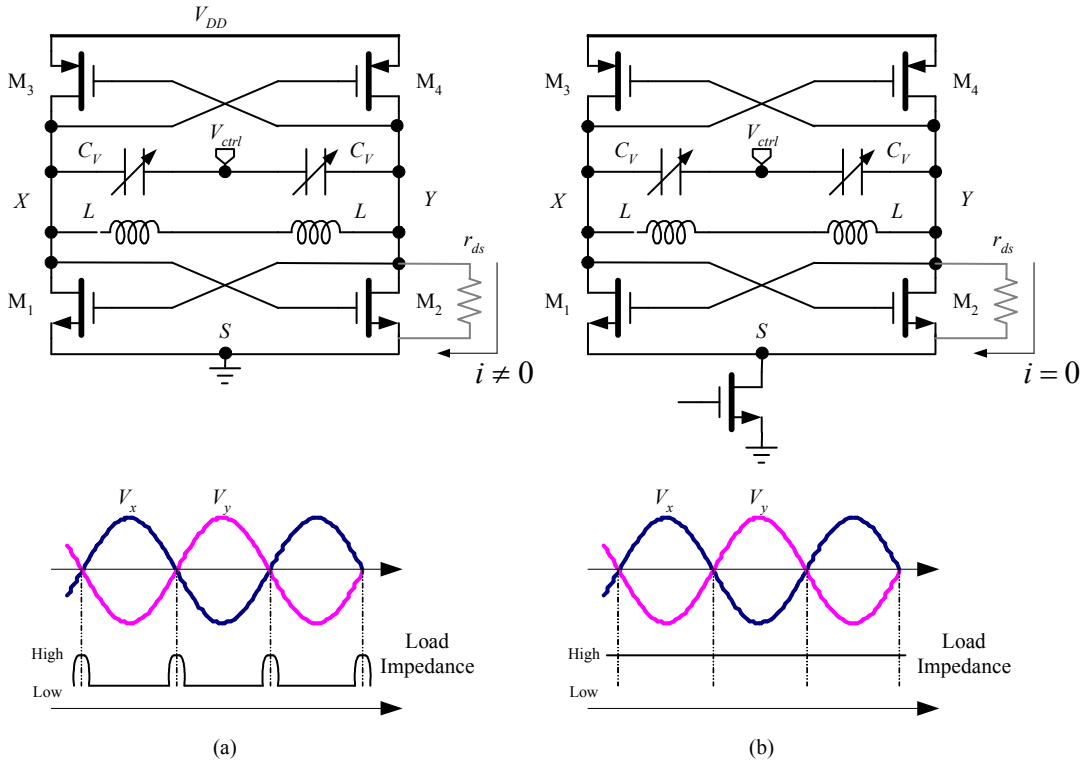


Figure 6.1 CMOS *LC* oscillators without (a) and with the tail current source (b)

However, this topology has two drawbacks. First, the oscillator will work at the voltage-limited region with a high overdrive voltage for coupled devices, resulting in relatively large current in the oscillator. Increasing bias current in the voltage-limited region will degrade the phase noise performance. To alleviate the problem, the *W*/*L* ratio has to be reduced for the smaller g_m. But the flicker noise generated by the transistors is increased since the flicker noise is reversely proportional to the device area. Second, removing tail current source also reduces the impedance at the common-mode point *S*, which actually reduces the resonator quality factor because of the load

effect [78]. At the zero differential oscillation voltage, two coupled transistors evenly share the tail current and both of them are in saturation. As the rising differential oscillation voltage crosses V_t, the V_{gd} of one MOSFET exceeds V_t, forcing it into the triode mode, and the V_{gd} of the other MOSFET falls below $-V_t$, driving it deeper into saturation. The r_{ds} of the device in the triode region decreases with the differential voltage and adds greater loss to the resonator because the current flowing through it is in-phase with the differential voltage. In the next half cycle, the same situation occurs to the other MOSFET. Hence, as the load of the resonator, the two transistors lower the average resonator quality factor. With a smaller resonator Q factor, the phase noise of the oscillator increases. On the other hand, if a current source with relatively large output impedance is inserted into node S (Fig. 6.1 (b)), the load impedance "seeing" by the sources of the MOSFETs is always high, resulting in negligible current through r_{ds}. Hence, it preserves the Q factor of the resonator. Due to these disadvantages, the LC oscillator without tail current source usually needs to be carefully designed in order to obtain significant phase noise improvement as reported in [77].

6.2.2 Capacitive Noise Filtering at the Tail Current Source

The white noise near the frequency $2n\omega_0 \pm \Delta\omega$ (n>0) in the tail current source directly generates the phase noise according to Samori's phase noise model. To suppress the phase noise originated by this noise source, a large capacitor, C_{tail}, can be inserted between the common mode node S and ground [74] [79], resulting in a capacitive noise filtering topology at the tail current source as depicted in Fig. 6.2.

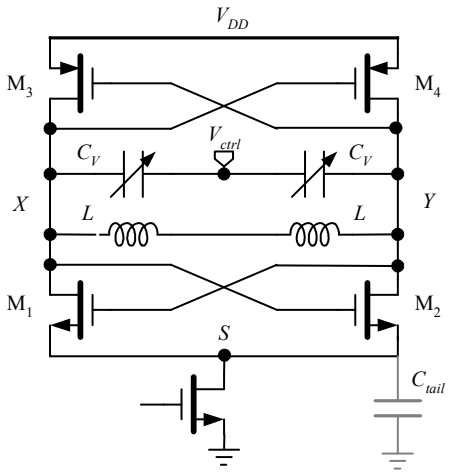


Figure 6.2 Capacitive filtering at the tail current source

The inserted C_{tail} functions as a low-pass filter that bypasses the noise at the frequency higher than $2\omega_0$. At the same time, the voltage fluctuation at S is depressed. Hence, the modulation voltage resulting from the flicker noise of the differential pair at this point is alleviated, resulting in less AM-to-PM phase noise. However, C_{tail} decreases the impedance at S, potentially reducing the Q factor of the resonator and thus degrading the phase noise performance. Therefore, the C_{tail} value should be properly chosen. The cutoff frequency of the resulting low-pass filter should be greater than ω_0 but less than $2\omega_0$.

6.2.3 LC Noise Filtering

The tail current source plays a twofold role in the *LC* oscillator: it provides the bias current, and it also inserts a high impedance in series with the switching MOSFETs of the differential pair. Reducing the impedance degrades the Q factor of the resonator and thus increases the phase noise, as mentioned in the above two methods. On the

other hand, it is well known that the common mode node of the differential pair is a "virtual-ground" point (low impedance point) for the differential signal. In any balanced circuit, odd harmonics circulate in a differential path, while even harmonics flow in a common-mode path [78], through the resonator capacitance and the switching MOSFETs to ground in this case. Therefore, strictly speaking, the current source need only provide high impedance to even harmonics. If the noise near the second-order harmonics is dominant, it suggests that a high impendence, narrow band circuit centered at $2\omega_0$ can be added to the common mode point of the *LC* oscillator. The resulting *LC* noise-filtering oscillator is shown in Fig. 6.3 [78] [80]. In this oscillator, C_{tail} is used to short the high frequency ($\geq 2\omega_0$) noise to ground. Since it decreases the impedance of the node S_1, an inductor L_1 is inserted between the current source and the node S_1. The inductance is chosen to resonate at $2\omega_0$ in parallel with whatever capacitance is present at the node S_1, i.e. C_1. Hence, the impedance for second-order harmonics is raised, and the Q factor is preserved. The high impedance *LC* filter circuit also blocks the noise in the tail current source near the frequency of $2\omega_0$. The L_2 and C_2 have the same function.

The well designed *LC* noise filtering circuit can significantly improve the phase noise performance of the *LC* oscillator. However, the additional capacitors and inductors increase the chip area. The inductor design is always troublesome because they are apt to pick up noise from the substrate, a severe problem especially in mixed-signal circuits. The shielding technique is helpful to reduce the noise coupled into the spiral inductors [24]. However, it also complicates the design process.

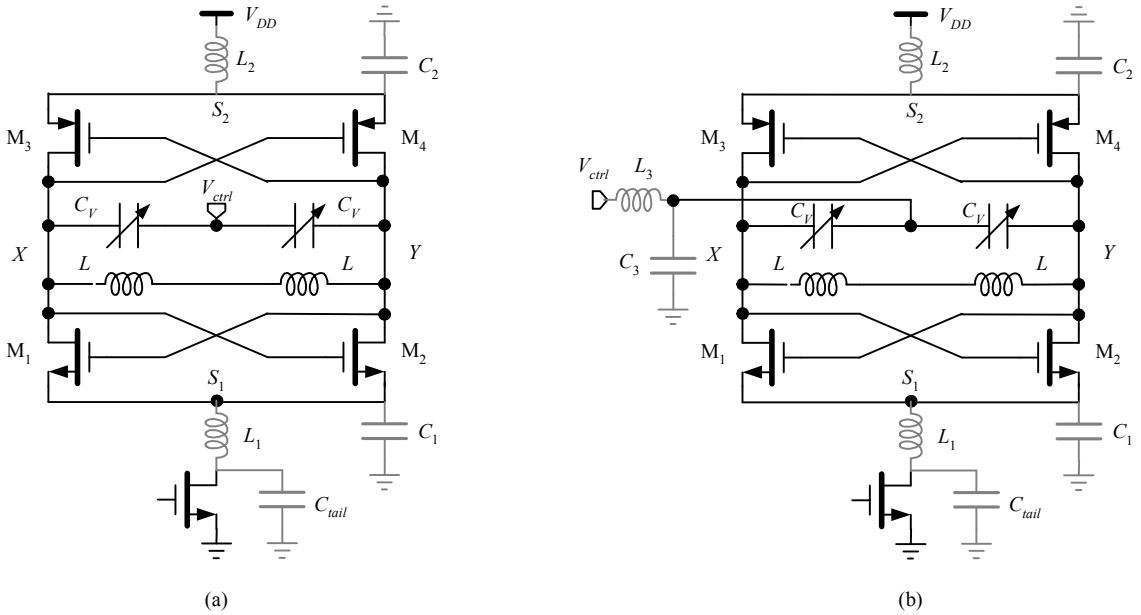


Figure 6.3 Oscillator with *LC* noise filter (a) and inductive control line (b)

6.2.4 Inductive Control Line

The Q factor of the resonator, as mentioned in the previous section, will be degraded if the common mode nodes S_1 and S_2 in the VCO have low impedance since the even harmonics will flow through the varactors to the control line, which is AC grounded. However, even if S_1 and S_2 have very high impedance, the control voltage V_x-V_{ctrl} and V_y-V_{ctrl} are different except at the zero-crossing time, resulting in the difference in the instantaneous capacitance of the two varactors. Such an unbalance generates the even harmonics that flow through the varactors to AC ground, degrading the Q factor and increasing the phase noise at the output.

The same *LC* noise filtering idea can be applied to the control line, leading to an inductive control line technique as shown in Fig. 6.3 (b). The inductance L_3 and capacitor C_3 should be tuned to resonate at the frequency $2\omega_0$. The narrow band *LC*

circuit only suppresses the second-order harmonic and has no effect on low frequency signal. Hence, the *f*- V_{ctrl} characteristic of the VCO is unchanged.

6.2.5 Inductive Degeneration

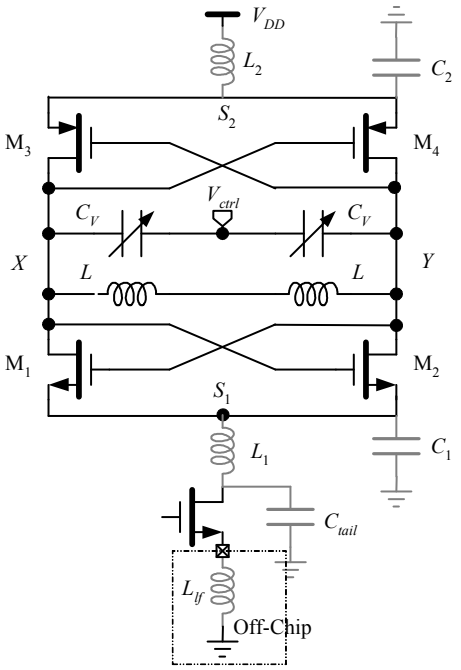


Figure 6.4 Oscillator with *LC* filtering and a degeneration inductor

The noise filtering techniques discussed in the previous sections focus on suppressing the high frequency noise in the tail current source. The low frequency noise, especially the flicker noise, can generate phase noise by the AM-to-PM up-conversion process. A usually used method to reduce the flicker noise is to increase the size of the tail current source device. However, a larger device increases the parasitic capacitance at common node, resulting in a smaller *Q* factor of the resonator.

To remove the low frequency noise in the tail current source, an off-chip large inductor can be added between the source of the tail transistor and the ground as shown

in Fig. 6.4 [81]. If the inductance is large enough, the degeneration inductor shunts the low frequency noise in the tail current source. Hence, the power of the noise current is reduced by the factor $\left|1+jg_m\omega L_{fl}\right|^2$, where g_m is the transconductance of the tail transistor. The technique suppresses the noise in a frequency band that is limited upwards by the parasitic parallel capacitance of the inductor, and downwards by the inductance value (the larger the inductance, the lower the frequency limit). Since the inductor carries no high-frequency signals, the Q factor, self-resonance frequency, package parasitics and PCB layout are uncritical.

6.2.6 Decouple the Common Node by a Capacitor

Flicker noise of the differential pair can be modeled as a low frequency, fluctuating offset voltage $V_{1/f}$ that unbalances the differential pair. It is responsible for the noisy current in the capacitor attached at the common mode node S_1 and S_2 in Fig. 6.4. After commutation, the fluctuation modulates the oscillation frequency and ultimately results in output phase noise. However, the balance may be restored by decoupling the source of differential pair with a capacitor C_{c1} as depicted in Fig. 6.5 [77]. If the value of C_{c1} is properly designed, the voltage across C_{c1} is able to effectively track the unbalance caused by the flicker noise voltage. Hence, the balance is restored and the up-conversion mechanism of the differential pair flicker noise is suppressed. However, the oscillator cannot start up if C_{c1} is too small. On the other hand, if it is too large, the second-order harmonics will be dominant in the oscillator. The C_{c2} in Fig. 6.5 has the same function.

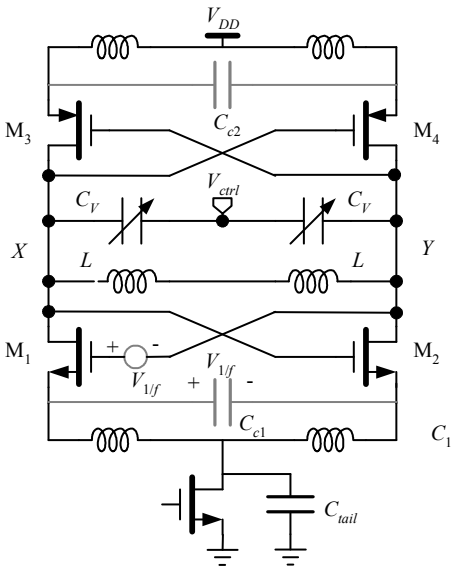


Figure 6.5 *LC* oscillator with the decouple capacitor

6.2.7 Reduce VCO Gain K_v by Switched Capacitors

In *LC* VCOs, the AM noise can be transferred to phase noise by modulating the effective capacitance of the varactors (AM-to-PM up-conversion). Obviously, more phase noise will be generated in this up-conversion process if the VCO has a larger gain K_v, which is determined by the sensitivity of the varactors. To alleviate the phase noise caused by such an up-conversion process, a smaller K_v is usually desirable in the modern VCO design. However, with the given power supply voltage, the smaller K_v leads to the smaller frequency-tuning range.

One way to resolve this conflict is by using the switched capacitor array as shown in Fig. 6.6 (a). In this design, the binary weighted capacitor array is made of Metal-Insulator-Metal (MIM) capacitors (with high Q) that can be selected by the MOSFETs switches. C_v is the varactor that can be tuned in a relatively small range. By

selecting MIM capacitors and tuning C_v, a set of f-V_{trcl} curves with slopes K_{v2} as shown in Fig. 6.6 (b) are obtained. In practical design, two consecutive tuning ranges should have enough overlaps to provide a continuous tuning range covering all desired frequencies. On the other hand, if only single varactor with a large tuning range is used in the oscillator, a higher VCO gain, K_{v1}, is required to cover the same frequency range. Therefore, the VCO with the switched capacitors array can effectively suppress the AM-to-PM up-conversion phase noise.

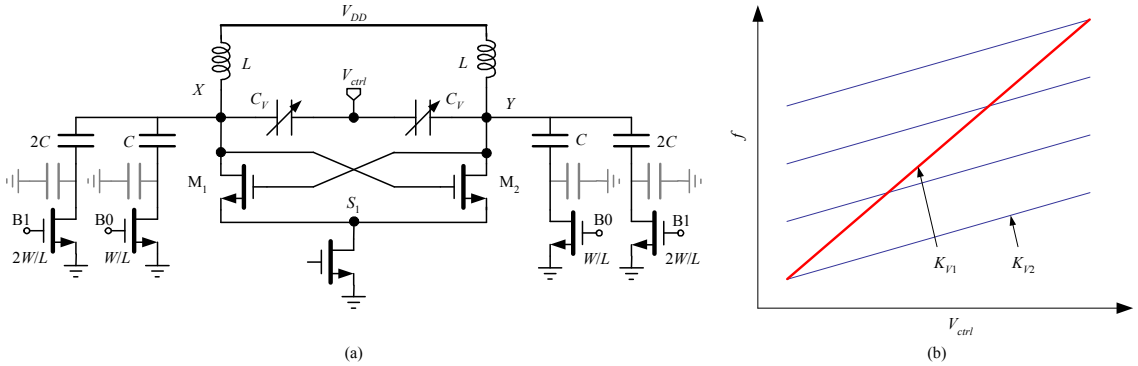


Figure 6.6 *LC* oscillator with switching capacitors (a) and its f-V_{trcl} curves (b)

However, the switch resistance must be sufficiently low to not degrade the Q of capacitors. This implies the MOSFETs must have a large W/L ratio. However, large device size will result in significant parasitic capacitance that reduces the capacitance of the MIM capacitors even when the switches are off. Furthermore, switches also reduce the Q factor of the resonator, degrading the phase noise performance.

6.2.8 Differential Control

The single-end control line commonly used in *LC* VCOs is sensitive to the noise since the even harmonics flowing through the varactor will reduce the Q factor of the

resonator. This shortcoming can be overcome by the differential control widely used in ring oscillators [18]. Such a voltage-controlled capacitor is shown in Fig. 6.7 (a) [82] [83].

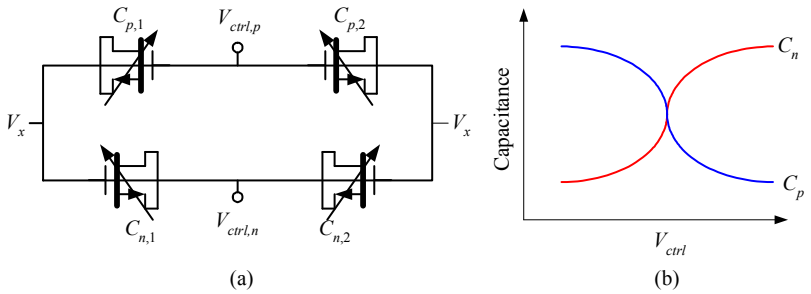


Figure 6.7 Different control structure (a) and C-V_{ctrl} characteristic (b)

In this topology, the anode of $C_{p,1}$ and $C_{p,2}$ ($C_{p,1} = C_{p,2}$) are connected with the positive control voltage $V_{ctrl,p}$ while the cathode of $C_{n,1}$ and $C_{n,2}$ ($C_{n,1} = C_{n,2}$) are connected with the negative control voltage $V_{ctrl,n}$. If the structures of the four varactors are identical, the complementary C-V_{ctrl} characteristic as shown in Fig. 6.7 (b) will be obtained. The instantaneous capacitance for $C_{n,1}$ and $C_{p,1}$ are given by

$$C_{n,1} = C_0 + k_{var,n}\cdot((V_x + V_{cm}) - V_{ctrl,n}), \tag{6.3}$$

$$C_{p,1} = C_0 - k_{var,p}\cdot(V_{ctrl,p} - (V_x + V_{cm})), \tag{6.4}$$

respectively, where C_0 is the capacitance at the zero bias voltage, $k_{var,n}$ and $k_{var,p}$ are the sensitivity coefficients of the varactors, V_{cm} is the common-mode noise voltage in the oscillator. If the $k_{var,n}$ and $k_{var,p}$ are perfectly complementary, $k_{var} = k_{var,n} = k_{var,p}$, the overall instantaneous capacitance $C = C_{n,1} + C_{p,1}$ can be expressed as

$$C = 2C_0 + k_{var}\cdot(V_{ctrl,p} - V_{ctrl,n}). \tag{6.5}$$

This equation shows that the differential control technique effectively suppresses the common mode noise in the *LC* oscillator. Hence, it can reduce the phase noise resulting from flicker noise in the tail current source.

6.3 Summary

The phase noise generation mechanisms were summarized in this chapter. The up-conversion mechanisms resulting from the flicker noise of tail current source and differential pair were analyzed qualitatively. Then, eight phase noise suppression techniques were introduced. By properly applying them, the phase noise caused by the high frequency noise in the tail current source, the flicker noise of the tail current source and differential pair may be removed or significantly reduced, leading to the phase noise performance of the *LC* oscillator approaching its intrinsic minimum value given by (6.1) and (6.2).

CHAPTER 7

LC OSCILLATORS DESIGN OPTIMIZATION

Several phase noise models have been discussed in chapter 5. They provide valuable insights in oscillator design. However, to minimize the phase noise, the circuit designer usually needs a simple procedure to reach the optimized phase noise. In this chapter, a simple physical phase model for the *LC* cross-coupled oscillator is introduced. Based on this model, several closed-form phase noise expressions are derived. These equations lead to a new inductance selection criterion. A new optimization procedure centered on the new inductance selection criterion is then proposed. For both bipolar and CMOS *LC* oscillators, the optimization procedure is visualized. Finally, to verify the effectiveness of the procedure, a bipolar oscillator is designed. The SpectreRF simulation shows the optimization procedure effectively reduces the phase noise generated by oscillators.

7.1 Physical Phase Noise Model

A simple physical phase noise model has been proposed by H. Darabi and A. Abidi [84]. The model is initially used to estimate the phase noise in the mixer circuit, and then it is extended to calculate the phase noise generated in the *LC* oscillators [85]. Using this model, the phase noise can be expressed by the closed-form equations. Therefore, it is very useful for *LC* oscillators design.

7.1.1 Tank Noise

The phase noise generated by the tank parasitic resistance has been derived in the LTI phase noise model discussed in Chapter 5. In that derivation, the tank was considered as a parallel *RLC* circuit with an inductor *L*, a capacitor *C* and a parasitic resistor R_p. In practical *LC* VCO design, the tank circuit is usually implemented by two inductors and two capacitors as depicted in Fig. 7.1. If their values are denoted as *L*/2 and 2*C* respectively and the noise current is evenly separated into two noise sources with spectral density of $4kT \cdot 2g_p$ ($g_p=1/R_p$), that spectral density of the output noise voltage generated by two noise current sources is unchanged, which is

$$\overline{V_{on,gp}^2(\Delta\omega)} = 2kTg_p \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2 \cdot \omega_0^2 L^2 . \tag{7.1}$$

Therefore, for a sine-wave oscillation with the amplitude of V_0, the phase noise resulting from parasitic g_p is

$$L_{gp}(\Delta\omega) = \frac{4kTg_p}{V_0^2} \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2 \cdot \omega_0^2 L^2 . \tag{7.2}$$

In *LC* oscillators, the integrated inductors are implemented by the on-chip spiral inductors. As discussed in Chapter 4, the spiral inductors usually have poor *Q* factors. They limit the *Q* factor of the tank in most of the oscillator designs. Therefore, the inductors' effective parasitic conductance provides a good approximation to g_p. In this case, the effective conductance for each *L*/2 inductor is $2g_p$. This assumption is used in the derivation of this chapter. Note that the capacitors can also deteriorate the tank *Q*

factor especially when switched capacitors are used to increase the frequency tuning range and reduce the gain of VCO (see Chpater VI).

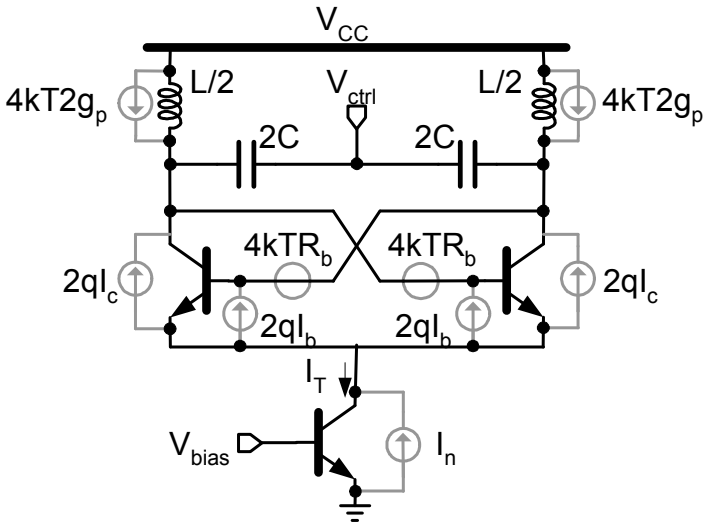


Figure 7.1 A differential bipolar *LC* oscillator with all major noise sources

7.1.2 Active Circuit Noise

The noise generated by the cross-coupled transistors also contributes to the output phase noise and it is the dominant portion in the overall phase noise in most cases. For the *LC* oscillator implemented by bipolar devices, the phase noise comes from the shot noise associated with the collector and base DC current, the thermal noise of the base spreading resistor and the flicker noise of device. In a CMOS *LC* oscillator, the channel thermal noise and the device flicker noise contribute to the oscillator's phase noise. Based on a simple physical phase noise model, several closedd-form equations will be derived to calculate the phase noise resulting from these noise sources. A bipolar *LC* oscillator depicted in Fig. 7.1 will be used as an example.

7.1.2.1 Phase Noise Generated by Base Spreading Resistance R_b

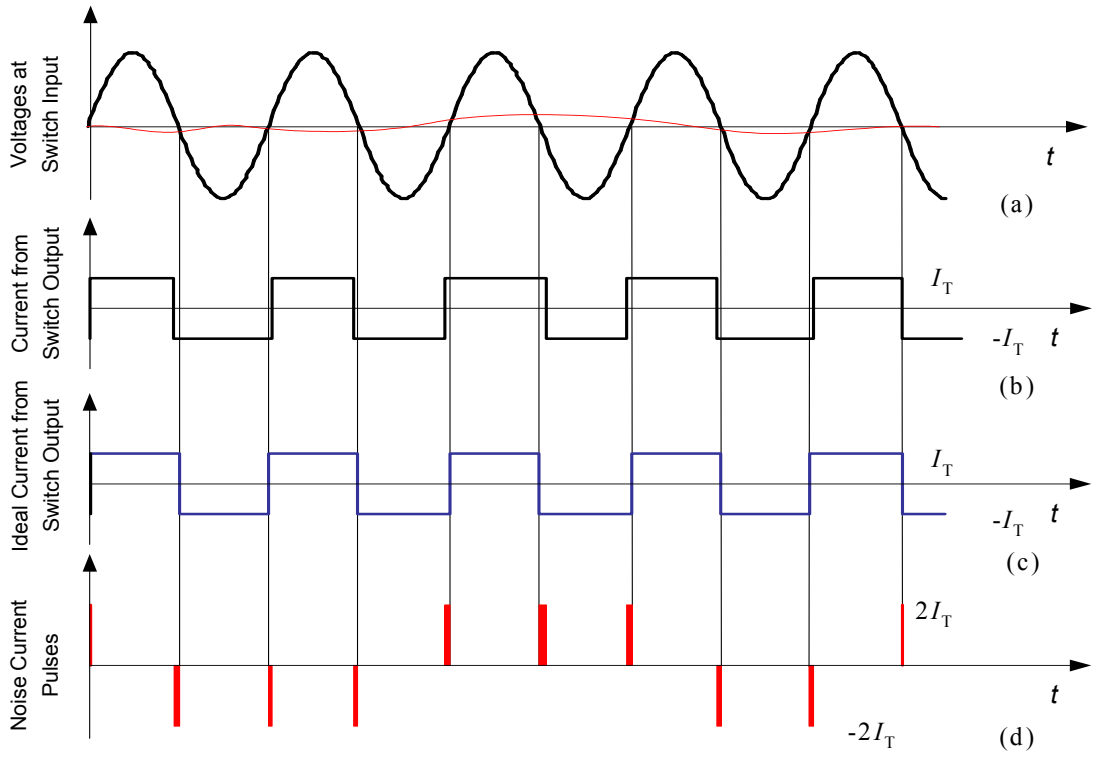


Figure 7.2 Noise at the input of the pair modulates the instants of zero crossing (a) output waveform and noise voltage (b) noise modulated the instants of zero crossing (c) ideal output current and (d) noise current pulses

The noise generated by R_b is modeled as a noise voltage with spectral density of $\overline{V_{n,Rb}^2} = 4kTR_b$ as shown in Fig. 7.1. If the oscillation amplitude is large enough (i.e. greater than 300 mV), during most of the carrier period the cross-coupled transistors are completely switched, with a single transistor of the pair conducting the current delivered by the tail current source. Thus the output current from the pair is ideally a square wave with a period of ω_0. However, as shown in the plot (a) of Fig. 7.2, the noise generated by R_b changes the zero crossing time of the oscillation waveform, making it depart from its ideal timing by a small random amount at each time. Accordingly, the resulting output current is not an

ideal square wave (plot (b)). This output current can be considered as a summation of two currents: (i) an ideal switched current with a period of ω_0 (plot (c)) and (ii) a series of noise current pulses with a rate of $2\omega_0$ (plot (d). Strictly speaking, the noise current pulse is not a period signal but a random signal). Note that the amplitude of the former is I_T (tail current), while the amplitude of the latter is $2I_T$. The width of this noise current pluses depends on not only the voltage of the noise, $\overline{V_{n,Rb}}$, but also the slope of the oscillation waveform, S. Obviously, the pulse width Δt can be expressed as

$$\Delta t = \frac{\overline{V_{n,Rb}}}{S}. \tag{7.3}$$

Note that Δt is a random variable. If the noise voltage is much smaller compared with the oscillation waveform, Δt is much smaller compared to the period of the oscillation, T. Therefore, the width modulated current pulse can be treated as an amplitude modulated current pulse with a constant pulse width as shown in Fig. 7.3. The new amplitude modulated pulse has an accurate frequency of $2\omega_0$, a constant pulse width of T_s and a random height of $\frac{2I_T}{S}\cdot\frac{\overline{V_{n,Rb}}}{T_s}$ modulated by noise voltage. For this periodic current pulse, the spectral density of the average noise current, $\overline{i_n^2}$, in one cycle is

$$\overline{i_n^2} = \frac{2}{T}\cdot\left[\frac{2I_T V_{n,Rb}}{ST_s}\right]^2\cdot T_s = \frac{2}{T}\cdot\frac{4I_T^2}{S^2}\cdot\frac{1}{T_s}\overline{V_{n,Rb}^2}. \tag{7.4}$$

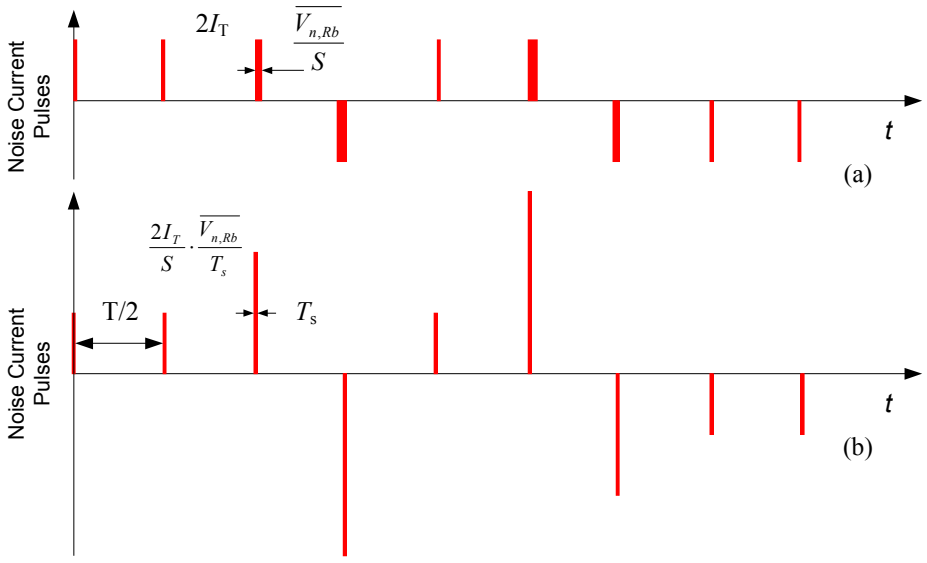


Figure 7.3 Approximate the pulse width modulated noise current by amplitude-modulated noise current

Assume the input voltage of the pair is changed ΔV in the duration of T_s, the output current of the pair will be switched from $-I_T$ to I_T at the same time. Therefore, the slope, S, is $\Delta V / T_s$ and the transconductance of the pair, G_m, is $2I_T/\Delta V$. Accordingly, the pulse width of the amplitude modulated current pulse, T_s, is given by

$$T_s = \frac{2I_T}{S \cdot G_m}. \tag{7.5}$$

Substituting (7.5) into (7.4), the noise current can be expressed as

$$\overline{i_n^2} = \frac{2}{T} \cdot \frac{2I_T \cdot G_m}{S} \cdot \overline{V_{n,Rb}^2}. \tag{7.6}$$

With the sine-wave oscillation amplitude of V_0, S can be expressed as $V_0 \cdot \omega_0$ at zero crossing time. The noise voltage and pair conductance are $\overline{V_{n,Rb}^2} = 4kTR_b$ and $G_m =$

$g_m/2 = I_c/(2\cdot V_T) = I_T/(4\cdot V_T)$, respectively. Substituting them into (7.6), the noise current is given by

$$\overline{i_n^2} = \frac{2qR_bI_T^2}{\pi \cdot V_0}, \tag{7.7}$$

where q is the charge of the electron. The spectral density of the output noise voltage at the small offset $\Delta\omega$ can be calculated by multiplying $\overline{i_n^2}$ by the square of the tank impedance at $\omega_0 \pm \Delta\omega$. Note that for the tank circuit in Fig. 7.1, the impedance is

$$Z_{noise,Rp}^2(\Delta\omega) = \left[\frac{1}{2j}\cdot\sqrt{\frac{L/2}{2C}}\cdot\frac{\omega_0}{\Delta\omega}\right]^2. \tag{7.8}$$

Hence the spectral density of output noise is given by

$$\overline{V_{on,Rb}^2(\Delta\omega)} = \frac{qR_bI_T^2}{2\pi V_0}\left(\frac{\omega_o}{2\Delta\omega}\right)^2\omega_0^2L^2. \tag{7.9}$$

Two spreading resistors will generate the same noise in the output, but only half of the noise is phase noise. Therefore, the phase noise generated by the base spreading resistance of the *LC* oscillator can be expressed as

$$L_{Rb}(\Delta\omega) = \frac{qR_bI_T^2}{\pi V_0^3}\left(\frac{\omega_o}{2\Delta\omega}\right)^2\omega_0^2L^2. \tag{7.10}$$

7.1.2.2 Phase Noise Generated by Shot Noise of the Collector DC Current

The shot noise associated with collector DC current is modeled as a noise current in Fig. 7.1. This noise current can be transformed to the input of the pair as a noise voltage. The equivalent noise voltage satisfies the relation $\overline{V_n^2} = \overline{I_n^2}/G_m^2$ [18]. Note that a linear approximation is used in this case. According to this approximation,

the $\overline{V_{n,Rb}^2}$ in (7.6) can be replaced by $2qI_C / G_m^2$. By applying the same procedure, the closed-form expression for the phase noise generated by the shot noise associated with I_c is given by

$$L_{Ic}(\Delta\omega) = \frac{4kTI_T}{\pi V_0^3} \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2 \cdot \omega_0^2 L^2 . \tag{7.11}$$

Note that the noise generated by the two transistors is considered here.

7.1.2.3 Phase Noise Generated by Other Noise Sources

The shot noise associated with the base DC current, modeled as $2qI_b$ in Fig. 7.1, can usually be neglected because it is much smaller than the collector current. By applying the techniques introduced in Chapter 6, the phase noise contributed by the differential pair flicker noise, the white noise in the tail current source and the flicker noise in the tail current source are assumed to be effectively suppressed. In other words, this study focuses on the phase noise limitation resulting from the white noise from the devices and the tank parasitic resistance in *LC* oscillators. Note that this is the minimum phase noise according to Samori's phase noise model.

7.1.3 Oscillation Amplitude

When the *LC* oscillator oscillates at ω_0, the reactance of the tank is zero. Therefore, the switched square wave output current only "sees" the resistant of R_p in the tank. The resulting output oscillation would be a square wave too. However, the tank is a narrow band circuit and all harmonics will be filtered out, resulting in a sine wave output.

For a square wave voltage signal with the amplitude of $I_T \cdot R_p$ and frequency ω_0, its Fourier expansion is:

$$V(t) = \frac{4}{\pi} I_T R_p \sin(\omega_0 t) + \frac{4}{\pi \cdot 3} I_T R_p \sin(3\omega_0 t) + \frac{4}{\pi \cdot 5} I_T R_p \sin(5\omega_0 t) + \cdots . \quad (7.12)$$

If all harmonics are completely removed, the oscillation amplitude will be $4 \cdot I_T \cdot R_p / \pi$. The conclusion is also true for the complementary topology, in which both *N*-type and *P*-type transistors are used. For the *LC* oscillator in Fig. 7.1, the amplitude is

$$V_0 = 2 \cdot I_T \cdot R_p / \pi . \quad (7.13)$$

Substituting it into (7.2), (7.10) and (7.11), the closed-form equations that estimate the phase noise resulting from $2kTg_p$, $4kTR_b$, $2qI_c$ are given by

$$L_{gp}(\Delta\omega) = \frac{\pi^2 kTg_p^3}{I_T^2} \cdot \left(\frac{\omega_0}{2\Delta\omega} \right)^2 \cdot \omega_0^2 L^2 , \quad (7.14)$$

$$L_{Rb}(\Delta\omega) = \frac{\pi^2 qR_b g_p^3}{4I_T} \cdot \left(\frac{\omega_0}{2\Delta\omega} \right)^2 \cdot \omega_0^2 L^2 , \quad (7.15)$$

$$L_{Ic}(\Delta\omega) = \frac{\pi^2 kTg_p^3}{2I_T^2} \cdot \left(\frac{\omega_0}{2\Delta\omega} \right)^2 \cdot \omega_0^2 L^2 , \quad (7.16)$$

respectively. Note that equation (7.13) is valid only if the oscillator works in the so-called "current limit" region [79]. In this region, the oscillation amplitude increases with the increase of the tail current. Hence, the phase noise is reduced according to (7.14), (7.15) and (7.16). However, the power supply or other effects limit the maximum amplitude in every practical oscillator. For example, the maximum amplitude of the bipolar *LC* oscillator in Fig. 7.1 is set by the varactors' maximum forward bias voltage (i.e. less than 600mV usually). In CMOS *LC* oscillators, the upper bound is usually

given by the power supply. After the oscillation amplitude reaches its maximum value, a further increase in the tail current cannot increase the amplitude. On the contrary, it increases the noise generated in the active devices and thus deteriorates the phase noise performance.

7.1.4 Model Validation – a 100 MHz Oscillator

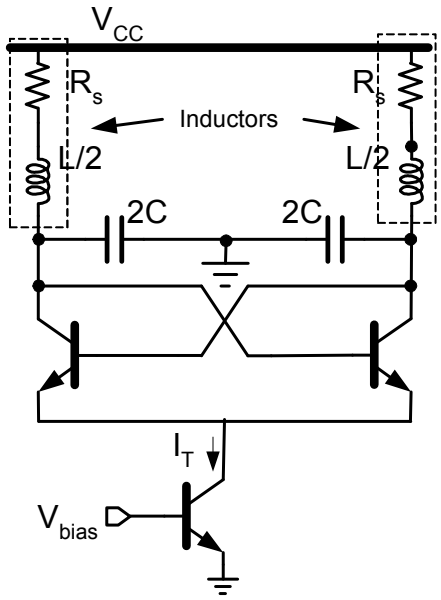


Figure 7.4 An 100MHz bipolar *LC* oscillator

To demonstrate the effectiveness of the model, a 100 MHz *LC* oscillator is designed and simulated by ADS. For simplicity, the inductor is modeled by an ideal inductor in series with a resistor as shown in Fig. 7.4. The Q factor of the inductor is fixed at 5 to make a fair comparison. Accordingly, the series resistance is changed to keep the Q constant. The parasitic conductance of the tank, g_p, is calculated by $g_p=1/(2\cdot Q^2\cdot R_s)$ [18], where R_s is the series resistance of $L/2$. In order to oscillate at about 100MHz, the capacitance of the tank is tuned accordingly too (The actual oscillation

frequency may have a small error relative to 100MHz). The tail current is I_T=2.94 mA and V_{CC}=3 V. The base spreading resistor for this transistor is R_b=57 Ω. The phase noise is measured at Δf=100 kHz.

The results listed in Table 7.1 show that the simulation and the model calculation are consistent for both the oscillation amplitude and phase noise. The maximum error between the simulated and calculated amplitude is only 4%. The maximum phase noise error is only about 1.8dB. So, the simple, physical phase noise model can be used to estimate the phase noise generated by *LC* oscillators.

Table 7.1 Comparison of oscillation amplitude and phase noise obtained by simulation and theoretical calculation

$L/2$ (nH)	20	30	40	50
R_s (Ω)	2.52	3.77	5.03	6.28
$2C$ (pF)	125	84	63	51
Simulated f_0 (MHz)	97.8	97.3	97.2	96.5
Theoretical f_0 (MHz)	100.7	100.3	100.3	99.7
Simulated V_0 (mV)	221	335	448	554
Theoretical V_0 (mV)	236	353	471	588
Simulated phase noise from g_p (dBc/Hz)	-123.2	-125.0	-126.3	-127.2
Theoretical phase noise from g_p (dBc/Hz)	-124.7	-126.5	-127.8	-128.9
Simulated phase noise from R_b (dBc/Hz)	-121.8	-123.8	-125.2	-126.2
Theoretical phase noise from R_b (dBc/Hz)	-122.6	-124.4	-125.7	-126.7
Simulated phase noise from I_c (dBc/Hz)	-126.2	-128.0	-129.2	-130.1
Theoretical phase noise from I_c (dBc/Hz)	-127.7	-129.5	-130.8	-131.9

7.2 A New Inductance Selection Criterion

The spiral inductor design is critical to *LC* oscillator performance. Generally speaking, a higher *Q* spiral inductor will decrease the bandwidth of the tank and filter

more noise out, resulting in a lower overall phase noise. As discussed in Chapter 4, however, the maximum Q value is essentially limited by the process technology. From the designer's standpoint, an optimization procedure is more important under such a Q limitation.

The spiral inductors are the largest components in most LC oscillators. Therefore, their area usually needs to be limited in a practical design. In the following discussion, the area of the spiral inductors is assumed to be constant to make a fair comparison between oscillators. The inductance selection criterion as well as the optimization procedure in LC oscillator design is based on this constraint.

Depending on the geometry layout, the inductance of the area-fixed spiral inductors still varies a lot. As shown in [86], the inductance selection has great effect on the phase noise performance. Although, the maximum inductance is set by the parasitic capacitance, choosing an optimum inductance in terms to achieve the best phase noise performance is still unsolved and need to be studied carefully.

The closed-form equations (7.14), (7.15) and (7.16) show that the phase noise for the given ω_0 and $\Delta\omega$ satisfies

$$L_{Rb}(\Delta\omega) \propto \frac{g_p^3 L^2}{I_{tail}}, \tag{7.17}$$

$$L_{Ic}(\Delta\omega), L_{gp}(\Delta\omega) \propto \frac{g_p^3 L^2}{I_{tail}^2}. \tag{7.18}$$

These two expressions prove the well-known trade-off between the phase noise and the power dissipation if the oscillator works in the current-limit region. More

important, they provide a value design insight – the phase noise is proportional to the product of L^2 and g_p^3. Therefore, a minimum product of L^2 and g_p^3 in the spiral inductor design will minimize the phase noise for a given tail current.

Usually, g_p is approximately equal to the equivalent parallel conductance of a spiral inductor, g_L, due to the poor Q of spiral inductors. To model the spiral inductor, the equivalent π circuit (Fig. 4.9) is commonly used. If one of two nodes of the π circuit is ac grounded, g_p is given by

$$g_p \approx g_L = \frac{\omega^2 R_{si} C_{ox}^2}{1+\omega^2 R_{si}^2 (C_{ox}+C_{si})^2} + \frac{R_s}{\omega^2 L_s^2}. \tag{7.19}$$

The ADS Momentum tool and the model parameter extraction method discussed in Chapter 4 are used to model typical on-chip spiral inductors. As one of the design constraints, the area of the square inductor is fixed at 400 μm×400 μm. The structure of the chip is illustrated in Fig 4.11 and the conductivity of the metal layer and substrate are identical to those values of the example in Chapter 4. The inductor is expected to work at the frequency of 900 MHz. Because the metal layer is relatively thin, the parasitic capacitance between the metal lines is negligible in this design. Therefore, a minimum metal line spacing, 2μm, is chosen for all the spiral inductors studied. In addition, the underpass is neglected too. Several sets of the spiral inductors with the metal line width from 25μm to 55μm are simulated. The g_L is calculated using (7.19) by the π model parameters extracted from the simulated Y parameters. The results are shown in Fig. 7.5 and 7.6.

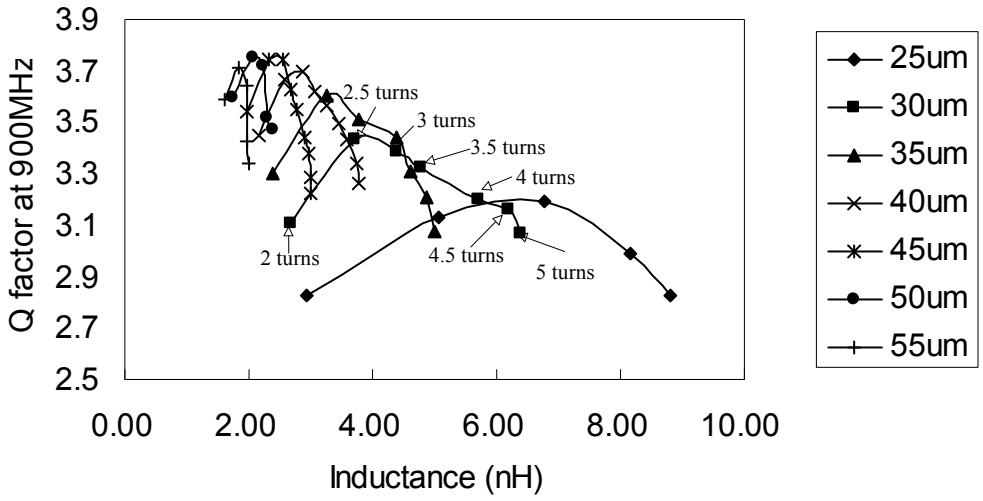


Figure 7.5 The *Q* factors of spiral inductors for $s = 2$ μm and various conductor widths, *w*, versus inductance

Fig. 7.5 plots the *Q* factors of the simulated inductors. Each curve in this figure corresponds to a series of layouts with the given metal width but with a different number of turns. For example, seven *Q* values of the 30μm metal line width inductors are plotted with the number of turns from 2 to 5 as shown in this figure. With the increase in the number of turns, the inductance increases accordingly. Also, the *Q* factor increases with the number of turns when the inductance is small. However, this trend is reversed when the inductance becomes large. Hence, there exists a maximum *Q* factor for each set of the inductors. For example, the maximum *Q* factor of the 30μm inductors is 3.436 with the number of turns equal to 2.5. This conclusion is reasonable because increasing the metal line length near the center by increasing the number of turns has little effect in increasing the inductance but it does increase the parasitic series resistance of the inductor. Therefore, the *Q* factor deteriorates. This figure also shows

that the processing technology limitation on the maximum Q factor. In this case, the maximum Q factor is about 3.8 for this 400 μm×400 μm inductor at 900 MHz.

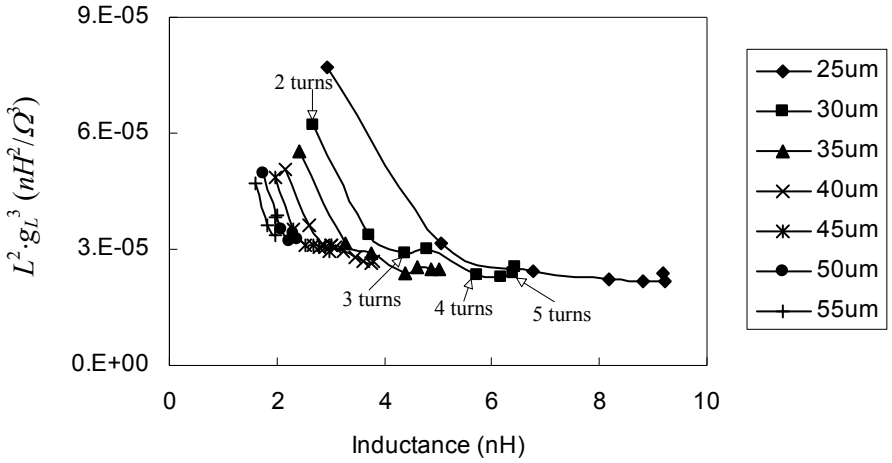


Figure 7.6 $L^2 \cdot g_L^3$ factor for s = 2 μm and various conductor widths, w, versus inductance

Similar plots are obtained for the factor $L^2 \cdot g_L^3$ of each inductor as depicted in Fig. 7.6. This factor decreases with the increase of inductance. However, it increases for a large number of turns, suggesting that a minimum value for $L^2 \cdot g_L^3$ exists for each set of the inductors. Note that the optimum points for the Q factor and the $L^2 \cdot g_L^3$ factor may occur at a different number of turns. For example, the smallest $L^2 \cdot g_L^3$ factor (2.26×10^{-23} H^2/Ω^3) for the 30μm inductors corresponds to 4.5 turns, while the largest Q factor is corresponds to a 2.5 turns inductor.

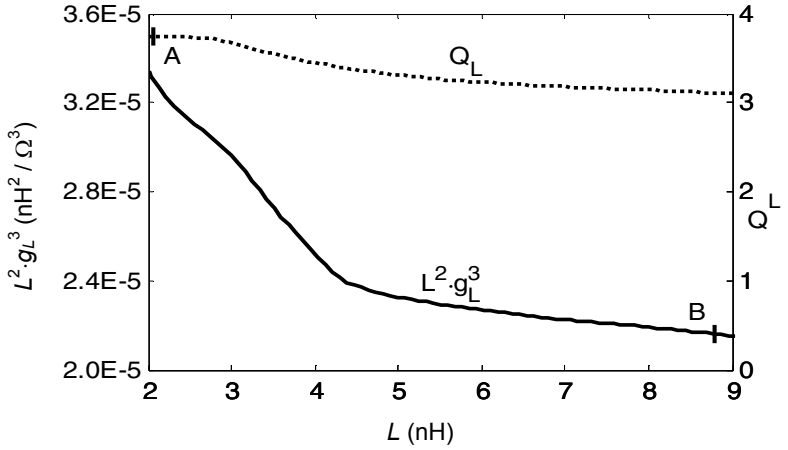


Figure 7.7 Simulated minimum $L^2 \cdot g_L^3$ and maximum Q_L versus the inductance L for an area-limited square spiral inductor

Figure 7.7 is obtained from the optimum Q_L and $L^2 \cdot g_L^3$ factor shown in Fig. 7.5 and 7.6 (An interpolation technique is used to smooth the data). The variation of the maximum Q_L is small for an area-fixed spiral inductor. The similar conclusion has been arrived in [86]. Another very important conclusion is that the minimum $L^2 \cdot g_L^3$ factor that an area-fixed inductor can reach monotonically decreases with the increase of the inductance. According to (7.17) and (7.18), it suggests that a large inductance spiral inductor is useful to reduce the phase noise generated in the *LC* oscillators.

The advantage of the spiral inductor with larger inductance is straightforward. Assuming $g_p \approx g_L$ is valid, decreasing g_L (or correspondingly, increasing R_p) will boost the oscillation amplitude according to (7.13). According to Fig. 7.7, the maximum Q_L has little variation in a relatively large inductance range, suggesting that $R_p \propto R_{dc}$ since $R_p \approx Q_L^2 R_{dc}$ for Q_L>3. So, the relation $g_p^3 \cdot L^2 \propto L^2 / R_{dc}^3$ is approximately valid. For an area-limited spiral inductor, the inductance increase is obtained by increasing the line

length (narrow lines and/or more turns). Although inductance increase causes the phase noise to deteriorate proportionally to L^2, the overall phase noise is improved because of the increase proportion to $R_{dc}^{\ 3}$ at the same time. Therefore, although a maximum Q_L inductor achieves the most effective noise attenuation, boosting the carrier power by increasing inductance results in more benefit in phase noise performance for an *LC* oscillator designed with area-limited spiral inductors. Note that the conclusion is only valid when the *LC* oscillators work in the "current-limited" region.

According to the previous analysis, a novel inductance selection criterion – choosing a large inductor value to minimize the $L^2 \cdot g_L^3$ factor – should be used in the *LC* oscillator design to reach the best phase noise performance. Note that this is opposite to the conclusion reported in [86], in which the author suggests a smaller inductance leads to a better phase noise performance.

7.3 Phase Noise Optimization Procedure

7.3.1 Design Constraints

There are several design constraints in practical *LC* VCO design and they are summarized in [86]. Similar design constraints are followed in the proposed optimization procedure.

First, the maximum power constraint is imposed in the form of the maximum tail current drawn from a given supply voltage, i.e.

$$I_T \le I_{max}. \tag{7.20}$$

Second, the tuning range specification should be satisfied. It leads to

$$LC_{\min} \le \frac{1}{\omega_{\max}^2}, \tag{7.21}$$

$$LC_{\max} \le \frac{1}{\omega_{\min}^2}, \tag{7.22}$$

where ω_{min} and ω_{max} are the minimum and maximum frequency the oscillator should reach.

Third, the oscillator should be able to start up properly. It requires

$$G_m \ge \alpha \cdot g_{tank}, \tag{7.23}$$

where α is greater than 1, usually set to 2~3 to guarantee startup.

Finally, the area occupied by spiral inductor should be fixed. The optimization procedure is also based on two assumptions:

(i) The spiral inductor dominates the Q factor of the tank. Hence, $g_{tank}=g_p \approx g_L$ always holds;

(ii) The noise generated from the tail current source has been effectively removed by the techniques such as the noise filtering as introduced in Chapter 6. In addition, there is no noise coupled into the oscillator from the power supply, the control line of varactors and the substrate.

Based on these design constraints and assumptions, the optimization procedure for the bipolar and CMOS *LC* VCO are presented in the following sections.

7.3.2 Optimization Procedure for Bipolar LC VCOs

The topology in Fig. 7.1 is used as the example of the bipolar *LC* VCOs. If the oscillator works at 900MHz with 10% tuning range, f_{max} is (1+0.05)×900MHz=945MHz

and f_{min} is (1–0.05)×900 MHz=855 MHz. The transistor size in the bipolar technology cannot be chosen arbitrarily. Therefore, if the differential pair transistors are selected, the parasitic capacitance at the output node contributed by the transistors' parasitic capacitance is a relatively constant value. Assuming this capacitance is 2pF, two curves can be obtained in the C_v-L plane according to (7.21) and (7.22) as depicted in Fig. 7.8, where C_v is the capacitance of varactors. In terms of the tuning range specification, the feasible design region is the area between these two curves. According to the new inductance selection criterion, the best phase noise performance comes from selecting inductance as large as possible (the value close to point A in Fig. 7.8) if the chip area constraint of the spiral inductor is imposed. Of course, a certain inductance margin should be reserved to obtain a robust design. Also, the tuning range of the varactor capacitance should not be too small to avoid a very large gain of the VCO, which usually results in the large phase noise coupled into the oscillator from the control lines in practical design.

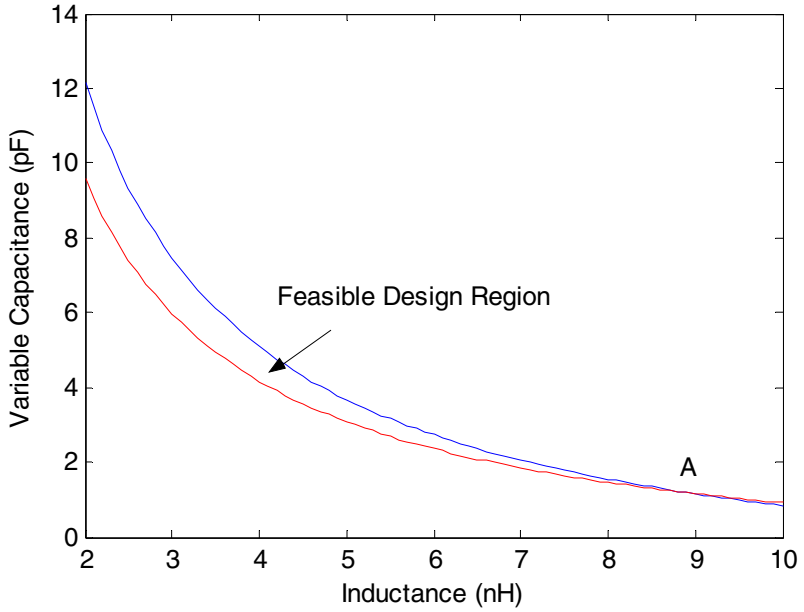


Figure 7.8 Varactor capacitance versus inductance for a given tuning range requirement

The other constraints will be applied to the bipolar *LC* VCO too. As pointed out by (7.17) and (7.18), a large bias current results in a better optimum phase noise. Therefore the I_T should always be set to its maximum allowed value. Hence, the design constraint is tight and the I_{max} should be chosen as I_T.

Regarding the startup constraint, a small g_{tank} is useful to oscillation startup according to (7.23). Since g_{tank} is approximated by g_L of the spiral inductors, the g_L versus L of the spiral inductor is calculated by (7.19) and plotted in Fig. 7.9. The figure clearly suggests that a larger inductance also corresponds to a smaller g_L. Hence, if a larger inductance is selected, it is easier start the oscillation. In other words, if the maximum allowed inductance cannot start up the oscillation, the G_m should be

increased, i.e. increasing I_{max} for this *LC* VCO. Hence, the power constraint has to be re-considered to make the oscillator design possible.

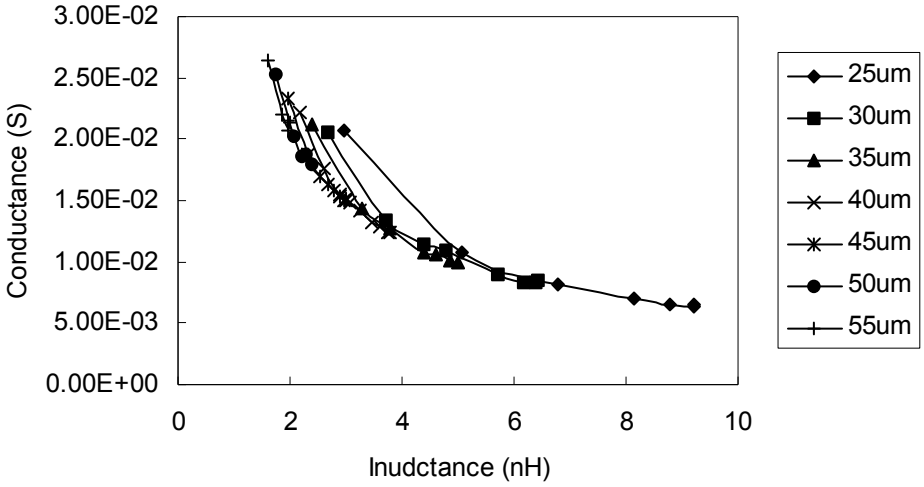


Figure 7.9 g_L for s = 2 μm and various conductor widths, w, versus inductance of the area-fixed spiral inductors

There also exists another possibility – the amplitude is too large so that the oscillator enters the voltage-limited region. For the bipolar *LC* VCO, the maximum amplitude is usually limited by the *bc* junction of the coupled transistors, since forward biasing the *bc* junction will significantly deteriorate the phase noise performance. The capacitive and inductive coupling topologies shown in Fig. 7.10 can be applied to overcome this problem. If the amplitude is still too large after applying them (for example, the amplitude is limited by the varactors or the next stage requirements), I_T should be reduced to decrease the amplitude.

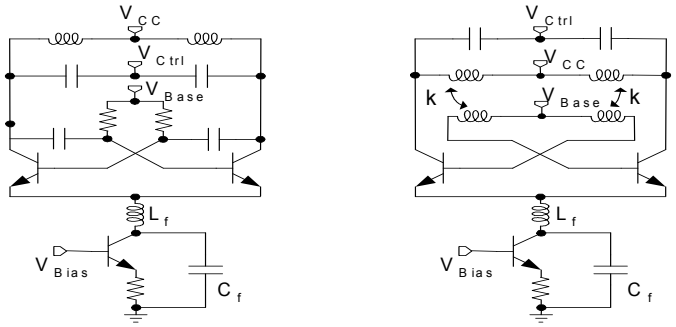


Figure 7.10 Capacitive coupling (left) and inductive coupling (right) *LC* oscillators

According to the previous analysis, an optimization procedure for bipolar *LC* VCOs under the design constraints is summarized as the follows:

(i) use the maximum I_T obtained from power dissipation specification.

(ii) choose the largest inductance permitted according to the tuning region specification, varactor characteristics and design margin requirement.

(iii) find the optimum layout for this inductance in terms of minimizing the $L^2 \cdot g_L^3$ factor. The method to find the optimum layout will be discussed in section 7.3.4.

(iv) from the I_T and the g_L of the inductor, estimate the oscillation amplitude. If the amplitude is so large that the *bc* junction of differential pair is at risk of being forward biased, use the capacitive and inductive coupling *LC* oscillators.

(v) if the amplitude is still too large, reduce the I_T to reduce the amplitude until the requirement is satisfied.

Finally, it is noteworthy that the optimization procedure may only lead to a near-optimum design. The simulation always needs to be performed to reach the refined optimum design.

7.3.3 Optimization Procedure for CMOS LC VCOs

The transistors size in the CMOS *LC* VCOs is adjustable. The *W*/*L* ratio of the device is closely related to some important parameters such as the transconductance of the differential pair and parasitic capacitance. Hence, it must be taken into account in the optimization procedure.

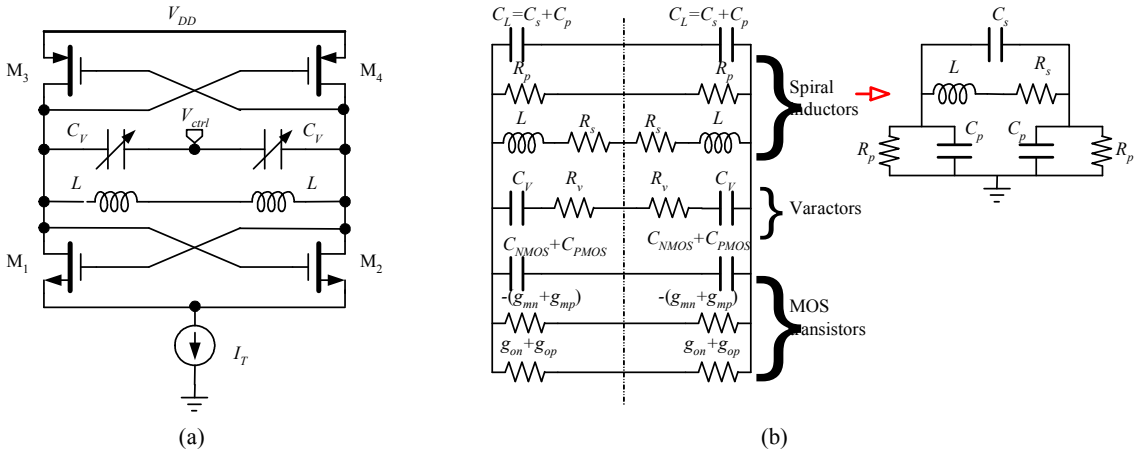


Figure 7.11 (a) A CMOS *LC* oscillator and (b) its equivalent model

Fig. 7.11(a) shows a complementary CMOS *LC* VCO and its equivalent model. This topology will be chosen to design a 2.4GHz oscillator with 15% tuning range and optimized phase noise performance. The on-chip spiral inductors are modeled by a seven element π model, and it is equivalent to the parallel *RLC* circuit in the oscillator model with $C_L=C_s+C_p$ (Fig. 7.11(b)). The varactors are modeled as a series *RC* circuit where R_v describes the loss of the varactors. C_{NMOS} and C_{PMOS} are the total parasitic capacitance of the NMOS and PMOS transistors, respectively. g_m and g_o are small signal transconductance and output conductance of the transistors, respectively. Although their values actually vary with the operating point of the transistors during the oscillation, the

values of g_m and g_o when the voltage across the *LC* tank is zero will be used in order to facilitate the analytical expressions in the design optimization. Note that g_m is negative to compensate the energy loss in the oscillator. From the above equivalent model, the following expressions can be obtained

$$2g_{tank} = g_{on} + g_{op} + g_v + g_L, \tag{7.24}$$

$$2g_{active} = g_{mn} + g_{mp}, \tag{7.25}$$

$$L_{tank} = 2L, \tag{7.26}$$

$$2C_{tank} = C_{NMOS} + C_{PMOS} + C_L + C_v, \tag{7.27}$$

where g_{tank}, $-g_{active}$, L_{tank} and C_{tank} are the tank loss, effective negative conductance, tank inductance and tank capacitance, respectively. In (7.24), g_v is the effective parallel conductance of the varactors. It is given by

$$g_v = \frac{C_v\omega}{Q_v} = \frac{C_v\omega}{1/(\omega C_v R_v)}. \tag{7.28}$$

The varactor implemented by the MOS transistor usually has a much larger *Q* factor compared with the *Q* of the spiral inductor. Q_v = 20 is used in this design example. g_L in (7.24) is the effective parallel conductance of the spiral inductor, it can be computed by

$$g_L = 1/R_p + R_s/(L\omega)^2. \tag{7.29}$$

The minimum g_L as a function of the inductance for an area-limited spiral inductor is plotted in Fig. 7.12 (data obtained from [86]). The corresponding minimum $L^2 \cdot g_L^3$ factor is plotted at the same figure. Both of them decrease with the increase of inductance.

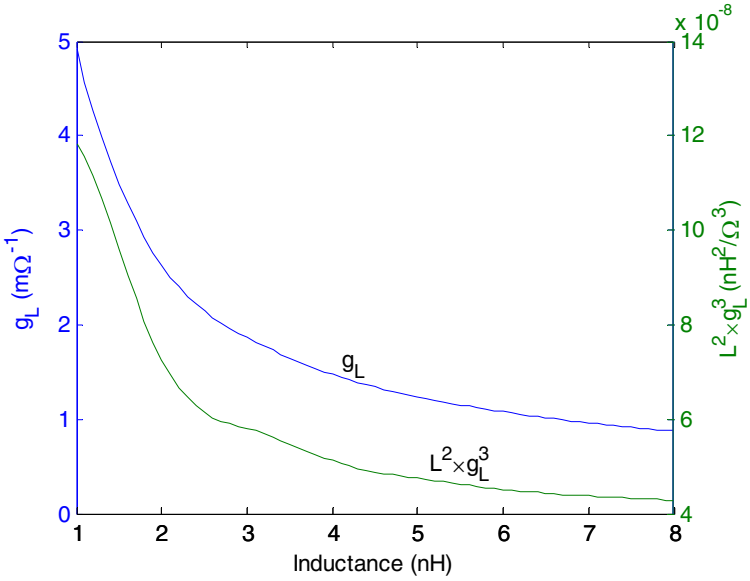


Figure 7.12 g_L and $L^2 \cdot g_L^3$ as a function of inductance for a spiral inductor used in the CMOS *LC* VCO

In equation (7.27), C_{NMOS} and C_{PMOS} are given by

$$C_{NMOS} = C_{gs,n} + C_{db,n} + 4C_{gd,n}, \tag{7.30}$$

$$C_{PMOS} = C_{gs,p} + C_{db,p} + 4C_{gd,p}, \tag{7.31}$$

respectively, where the factor 4 is due to the Miller effect. C_L in (7.27) is the total capacitance of the spiral inductor given by C_s+C_p. It is approximated by a constant capacitance 200fF in this design example. Regarding to the MOS varactor C_v, the ratio $C_{v,max}/C_{v,min}$ is nearly a constant that is primarily determined by the underlying physics of the capacitors (i.e. the process). Hence, $\beta = C_{v,max}/C_{v,min} = 2$ is used in this design. g_{mn} and g_{mp} in (7.25) are set to equal. As pointed out in [63], such a symmetrical arrangement is helpful to suppress the close-in phase noise. Finally, the channel length L_n and L_p are set to the minimum allowed by the process technology to reduce the parasitic capacitance

and achieve the highest transconductance. In this TSMC 0.25μm technology, this minimum value is 300nm.

The same design constraints listed in section 7.3.1 are imposed on this CMOS *LC* VCO. Similar to the bipolar *LC* VCO design, the optimization procedure is visualized by Fig. 7.13 and 7.14. As mentioned previously, the power consumption constraint is tight and I_T should be set to maximum current allowed. If the inductor design is left to the next section, the only two variables in the design are the width of NMOS transistor, W_n, and the capacitance of varactor, C_v. All other parameters appearing in (7.24) to (7.31) can be obtained from W_n and C_v. Therefore, the *x*-axis and *y*-axis in Fig. 7.13 and 7.14 are W_n and C_v, respectively.

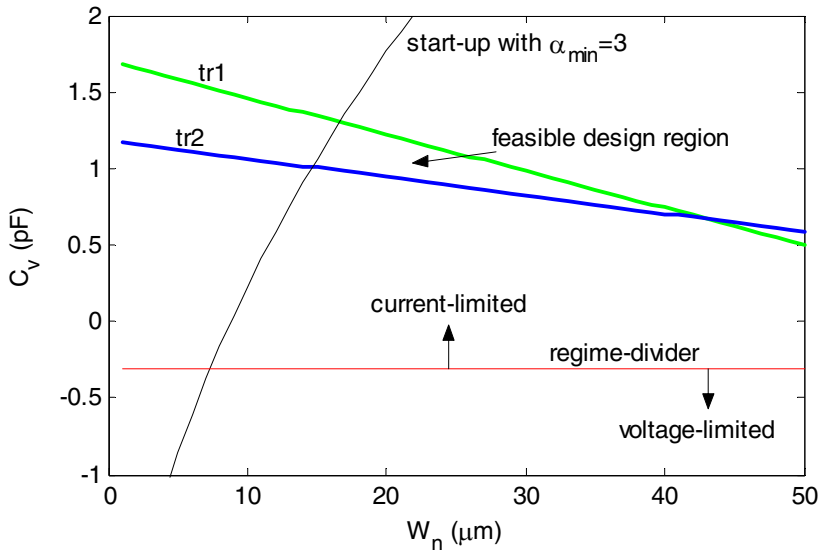


Figure 7.13 Feasible design region of the CMOS *LC* VCO

For a given *L*, (7.21) can be written as

$$2L \cdot \frac{C_{PMOS} + C_{NMOS} + C_L + C_v}{2} \le \frac{1}{\omega_{\max}^2}. \tag{7.32}$$

This inequality leads to

$$C_v \le \frac{1}{L\omega_{\max}^2} - C_{PMOS} - C_{NMOS} - C_L . \tag{7.33}$$

In (7.22), C_{max} is obtained by setting $C_{v,max}=\beta C_{v,min.}$. Hence it leads to s similar inequality as follows

$$C_v \ge \frac{1}{\beta}\left(\frac{1}{L\omega_{\max}^2} - C_{PMOS} - C_{NMOS} - C_L \right). \tag{7.34}$$

If the equal signs are chosen in (7.33) and (7.34), the curves *tr1* and *tr2* will be obtained as shown in Fig. 7.13 respectively. In this example, the L is chosen as 2nH and β and C_L is set to 2 and 200fF respectively as mentioned before. C_{NMOS} and C_{PMOS} (including C_{gs}, C_{db} and C_{gd}) are approximated by the well-known expressions [18]. If a point lies between the *tr1* and *tr2* curves in the C_v-W_n plane, it will satisfy the tuning range constraint.

The start-up constraint corresponds to the following expression

$$g_{mn} + g_{mp} = 2g_{mn} \ge \alpha\cdot(g_{on} + g_{op} + g_v + g_L). \tag{7.35}$$

To guarantee start-up, the minimum α_{min} is chosen as 3. g_m and g_o can be easily calculated according to the device size and the tail current, which is the maximum allowed current (3mA in this case). From (7.35), g_v can be solved. Then, using (7.28), the corresponding C_v curve as shown in Fig. 7.13 is obtained. If a point is located at the right of the curve, the corresponding α will be greater than 3 and the start-up constraint is satisfied. Therefore, the feasible design region is formed by the curves of *tr1*, *tr2* and start-up curve as depicted in Fig. 7.13.

Finally, the oscillator should work in the current-limited region in order to avoid wasting energy. In this region, the amplitude linearly grows with the tail current according to $V=I_T/g_{tank}$. The voltage supply for this oscillator is 2.5V. Thus, V_{max} is 2.5V and g_{tank} should be less than 4mA/2.5V=1.6mΩ^{-1}. Combing (7.24) and (7.28), the regime-divider curve can be plotted. The area below this curve is the voltage-limited region in which the energy is wasted. The feasible design region should be always kept above this curve. Otherwise, the tail current should be reduced. Obviously, the feasible design region in Fig. 7.13 satisfies this requirement if L=2nH.

As pointed out before, the larger the inductor value, the better the phase noise performance if the inductor layout is properly designed. Hence, the inductance is increased to 3nH in the oscillator design and the *tr1*, *tr2*, start-up and regime-divider curves are plotted in Fig. 7.14 (the dotted curves). It can be concluded that both the region formed by *tr1* and tr2 and the start-up curve are moved to the left according to this figure. However, an important finding is that the former is shifted faster than the latter. It suggests that the feasible design region will shrink into a point with the increase of the inductance, which corresponds to the optimum C_v-W_n pair. At the same time, the inductance reaches the maximum inductance. From Fig. 7.12, the minimum $L^2 \cdot g_L^3$ factor can be reached with the proper layout design. Therefore, the VCO with this inductance for its tank circuit will have the best phase noise performance according to the phase noise model.

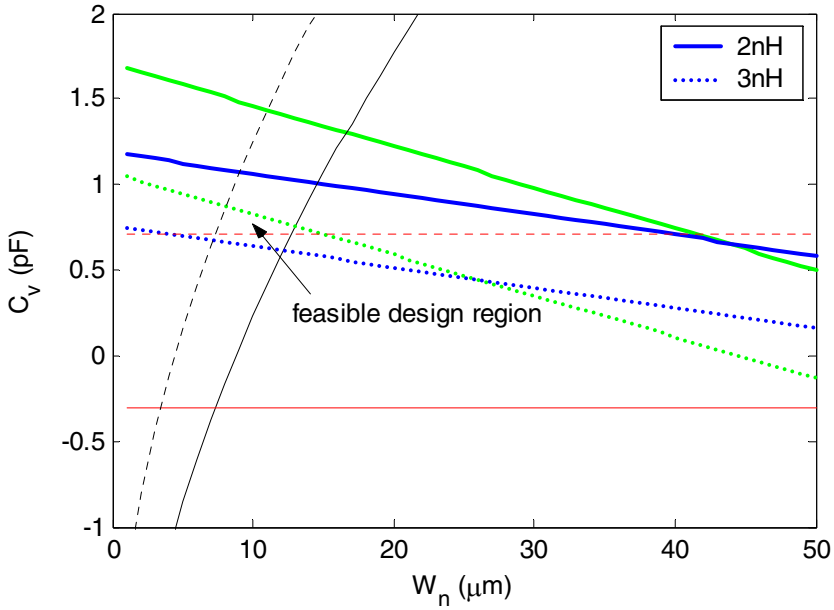


Figure 7.14 Feasible design region is shrunk by increasing the inductance

The effect of the regime-divider curve has to be considered too. As shown in the same figure, the curve is moved up when inductance increases and it crosses the feasible region formed by *tr1*, *tr2* and start-up curves. Hence, the feasible design region without energy waste is further shrunk. If the curve lies above the feasible region formed by *tr1*, *tr2* and start-up curves, the tail current has to be reduced.

The design optimization procedure for CMOS *LC* VCO can be summarized as follows. Set the tail current to the maximum current allowed by the power consumption specification. Pick an initial guess for the inductance value and obtain feasible design region on the C_v-W_n plane as shown in Fig. 7.13. If there are more than one feasible design points, increase the inductance and repeat until the feasible design area shrinks to a single point. The point corresponds to the optimum devices size and varactor capacitance. It also provides the optimum inductance value. If the point lies in the

voltage-limited region, the tail current should be reduced until the regime-divider line passes through the single feasible design point to avoid wasting power. In the end, the optimum inductor layout will be developed, which will be discussed in detail in the next section. Note that a certain design margin is always needed and thus the feasible design region may not be shrunk to a single point in a practical, robust circuit.

7.3.4 Spiral Inductor Layout Optimization

The best phase noise performance requires using the spiral inductors with the maximum permitted inductance. After the inductance value is obtained from the optimization procedures, an optimum layout that leads to the minimum $L^2 \cdot g_L^3$ factor needs to be found. The simulation tools such as ADS and ASITIC are helpful in finding the optimum spiral layout. However, they can only obtain the near-optimum layout and are usually time-consuming. An algorithm called geometric programming is very efficient in solving this inductor synthesis problem [87].

7.3.4.1 The Geometric Programming Problem

Let f be a real-valued function of n real, positive variables x_1, x_2, …, x_n. The polynomial function has the form

$$f(x_1, \cdots, x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}}, \tag{7.36}$$

where $c_j \geq 0$ and $\alpha_{ij} \in \mathbb{R}$. If $t = 1$, f is called a monomial function.

A geometric programming problem has the standard form

minimize $f_0(x)$

subject to $f_i(x) \leq 1$, $i = 1, 2, \ldots, m$,

$$g_i(x) = 1,\ i = 1, 2, \ldots, p,$$

$$x_i > 0,\ i = 1, 2, \ldots, n, \tag{7.37}$$

where f_i are polynomial functions and g_i are monomial functions.

If the spiral inductor optimization can be transformed to the geometric programming problem, it is changed to a pure mathematical problem. Hence, many classical algorithms, such as the interior-point method, can be applied to find the global optimum solution with great efficiency.

7.3.4.2 Polynomial Expressions for the π Model Parameters

For a spiral inductor, its geometry can be characterize by the number of turns n, the metal line width w, the turn spacing s, the outer diameter d_{out} and the average diameter $d_{avg} = 0.5(d_{out} + d_{in})$. These five variables are not independent, but it will be convenient to consider this as a redundant set of variables. Also, the number of turns, n, is restricted to take values that are integer multiplies of 0.25, and w and s are usually integers limited by the process technology. However, these constraints are ignored in the optimization algorithm and the final layout is then obtained via rounding to the nearest number. Such an approximation will cause no significant error.

The π model is used to describe the spiral inductor. As demonstrated in Chapter 4, this model is accurate as long as the assumption of a lumped model is valid (inductive region). In addition, the π model parameters are also computed according to the expressions given in that chapter. However, some of them are too complicated to be used in the optimization algorithm. The π model parameters will be expressed by the simple, approximate polynomial or monomial functions of the layout variables.

For the inductance L_s, Mohan's data-fitting model [51] will be used, which is

$$L_s = \gamma d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}. \tag{7.38}$$

The series resistance R_s, given by (4.6), is a monomial expression

$$R_s = \frac{l}{\sigma w \delta (1 - e^{-t/\delta})} = k_1 l / w. \tag{7.39}$$

The spiral-substrate oxide capacitance, C_{ox}, usually accounts for most of the inductor's parasitic capacitance. It can be approximated by a monomial expression according to (4.9)

$$C_{ox} = (\varepsilon_{ox} lw)/(2t_{ox}) = k_2 lw. \tag{7.40}$$

From (4.8), the series capacitance C_s can be written as a monomial expression

$$C_s = (\varepsilon_{ox} nw^2)/(t_{ox,M1\text{-}M2}) = k_3 nw^2. \tag{7.41}$$

The substrate capacitance C_{si} can be expressed as the following monomial expression according to (4.17)

$$C_{si} = (C_{sub} lw)/2 = k_4 lw. \tag{7.42}$$

The substrate resistance R_{si} is also given by a monomial expression according to (4.13)

$$R_{si} = 2/(G_{sub} lw) = k_5/(lw). \tag{7.43}$$

The nine element π model can be transformed to the seven elements π model as shown in Fig. 7.11. In this equivalent model, the shunt resistance R_p and shunt capacitance C_p are given by

$$R_p = \frac{1 + [\omega R_{si}(C_{si} + C_{ox})]^2}{\omega^2 R_{si} C_{ox}^2} = k_6/(lw), \tag{7.44}$$

$$C_p = \frac{C_{ox} + \omega^2 R_{si}(C_{si} + C_{ox})C_{si}C_{ox}}{1 + [\omega R_{si}(C_{si} + C_{ox})]^2} = k_7 lw + k_8 (lw)^2, \tag{7.45}$$

respectively. Note that the constant k_1 to k_8 are dependent on the technology and frequency. Therefore, for the given technology and center frequency, after all the constants (γ, α_1 to α_5 and k_1 to k_8) are obtained, the optimum layout can be quickly achieved using geometric programming. For example, the typical design problem for *LC* oscillators design can be written as [87]

$$\begin{aligned} &\textit{minimize} && L^2 \cdot g_L^{\ 3} \\ &\textit{subject to} && L(C_s + C_p + C_{v,\min}) \le 1/\omega_{\max}^2 \\ & && (r-1)(C_s + C_p / C_{v,\max} + rC_{\min} / C_{v,\max} \le 1 \\ & && C_{v,min} \ge C_{v,max}/\beta \end{aligned} \tag{7.46}$$

where the constraints come from the frequency tuning range and varactor tuning range specifications.

7.4 Validate the Optimization Procedure by Two Bipolar LC VCO

Two 900MHz bipolar *LC* oscillators are designed to validate the optimization procedure. The tail current and inductor area are limited to 5 mA and 400 μm × 400 μm, respectively. Since only the phase noise will be compared, the frequency tuning range specification is ignored here. According to the widely accepted inductor selection criterion, the inductor layout that leads to the maximum achievable *Q* is chosen in one of the oscillator design. This maximum *Q* spiral inductor corresponds a 2.25 turns, 50 μm line width spiral inductor with the highest Q_L = 3.752 at 900MHz. The inductance is L_{dc} = 2.07 nH. It corresponds to point *A* in Fig. 7.7. The second inductor is 8.80 nH

inductor corresponding to point B in the same figure. It is a 5.5 turns, 25 μm line width inductor with the minimum $L^2 \cdot g_L^3 = 2.16 \times 10^{-5}$ nH^2/Ω^3. The π model parameters for these two inductors are listed in Table 7.2. Note that Q_L (= 2.827) of the second inductor is less than the maximum achievable Q_L for this inductance.

Table 7.2 Parameters of two spiral inductors

Parameters	1st inductor	2nd inductor	Parameters	1st inductor	2nd inductor
L (nH)	2.07	8.80	R_{si} (Ω)	162	87
R_s (Ω)	2.46	10.9	C_{si} (fF)	35	65
C_s (fF)	228	140	$Q_{L\ @\ 900\ MHz}$	3.752	2.827
C_{ox} (fF)	841	985	g_L (mΩ^{-1})	20.20	6.53

The estimated amplitude of the 8.80 nH oscillator is about 1 V. Therefore, the capacitive coupling topology (Fig. 7.10 left) is employed for both oscillators. For V_{CC}=3V, V_{Base} = 2V is chosen to avoid the forward biasing *bc* junctions of devices. The oscillation frequency is tuned to 900 MHz for both circuits by setting 2*C* to 12.5 pF and 1.65 pF, respectively. It is worth pointing out that the coupling capacitor (2 pF for both oscillators) should be large enough for proper start-up. Finally, to focus on the phase noise generated by the intrinsic noise sources, a noise filtering circuit (Fig. 7.10) is added to attenuate the phase noise from tail current source (L_f = 2nH and C_f = 2pF). SpectreRF was utilized to simulate the phase noise of the oscillators. The simulation result (Fig. 7.15) shows that the optimization procedure centered on the new inductance selection criterion results in a more than 3.6dB phase noise improvement.

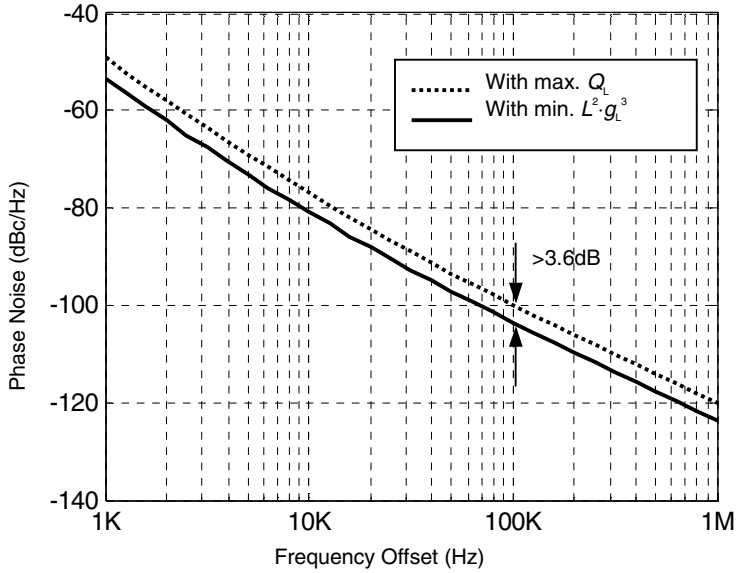


Figure 7.15 Simulated phase noise of two *LC* oscillators using spiral inductors with maximum Q_L and minimum $L^2 \cdot g_L^3$

7.5 Summary

A simple physical phase noise model was presented in this chapter. Based on this model, several closed-form equations were derived to describe the phase noise generated in the *LC* oscillators. The equations indicate that the phase noise is proportional to $L^2 \cdot g_L^3$ factor. For an area-limited spiral inductor, the minimum $L^2 \cdot g_L^3$ factor is found to be decreased with increasing inductance. This conclusion leads to a new inductance selection criterion in *LC* oscillator design, which is to minimize the $L^2 \cdot g_L^3$ by choosing the inductance as large as possible. Centered on the new inductance selection criterion, an optimization procedures for both bipolar and CMOS *LC* VCO design under several widely used design constraints was proposed. Finally, the optimization procedure was validated by two oscillators utilizing the two inductors with

the maximum quality factor and minimum $L^2 \cdot g_L^3$ factor. The simulation result illustrates the phase noise was effectively reduced in oscillators designed by the optimization procedure.

CHAPTER 8

LAYOUT AND MEASUREMENTS

The layout and measurement result of three oscillators are presented in this chapter. All circuits were fabricated by National Semiconductor's Dielectric Isolated Bipolar Junction Transistor (DIBJT) process. The first oscillator is based on the active inductor topology discussed in Chapter 3. The second and third oscillators are low-phase-phase noise *LC* oscillators working at the 900MHz band. Two oscillators have the same capacitive feedback topology as depicted in Fig. 7.10. The difference is that they use different fixed-area spiral inductors. The first *LC* oscillator uses an inductor obtained by the optimization procedure presented in Chapter 7 while the second oscillator applies an inductor with the maximum *Q* factor at 900 MHz. Accordingly, the capacitance of varactors are different for these two designs.

8.1 Active Inductor Based Oscillator

8.1.1 Schematic and Layout

The core of the oscillator is based on the active inductor topology shown in Fig 3.13. The completed schematic is illustrated in Fig 8.1. The active inductor is single-ended consisting of $Q_1 - Q_3$. No additional capacitor is used in the oscillator to achieve the maximum oscillation frequency. According to the analysis in Chapter 3, this topology can oscillate directly due to the negative resistance if biased properly.

Transistors Q_4-Q_{13} are the self-bias circuit which provides the DC current to the core [88]. The transistors Q_{10}-Q_{13} consist the start-up circuit for the bias circuit. In order to tune the oscillator frequency, the bias current of the active inductor should be able to be changed. In this design, the bias current for Q_3 is controlled by the simple current mirror formed by Q_{14}-Q_{15} and resistor R_4. The port QCTRL is connected with a DC voltage source to bias Q_2 at the active region. Finally, V_{CC} is set to 3V.

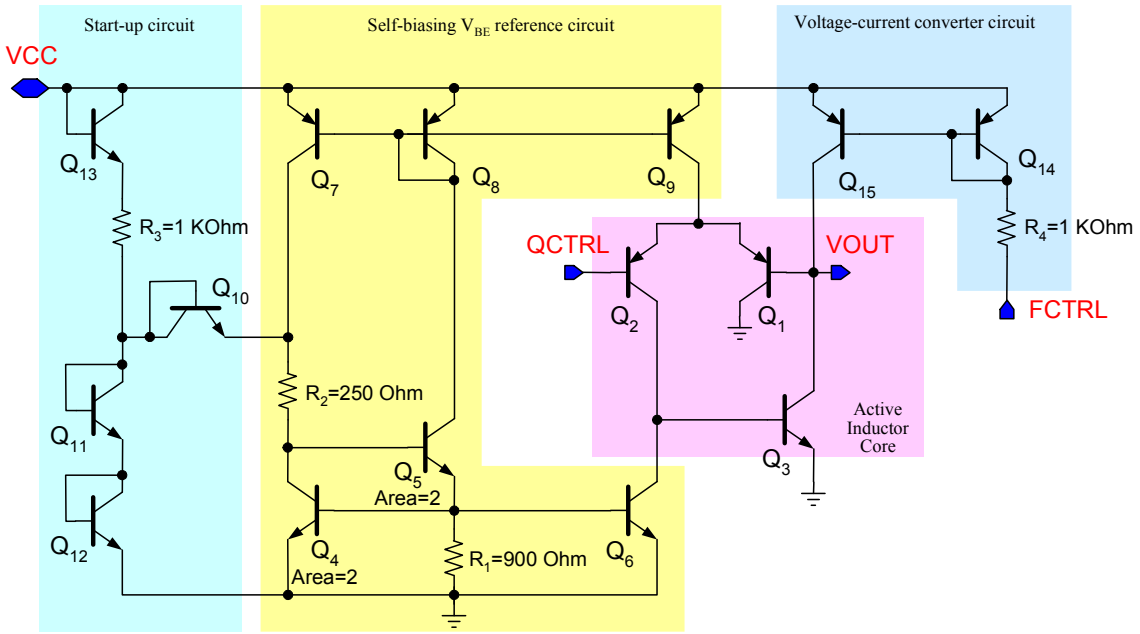


Figure 8.1 Schematic of the active inductor based oscillator

The layout of the oscillator is shown in Fig. 8.2. The overall layout is very compact since there are no passive inductors. The whole oscillator circuit (without pads) only occupies 150μm×100μm chip area.

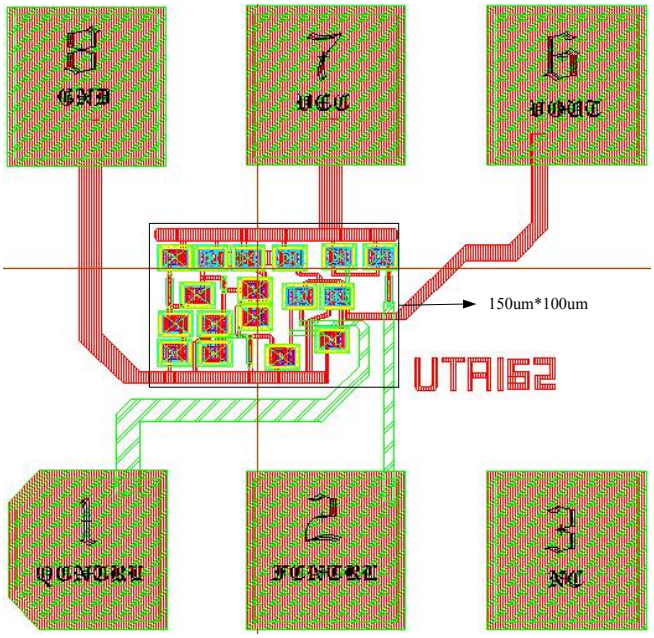


Figure 8.2 Layout of the oscillator based on the active inductor [108]

8.1.2 Matching Circuit and Print Circuit Board Design

The diagram of the measurement setup is illustrated in Fig. 8.3. Because there is no buffer stage in the VCO, the matching circuit is required in order to drive the 50 Ω load of the spectrum analyzer. A *L*-matching circuit is utilized for this purpose [89]. Although the matching circuit only consists of *L* and *C* in Fig. 8.4 (a), parasitics from the bonding wire, pad, discrete components, and board are considered. For example, the parasitic of the discrete inductor and capacitor are modeled according their data sheets [90] [91]. The inductance of bonding wire is modeled by a 3nH inductor (L_b) while the pad parasitic capacitance is approximated by a 100 fF capacitor (C_p). The parasitic capacitances of metal lines on board are modeled by C_1 and C_2, respectively. The small

signal simulation shows this circuit has a center frequency around 1.5GHz (Fig. 8.4 (b)), which is close to the VCO oscillation frequency [108].

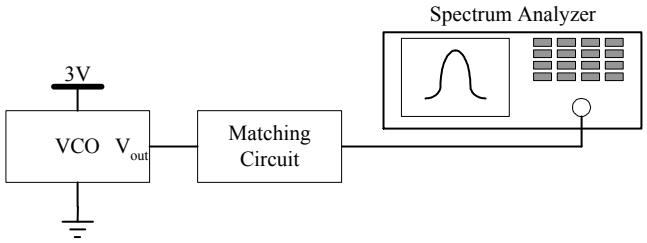


Figure 8.3 Measurement setup for active inductor based oscillator

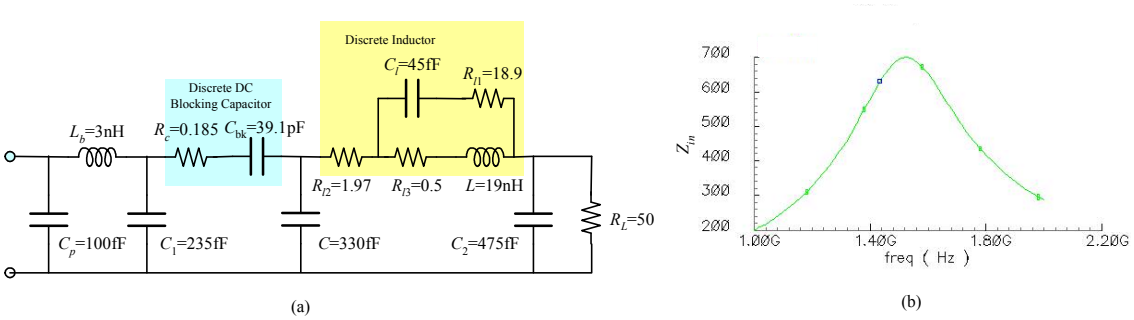


Figure 8.4 Matching circuit and its input impedance

8.1.3 Measurement Results

Figure 8.5 shows the testing structure. The fabricated chip uses the Dual In-line Package (DIP) and is mounted on the reverse side of the printed circuit board (PCB). The major specifications of the oscillator are listed in Table 8.1. The measured and simulated oscillation frequencies as a function of the control voltage are plotted in Fig 8.6 (a). Note that the measured oscillation frequency is much lower compared with the simulated data. This difference is primarily caused by the DIP, which has relatively poor performance at high frequency. Also, the parasitic in PCB design has significant

effects on the oscillation frequency due to the lack of a buffer stage. Finally, the transistor parasitic capacitance was not extracted in the design phase because of a malfunction in the post-layout simulation. Although the oscillation frequency between the simulation and measurement is different, the tuning range in both cases is very close to each other (4.3% in measurement and 3.6% in simulation).

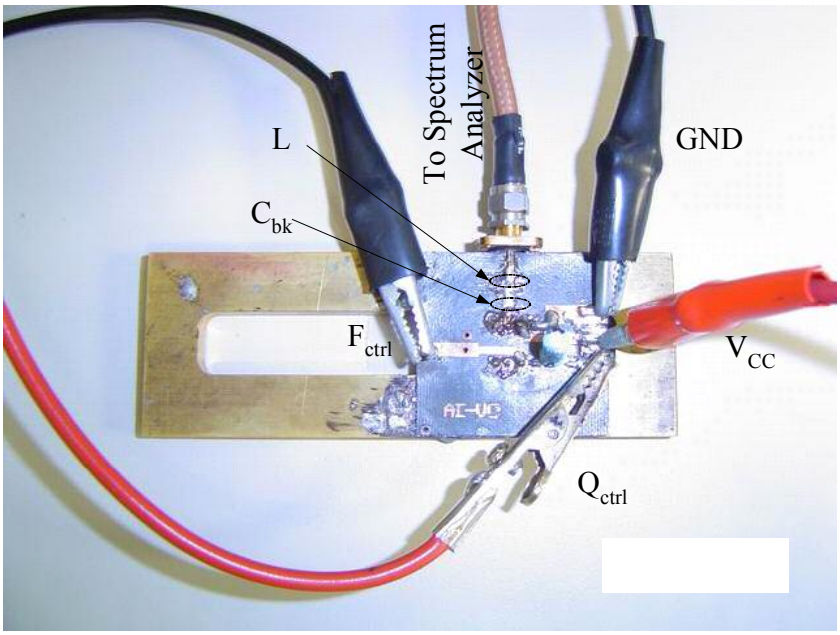
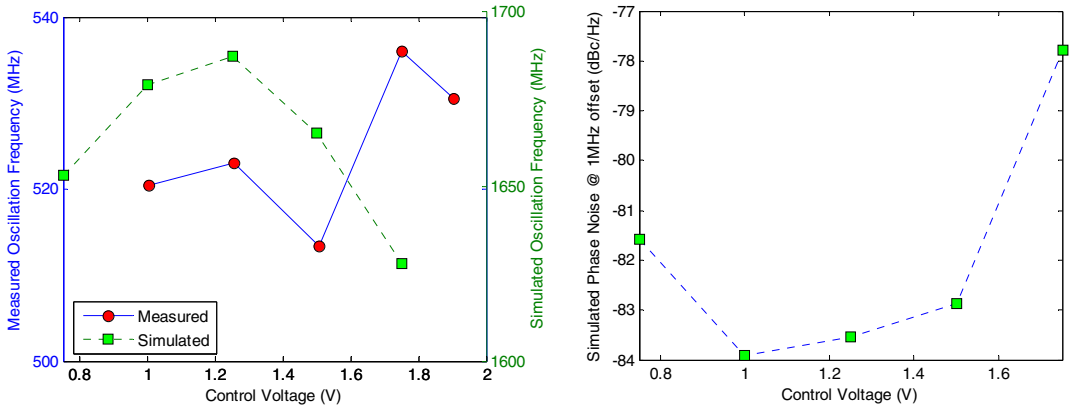


Figure 8.5 Photo of the testing structure for the active inductor based VCO

Table 8.1 Specifications of the active inductor based oscillator

Supply voltage	3 V
Current	4.4 mA
Center frequency	524.7 MHz
Tuning range	513.3 MHz ~ 536.0 MHz (4.3%)
Phase noise (simulated, Fctrl=1V)	-83.92 dBc/Hz @ 1 MHz



(a) (b)

Figure 8.6 Oscillation frequency (a) and simulated phase noise (b) as a function of the control voltage

The spectrum analyzer used in this measurement cannot measure the phase noise. The simulated phase noise is plotted in Fig 8.6 (b). As expected, the minimum phase noise at 1 MHz offset in the tuning range is only about –84 dBc/Hz. Hence, the active inductor based oscillator may not be used to those applications where the noise requirement is stringent.

8.2 Two 900MHz LC Oscillators

8.2.1 Schematic and Layout

The design of the *LC* oscillators obeys the constraints presented in Chapter 7. The tail current should be less than 5 mA and the spiral inductor area is fixed at 400μm×400μm. Since only the phase noise performance is of interest, the tuning range constraint is neglected here. The varactor's *Q* factor is assumed much better than the spiral inductor's and the noise generated from the bias circuit is suppressed.

The completed schematics of the two oscillators are depicted in Fig. 8.7. To avoid forward biasing the *bc* junction of Q_1 and Q_2, the VCO core is implemented by the capacitive feedback *LC* oscillator topology in Fig. 7.10. The feedback capacitors C_{fb1} and C_{fb2} are chosen to be 1.7 pF, which is large enough to guarantee oscillation start-up. The base bias voltage of Q_1 and Q_2 is provided by the external voltage source V_b=2V and R_{b1}=R_{b2}=3KΩ. The inductors L_1 and L_2 in the first design are 5.5 turns, 8.8nH inductors with the minimum $L^2g_L^3$ factor, while they are 2.25 turns, 2.07 nH inductors with the maximum Q factor (Q=3.75) at 900 MHz in the second oscillator. The corresponding π models are obtained by extracting parameters from an ADS Momentum simulation result and are shown in Fig. 8.8 (a) and (b), respectively.

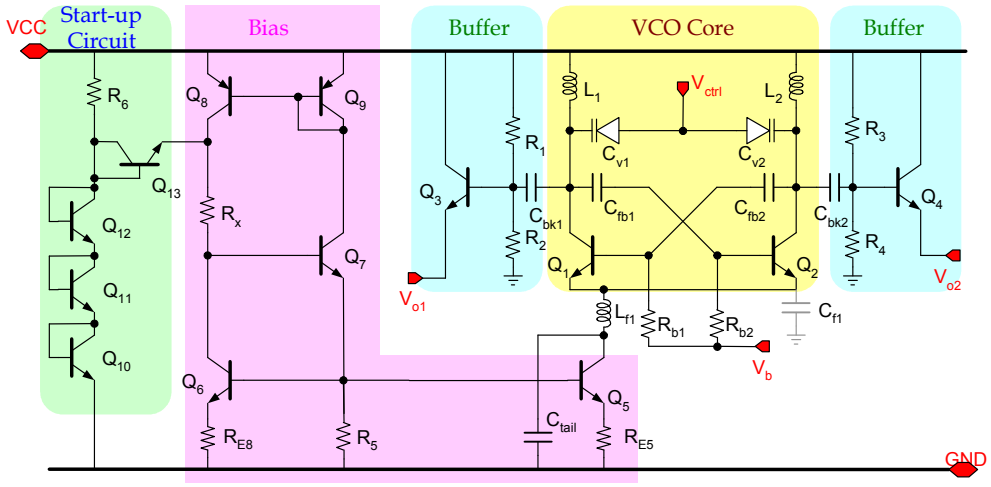


Figure 8.7 Overall schematic of the capacitive coupled *LC* oscillator

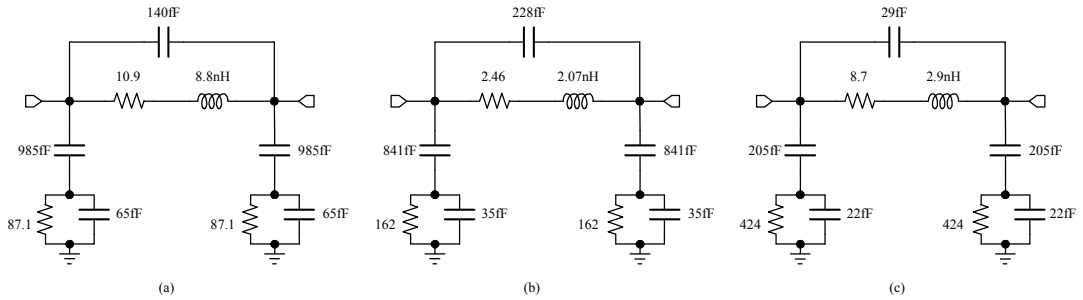


Figure 8.8 π models of the three spiral inductors (a) 8.8nH (b) 2.07nH and (c) 2.8nH

The varactors are realized by the *bc* junction of the NPN device. The simulation shows that their minimum *Q* factor (measured at zero bias voltage) is greater than 19 at 900 MHz. Hence, the assumption regarding the *Q* factor is valid. By inserting a noise filtering circuit, which consists of C_{f1}, L_{f1} and C_{tail}, the noise from the tail current source is effectively reduced. Therefore, the other assumption is also valid. L_{f1} in the two oscillators is realized by the same 2.8 nH, 5 turns inductor with 175 μm×175 μm chip area. Its π model is shown in Fig. 8.8 (c). C_{tail} is a 2.8 pF capacitor which bypasses the high frequency noise from the tail current source. In order to drive the 50 Ω load, emitter follower buffer stages are added to the differential output of the oscillator core. C_{bk1} and C_{bk2} are 350 fF capacitors used for DC blocking. R_1 to R_4 are used to provide the base bias voltage for the emitter followers (R_1=R_3=10 kΩ and R_2=R_4=7 kΩ). Finally, the similar self-biasing circuit with the start-up circuit is designed.

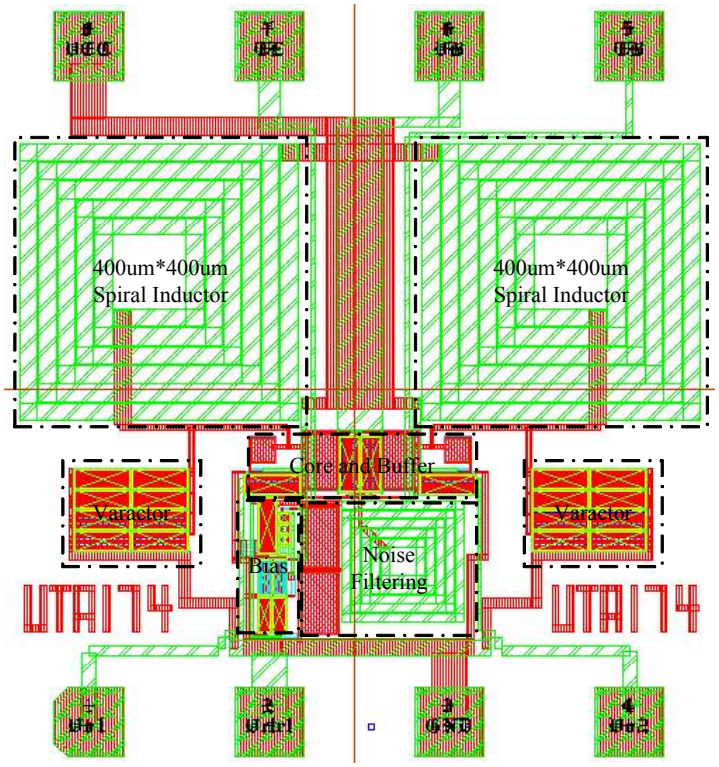


Figure 8.9 Layout of the oscillator with 8.8nH inductor [108]

The layouts of two oscillators are shown in Fig. 8.9 and 8.10, respectively. Both layouts occupy 1020 μm×1000 μm chip area. Note that larger capacitance is required in the second oscillator due to the smaller inductance in the tank. Therefore, two 6.8pF fixed capacitors are paralleled with the varactors in order to save the chip area as depicted C_{fix} in Fig. 8.10.

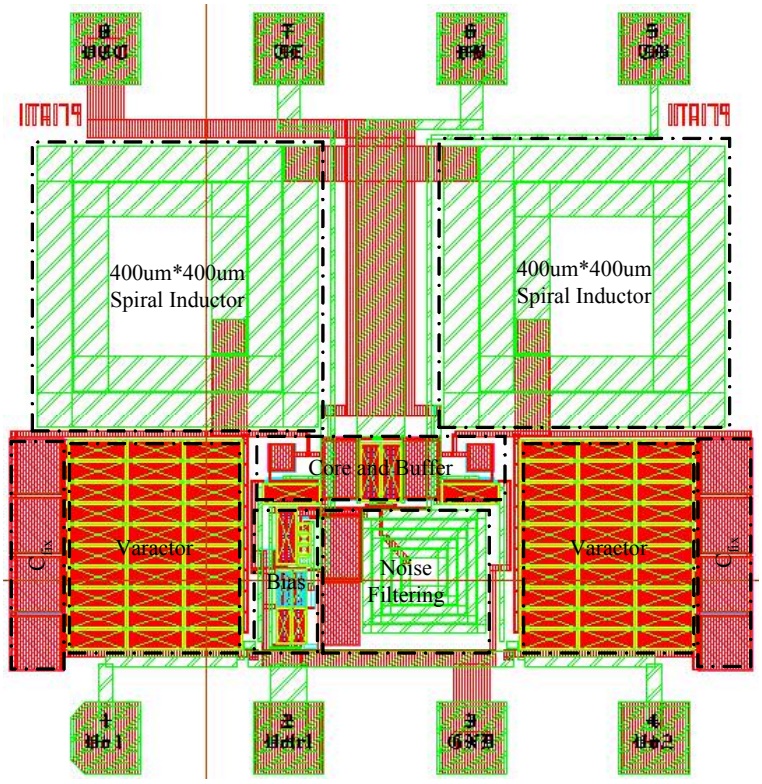


Figure 8.10 Layout of the oscillator with 2.07nH inductor [108]

8.2.2 Measurement Results

Due to the buffer stage, the 50 Ω load can be directly connected to the oscillator. The measurement setup is demonstrated in Fig. 8.11 and the testing structure is illustrated in Fig. 8.12. Two VCO chips use the same PCB as depicted in this figure. The fabricated chips use the DIP package and are mounted in the reverse side of the PCB. The measured and simulated oscillation frequencies as a function of the control voltage of the first 8.8 nH inductance VCO (UTA174) are plotted in Fig 8.13 (a). Note that the measured oscillation frequency is about 100 MHz lower than the simulated data. This difference is primarily caused by the DIP. Also, the transistor parasitic

capacitance was not extracted in the design phase because of a malfunction in the post-layout simulation. It also contributes to this difference. Note that the tuning range of simulation and measurement is very close to each other (9% in measurement and 7% in simulation when the control voltage is from 0 to 2.5V). The phase noise measurement is not completed, but the simulated data is provided in Fig. 8.13 (b).

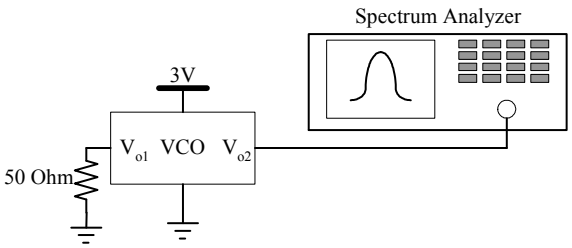


Figure 8.11 Measurement setup for two *LC* oscillators

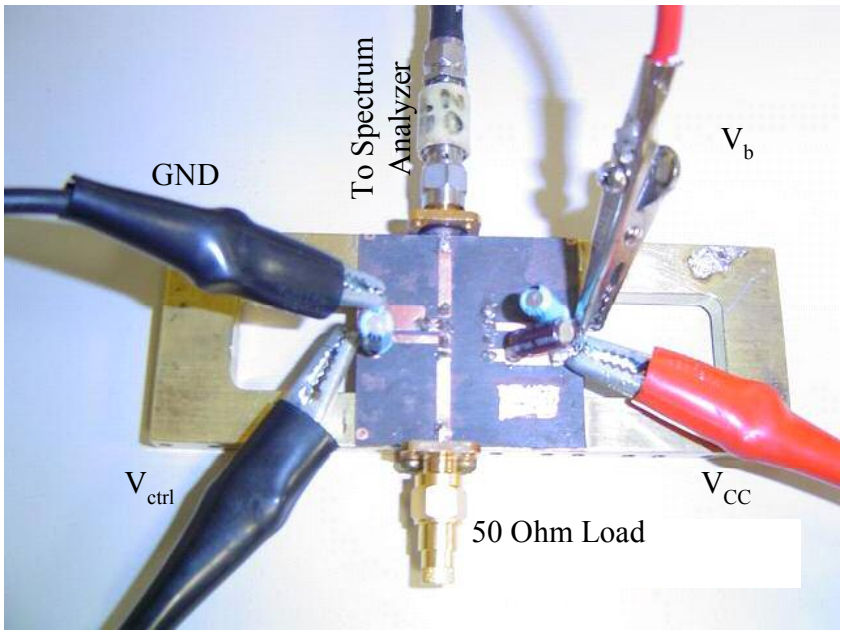
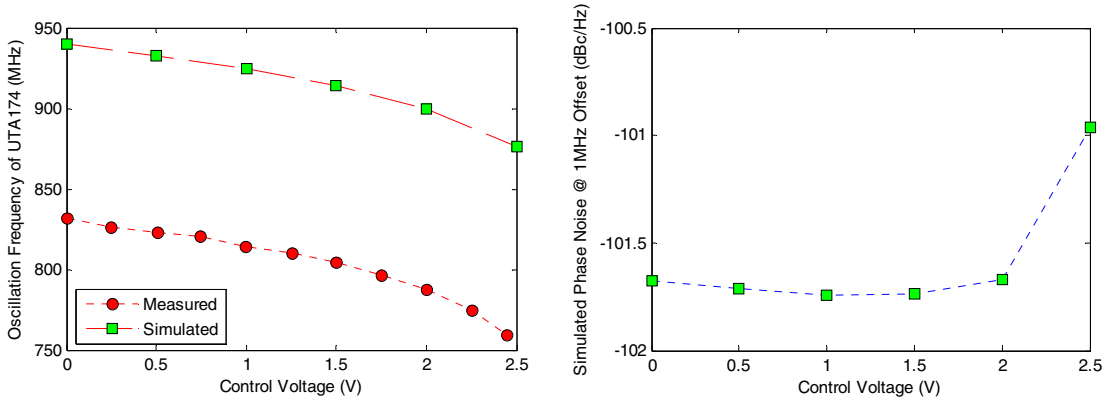
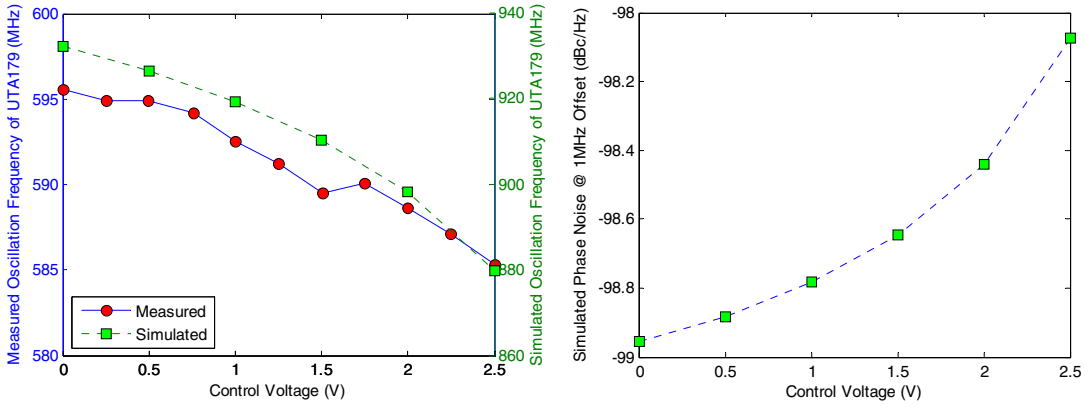


Figure 8.12 Photo of the testing structure for the LC VCOs



(a) (b)

Figure 8.13 Oscillation frequency (a) and simulated phase noise (b) as a function of the control voltage of UTA174



(a) (b)

Figure 8.14 Oscillation frequency (a) and simulated phase noise (b) as a function of the control voltage of UTA179

The oscillation frequency and the phase noise as a function of control voltage of the 2.07 nH inductance VCO (UTA179) are plotted in Fig. 8.14 (a) and (b). Note that the oscillation frequency is much lower compared with the measured oscillation frequency of UTA174. Since the inductor is only 2.07 nH in this VCO, the capacitance is much larger in order to make the two oscillators working near 900 MHz band for the

purpose of comparison. Although, two 6.8pF fixed capacitors are used, the second VCO still has more transistors acting as varactors. They contribute more parasitic capacitance, which is not included in the design phase due to the malfunction of the post-layout simulation. Hence, the oscillation frequency of the UTA179 should be lower than its counterpart UTA174. In addition, two wider underpass metal lines are used in the UTA179 to connect the external circuit to the center of the spiral inductors. These two lines also contribute parasitic capacitance, but they are neglected in the Momentum simulation. They further reduce the oscillation frequency of the UAT179. The tuning range is smaller than the simulated data due to these parasitic capacitances. The measured tuning range is only 1.7% while the design tuning range is about 5.7% when control voltage varies from 0 to 2.5V. The simulated phase noise of UTA179 is plotted in Fig 8.14(b). Note that the phase noise performance of the UTA174 is nearly 3dB better compared with the UTA179. The specification of two oscillators are summarized in Table 8.2

Table 8.2 Specification of two *LC* oscillators

Specifications	**8.8nH oscillator**	**2.07nH oscillator**
Power supply	3 V	3 V
Power dissipated by VCO core	15 mW	15 mW
Total power dissipation	48.1 mW	48.5 mW
Tuning range (V_{ctrl} = 0 – 2.5V)	759.5 MHz ~ 832.0 MHz	585.3 MHz ~ 595.58 MHz
Simulated phase noise at 100kHz (f_{osc} =900MHz)	-101.671 dBc/Hz	-98.442 dBc/Hz
Simulated phase noise at 1MHz (f_{osc}=900MHz)	-121.844 dBc/Hz	-118.458 dBc/Hz

When the control voltage is 2V, the simulated output of both oscillators is approximately 900 MHz. The phase noise versus offset frequency of the two oscillators is plotted in Fig. 8.15. Clearly, the 8.8 nH oscillator has a better phase noise performance at all offset frequencies, validating the optimization procedure proposed in Chapter 7.

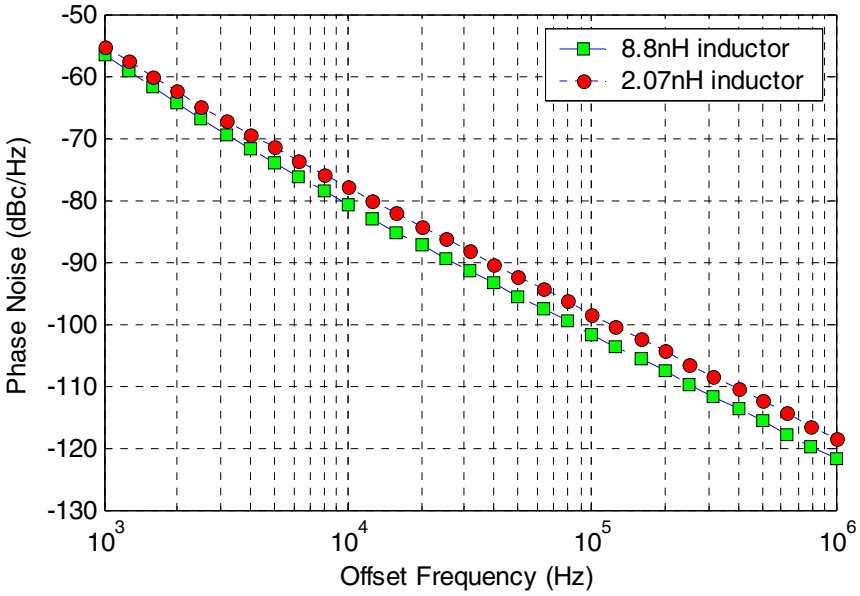


Figure 8.15 Phase noises versus offset frequency of two oscillators

Finally, the overall performance of the two oscillators is compared with published designs. A widely used figure of merit for VCOs is given by [12]

$$FOM = \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \frac{1}{L(\Delta\omega)\cdot P_D \cdot Q^2} \tag{8.1}$$

where P_D is power dissipation of the VCO and Q is the quality factor of the tank. According to this formula and the simulated phase noise data, the FOM of the two oscillators are computed, and the results are listed in Table 8.3. The FOM of the 8.8 nH

oscillator is close to the published results although the bipolar process used is not designed for RF integrated circuits.

Table 8.3 FOM of several bipolar Si/SiGe VCOs

Reference	Q	f_0 (GHz)	P_D (mW)	$L(\Delta\omega)$ (dBc/Hz)	FOM (dB)
[92]	9.3	2.4	50	-92@100kHz	143.2
[93]	~9	1.55	21.6	-102@100kHz	153.4
[94]	~9	1.5	28	-105@100kHz	160.1
[95]	~13	3.6	1	-106@2MHz	148.8
[11]	~4	1.96	32.4	-102@100kHz	160.7
[96]	8	1.9	21.6	-123@600kHz	161.6
[97]	16	0.8	4.3	-106@100kHz	153.6
[98]	<14	5.05	15	-98@100kHz	154.8
[12]	8	2.56	14	-104@100kHz	162.6
2.07nH oscillator of this work	3.75	0.9	15	-101.7@100kHz	154.3
8.8nH oscillator of this work	**2.83**	**0.9**	**15**	**-98.4@100kHz**	**160.0**

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

The phase noise of the high-frequency VCOs is studied extensively in this work. In Chapter 3, the possibility of oscillator design based on the active inductor topology directly was demonstrated. Although, this type of VCO has relatively limited phase noise performance, it provides an alternative VCO design method.

The low-phase-noise *LC* oscillator design was then investigated. To reach the minimum phase noise design, the integrated inductor design, which is the key for *LC* oscillators, was described. The existing phase noise models were presented and reviewed in Chapter 5. The flicker noise up-conversion mechanisms in *LC* oscillators were analyzed and several phase noise suppression techniques were introduced in Chapter 6.

A novel optimization procedure in *LC* oscillator design centered on a new inductance selection criterion was proposed in Chapter 7, which was constrained by power dissipation and chip area. According to a simple physical phase noise model, several closed-form expressions were derived to describe the phase noise generated in the *LC* oscillators. The expressions indicate that the phase noise is proportional to $L^2 \cdot g_L^3$ factor for the given bias current and oscillation frequency. If the integrated inductor has a fixed area, the minimum $L^2 \cdot g_L^3$ was found to decrease monotonically with increasing

inductance by simulating a series of area-limited spiral inductors with different layouts. This conclusion leads to a new inductance selection criterion in *LC* oscillator design, choosing the inductance as large as possible to minimize the $L^2 \cdot g_L^3$ factor. This result is opposite to Ham and Hajimiri's conclusion [86], where they suggested the smaller inductance is better in terms of phase noise suppression. Two *LC* VCOs were designed and fabricated. One has a smaller inductance with maximum Q in its tank while the other uses a larger inductance with minimum $L^2 \cdot g_L^3$ factor and lower Q in its tank. The simulation provided in Chapter 8 shows the phase noise of the latter oscillators is effectively reduced due to the optimization procedure.

9.1 Recommendations for Future Work

The Samori's phase noise model provides valuable design insights in *LC* oscillator design. However, this theory can be only applied to the topologies based on the differential pairs. The possibility to extend this NTI model to a general phase noise model which is suitable to other types of oscillators (Colpitts, ring and etc.) is a topic worth further investigation.

Oscillator phase noise has received enormous investigations in recent years. On the other hand, the phase noise of other circuits may be also worthy of notice. For example, the frequency divider (prescaler) in PLLs contributes in-band phase noise, especially if a high division factor is used. Hence, its phase noise performance is important [99]. Also, the nonlinearity of a charge-pump may also fold the high-frequency noise into the bandwidth of the PLLs [100]. Investigation of the possibility to apply the oscillators' phase noise theories to these circuits is desirable.

The phase noise of PLLs and delay-locked loops (DLLs) is another promising research topic although it has been studied extensively in the past. In [101, Demir's phase noise model has been further developed to predict the phase noise of PLLs in [101]. However, it is relatively complicated for hand calculation. Simple, accurate and insightful phase noise models are always valuable to PLL design.

Beside the internal noise sources, the external noise sources, such as the substrate noise, also degrade the output phase noise. Research on this topic is still on its initial stages [102]-[105]. However, due to the importance to the mixed-signal circuit, it will attract more research in the near future.

APPENDIX A

TMSC0.25μM TRANSISTOR MODEL FILES [106]

```
.MODEL CMOSN NMOS (                              LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 5.7E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3731371
+K1      = 0.4626989    K2      = 3.610998E-3   K3      = 1E-3
+K3B     = 3.4473437    W0      = 1E-7          NLX     = 2.161822E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.465353     DVT1    = 0.4682776     DVT2    = -0.3600181
+U0      = 291.8807271  UA      = -1.358982E-9  UB      = 2.600205E-18
+UC      = 3.68755E-11  VSAT    = 1.453872E5    A0      = 1.7973899
+AGS     = 0.3280843    B0      = -1.492756E-7  B1      = 5.826141E-7
+KETA    = -7.07971E-3  A1      = 5.600633E-4   A2      = 0.4445546
+RDSW    = 186.5665001  PRWG    = 0.5           PRWB    = -0.2
+WR      = 1            WINT    = 0             LINT    = 0
+XL      = 3E-8         XW      = -4E-8         DWG     = -1.627919E-8
+DWB     = 2.793508E-9  VOFF    = -0.0951886    NFACTOR = 1.5570816
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 4.389028E-3   ETAB    = 4.381099E-4
+DSUB    = 0.0217698    PCLM    = 1.679854      PDIBLC1 = 0.4416943
+PDIBLC2 = 2.720463E-3  PDIBLCB = -0.1          DROUT   = 0.7370237
+PSCBE1  = 6.82413E8    PSCBE2  = 5E-10         PVAG    = 0
+DELTA   = 0.01         RSH     = 4.6           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 5.72E-10     CGSO    = 5.72E-10      CGBO    = 1E-12
+CJ      = 1.730461E-3  PB      = 0.9837155     MJ      = 0.4592833
+CJSW    = 4.058445E-10 PBSW    = 0.99          MJSW    = 0.3212178
+CJSWG   = 3.29E-10     PBSWG   = 0.99          MJSWG   = 0.3212178
+CF      = 0            PVTH0   = -0.01         PRDSW   = -10
+PK2     = 2.212933E-3  WKETA   = 7.871804E-3   LKETA   = -4.438935E-3   )


.MODEL CMOSP PMOS (                              LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 5.7E-9
+XJ      = 1E-7         NCH     = 4.1589E17     VTH0    = -0.5502511
+K1      = 0.6400201    K2      = -1.704113E-3  K3      = 0
+K3B     = 15.9111313   W0      = 1E-6          NLX     = 1.607639E-9
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 2.7644417    DVT1    = 0.8479803     DVT2    = -0.1546672
+U0      = 105.2755214  UA      = 1.186284E-9   UB      = 1.176835E-21
```

+UC = -1E-10 VSAT = 2E5 A0 = 0.9791315
+AGS = 0.1953302 B0 = 1.093685E-6 B1 = 5E-6
+KETA = 0.0143725 A1 = 2.376941E-3 A2 = 0.3
+RDSW = 774.3628818 PRWG = 0.5 PRWB = -0.3137681
+WR = 1 WINT = 0 LINT = 3.367961E-8
+XL = 3E-8 XW = -4E-8 DWG = -4.703854E-8
+DWB = 4.628024E-9 VOFF = -0.1352255 NFACTOR = 0.9595714
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.9487547 ETAB = -0.5
+DSUB = 1.327526 PCLM = 1.2246157 PDIBLC1 = 4.978793E-3
+PDIBLC2 = -1.067618E-8 PDIBLCB = -1E-3 DROUT = 0.0589797
+PSCBE1 = 6.155146E9 PSCBE2 = 5.00025E-10 PVAG = 2.250493E-6
+DELTA = 0.01 RSH = 3.4 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 6.76E-10 CGSO = 6.76E-10 CGBO = 1E-12
+CJ = 1.906078E-3 PB = 0.99 MJ = 0.4662316
+CJSW = 3.337172E-10 PBSW = 0.6541995 MJSW = 0.3130577
+CJSWG = 2.5E-10 PBSWG = 0.6541995 MJSWG = 0.3130577
+CF = 0 PVTH0 = 7.047217E-3 PRDSW = 3.0435715
+PK2 = 3.077599E-3 WKETA = 0.033745 LKETA = -9.457104E-3)

APPENDIX B

BIPOLAR TRANSISTOR MODEL FILES [107]

```
.MODEL QINN NPN
+ IS =0.166F    BF =3.239E+02 NF =1.000E+00 VAF=84.6
+ IKF=2.462E-02 ISE=2.956E-17 NE =1.197E+00 BR =3.719E+01
+ NR =1.000E+00 VAR=1.696E+00 IKR=3.964E-02 ISC=1.835E-19
+ NC =1.700E+00 RB =68        IRB=0.000E+00 RBM=15.1
+ RC =2.645E+01 CJE=1.632E-13 VJE=7.973E-01
+ MJE=4.950E-01 TF =1.948E-11 XTF=1.873E+01 VTF=2.825E+00
+ ITF=5.955E-02 PTF=0.000E+00 CJC=1.720E-13 VJC=8.046E-01
+ MJC=4.931E-01 XCJC=171M     TR =4.212E-10 CJS=629F
+ MJS=0         KF =100F      AF =1.000E+00
+ FC =9.765E-01

.MODEL QINP PNP
+ IS =0.166F    BF =7.165E+01 NF =1.000E+00 VAF=3.439E+01
+ IKF=1.882E-02 ISE=6.380E-16 NE =1.366E+00 BR =1.833E+01
+ NR =1.000E+00 VAR=1.805E+00 IKR=1.321E-01 ISC=3.666E-18
+ NC =1.634E+00 RB =28.8      IRB=0.000E+00 RBM=7.6
+ RC =3.739E+01 CJE=1.588E-13 VJE=7.975E-01
+ MJE=5.000E-01 TF =3.156E-11 XTF=5.386E+00 VTF=2.713E+00
+ ITF=5.084E-02 PTF=0.000E+00 CJC=2.725E-13 VJC=7.130E-01
+ MJC=4.200E-01 XCJC=170M     TR =7.500E-11 CJS=515F
+ MJS=0         KF =100F      AF =1.000E+00 FC =8.803E-01
```

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