DESIGN OF A CMOS VCO AND FREQUENCY DIVIDER FOR 5 GHz APPLICATIONS

by

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ABSTRACT

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This thesis presents the design of a new CMOS Voltage Controlled Oscillator and a frequency divider, both of which form important blocks in the design of a PLL synthesizer. These components are important because they operate at the highest frequencies within the PLL and also consume most of the power as compared to the other components. Both these circuits have been an active topic of research in recent years especially with the scaling of technology bringing hopes of complete system-on-chip (SOC) integration at RF frequencies. The circuits in this thesis are designed for 5 GHz applications, mainly for the IEEE Wireless Local Area Network (WLAN) 802.11a standard which spans the frequency range from 5.14 GHz to 5.72 GHz.

The first part of the thesis is an introduction to receiver architectures, VCO's and frequency dividers in general. The second part deals with the design, analysis and simulation results of a novel VCO presented in this work. The VCO achieves a tuning range of 130 MHz around a center frequency of 5.70 GHz and a low phase noise of -114 dBc/Hz at an offset of 1 MHz.

The third part presents the design approach adopted here to designing a high frequency divider using dynamic logic and its simulation results. The logic used here is True Single Phase Clocking (TSPC), which makes use of a single clock thereby avoiding the problems of clock skew and loading. Two main blocks have been presented, the divide-by-2 and divide-by-2/3. These blocks are then cascaded to achieve higher division ratios.

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CHAPTER 1

INTRODUCTION

1.1 Receiver Architectures

The traditionally used architecture, the superheterodyne or superhet in short (Fig. 1.1), down-converts a RF signal to baseband in one or sometimes two stages depending on the frequency plan for the chosen architecture. Mixers, used for this down conversion, convert the RF frequency to a lower intermediate frequency (IF) for filtering and amplification before finally converting it to baseband. The IF is defined as:

$$f_{IF} = \left| f_{RF} - f_{LO} \right| \tag{1.1}$$

where f_{RF} and f_{LO} are the frequency of the RF and local oscillator (LO) signals respectively. These signals form the input to the mixer, which performs analog multiplication on them to give rise to the signal at IF. The major drawback of this architecture which also limits its integrability onto a single chip is the presence of image frequencies. An image is defined as a signal other than the signal of interest that mixes to the same IF as the desired signal. Down-conversion of two different frequencies to the same IF occurs because of the inability of the mixer to recognize the polarity of the frequency difference between the RF and LO. For example, if the RF signal is located one IF higher than the LO (low-side injection), the image frequency is located at,

$$f_{IM} = f_{LO} - f_{IF} = f_{RF} - 2f_{IF} \tag{1.2}$$

and if the RF signal is located one IF lower than the LO (high-side injection), the image frequency is located at,

$$f_{IM} = f_{LO} + f_{IF} = f_{RF} + 2f_{IF} \tag{1.3}$$

Therefore in the superhet architecture the mixer has to be preceded by filters for the purpose of image rejection and channel selection and these filters have to have steep roll-off and very high out-of-band rejection to attenuate the unwanted signals. To accommodate these stringent requirements, the filters need to be designed with high Quality (Q) factor resonators and multiple poles. The low Q factor of on-chip inductors results in prohibitively high passband insertion loss for multiple-poled integrated inductor and capacitor (LC) filters. Furthermore, since monolithic inductors and capacitors require a great deal of die area, multiple pole LC filters quickly become excessively large for on-chip integration.

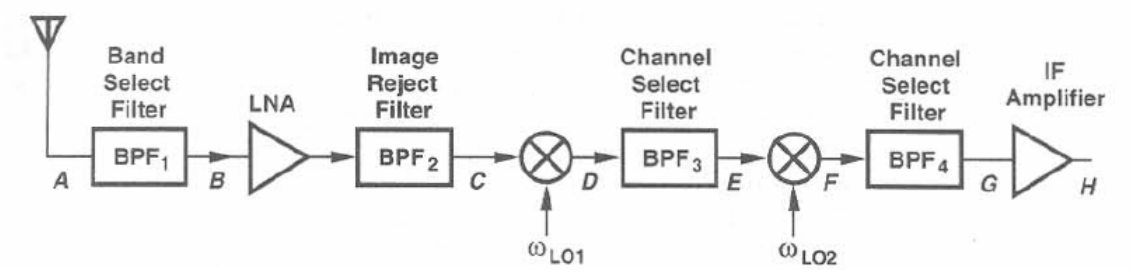


Figure 1.1 Superheterodyne receiver architecture [2]

1.1.1 Direct Conversion Receivers (DCRs)

An alternative approach to heterodyning described above is to convert the RF frequency directly to baseband frequency thereby getting rid of multiple stages of

downconversion. This method is also called direct conversion, homodyning or Zero-IF (i.e., $f_{LO} = f_{RF}$). The greatest advantage of direct conversion is that since the signal is its own image, off-chip image rejection filters can be eliminated and in addition to this channel selection can be performed at baseband further reducing filter requirements. This allows for higher levels of integration of the front end of receivers and as a result has been an active topic of research in recent years [1], [3]. Figure 1.2 shows a simple implementation of a DCR.

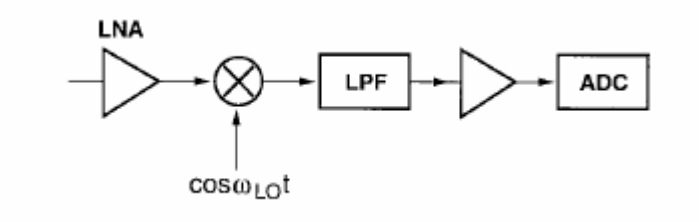


Figure 1.2 Direct Conversion Receiver [2]

Despite its advantages DCRs, have a number of drawbacks which make it a challenging architecture to implement. One of these problems is known as self-mixing. LO leakage from the mixer can be reflected back into the mixer from the output of the LNA, the IC package, the antenna, or even the environment around the receiver. For fundamental direct conversion, the LO is at the same frequency as the RF signal, so these LO reflections combine with the RF signal, pass through the LNA, and self-mix to create a DC offset. Self-mixing can also occur when a large interferer leaks from the RF path to the LO input of the mixer. These DC offsets may be difficult to eliminate; in some cases they may vary with time due to changes in the LO reflections or interferers as the receiver itself or objects in the surrounding environment move. In addition, low frequency noise makes it difficult to achieve low noise figures in direct conversion

receivers. The low frequency noise of transistors is called "1/f noise" because it has a 1/f slope versus frequency. For DCRs, this results in higher receiver noise figures because the output frequency of the mixers lies within the 1/f noise region. More noise at the receiver output requires more gain and lower noise figure in the components at the input to attain the required overall noise figure for a particular application.

Another implementation challenge for DCRs is in-phase and quadrature (I/Q) mismatch. Direct conversion requires the signal to be down-converted into separate I and Q channels to recover the negative and positive frequency components of the signal. If the gain and phase of these two channels are not identical, the output of the receiver will have an I/Q mismatch, resulting in errors in the recovery of the transmitted data [5].

1.1.2 Low-IF or Digital-IF Receivers

The low-IF receiver is an alternative to the DCR which avoids the problems of DC offsets and 1/f noise, but which still allows high degrees of integration [5]. As in a superheterodyne receiver, the RF and LO inputs to the down-conversion mixer of a low-IF receiver differ in frequency by a non-zero IF. However, low-IF receivers have an IF low enough to be easily sampled by an analog-to-digital converter (ADC). Thus, this approach is sometimes called digital-IF. Once in the digital domain, the signal can be filtered and converted to baseband using a DSP. On the other hand, low-IF receivers, while avoiding DC offset issues, have the same image problem as superheterodyne architectures. Image canceling architectures, such as the Hartley or the Weaver (Figure 1.3), can be used for low-IF receivers to avoid the need for expensive off-chip image-

reject filters [5]. These image rejection architectures are not typically used for conventional receivers due to design limitations involving the bandpass and lowpass filters (Figure 1.3). Inductor and capacitor values for passive filters at the IF are too large to be implemented on chip, so operational amplifier based active filters should be used. However, traditional IFs often exceed the slew rate limitation and/or unity gain frequency of standard operational amplifiers. By decreasing the IF to a suitable range for the operational amplifier, active filters can be used in low-IF receivers to implement either the Hartley or Weaver image rejection architectures.

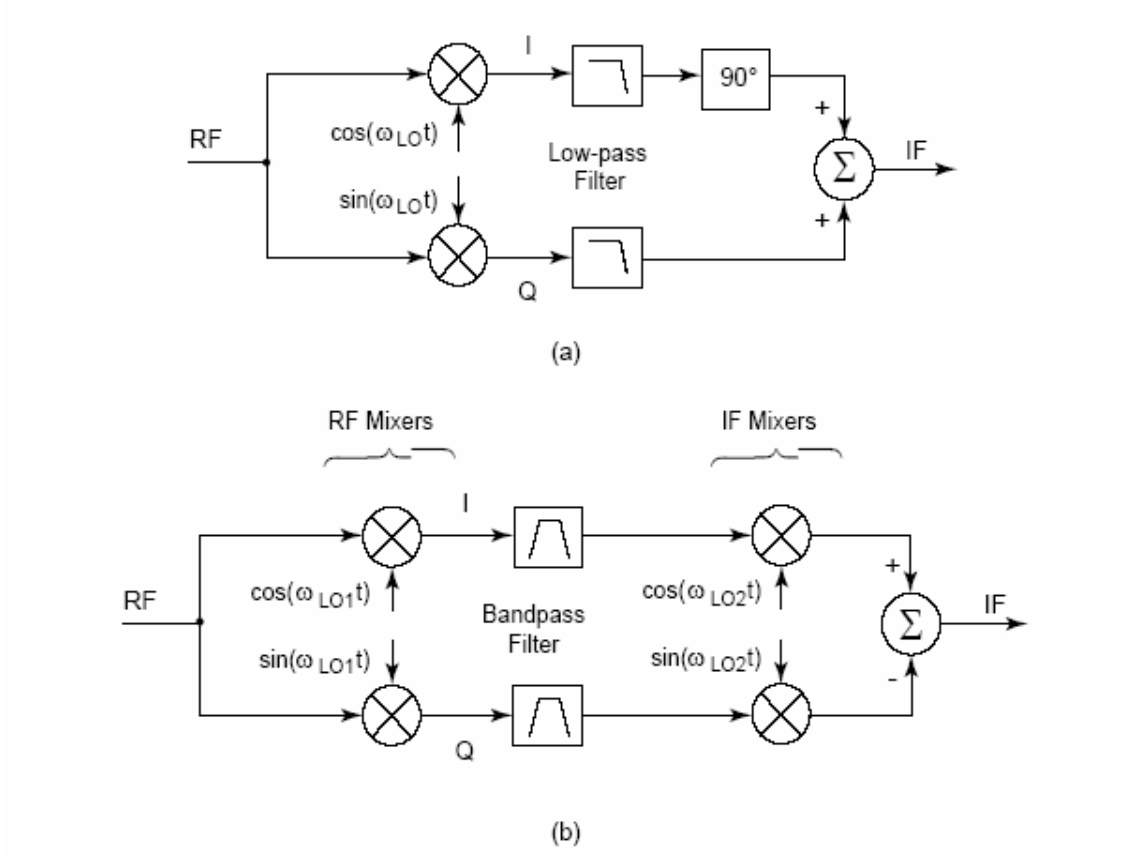


Figure 1.3 Block Diagrams of a) Hartley and b) Weaver image rejection architectures [5]

Mathematically, both of these architectures rely on the following two trigonometric identities:

$$2\cos(\omega_{LO})\cos(\omega_{RF}) = \cos(\omega_{LO} + \omega_{RF}) + \cos(\omega_{LO} - \omega_{RF}) \quad (1.4)$$

$$2\cos(\omega_{LO})\sin(\omega_{RF}) = \sin(\omega_{LO} + \omega_{RF}) - \sin(\omega_{LO} - \omega_{RF}) \quad (1.5)$$

Both the Hartley and Weaver architectures take advantage of the polarity difference in equations 1.4 and 1.5 by using quadrature mixers to process the signal and image differently. As will be described below, in each case the down-conversion process preserves the input signal and cancels the image.

Hartley Architecture

The Hartley architecture employs quadrature mixers that separate the signal into I and Q channels. The branches undergo a relative 90◦ phase shift and the two channels are summed to produce an image-free output [Figure 1.3(a)]. The 90◦ phase shift is implemented in practice with an RC-CR or polyphase network. Assuming low-side injection, the input is $x(t) = A\cos(\omega_S t) + B\cos(\omega_{IM} t)$, where $\omega_{IM} = \omega_S - 2\omega_{IF}$ and ω_S is the signal frequency. After mixing with the Quadrature LO, the output of the low-pass filters is:

$$x_{I-LPF}(t) = \frac{A}{2}\cos(\omega_s - \omega_{LO})t + \frac{B}{2}\cos(\omega_{LO} - \omega_{im})t \quad (1.6)$$

$$x_{Q-LPF}(t) = \frac{A}{2}\sin(\omega_s - \omega_{LO})t - \frac{B}{2}\sin(\omega_{LO} - \omega_{IM})t \quad (1.7)$$

Using the trigonometric identity, $\cos(\omega + 90◦) = \sin(\omega)$, the 90◦ phase shift converts equation 1.6 to:

$$x_{I-90}(t) = \frac{A}{2}\sin(\omega_s - \omega_{LO})t + \frac{B}{2}\sin(\omega_{LO} - \omega_{IM})t \quad (1.8)$$

Finally, summing equations 1.7 and 1.8 results in an image-free output:

$$x_{IF}(t) = A\sin(\omega_s - \omega_{LO})t \quad (1.9)$$

The image rejection ratio (IRR), a measure of the receiver's ability to suppress images, depends on the accuracy of the 90◦ phase shift over the signal bandwidth and the gain balance of the I and Q channels.

Weaver Architecture

The Weaver architecture also has quadrature mixers for separate I and Q channels, but uses two IF stages [Figure 1.3(b)]. A second set of mixers is used to process the image through the I and Q channels so that it is cancelled out at the output summer at the second IF. In a sense, the second stage of I and Q mixing provides the 90◦ phase shift function present in the Hartley architecture.

Figure 1.4 shows a graphical frequency analysis of the image rejection process. The RF signal (f_S) and image ($f_{IM1} = f_{LO1} - f_{IF1}$) are converted to the first IF ($f_{IF1} = f_S - f_{LO1}$) by quadrature mixers without any image filtering. At this point, the image and the signal are at the same frequency. However, in the Q channel, the signal and image are located on the imaginary axis and have opposite polarities. A bandpass filter is often used to pass the desired mixing product and attenuate a secondary image ($f_{IM2} = 2f_{LO2} - f_S - 2f_{LO1}$), which is caused by the second pair of Quadrature mixers. At the second IF ($f_{IF2} = f_S - f_{LO1} - f_{LO2}$), the signal, first image, and second image are located at the same frequency and have the same polarity in the I channel. Meanwhile, in the Q channel, the

second set of mixers converts the signal, first image, and second image from the imaginary axis back to the real axis. Most importantly, the signal and second image continue to have opposite polarity to the first image. The Q channel is then subtracted from the I channel to cancel the first image. The IRR of the Weaver architecture depends on the gain and phase balance of the I and Q channels. It should be noted that the only protection the Weaver architecture provides against the second image is either the out-of-band rejection of the filters shown in Figure 1.4 or, if possible, frequency planning to position the second image where no signal exists.

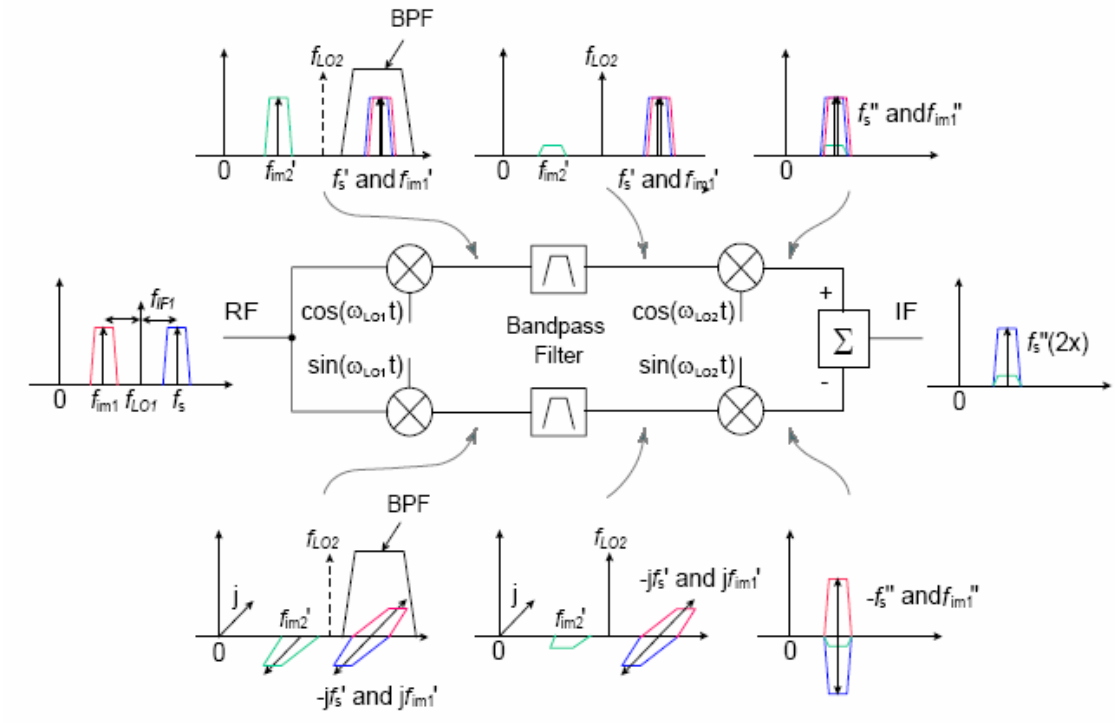


Figure 1.4 A graphical analysis of the Weaver image rejection architecture [5]

1.2 Introduction to Frequency Synthesizers

The LO frequency in the above described architectures, in most cases is generated by a PLL-based frequency synthesizer. Frequency synthesizers are used in many electronic applications where a range of output frequencies are to be generated from a single stable reference frequency usually from a crystal oscillator. For example, in most of the FM radios, a phase-locked loop frequency synthesizer technique is used to generate 101 different frequencies. Also most of the wireless transceiver designs employ a frequency synthesizer to generate highly accurate frequencies, varying in precise steps, such as from 600 MHz to 800 MHz in steps of 200 KHz [4].

The frequency synthesizer's simplified block diagram is shown in Fig. 1.5 (a). In the frequency synthesizer, the PLL block is responsible for generating an output signal whose frequency is dependent on the phase relationship between two input signals. The phases of a reference signal, f_{ref}, and a feedback signal, f_{fb}, are compared in a phase frequency-detector (PFD), and the phase difference is then converted by a charge pump and low pass filter (CP/LPF) circuit into a control voltage. This voltage controls the VCO to generate a signal with the desired frequency. A divider is inserted on the feedback path, giving $f_{fb} = f_0/M$. Since in the locked condition, f_{ref} and f_{fb} must be equal, f_{out} is simply equal to the product of f_{ref} by M. Shown in Figure 1.5 (b) are the simple waveforms with M=4. By changing the multiplication factor, M, signals with desired frequency can be generated.

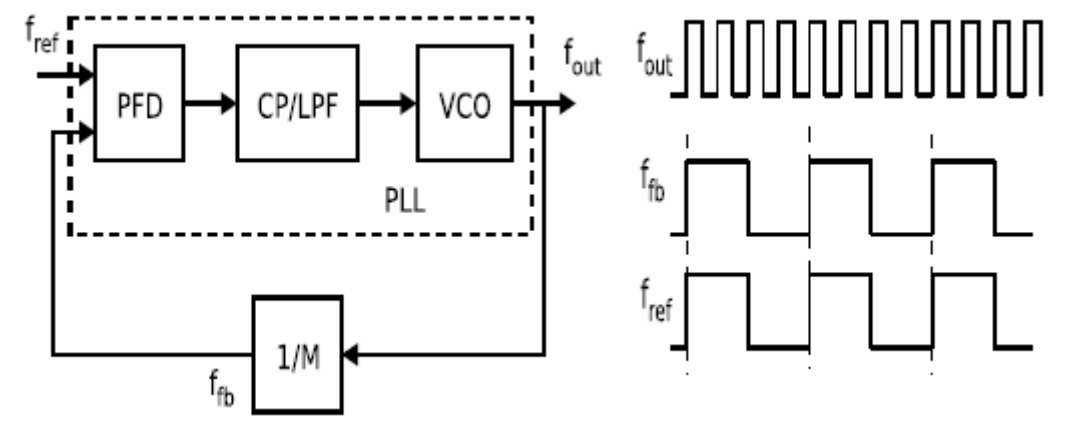


Figure 1.5 a) Simple block diagram and b) waveforms of a frequency synthesizer [16]

As seen in the block diagram above, the frequency synthesizer has four sub blocks: PFD, CP/LPF, VCO, and feedback divider blocks. The PFD block is used to determine the phase difference between the reference and feedback signals. Depending on the input signals' phase relationship, i.e. one leads or lags the other, the PFD produces an appropriate output signal. This is best described with the PFD phase characteristics plot shown in Fig. 1.6, in which, $\Delta\phi = \phi_{ref} - \phi_{feedback}$. The plot shows that the PFD is a nonlinear device and it has a linear phase range within 360 degrees. When the synthesizer is in locked state, the phase error between feedback and reference signals are normally small, which is well within the PFD's linear operating region. Therefore, in locked mode, the PFD block can be considered to be a linear device.

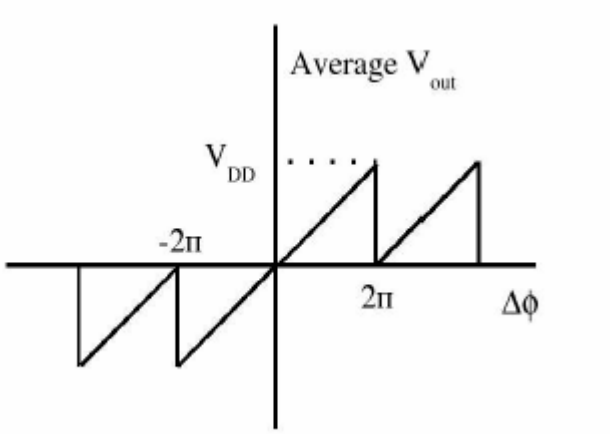


Figure 1.6 Phase error vs Vout plot [16]

The phase frequency detector described above can be implemented by a digital state machine, whose state diagram and schematic are shown in Fig.1.7. The PFD design produces non-complementary outputs UP and DN. The UP signal is used for increasing the value of control voltage and therefore, increasing the output frequency of the VCO. A DN signal does the exactly opposite job, and is used for lowering the output frequency. The duty cycle of each signal is dependent on the phase relationship between the two input signals and their phase difference. Assuming f_{ref} is leading, the DN signal remains inactive while the UP signal becomes active with a duty cycle of $\frac{\Delta\phi}{2\pi}$, as shown in Figure 1.8. When f_{fb} leads, the UP and DN signals behave exactly the opposite.

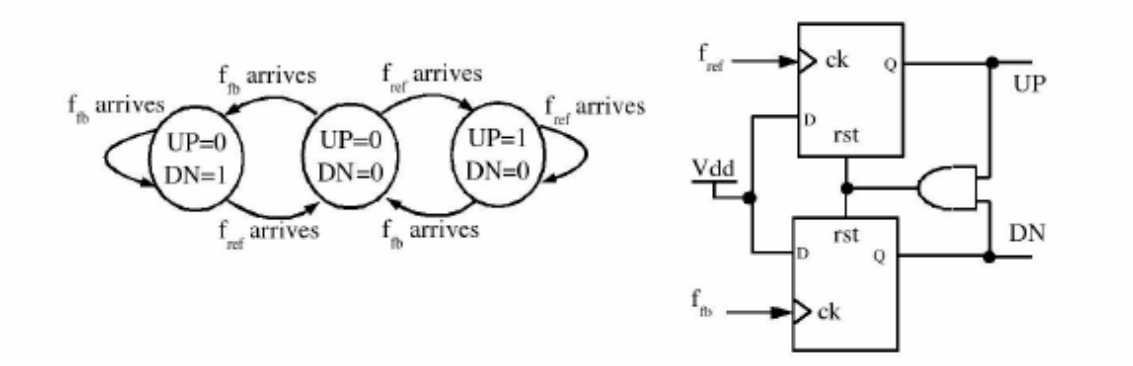


Figure 1.7 State diagram and schematic of PFD [16]

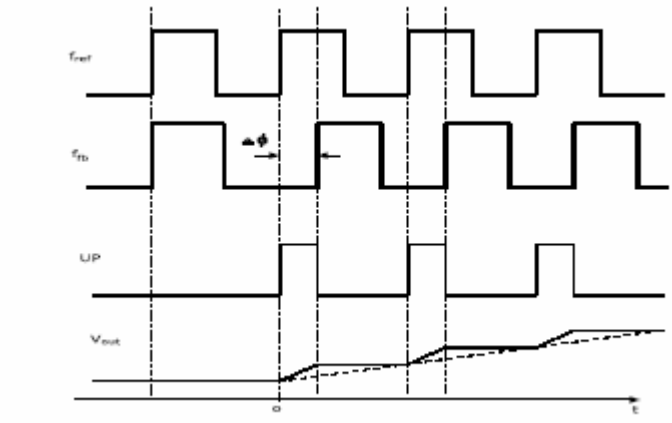


Figure 1.8 Sample waveforms for PFD/CP/LPF combination [16]

Since the UP and DN signals are digital signals, they must be converted into DC to control the VCO. The output of a PFD can be converted to DC (voltage/current) in many different ways. One approach is to sense the difference between the two outputs by using a differential amplifier and apply the result to a low pass filter [5]. The second method is by using a charge pump and a low pass filter.

A charge pump is a three state design. It basically consists of two current sources controlled by the two inputs from the PFD and drives a low pass filter at the output. The charge pump either charges or discharges a capacitor with voltage or

current pulses as shown in the Fig. 1.9. A filter is used to limit the rate of change of the capacitor voltage, and the result is a slowly rising or falling voltage that depends on the frequency difference between the PLL output voltage and the reference frequency. The VCO increases or decreases its frequency of operation as the control voltage is increased or decreased [16].

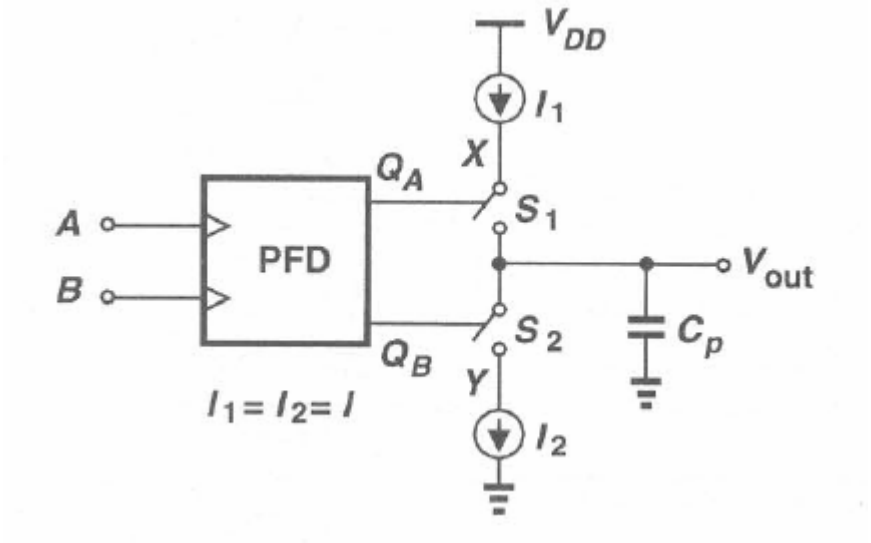


Figure 1.9 PFD with charge pump [2]

1.3 Voltage Controlled Oscillator (VCO)

The output voltage from the low-pass filter is fed into the voltage-controlled oscillator unit. There are two types of VCO designs that are widely used in the industry, ring oscillator VCO and LC VCO. Though it occupies larger area and has narrower tuning range compared with the ring oscillator, an LC VCO offers good phase noise performance. For high frequency transceivers the LC topology is preferred for this very reason. In this work an LC VCO has been designed for 5 GHz applications.

An ideal VCO can be defined as a circuit that generates a periodic output whose frequency is a linear function of a control voltage V_{cont}: $\omega_{out} = \omega_{FR} + K_{VCO}V_{cont}$, where ω_{FR} is the free running frequency and K_{VCO} is the gain of the VCO (specified in rad/s/V) [2]. V_{cont} simply creates a change around ω_{FR} and for the practical range of V_{cont}, ω_{out} may not approach zero because of the existence of ω_{FR} in the above equation. Since phase is the integral of frequency with respect to time, the output of a sinusoidal VCO can be expressed as

$$y(t) = A\cos\left(\omega_{FR}t + K_{VCO}\int_{-\infty}^{t} V_{cont}\,dt\right) \tag{1.10}$$

The output signal generated by the VCO unit is then fed back to the PFD via a divider unit.

1.3.1 Phase Noise

The output of an ideal oscillator can be described by the following equation

$$y(t) = A\cos(\omega_0 t + \phi) \tag{1.11}$$

where A is the amplitude of oscillation, ω_0 is the frequency of oscillation, and Φ is the phase offset. However, the active and passive devices used to implement a real oscillator introduce random noise into both the amplitude and phase of the output. The introduction of noise changes equation above equation to

$$y(t) = A(t)\cos(\omega_0 t + \phi(t)) \tag{1.12}$$

Since frequency is the time derivative of the total phase, the output spectrum of the oscillator will have sidebands because of random variations in the phase. This is known as phase noise. The amplitude noise can also manifest itself as phase noise due to the

non-linear, amplitude-limiting nature of an oscillator. Thus, both sources of noise serve to widen the phase-noise spectrum of the oscillator.

Phase noise is measured as a power spectral density in units of decibels below the carrier per Hertz (dBc/Hz) reported at some offset frequency from the carrier frequency. For example, the IEEE 802.11a standard requires signal generators to have a phase noise less than −107 dBc/Hz at a 1 MHz offset from the carrier.

1.4 Frequency Dividers

The frequency divider is a key component in a PLL synthesizer for the translation from high to low frequencies. There are many types of circuits that can perform frequency division and different applications impose different requirements on the divider, however, none of the circuits meet all the requirements simultaneously. Some of the basic requirements are listed below,

- high operating frequency,
- wide range of operation,
- high division ratio,
- variable and controllable division ratio,
- no RF signal in the absence of input signal,
- low cost

Some common types of frequency dividers are,

- Regenerative frequency dividers
- Frequency dividers based on injection locking
- Carrier storage and parametric frequency dividers

- Phase-locked loop frequency dividers
- Digital frequency dividers

Since in this work, a digital frequency divider has been designed, a brief description of digital frequency dividers is provided below.

1.4.1 Digital Frequency Dividers

Digital frequency divides are the most popular divider structures in use today. The advancement in technology has made it possible to build digital frequency dividers operating up to 15 GHz or more. Not only are the digital logic design methods fairly well established but digital frequency dividers also offer the flexibility of programmability, high division ratios and easier digital control.

The fundamental element of a digital frequency divider is a flip-flop, typically composed of two level-sensitive latches in a master-slave configuration to form an edge triggered flip-flop. The basic principle behind their operation is that of finite state machines. Digital dividers count input clock signal transitions either from high-to-low or vice-versa. This is the same as counting the dock periods or in other words, the clock frequency. Thus by counting specific clock periods, while skipping others on purpose, any function of period-counting may be implemented. Although the terms frequency divider or frequency counter may refer to the same logic circuit, the difference between the two is that for counting purposes, all the bits from the counter are taken out as the output digital data (in parallel) while in a frequency divider usually a single bit output is taken, typically from the last flip-flop stage. The frequency divider is also known sometimes as the prescaler.

Generally, dividers can be classified into two types, synchronous and asynchronous frequency dividers. In synchronous dividers, all the flip-flops evaluate their respective states on the same clock edge. On the other hand, in asynchronous dividers, the clock signal triggers the first flip-flop, the output of the first flip-flop triggers the second flip-flop and the change flows or ripples down the flip-flop chain. Both types of dividers have their own advantages. Synchronous dividers are inherently faster since changes in state occur almost simultaneously on the same clock edge but the division ratio is relatively low whereas asynchronous dividers provide higher division ratios but are slower because the changes from one flip-flop to the next do not arrive until the previous one has settled. Also, the output of the asynchronous dividers is not synchronized with the input clock signal and may contribute to the overall phase-noise, therefore, a usual solution is to logically *AND* the output with the input to bring the output in synchronization with the input.

The speed and power performance of a digital divider depends on the technology used, type of the logic involved and circuit topology employed [22]. Silicon Bipolar and GaAs technologies offer higher speed while consuming relatively more power while CMOS technology is generally slow but takes much less power. The circuits themselves can be either static or dynamic in CMOS technology. Static circuits are more robust and provide broadband operation but are slow while CMOS dynamic circuits can go to higher frequencies but work only in a limited range of frequencies.

In this work, the design of a CMOS dual-modulus prescaler with a divide ratio of 256/288 is presented.

CHAPTER 2

VCO DESIGN

2.1 Introduction

Voltage Controlled Oscillators are essential building blocks of modern communication systems [6] because it works at a high frequency and requires a low phase noise [12]. Important characteristics of VCO's include frequency of operation, frequency stability with temperature, linearity of the voltage-to-frequency characteristic, tuning range, phase noise and cost of fabrication. The other important parameter is low power consumption particularly for applications such as WLAN where the WLAN Network Interface Card (NIC) plugs into laptops, Personal Digital Assistants (PDA's) and Tablet Personal Computers (PC's), which have limited battery life [6]. There are many important design trade-offs to observe in the design of a VCO.

Single chip 5 GHz transceivers for the IEEE 802.11a WLAN and other technologies require both low power and low phase noise VCO's. Phase noise has to be low to avoid compromising transmit Error Vector Magnitude (EVM) performance particularly at the high 54 Mbps rate.

There are several ways to build a VCO. A brief description of the LC tank VCO follows since it has the best normalized phase noise performance compared to other fully integrated structures like ring oscillators, relaxation oscillators, multivibrators and

other gm-C oscillators. In other words, it provides the lowest phase noise for a given amount of power. This work is based on a LC tank VCO for these reasons.

2.1.1 Typical LC Tank CMOS VCO's

In most RF oscillators, a frequency selective network or in other words a resonator such as an LC tank is included as part of the feedback loop of the VCO to stabilize the frequency [2]. The quality of an LC tank VCO relies on the quality of the LC tank. It determines the quality factor of the oscillator. Therefore, the ideal VCO would have an infinite-Q LC tank. However, in practice, the Q of inductors is not very high in CMOS standard processes. So, a negative resistance is needed to replenish the tank with energy and sustain the oscillations. For a simple RLC circuit, the current consumption is inversely proportional to the value of the inductance. This indicates that to get the best VCO phase noise at the lowest power dissipation, the inductor should have the largest Q possible. The Q is process dependent whereas the value of the inductance depends on the node capacitance and the required frequency of oscillation. This fixes pretty much the phase noise and the power dissipation for a given frequency in a given process.

Figure 2.1 shows the schematic of a basic LC tank VCO. The negative resistance is typically provided by a cross-coupled pair of NMOS transistors. The frequency of oscillation of this circuit is given by, $f = \frac{1}{2\pi\sqrt{LC}}$, where C represents the sum of all capacitances at the output node.

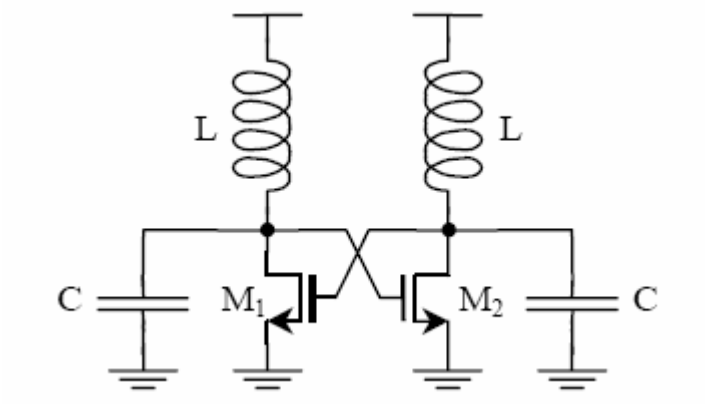


Figure 2.1 Basic LC Tank VCO schematic [12]

A more elaborate small-signal equivalent circuit of one side of the VCO is given in Figure 2.2. It shows that the actual resonant circuit is made of a lossy inductor (L, R_L (R_L represents the series resistance contributed by virtue of the layout of the inductor which causes the loss)), a lossy capacitor (usually a varactor defined by C and R_C where R_C represents the resistive loss contributed by virtue of the layout of the capacitor), the gate-source capacitance of the active device C_{GS}, four times its gate-drain capacitance C_{GD} (two times for it is a differential circuit (Miller effect) and another two times for the two equal C_{GD} in parallel) and its output impedance r_0. In fully integrated implementations, the quality limitation of the tank comes from R_L.

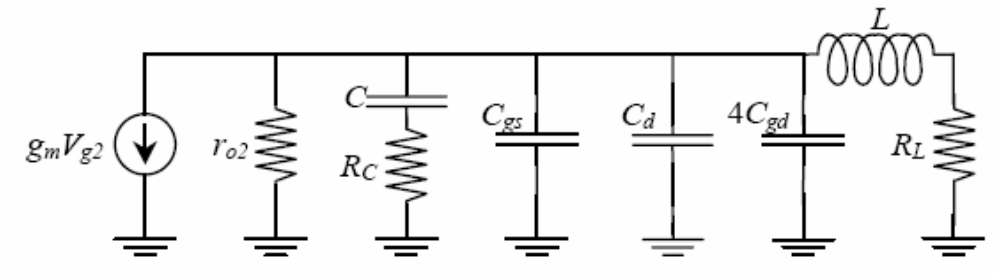


Figure 2.2 Small-signal circuit of one half of the basic LC tank VCO [12]

In order for oscillations to occur, the negative resistance $\left(-\frac{1}{g_m}\right)$ provided by the cross-coupled active devices has to be smaller (in absolute value) than the parallel resistance R_P of the tank. It should be noted here that R_P denotes the resistance that accounts for all the losses in the circuit at the given frequency. In other words $R_p - \frac{1}{g_m} \geq 0$. If it is not the case, the output nodes will rest at the supply voltage. On the other hand, if oscillations develop, their amplitude will be limited by the clipping effect of the active devices. When the amplitude grows larger and larger, there is a point where the negative resistance is not strong enough to balance the positive resistance of the LC tank. That is when the amplitude stops growing. This point determines the swing on the output nodes of the VCO. The maximum swing possible is from 0 volt to $2V_{DD}$. There is no way that the oscillations could go over 2 V_{DD}. First, the DC average cannot go beyond V_{DD} (otherwise, we would have a free source of energy). Secondly, the lowest voltage obtainable is 0 volt (at that point, the transistor is turned off and the output node can only rise). When the cross-coupled pair is close to clipping the amplitude, one node is high and the other one is low. Thus one of the transistors is switched off and the other one is deeply in the linear region. The deeper in the linear region, the smaller the negative resistance and it eventually limits the growth of the amplitude of the output node. When the g_m is much larger than required, the VCO of Figure 2.1 could be seen as a simple LC circuit whose energy is replenished by the NMOS pair.

When the amplitude of the oscillations is large enough, the transistors enter the linear region, thereby showing a resistance between the drain and source. When they are in the deep linear region, their resistance degrades the overall Q of the tank. Hence, it would be interesting to reduce and even avoid any excursion in the linear region. In this work the circuit is biased to always keep the transistors in saturation.

2.1.2 Current Steered LC Tank VCO

Figure 2.3 shows a current steered VCO. The addition of a tail current source has several effects on the behavior of the VCO. First, the oscillation amplitude is now determined by the tail current. At the resonance frequency, the admittances of L and C cancel, leaving R_P, the equivalent parallel resistance of the LC tank.

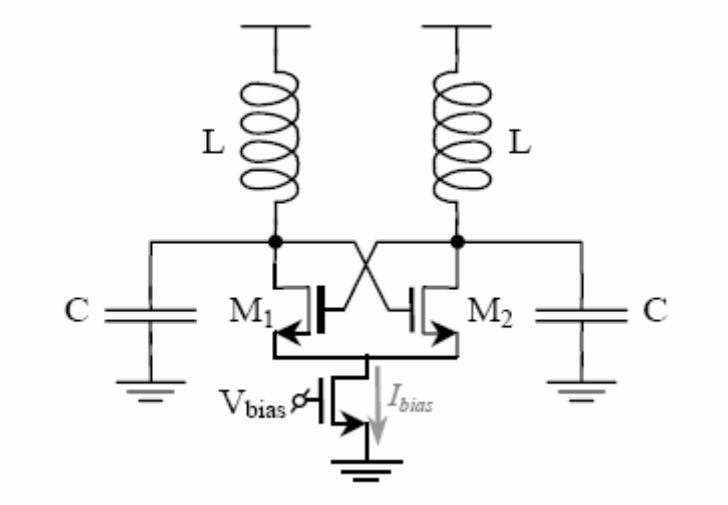


Figure 2.3 Current controlled LC tank VCO schematic [12]

The peak-to-peak voltage swing amplitude across the tank is given to a first approximation by $V_{\max} = 2I_{tail}R_P$. This regime of operation is referred to as the current limited region [13]. In this case, the tank amplitude does not depend on the supply

voltage. The previous estimate of V_{max} is valid as long as the active devices work in the saturation region. If they are driven into the deep linear region (which happens when the amplitude grows closer to the supply voltage), they act as resistors in parallel with R_P. This is equivalent to a reduction in the effective R_P (or equivalently in a reduction of the absolute value of the negative resistance that balances R_P). The tank voltage amplitude is then limited to $2V_{DD}$. This region of operation is referred to as voltage limited region [13]. The same amplitude limitation phenomenon appears in the basic LC tank without a current source.

The reduction in voltage swing is more than compensated by the reduction in current consumption. Compared to the basic VCO, this reduces current, especially in the case of an over-designed g_m (larger transistors than necessary to sustain oscillations). In that case, the basic VCO consumes a lot of "short-circuit current" that is useless to the functioning of the oscillator.

A drawback of the current steered VCO is that the current source NMOS reduces the headroom available for oscillations by around 400mV which is not negligible when working with low supply voltages. In addition, that raises the source voltage of the cross-coupled pair, thereby reducing their g_m because of the body effect. That means a smaller inductance to keep the same frequency of oscillation at the output node (which is now more loaded to keep the same g_m).

The topologies described above form the basis for the circuit design in this work. In this work a new monolithic LC VCO using 0.25 μm CMOS Technology, for

802.11a WLAN applications, is presented. A similar scheme applied to an LC VCO implemented in a Si bipolar technology is described in [7].

The VCO achieves excellent performance in terms of tuning range, phase noise and linearity of voltage-to-frequency change. It draws a current of approximately 2.4 mA from a power supply of 2.5 V.

2.2 Circuit Configuration and Working

The VCO designed in this work is shown in Figure 2.4 below. This design is unique in the sense that this VCO does not make use of varactors in the LC tank but instead, relies on characteristics inherent in the circuit configuration for frequency tuning. There are certain advantages that are gained by not using varactors in the design. Varactors in silicon are usually implemented by using inversion or accumulation mode

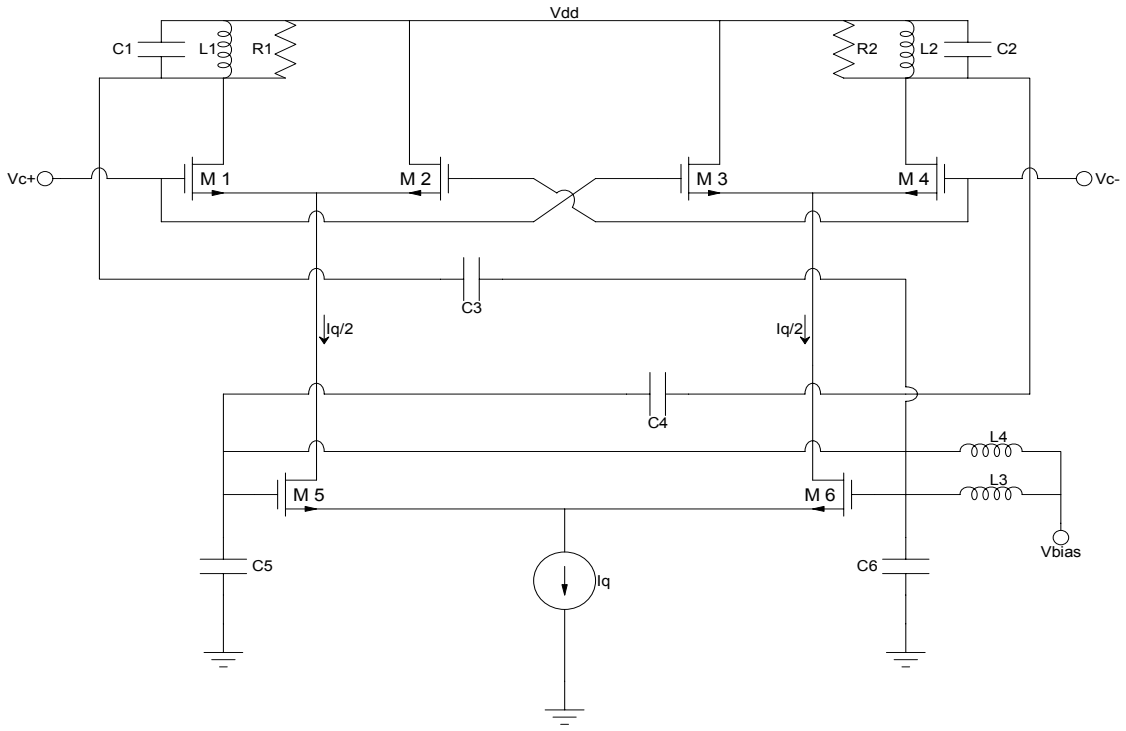


Figure 2.4 Schematic of the LC VCO

MOS devices and since MOS devices are susceptible to flicker noise and other noises like thermal noise, shot noise and so on, they can contribute to increasing the overall phase noise of the circuit. Also when incorporated into the VCO tank circuit, the large-signal swing of the VCO output oscillation modulates the varactor capacitance in time, resulting in a VCO tuning curve that deviates from the dc tuning curve of the particular varactor structure [14].

The designed VCO (Figure 2.4) contains two LC tuned circuits with different resonant frequencies. The operation of the circuit relies on two feedback loops, which are applied to each tuned circuit in a classical Colpitts configuration. A differential controlling voltage V_c^+ and V_c^-, is applied to the Gilbert quad to vary the loop transmission applied to each resonator. The transistors M1, M2, M3 and M4 form the Gilbert quad and M5 and M6 provide gain. The circuit makes use of controlling voltages to vary the loop gain, which in turn varies the frequency of operation of the circuit. The oscillation frequency is varied continuously from the resonant frequency of the left resonator when M1 is on and M4 is off to the resonant frequency of the right resonator when M1 is off and M4 is on.

To gain insight into the working of this cross-coupled LC VCO, consider it to be a feedback circuit with two feedback loops. Let the left feedback loop gain be denoted by $A_{v1}(s)$ and the right feedback loop gain be denoted by $A_{v2}(s)$. Furthermore, let α_1 and α_2 denote the fractions of bias current $I_q/2$ that drive the transistors M1 and M4. The controlling voltages V_c^+ and V_c^- set the values of α_1 and α_2 ($0 \leq \alpha_1 \leq 1$; $0 \leq \alpha_2 \leq$

1) in such a way so as to keep the sum ($\alpha_1 + \alpha_2$) a constant equal to 1 i.e., $\alpha_1 = 1$ if M1 is on and M4 is off; $\alpha_2 = 1$ if M1 is off and M4 is on. The simplified ac circuit of the VCO

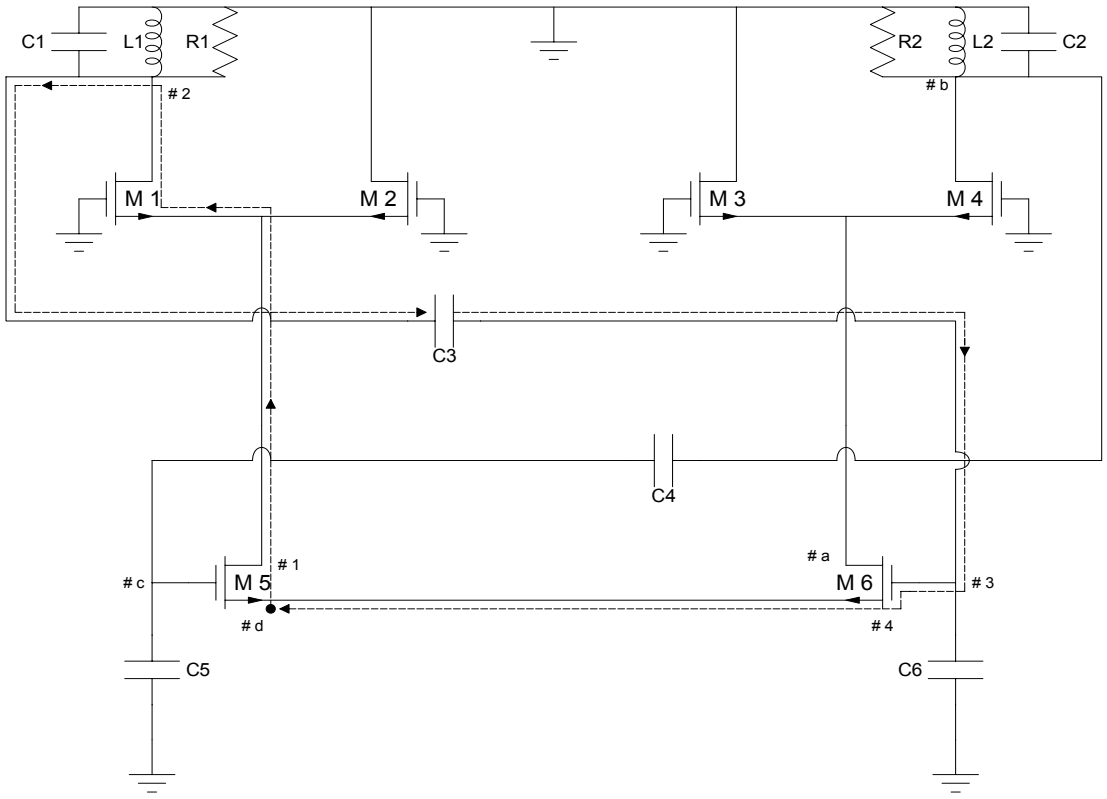


Figure 2.5 Simplified ac circuit schematic

is shown in Figure 2.5 above. Now lets say, the loop is broken at the common source node shared by the transistors M5 and M6 and a test signal is applied at this point, this signal would traverse through the left and right loops along the paths numbered 1 to 4 and a to d respectively (the signal flow along the left loop is shown in Figure 2.5). A block diagram depicting the signal flow in the two loops is shown in Figure 2.6. Upon traversing through the loops, the two signals return to the source node of M5 and M6 and are added up due to the summing property of the source-coupled pair [15].

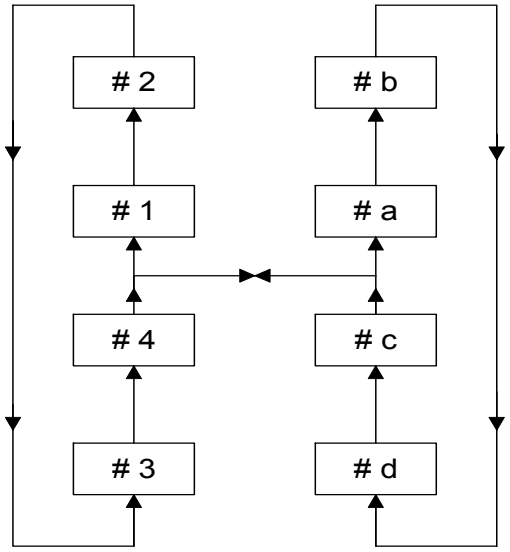


Figure 2.6 Flow of the feedback loops

The equivalent ac circuit of the left loop at full gain is shown in Figure 2.7 where, the gate of the transistor M5 is assumed grounded for ease of analysis. Under

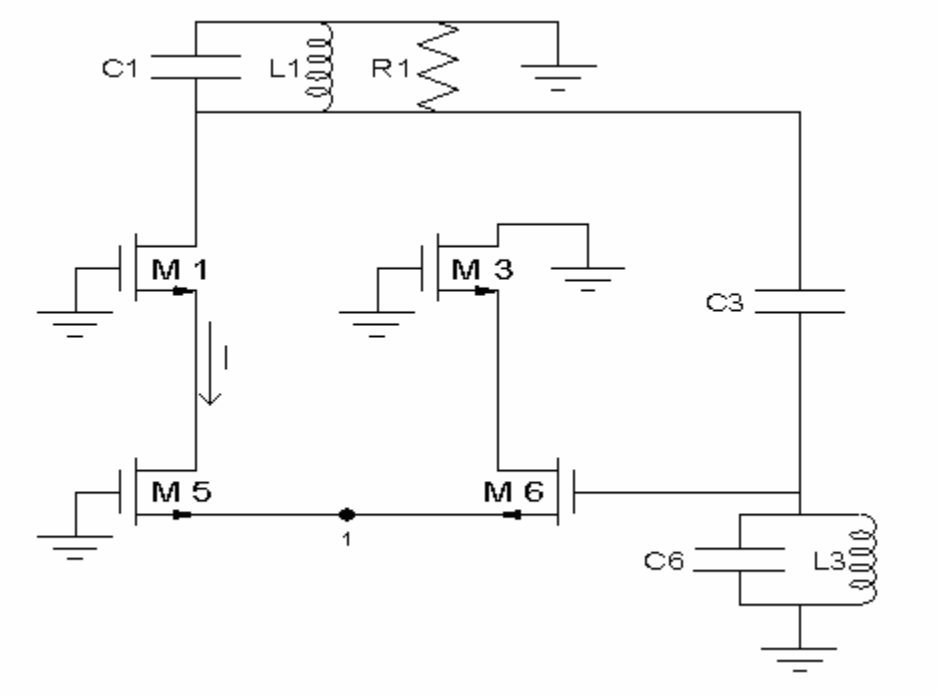


Figure 2.7 Equivalent ac circuit of the left loop

this assumption the transistors M5 and M6 can be depicted by their equivalent models as shown in Figure 2.8 and then further simplified as shown in Figure 2.9.

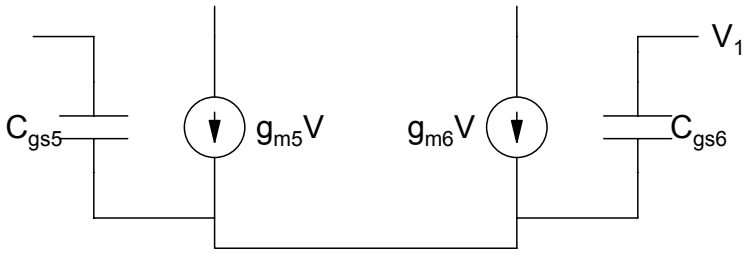


Figure 2.8 M5 and M6 replaced by equivalent models

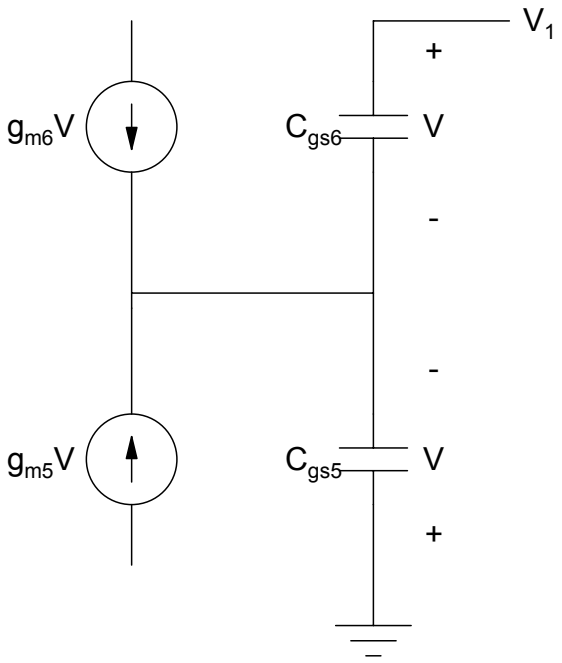


Figure 2.9 Simplified diagram of Figure 2.8 showing M5 and M6 connected at the source

From Figure 2.9, by reversing the polarity of the voltage controlled current source $g_{m5}V$, it can be observed that current I can be written as,

$$I = g_{m6}V = g_{m5}V \tag{2.1}$$

$$\Rightarrow I = \frac{g_{m5}V_1}{2} = \frac{g_{m6}V_1}{2} \tag{2.2}$$

Therefore the transconductance is,

$$\frac{dI}{dV_1} = \frac{g_{m5}}{2} = \frac{g_{m6}}{2} = G_m \tag{2.3}$$

From this, the approximate capacitance looking into the gate of M6 is given as,

$$\frac{C_{gs5}}{2} = \frac{C_{gs6}}{2} = \frac{C_{gs}}{2} \tag{2.4}$$

All the above equations are derived assuming that transistors M5 and M6 are identical.

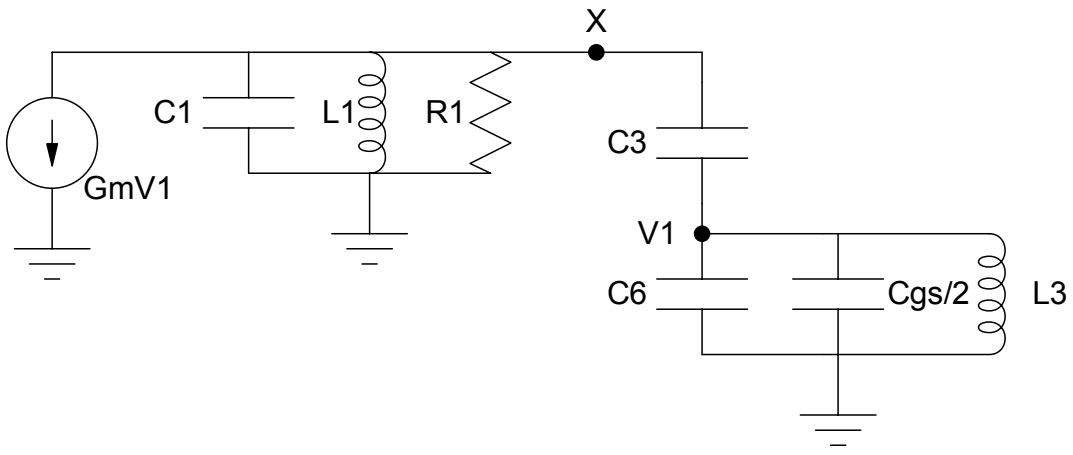


Figure 2.10 Small signal model for loop gain

Figure 2.10 shows the simplified equivalent circuit used for deriving the loop gain $A_{v1}(s)$, which approximates linear operation just before the oscillator breaks into

oscillation. $A_{v1}(s)$ is found by applying the loop breaking technique [24] at node X in the loop, as shown in Figure 2.10. The capacitor C_3 acts as a dc blocking capacitor and is of several pico Farads and thus it is approximated by a short while deriving the equation for $A_{v1}(s)$.

Consider the impedance of the parallel combination of C_1, R_1 and L_1 to be denoted by Z_x,

$$Z_x = X_{C1} \| R_1 \| X_{L1} \tag{2.5}$$

$$Z_x = \frac{sL_1R_1}{sL_1 + R_1} \left\| \frac{1}{sC_1} \right. \tag{2.6}$$

$$Z_x = \frac{\dfrac{sL_1R_1}{(sL_1 + R_1)\cdot sC_1}}{\dfrac{sL_1R_1}{sL_1 + R_1} + \dfrac{1}{sC_1}} \tag{2.7}$$

$$Z_x = \frac{sL_1}{s^2L_1C_1 + s\dfrac{L_1}{R_1} + 1} \tag{2.8}$$

Let the impedance of the parallel combination of C_6, $C_{gs}/2$ and L_3 be denoted by Z_y,

$$Z_y = X_{C6} \| X_{Cgs/2} \| X_{L3} \tag{2.9}$$

$$Z_y = \frac{\dfrac{sL_3}{s(C_6 + C_{gs/2})}}{sL_3 + \dfrac{1}{s(C_6 + C_{gs/2})}} \tag{2.10}$$

$$Z_y = \frac{sL_3}{s^2L_3(C_6 + C_{gs/2})} \tag{2.11}$$

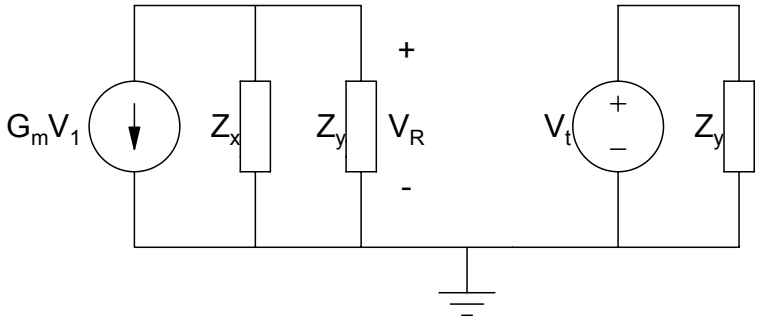


Figure 2.11 Loop Breaking technique applied to circuit in Figure 2.8

The parallel combination of Z_x and Z_y derived above is given by,

$$Z = Z_x \| Z_y \tag{2.12}$$

$$Z = \frac{sL_1}{s^2 L_1 C_1 + s\frac{L_1}{R_1} + 1} \Bigg\| \frac{sL_3}{s^2 L_3 (C_6 + C_{gs/2}) + 1} \tag{2.13}$$

$$Z = \frac{s^2 L_1 L_3}{s^3 L_1 L_3 \left(C_1 + C_6 + C_{gs/2}\right) + s^2 \frac{L_1 L_3}{R_1} + s\left(L_1 + L_3\right)} \tag{2.14}$$

Dividing the numerator and denominator of equation (2.14) by sL_3 yields,

$$Z = \frac{sL_1}{s^2 L_1 C_x + s\frac{L_1}{R_1} + \left(\frac{L_1}{L_3} + 1\right)} \tag{2.15}$$

where

$$C_x = C_1 + C_6 + C_{gs/2} \tag{2.16}$$

According to the loop breaking technique the voltage gain of the loop is given as,

$$A_{v1}(s) = \frac{V_R}{V_t} \tag{2.17}$$

where,

$$V_R = G_m V_1 \cdot Z \tag{2.18}$$

and,

$$V_t = V_1 \tag{2.19}$$

Therefore gain of the left loop $A_{v1}(s)$ is given by,

$$A_{v1}(s) = G_m Z \tag{2.20}$$

which is,

$$A_{v1}(s) = G_m \left[\frac{sL_1}{s^2 L_1 C_x + s\frac{L_1}{R_1} + \left(\frac{L_1}{L_3} + 1\right)} \right] \tag{2.21}$$

The loop gain of the right loop $A_{v2}(s)$ can be derived in a similar fashion and is given by,

$$A_{v2}(s) = G_m \left[\frac{sL_2}{s^2 L_2 C_y + s\frac{L_2}{R_2} + \left(\frac{L_2}{L_4} + 1\right)} \right] \tag{2.22}$$

where

$$C_y = C_2 + C_5 + C_{gs/2} \tag{2.23}$$

The effective loop gain of the circuit can be calculated as follows. Assume a test signal v_x inserted at the common-source point, indicated as node 1 in Figure 2.7. This test signal will traverse the left loop and return as the signal,

$$v_{y1} = \alpha_1 A_{v1}(s) v_x \tag{2.24}$$

The same excitation v_x traverses the right loop and returns to the common-source point as the signal,

$$v_{y2} = \alpha_2 A_{v2}(s) v_x \tag{2.25}$$

Recall from above that α_1 and α_2 denote the fractions of bias current $I_q/2$ that drive transistors M1 and M4. The total signal transmission around both loops is given by,

$$v_y = v_{y1} + v_{y2} \tag{2.26}$$

and thus the effective loop gain of the complete circuit is,

$$A_v(s) = \frac{v_y}{v_x} = \alpha_1 A_{v1}(s) + \alpha_2 A_{v2}(s) \tag{2.27}$$

The resonant frequencies of the two tuned circuits in the LC VCO are given by the following equations. The resonant frequency of the left tuned circuit is given by,

$$\omega_1 = \frac{1}{\sqrt{L_x C_x}} \tag{2.28}$$

where

$$L_x = \frac{L_1 L_3}{L_1 + L_3} \tag{2.29}$$

and C_x is given by equation (2.16). The resonant frequency of the right tuned circuit is given by,

$$\omega_2 = \frac{1}{\sqrt{L_y C_y}} \tag{2.30}$$

where

$$L_y = \frac{L_2 L_4}{L_2 + L_4} \tag{2.31}$$

and C_y is given by equation (2.23).

In the next subsection the procedure followed for the design of the VCO will be discussed.

2.3 Design Procedure

Figure 2.12 shows the full VCO schematic with the current mirror circuit. Transistors M7, M8 and M9 form the current mirror and current sink. Transistors M10 and M11 help to bias transistors M5 and M6 that are part of the core VCO.

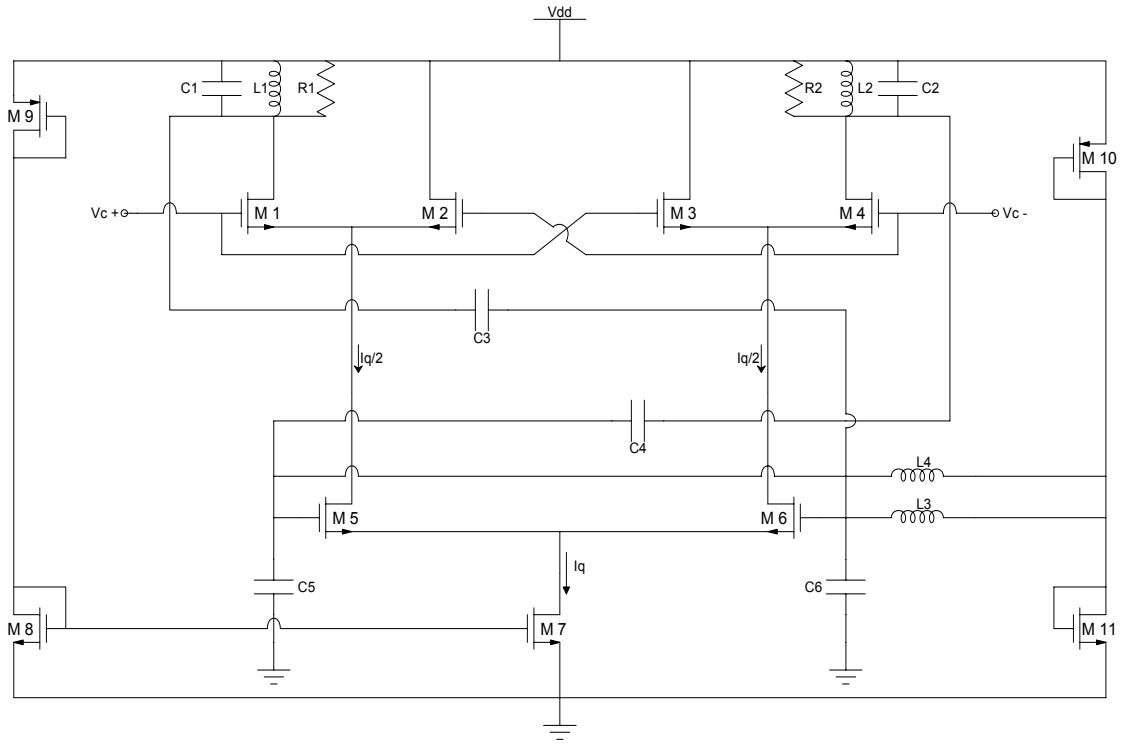


Figure 2.12 Schematic of entire VCO circuit

2.3.1 Current Mirror and Biasing Transistors

Current mirrors are fundamental building blocks in analog circuits. They can be used to provide a current source to the circuit and also act as an active load at the output. An NMOS current sink was used to drive the VCO as shown in figure 2.13. Ideally, a small reference current is desired that can be scaled by M1.

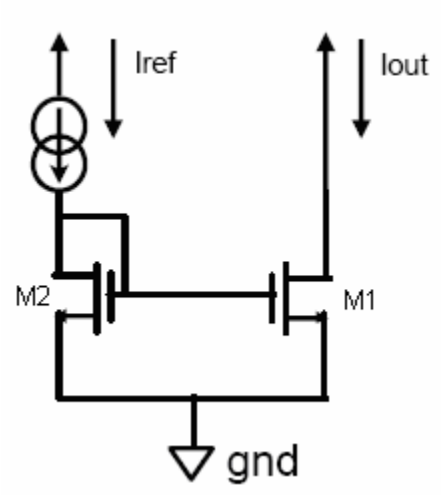


Figure 2.13 A simple NMOS current sink

Assuming both transistors M1 and M2 are in the active region and neglecting channel length modulation for simplicity, the following equation for drain current in the saturation region can be used

$$I_{DS1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}\left(V_{GS1} - V_{th}\right)^2 \tag{2.32}$$

$$I_{DS2} = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}\left(V_{GS2} - V_{th}\right)^2 \tag{2.33}$$

And since the gates of both transistors are connected together and the sources grounded, $V_{GS1} = V_{GS2}$. Therefore,

$$\frac{I_{DS1}}{I_{DS2}} = \frac{I_{out}}{I_{ref}} = \frac{W_1 / L_1}{W_2 / L_2} \tag{2.34}$$

This shows that by changing the ratios of W and L of each transistor, the current can be scaled. In reality, I_{out} is not constant because M1 has a variable V_{DS}. Therefore the current mirror has to be designed so that I_{out} is less sensitive to the change in V_{DS} which can be achieved by increasing the output resistance of M1. This is done by increasing the length of the transistor, $r_0 = 1/\lambda I_{DS}$.

For the current mirror used in this work, the length of the transistors is assumed to be $2L_{min}$ ($\approx$ 0.50 μm). A current of 3 mA is assumed for I_{out} and a reference current I_{ref} of 1mA is assumed. The TSMC 0.25 μm model parameter file used to calculate the design values for this VCO is attached in appendix A, and some of the key values are listed in table 2.1 below.

Table 2.1 Some Key 0.25 um Model Parameter Values

NMOS	**PMOS**
$\mu_n = 274.384\ cm^2/V/s$	$\mu_p = 100\ cm^2/V/s$
$t_{ox} = 5.7 * 10^{-7}$ cm	$t_{ox} = 5.7 * 10^{-7}$ cm
$C_{ox} = \varepsilon_{ox}/t_{ox} = 6.058e^{-7}$	$C_{ox} = \varepsilon_{ox}/t_{ox} = 6.058e^{-7}$
$\mu_n C_{ox} = 1.662e^{-4}$	$\mu_p C_{ox} = 6.058e^{-5}$

From figure 2.12 and the above explanation, it can be seen that the current I_{DS7} = 3 mA and I_{DS8} = 1 mA. Assuming a V_{GS} of 0.6 V (which gives an approximate overdrive voltage (V_{GS}-V_{th}) of about 0.23 V, typically the overdrive voltage should be between 200 mV to 400 mV), for transistor M7 and substituting this value in equation

(2.32) along with the values for current and model parameters, the aspect ratio (W/L) for M7 is obtained.

$$\frac{W_7}{L_7} = \frac{1}{2}\frac{\mu_n C_{ox}}{I_{DS7}}\left(V_{GS1} - V_{tn}\right)^2 = 689 \tag{2.35}$$

where $L_7 = 2L_{min}$, therefore,

$$W_7 = 689 \times 2 \times 0.25e-6 = 344.5e-6 \tag{2.36}$$

Now, the width of the transistor M8 can be found using the equation (2.34). It is found to be,

$$W_8 = 114.8e-6 = 114.8\mu m \tag{2.37}$$

Transistor M9 is a diode connected PMOS transistor used as a load to provide a resistive drop. The width of the transistor is calculated using the current equation for a PMOS transistor in saturation, which is

$$I_{DS9} = \frac{1}{2}\mu_p C_{ox}\frac{W_9}{L_9}\left(V_{SG9} - \left|V_{tp}\right|\right)^2 \tag{2.38}$$

Since M8 is diode connected, $V_{GS8} = V_{DS8}$ which is equal to V_{GS7} =0.6V. So the drop across M9 should be V_{DD} - 0.6 = 2.5 - 0.6 = 1.9V. Thus, taking L_9 as 0.25μm, W_9 is calculated to be,

$$W_9 = 4.5e-6 = 4.5\mu m \tag{2.39}$$

The aspect ratio of the biasing transistors M10 and M11 can be found in the same way as described above for M9. The widths of these transistors were found to be,

$$W_{10} = 9e-6 = 9\mu m \tag{2.40}$$

and,

$$W_{11} = 7.5e-6 = 7.5\mu m \tag{2.41}$$

2.3.2 Gain Stage and Gilbert Quad

Since the total current flowing through the core is 3mA, the current in each branch i.e., through each of the transistors M5 and M6 will be 1.5mA. Also M5 and M6 are assumed to be identical transistors and perfectly matched. Assuming a g_m of about 20mS for each of these transistors, their aspect ratios can be calculated.

$$g_{m5} = \sqrt{2\mu_n C_{ox} \frac{W_5}{L_5} I_{DS5}} \tag{2.42}$$

Substituting the appropriate values in the above equation of g_m, the aspect ratio of M5 is found to be, $\frac{W_5}{L_5} = 827$. With the value of $L_5 = 0.25$ μm, W_5 is calculated to be,

$$W_5 = 206.75e-6 = 206.75\mu m \tag{2.43}$$

Since M5 and M6 are identical, $W_6 = W_5$.

In the Gilbert quad, the transistors M1, M2, M3 and M4 are identical. The current flowing through each of these transistors would be 0.75 mA. The threshold voltage of these transistors is given by the equation,

$$V_{th} = V_{T0} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right) \tag{2.44}$$

Using the equation (2.32) and substituting the right values, gives the width of these transistors, which is

$$W_1 = W_2 = W_3 = W_4 = 67\mu m \tag{2.45}$$

2.3.3 LC Tuned Circuits

The design of the two tuned circuits follows. The left tuned circuit is assumed to be resonating at a frequency, $f_1 = 5.65$ GHz and the right tuned circuit at a frequency, f_2

= 5.85 GHz. The inductance values are chosen to be as low as possible because as the value of the inductance increases its series parasitic resistance also increases. For the left loop, the values of the inductors are L_1 = 3 nH and L_3 = 0.5 nH and for the right loop, L_2 = 2 nH and L_4 = 0.5 nH. Substituting these values in equations (2.28) and (2.30), the values of C_x and C_y are calculated to be equal to, $C_x = C_y$ = 1.85 pF.

The value of gate-source capacitance C_{GS} is calculated using the equation,

$$C_{GS} = \frac{2}{3} C_{ox} WL = 0.1pF \tag{2.46}$$

The values of the other capacitors are calculated as $C_1 = C_2$ = 250 fF and $C_5 = C_6$ = 1.5 pF.

2.4 Simulation Results and Inferences

A monolithic LC VCO has been designed and simulated using Cadence SpectreRF, that achieves a tuning range of around 130 MHz extending from 5.63 GHz to 5.77 GHz when the controlling voltage is varied from 1 V to 1.5 V. The center frequency is 5.7 GHz. The change of frequency with respect to voltage is almost linear in this range as shown in figure 2.14. The hand calculated values for the two extreme frequencies defined by the two resonators are 5.65 GHz and 5.85 GHz. There is about 0.87% difference between hand calculated and simulated values of the center frequency. A parametric sweep of the controlling voltage was performed using the Analog Design Environment in Cadence to obtain this plot.

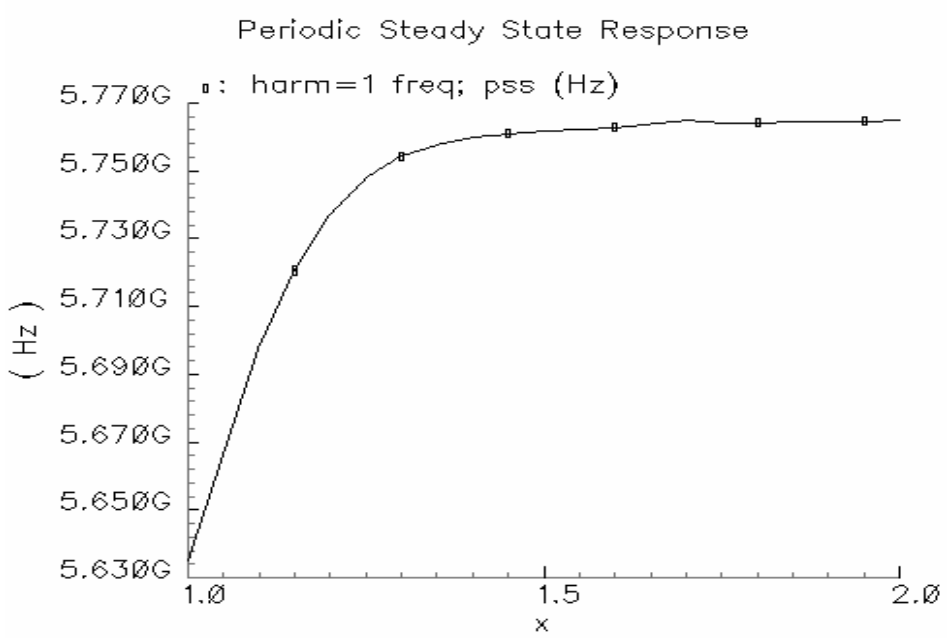


Figure 2.14 Plot showing the linear tuning range of the VCO

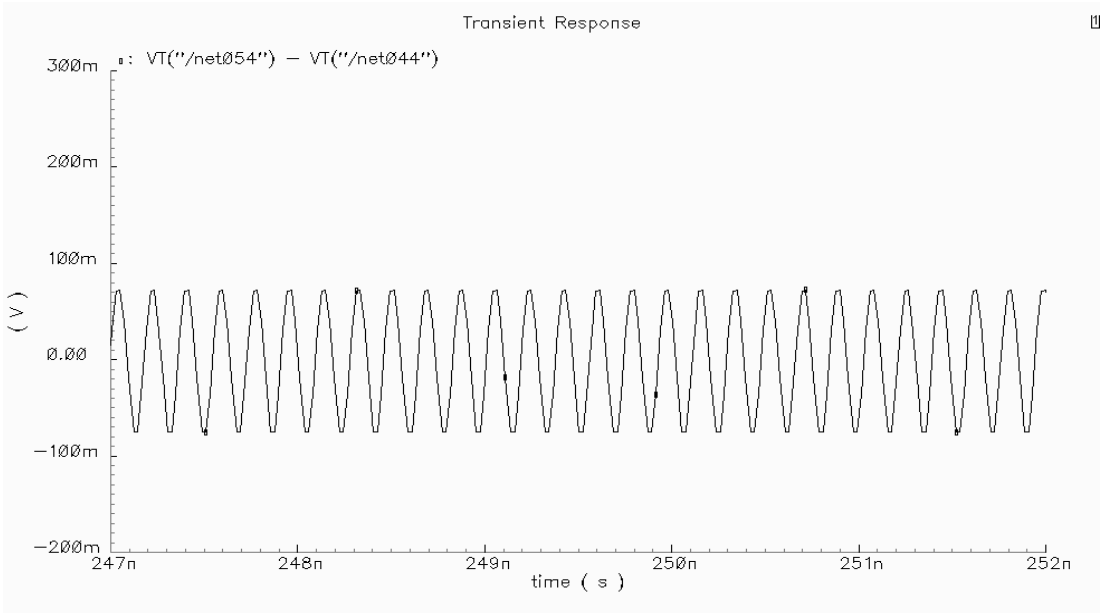


Figure 2.15 Transient response

Figure 2.15 shows the transient waveform of the VCO output and figure 2.16 below shows the Periodic Steady State (PSS) response of the VCO with respect to time. It shows just one period of the wave when the oscillator has achieved steady state

operation. PSS is performed using Cadence SpectreRF, a Spice implementation used to simulate high frequency RF circuits. During PSS simulation, it uses an estimate of the oscillation period provided by the designer to compute the precise period and the periodic solution waveforms.

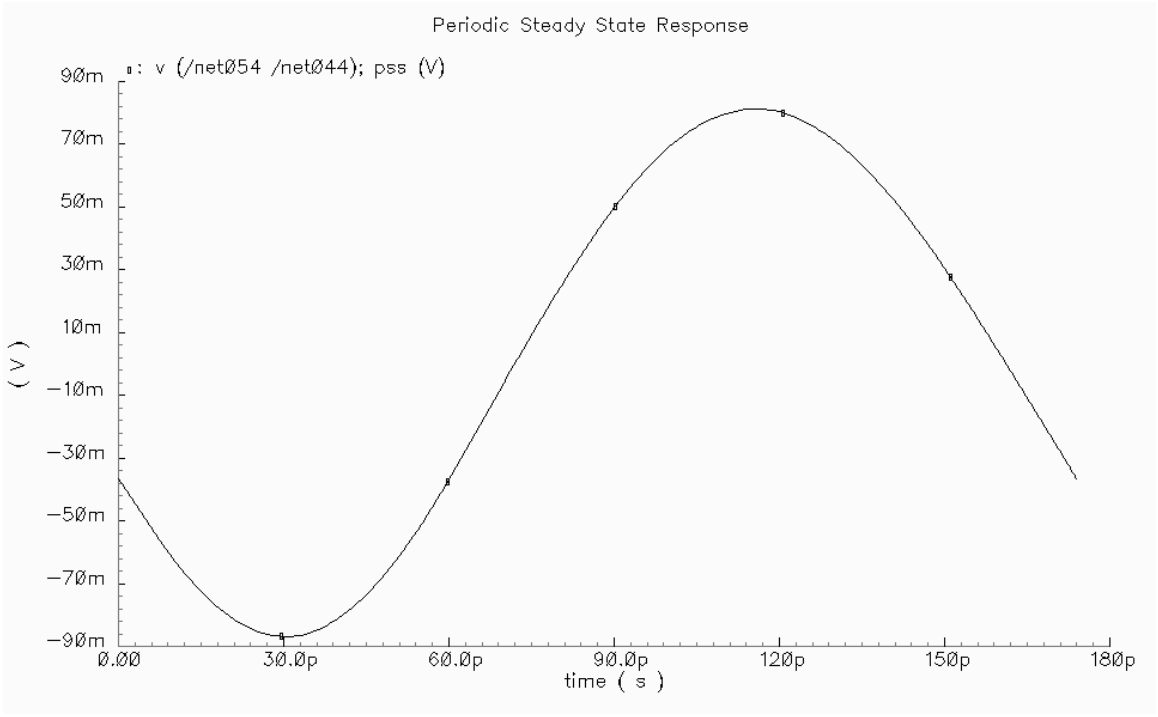


Figure 2.16 PSS waveform in time domain

Figure 2.17 shows the first harmonic frequency of the VCO at 5.748 GHz. This is the oscillating frequency of the VCO when the controlling voltage is set equal to 1.25 V.

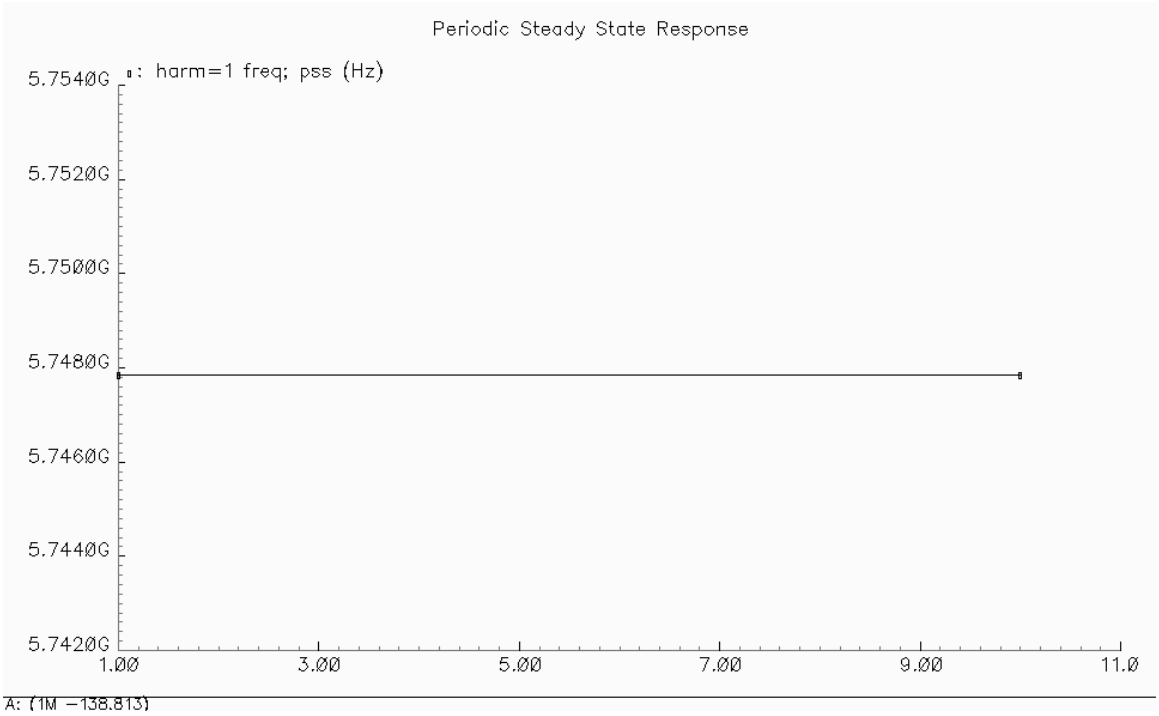


Figure 2.17 PSS showing first harmonic frequency

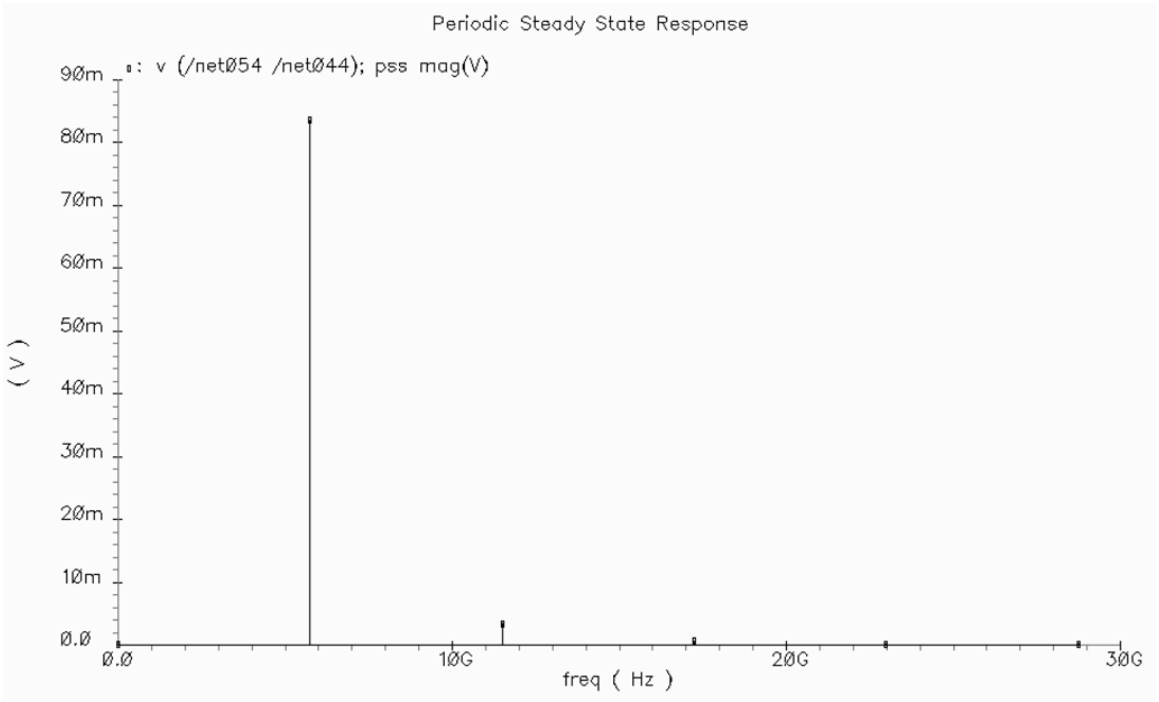


Figure 2.18 Voltage in magnitude of different harmonics

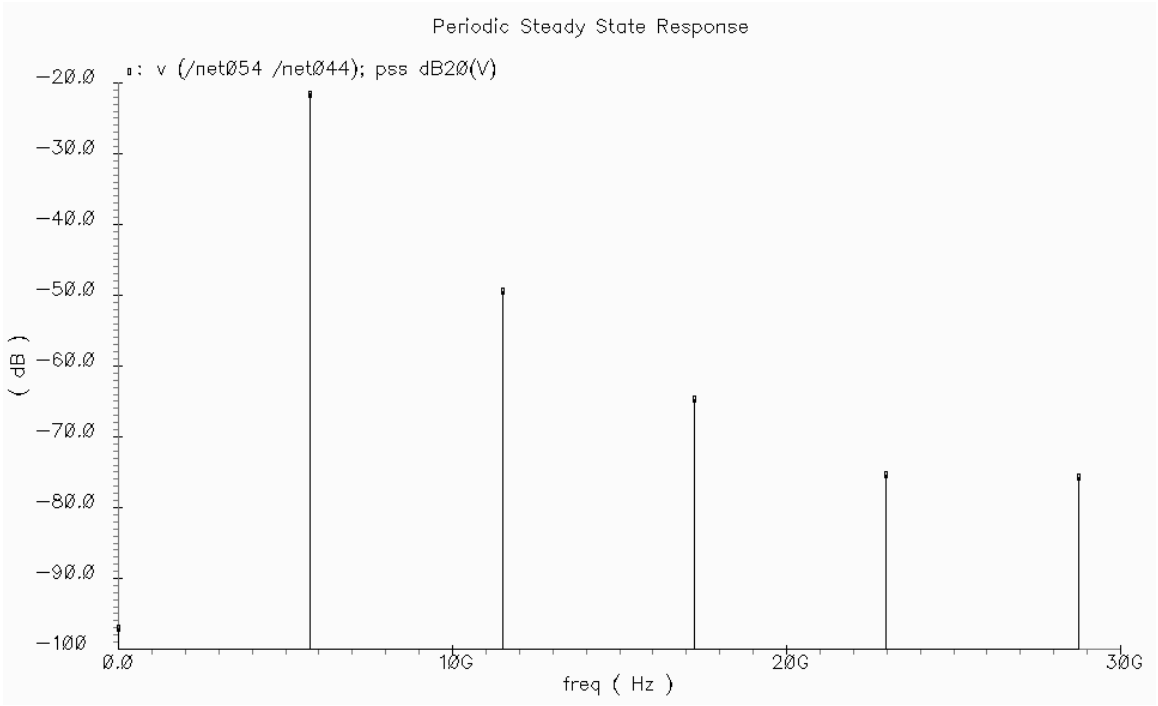


Figure 2.19 Voltage in dB of different harmonics

Figures 2.18 and 2.19 show the voltage levels of different harmonics in magnitude and dB respectively. It can be observed that the voltage level of the first harmonic is much above the other harmonics, which is desirable.

To obtain the phase noise and output noise of the circuit the Pnoise simulation option is used along with PSS in SpectreRF. Figure 2.20 is a plot of the phase noise of the circuit and 2.21, a plot of output noise. The phase noise of the circuit measured at an offset of 1 MHz is -114 dBc/Hz and the output noise measured at the same offset is -139 dB.

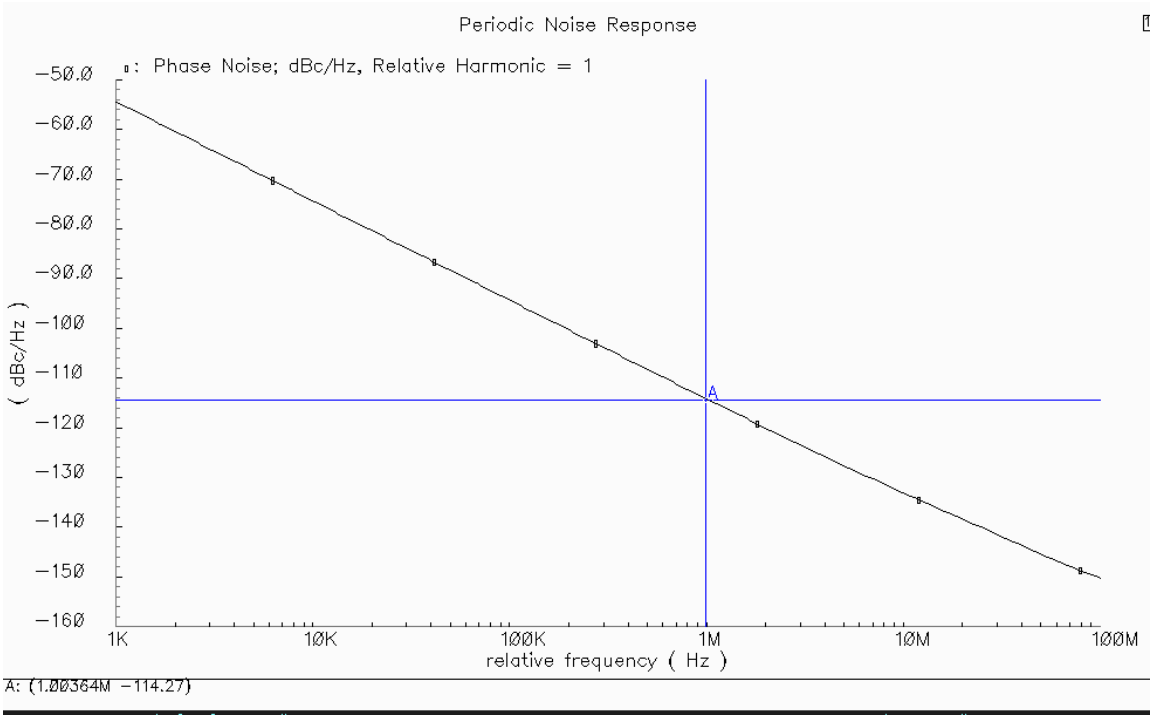


Figure 2.20 Phase noise of the VCO

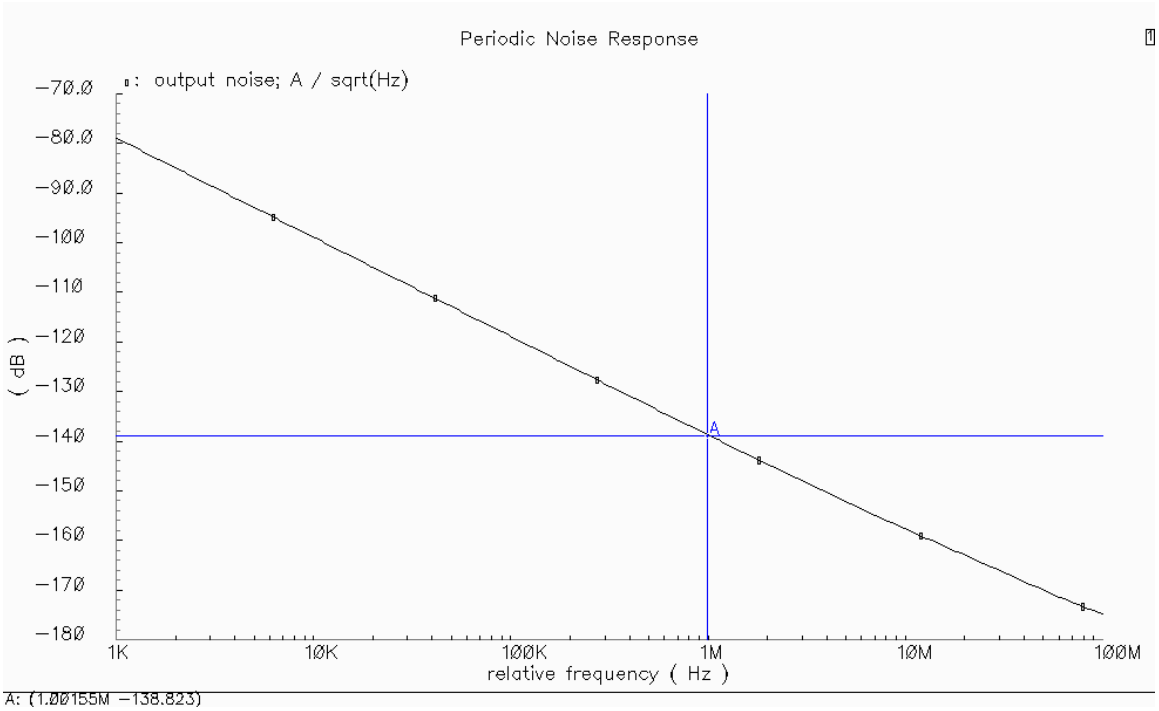


Figure 2.21 Output noise of the VCO

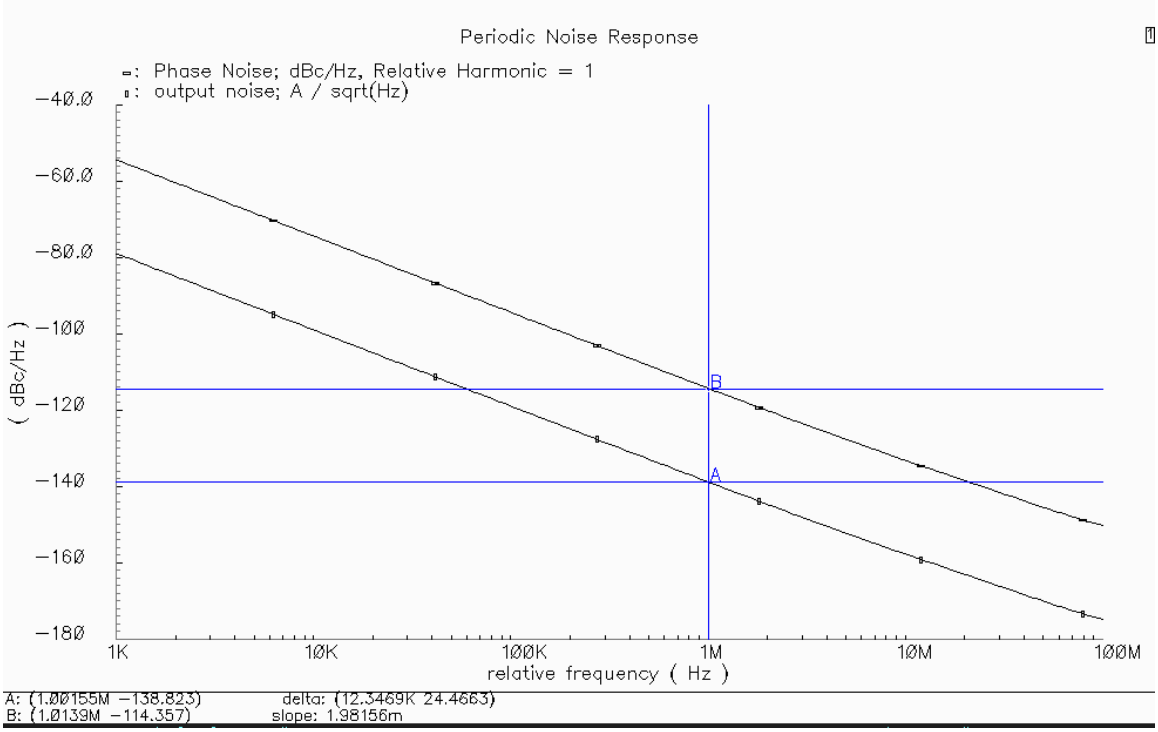


Figure 2.22 Output and phase noise of the VCO

Figure 2.22 shows both phase noise and output noise and it can be seen from this plot that phase noise is mostly the shifted version of the output noise. The output noise is scaled by the carrier amplitude to produce phase noise values. Figure 2.23 shows the output power at different frequencies in the tuning range and figure 2.24 is a plot of the same. It can be observed from these plots that an output power of about -12 dBm is achieved between 5.69 to 5.77 GHz. Below 5.69 GHz the output power is not significant, but it may be possible to improve this by increasing the current through the circuit.

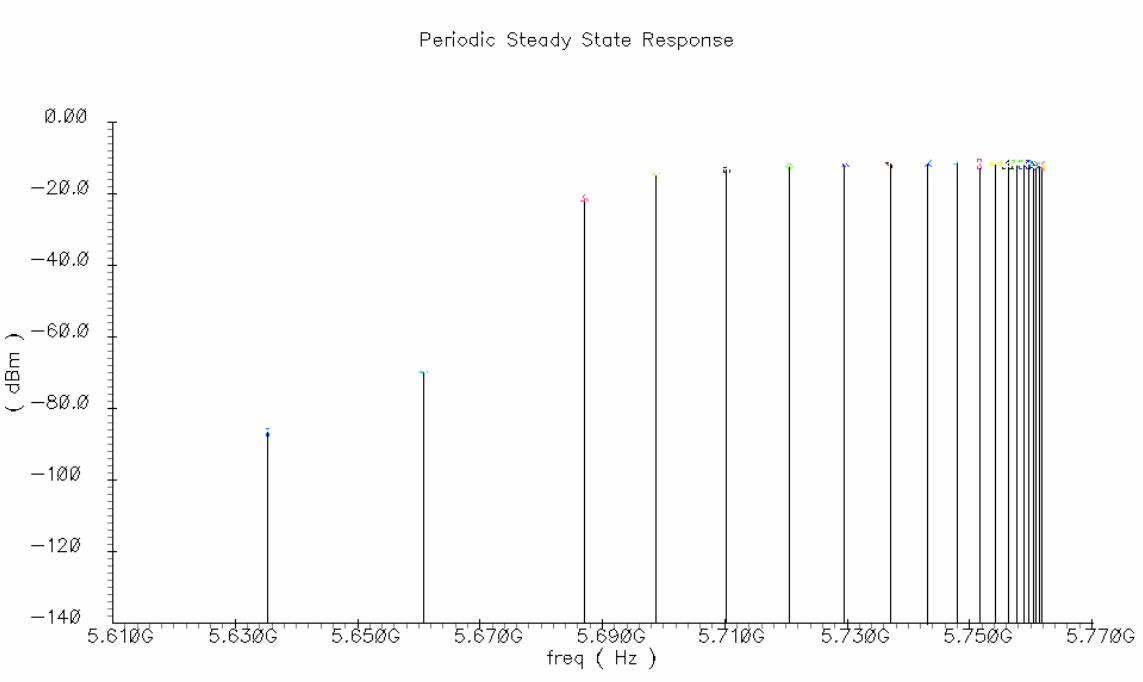


Figure 2.23 Output power at different frequencies

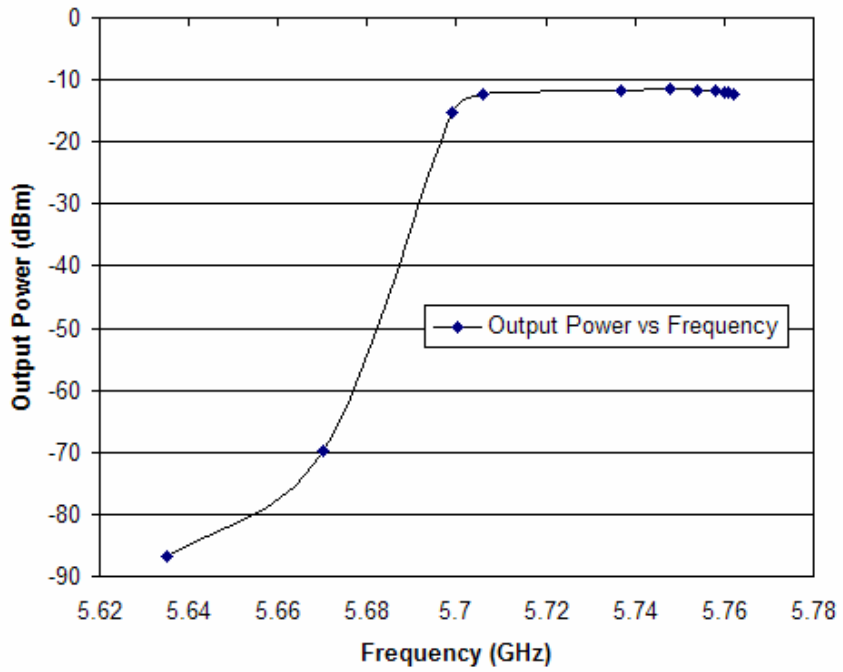


Figure 2.24 Plot of output power vs frequency

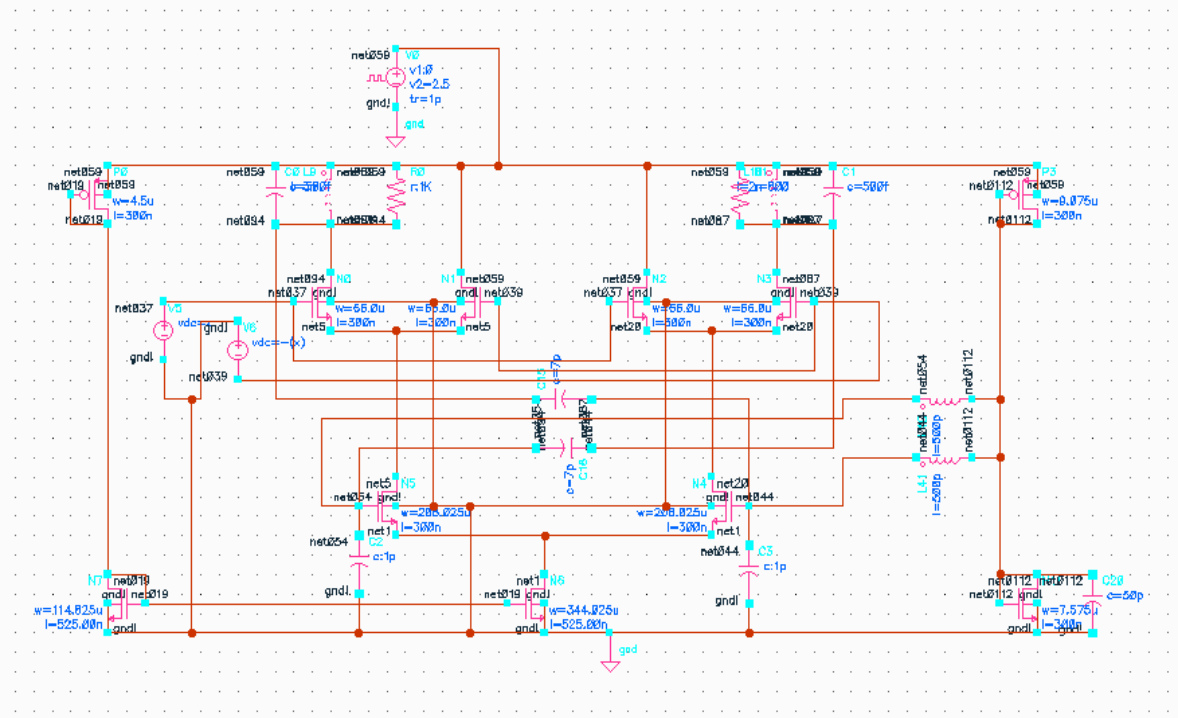


Figure 2.25 Cadence snap shot of figure 2.12

A Matlab analysis of the designed VCO follows. Recall the equation for loop gain of the complete circuit $A_v(s)$, repeated below for convenience and recall that α_1 and α_2 denote the fractions of bias current flowing through the two loops.

$$A_v(s) = \frac{v_y}{v_x} = \alpha_1 A_{v1}(s) + \alpha_2 A_{v2}(s) \tag{2.27}$$

The root locus for the VCO as a function of bias current is constructed using the characteristic equation derived from the expression $1 - A_v(s) = 0$. Figures 2.26, 2.27 and 2.28 show the root loci for $\alpha_1 > \alpha_2$, $\alpha_1 = \alpha_2$ and $\alpha_1 < \alpha_2$. It is observed from these figures that the circuit always has a pair of poles that travel to the right half plane ensuring that there is an oscillation build-up with sufficient loop gain.

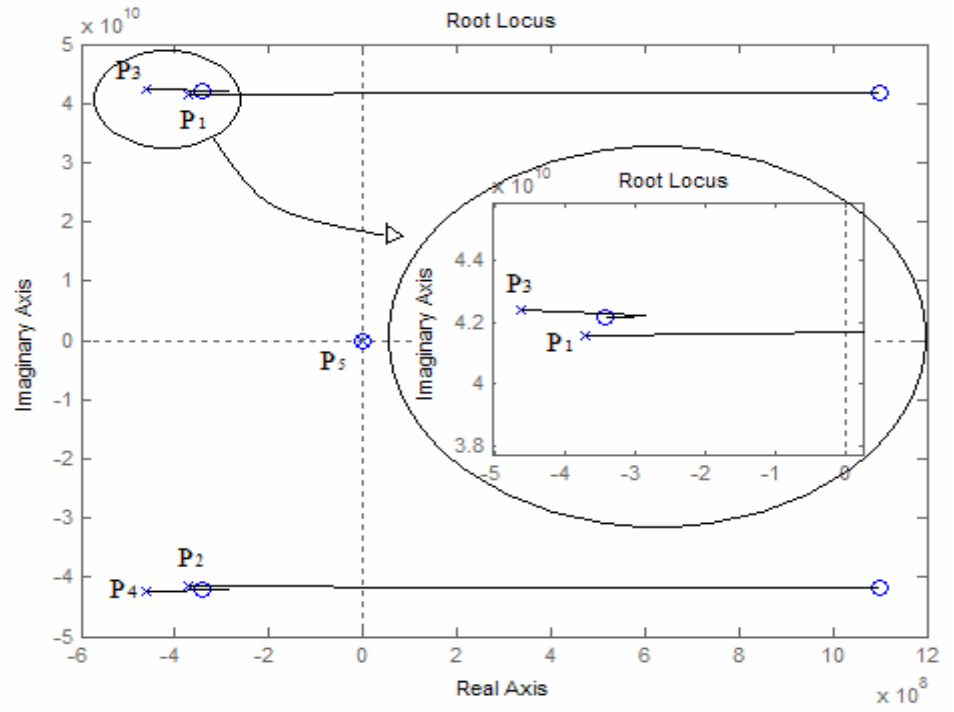


Figure 2.26 Root locus for $\alpha_1 > \alpha_2$

In Figures 2.26, 2.27 and 2.28 the inset pictures show how the poles change their positions depending upon loop gain. Pole P_1, contributed by the left tank always remains in the right half of the s-plane with sufficient loop gain and controls the oscillation of the circuit for $\alpha_1 \geq \alpha_2$. As α_2 becomes greater than α_1, pole P_3 contributed by the right tank remains in the right half of the s-plane with sufficient loop gain and takes over control of the oscillation. Poles P_2 and P_4 behave in a similar fashion.

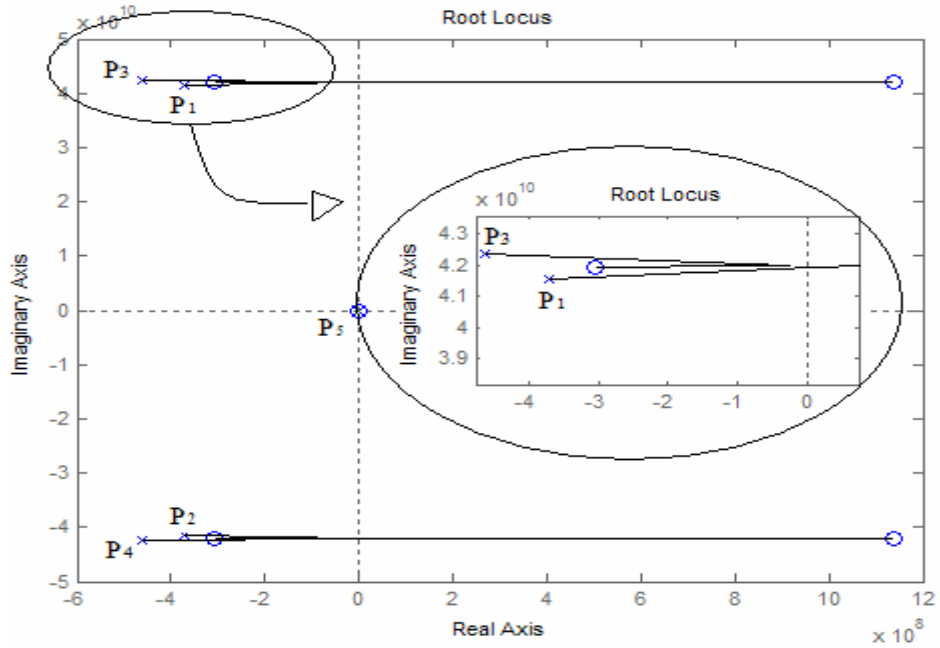


Figure 2.27 Root locus for $\alpha_1 = \alpha_2$

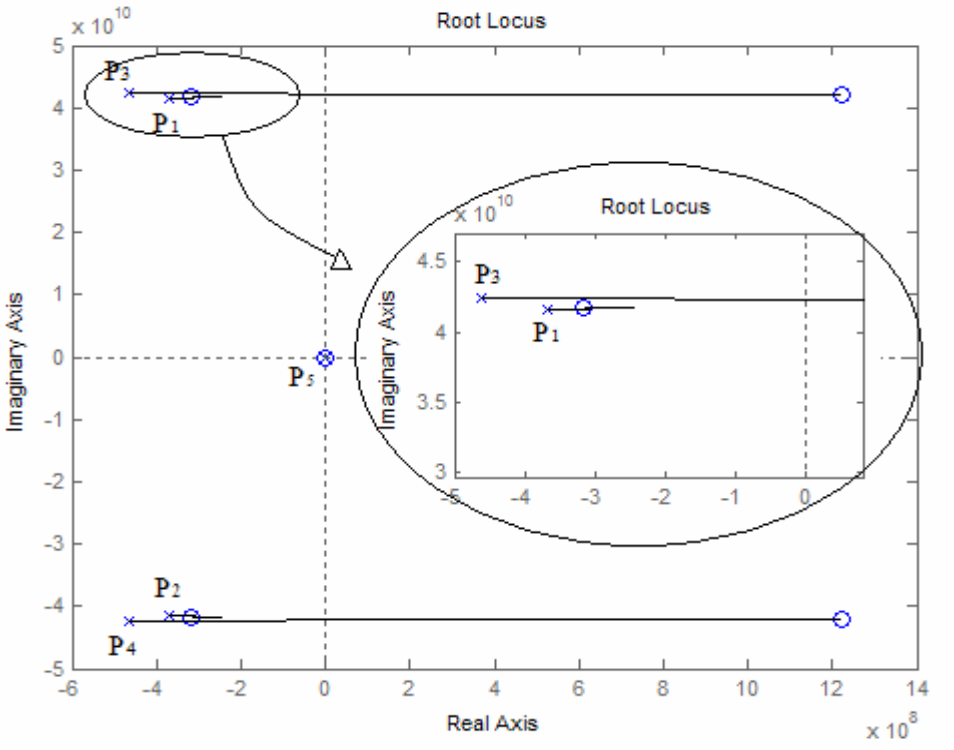


Figure 2.28 Root locus for $\alpha_1 < \alpha_2$

CHAPTER 3

FREQUENCY DIVIDER DESIGN

3.1 Introduction

In a PLL synthesizer, of all the PLL components, circuit design of the VCO and the frequency divider is very critical. The reason partly is these components operate at the highest frequencies within the PLL and also consume most of the power as compared to the other components. As part of this thesis, a digital frequency divider based on True Single Phase Clocking (TSPC) has been designed. It was more an attempt to learn the different aspects of digital design at high frequencies. This work is mostly based on the concepts provided in [20]. A divider with dual modulus of 256/288 has been designed to divide the band of frequencies specified for the 802.11a WLAN standard which is from 5.14 GHz to 5.72 GHz to a frequency of 20 MHz which forms the reference frequency to the frequency synthesizer. This work does not include a swallow counter needed for dynamic programmability.

3.2 Circuit Configuration and Working

The frequency divider designed here consists of three main blocks, a divide-by-2, a divide-by-8/9 and a divide-by-16 block, as shown in figure 3.1. The divide-by-8/9 prescaler whose structure is shown in figure 3.2 proves to be a rather critical block. The input frequency is first halved by a divide-by-2 circuit so that the speed constraints of this prescaler can be relaxed. The prescaler is usually followed by a program counter

and a swallow counter which allows to dynamically control the overall division ratio between 256 and 288 and to sweep the output frequency between 5.14 and 5.74 GHz in 20-MHz steps. Hence, the synthesized signal is suitable to operate both in the HiperLAN II bands [18] and in the 802.11a lower and middle bands [19], assuming direct-conversion or low-IF receiver architectures.

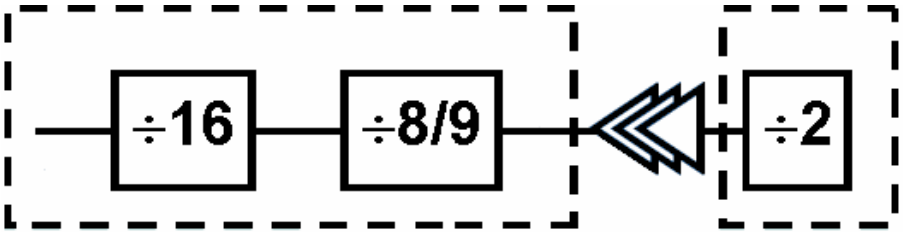


Figure 3.1 Block diagram of frequency divider

Generally, a TSPC logic flip-flop (FF) is used to synchronize the programmable divider output to the first divide-by-2 circuit output. This FF can cancel out the accumulated time jitter due to the divide-by-8/9 prescaler and the divide-by-16 program counter [12]. Two or three cascaded CMOS logic inverters are needed after the first divide-by-2 to drive the divide-by-8/9 prescaler and the synchronizing FF.

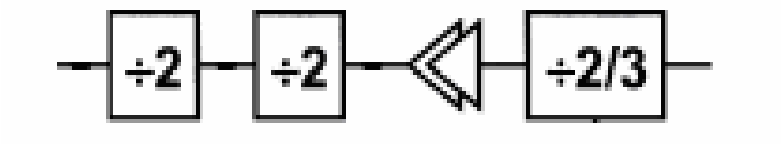


Figure 3.2 Divide-by-8/9 prescaler topology

3.2.1 Divide-by-2 Circuit

The divide-by-2 circuit realized in the TSPC logic is shown in figure 3.3. The salient feature of the TSPC clocking technique is that there is only one clock signal

needed to trigger the flip-flops and no extra clock phase is required whatsoever. This technique is mainly used in dynamic CMOS circuits and helps to simplify the design.

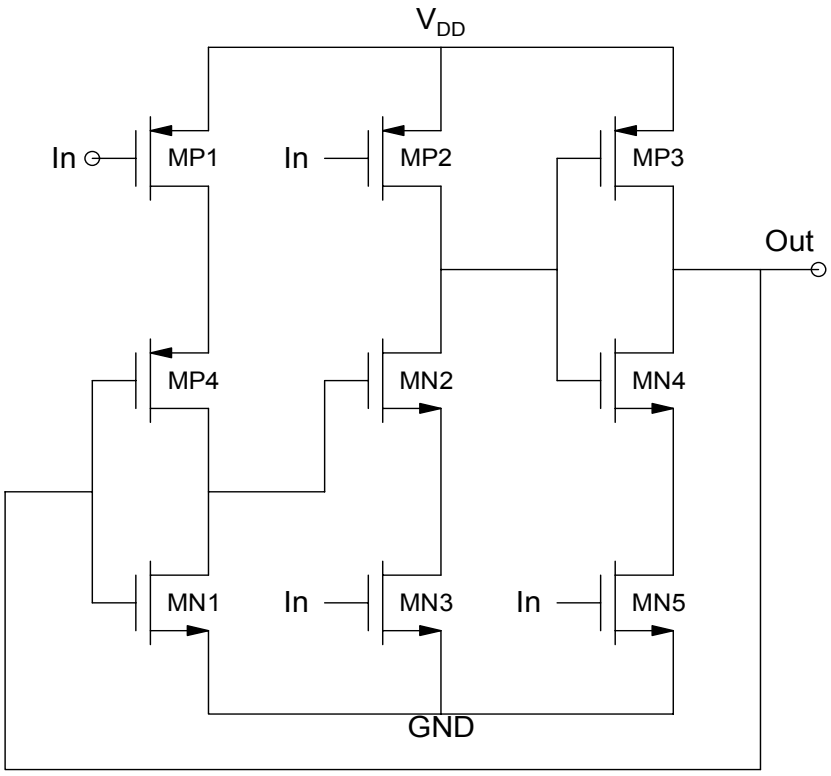


Figure 3.3 Circuit schematic of a TSPC divide-by-2

The circuit consists of three parts. The first part is a gated inverter that consists of MP1, MP4 and MN1, which passes the divider output to the following stage when In goes low. The second part is a latch stage that consists of MP2, MP3, MN2, MN3, MN4 and MN5. This circuit will be activated and store the output of the gated inverter when In is high. The PMOS transistors MP1 and MP2 are used to pre-charge the internal nodes to increase the speed of the circuit. The output of the flip-flop is directly connected back to the D-input to obtain the divide-by-2 function because the TSPC circuit can completely isolate the sense and latch stage at different phases of the clock

signal. The static power of the circuit is zero because no direct path from supply to ground exists and it only consumes dynamic power. One of the advantages of the TSPC divider is its simplicity. The circuit consists of only nine transistors. In some cases where the inverted output is required an inverter is included which adds two more transistors. The circuit requires an input signal of large amplitude, and it is very sensitive to the slope of the signal. Therefore, a high-frequency input buffer may sometimes be needed in front of the divider to drive it. The speed of the circuit greatly depends on the voltage supply. The circuit will be slow if a low-voltage supply is used. In order to operate at higher frequency, larger sizes of the transistors are needed to increase the g_m and thus make it operate faster. However, increasing the size also increases loading for the previous stage and thus the trade-off should be considered during design. Moreover, using larger transistor sizes will increase the degree of charge leakage and charge sharing at the output nodes and thus will affect the minimum operation frequency of the circuit.

3.2.2 Divide-by-8/9 Circuit

The divide-by-8/9 prescaler shown in figure 3.2 above, is comprised of a divide-by-2/3 synchronous divider and two asynchronous divide-by-2 circuits. While the latter are implemented again in TSPC logic, the divide-by-2/3 circuit has been realized using the extended true-single-phase-clock (E-TSPC) logic proposed in [21]. A block diagram representation and the schematic of the divide-by-2/3 circuit are shown in figure 3.4 and figure 3.5 respectively. Compared to the classical TSPC logic, the E-TSPC avoids the stacked MOS structure that slows the switching speed, and all the transistors are free

from the body effect. For these reasons, E-TSPC logic allows higher operating frequencies, although it features static power dissipation. However, this causes only a small increase in power dissipation, since at the frequencies of interest the dynamic power consumption is dominant over the standby current [21].

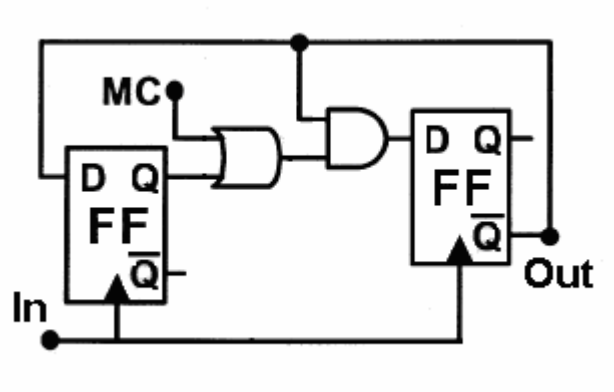


Figure 3.4 Block level representation of divide-by-2/3 circuit

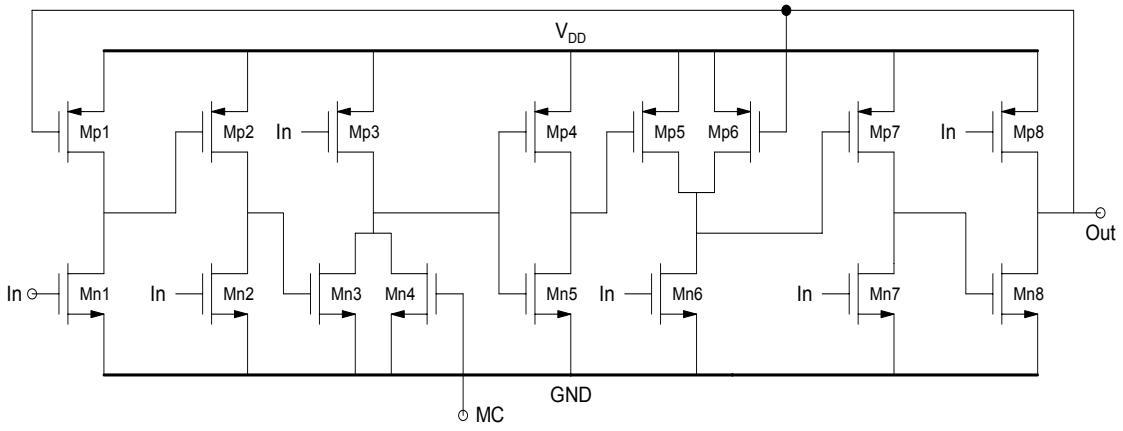


Figure 3.5 Schematic of divide-by-2/3 circuit

This logic also allows embedding complicated logic functions within the latches. This results in very compact circuits and in a reduced number of transistors. The concept is applied in the design of the divide-by-2/3 circuit, where the AND and the OR gates are realized by adding only one transistor each as evident from figure 3.4.

3.2.3 Divide-by-16 Circuit

The divide-by-16 program counter can be viewed as an extension of the divide-by-2 circuit. It is implemented by simply cascading four divide-by-2 circuits as shown in figure 3.6. The output of this circuit is fed into the frequency synthesizer where the PFD compares it with the reference frequency.

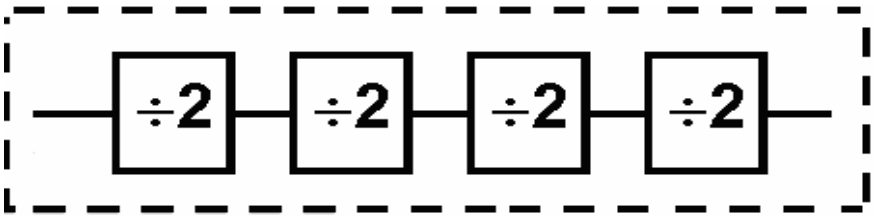


Figure 3.6 Block diagram of divide-by-16 circuit

3.3 Design Procedure

Detailed below is the approach followed to design the first divide-by-2 circuit. The divide-by-2 circuit schematic is shown in figure 3.3 and is repeated below for convenience. Consider that this circuit is divided into three stages, the first made up of transistors MP1, MP4 and MN1, the second made up of MP2, MN2 and MN3 and the third made up of MP3, MN4 and MN5. The output of this divider has to drive both the input of the following stage and an inverter in its own first stage, both of which appear to the output simply as capacitive loads. Besides these capacitive loads there are other capacitances that should be considered like the interconnect capacitance and the parasitic capacitances of the output transistors.

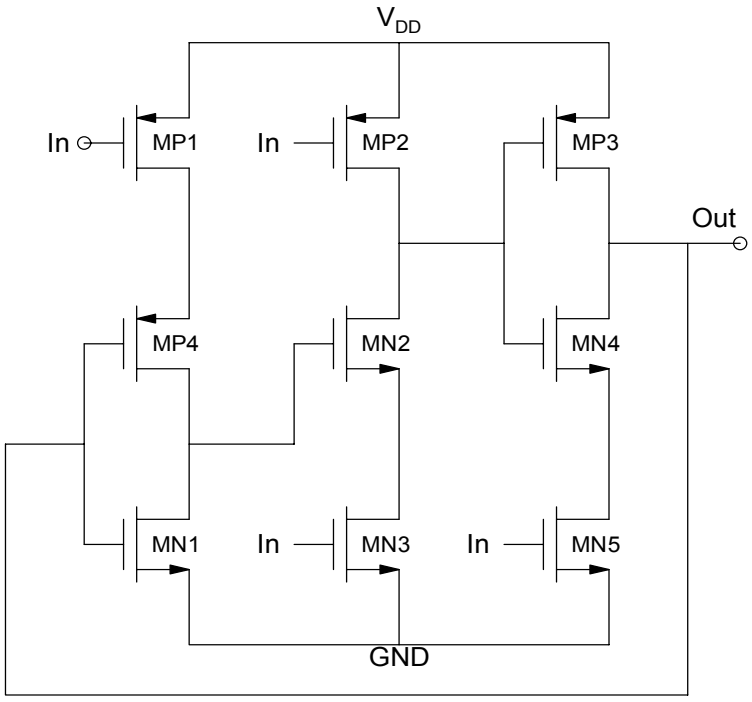


Figure 3.3 Circuit schematic of divide-by-2

To begin designing, a frequency of operation f_{out} is assumed for the circuit. From this, the approximate switching time is obtained as,

$$\tau_{sw} = \frac{1}{f_{out}} \tag{3.1}$$

Switching time is made up of rise time τ_{LH} and fall time τ_{HL},

$$\tau_{sw} = \tau_{LH} + \tau_{HL} \tag{3.2}$$

and τ can also be written as,

$$\tau = R \bullet C \tag{3.3}$$

Consider the third stage of the divide-by-2 circuit made up of transistors MP3, MN4 and MN5 as shown in figure 3.7. The figure also shows the various capacitances to be considered while designing this stage. The sum of parasitic capacitances

associated with the output transistors MP3 and MN4 is denoted as C_0. The equations for C_0, CL and C_x are,

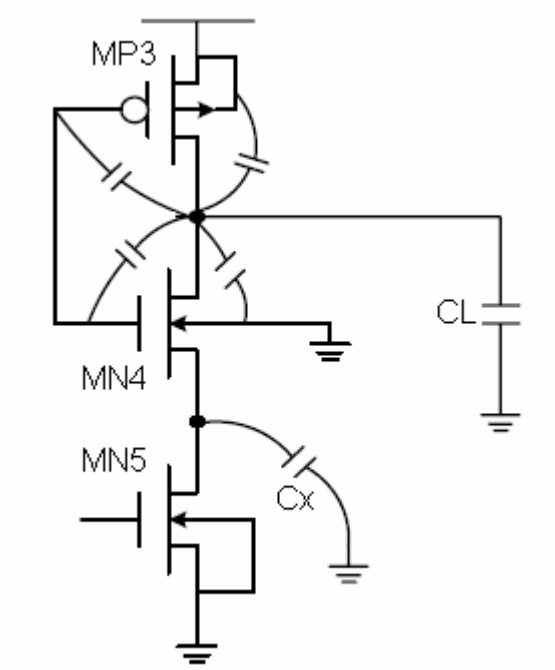


Figure 3.7 Third stage of divide-by-2 circuit showing capacitances

$$C_0 = C_{GD_{MP3}} + C_{DB_{MP3}} + C_{GD_{MN4}} + C_{DB_{MN4}} \tag{3.4}$$

where C_{GD} is the gate-to-drain capacitance and C_{DB} is the drain-to-bulk capacitance.

$$CL = C_{L1} + C_{L2} + C_{\text{int}} \tag{3.5}$$

where CL represents total load capacitance, C_{L1} is the input capacitance looking into the next stage which is given as,

$$C_{L1} = C_{ox}WL \tag{3.6}$$

(here W and L denote the gate width and length respectively, of the transistor being driven in the next stage, C_{ox} (= ε_{ox}/t_{ox}) is the gate oxide capacitance,) C_{L2} is the

capacitance looking into the inverter in the first stage of this same circuit (refer figure 3.3),

$$C_{L2} = (C_{ox}WL)_{MP4} + (C_{ox}WL)_{MN1} \tag{3.7}$$

and C_{int} is the interconnect capacitance (the parasitic capacitance associated with the metal layer forming the connection and the substrate).

$$C_x = C_{GS_{MN4}} + C_{SB_{MN4}} + C_{GD_{MN5}} + C_{DB_{MN5}} \tag{3.8}$$

where C_{GS} is the gate-to-source capacitance and C_{SB} is the source-to-bulk capacitance. A table given below shows the formulae for the calculation of C_{GS} and C_{GD}, when the transistor is operating in different regions.

Table 3.1 Transistor Parasitic Capacitance Formulae

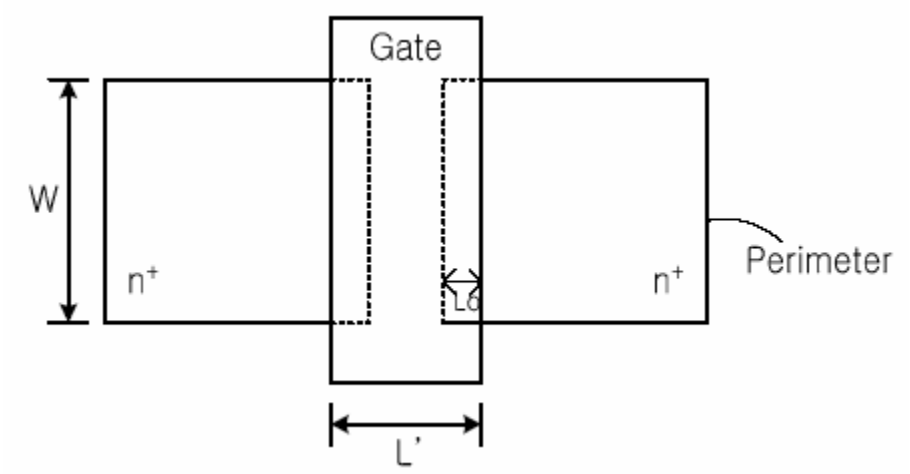
Region of operation	**C_{GS}**	**C_{GD}**
Cut-off	0	0
Linear	½ C_{ox}WL	½ C_{ox}WL
Saturation	2/3 C_{ox}WL	0

The source-to-bulk C_{SB} and drain-to-bulk C_{DB} capacitances are given as,

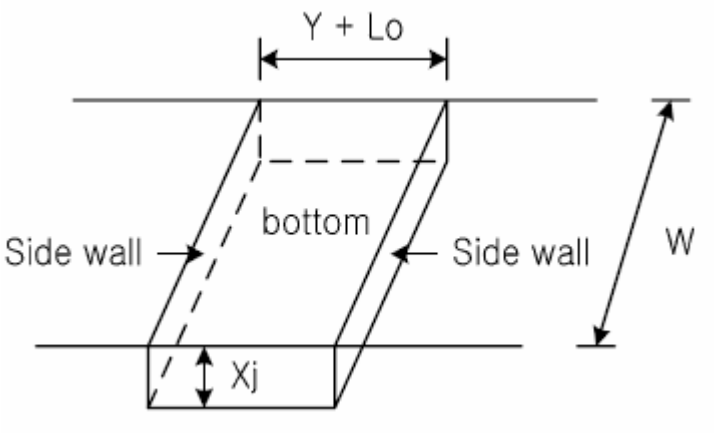
$$C_{SB} = C_{DB} = C_{j0}W(Y + L_0) + C_{j0sw}x_j.2(W + Y + L_0) \tag{3.9}$$

where C_{j0} denotes the zero-bias capacitance per unit area of the bottom of the source or drain region, Y denotes the effective length of the source or drain region, L_0 denotes the gate overlap capacitance, C_{j0sw} denotes the zero-bias sidewall capacitance per unit perimeter of the source or drain and x_j denotes the junction depth. Figure 3.8 below, helps to understand these terms better. Further information and related derivations are

provided in [17]. The values for C_{j0}, C_{j0sw}, L_0 and x_j can usually be found in the model file for the CMOS technology being used. The model file used for this design is provided in appendix B.



(a)



(b)

Figure 3.8 (a) NMOS transistor layout showing gate, drain and source and (b) detailed view of source/drain

In order to calculate the switching times, RC modeling [17] can be used where the transistor is modeled as a resistor driving a capacitance. It can be observed from

figure 3.7 that the rise time τ_{LH} depends mainly on the PMOS transistor MP3 through which the output node capacitance is charged. Therefore τ_{LH} can be given as,

$$\tau_{LH} = S_p \tau_p \tag{3.10}$$

where S_p is the voltage dependent scaling multiplier given by the equation,

$$S_P = \frac{2\left(|V_{TP}| - V_0\right)}{V_{DD} - |V_{TP}|} + \ln\left(\frac{2\left(V_{DD} - |V_{TP}|\right)}{V_0} - 1\right) \tag{3.11}$$

(Here V_{TP} it the PMOS threshold voltage and V_0 = 10% of V_{DD} as rise time is defined as the time taken for the signal to rise from 10% to 90% of V_{DD}). The derivation for S_p is given in [17].

$$\tau_P = R_p C_{out} \tag{3.12}$$

where R_p denotes the equivalent resistance between the source and drain of the PMOS transistor MP3 and is given by the equation below,

$$R_P = \frac{1}{k_p^{'}\left(\frac{W}{L}\right)_{MP3}\left(V_{DD} - |V_{TP}|\right)} \tag{3.13}$$

The variable $k_p^{'} = \mu_P C_{ox}$, μ_P denotes the mobility of holes, and C_{out} is the total output capacitance given by the equation,

$$C_{out} = C_0 + CL \tag{3.14}$$

Similarly from figure 3.7, it can be observed that the fall time τ_{HL}, defined as the time taken for the signal to fall from 90% to 10% of V_{DD}, depends on the two transistors, MN4 and MN5, since they form the discharge path for the output capacitance node. τ_{HL} given as,

$$\tau_{HL} = S_N \tau_N \tag{3.15}$$

Here again S_N is the voltage dependent scaling multiplier given by the equation,

$$S_N = \frac{2(V_{TN} - V_0)}{V_{DD} - V_{TN}} + \ln\left(\frac{2(V_{DD} - V_{TN})}{V_0} - 1\right) \tag{3.16}$$

where V_{TN} is the NMOS threshold voltage. Now, τ_N is given as,

$$\tau_N = (R_{N1} + R_{N2})C_{out} + R_{N2}C_x \tag{3.17}$$

where R_{N1} and R_{N2} denote the equivalent resistances of the NMOS transistors MN4 and MN5 and are given by the equations below,

$$R_{N1} = \frac{1}{k_N^{'}\left(\frac{W}{L}\right)_{MN4}(V_{DD} - V_{TN})} \tag{3.18}$$

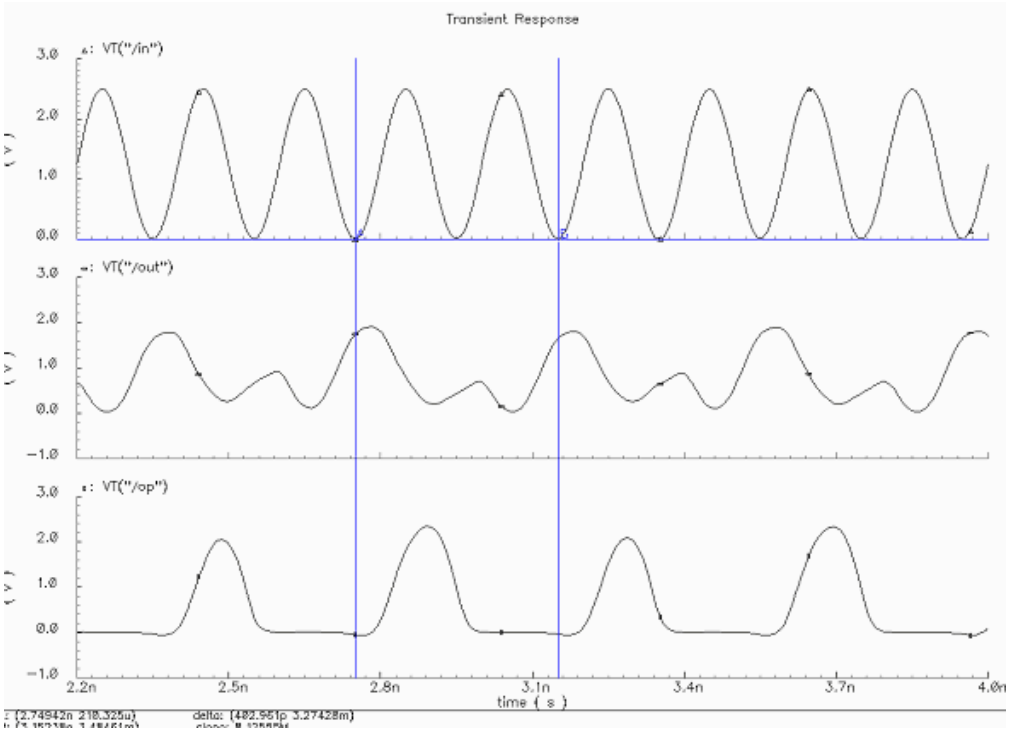
$$R_{N2} = \frac{1}{k_N^{'}\left(\frac{W}{L}\right)_{MN5}(V_{DD} - V_{TN})} \tag{3.19}$$

C_{out} and C_x are the same as defined before by equations 3.14 and 3.8 respectively.

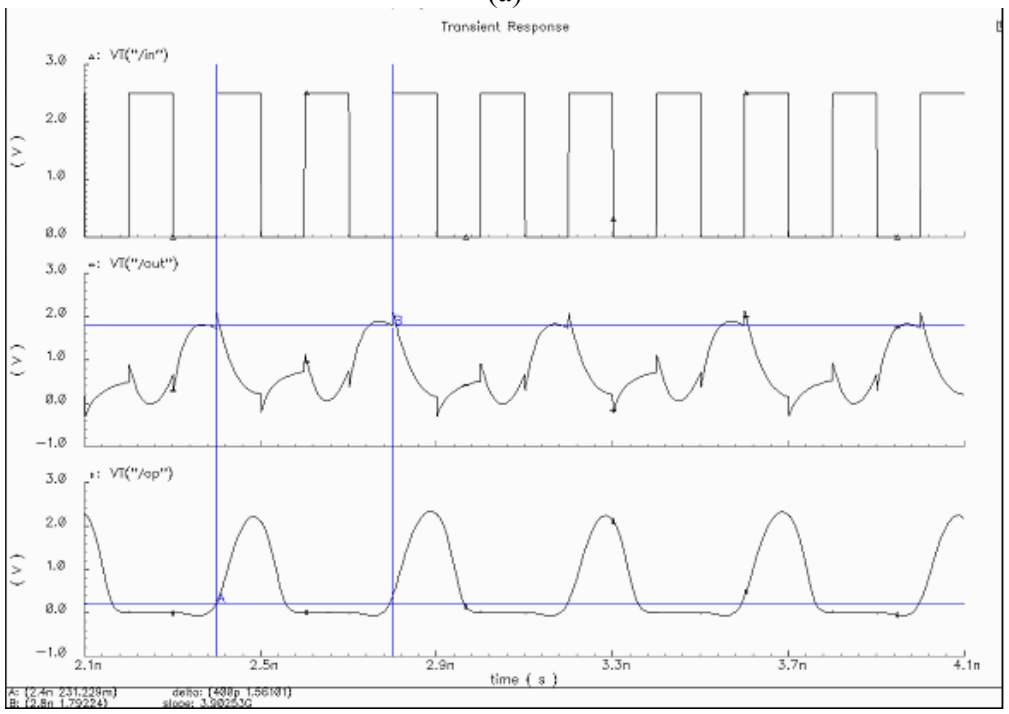
The design procedure outlined above was followed for the design of the second and first stage of the divide-by-2 circuit. The divide-by-2/3 circuit was designed as stated in [20].

3.4 Simulation Results and Inferences

A frequency divider has been designed to operate at a frequency of 5 GHz. The circuit was simulated using the Cadence Spectre Tool. The transient response of the circuit to both sine wave and square wave input is shown in the plots that follow.



(a)



(b)

Figure 3.9 Transient response of divide-by-2 circuit to (a) sine wave input and (b) square wave input

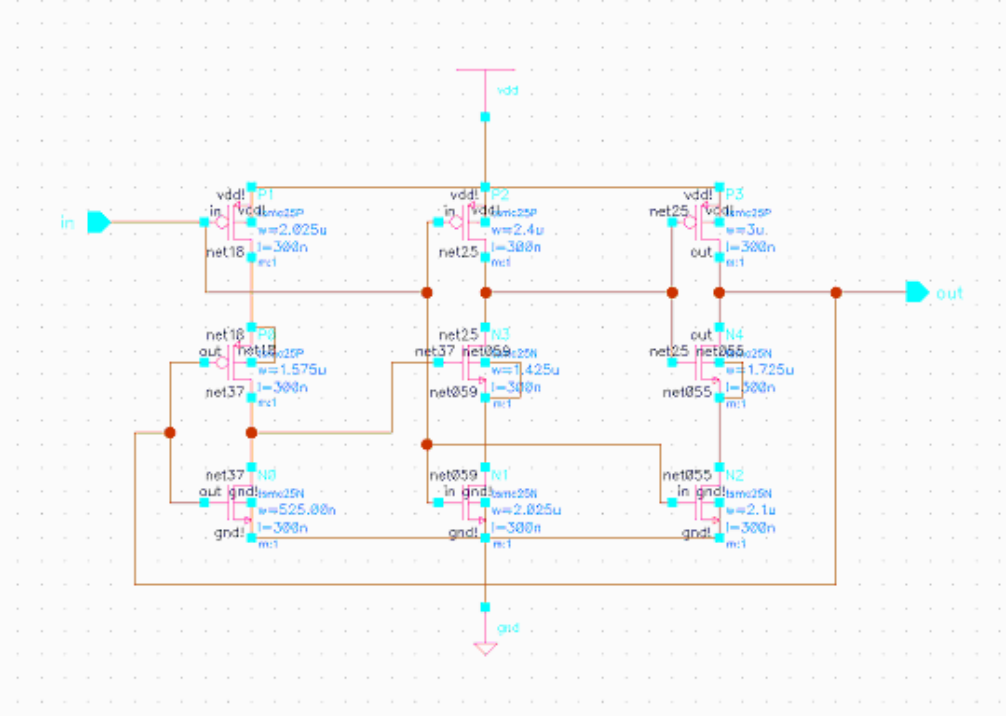
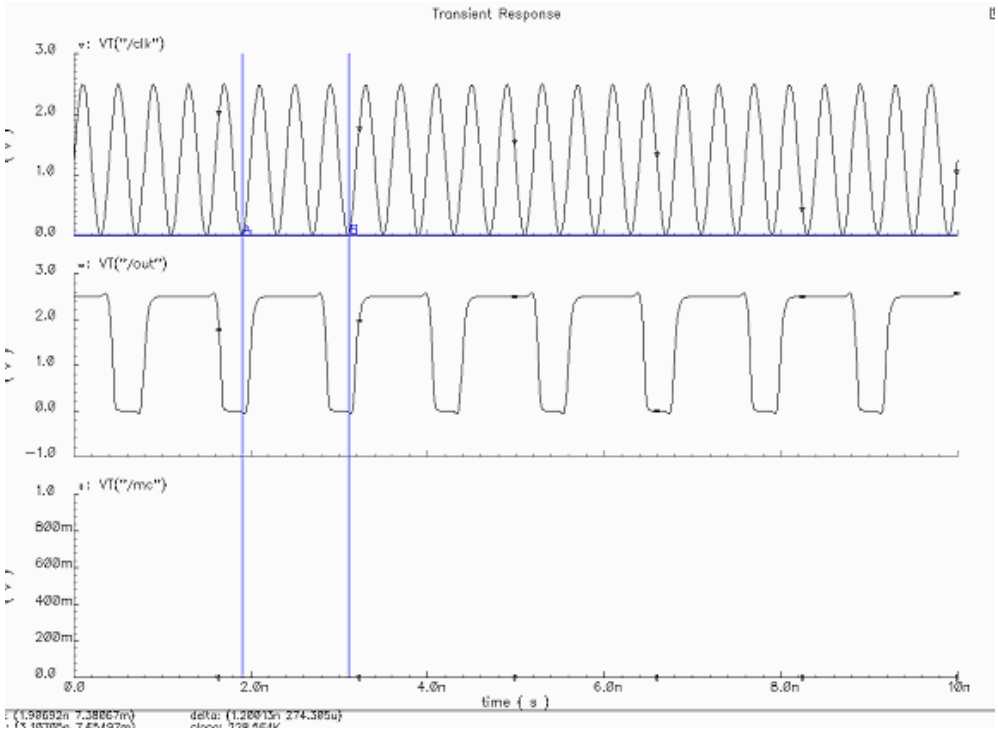
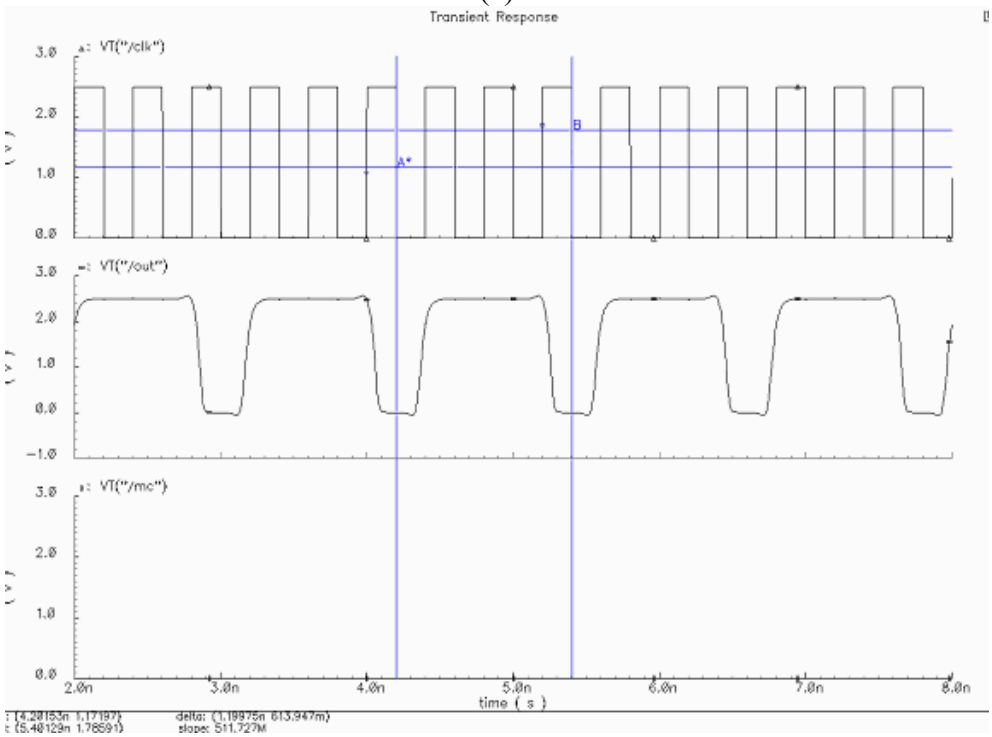


Figure 3.10 Cadence schematic of divide-by-2 circuit (refer figure 3.3)

The divide-by-2/3 circuit has a control input MC. By applying the right voltage at the control input the divider can be configured to work as either a divide-by-2 or divide-by-3. If divide-by-2 operation is required MC should be set to a binary value of 1 (2.5 V) and if divide-by-3 operation is required MC should be set to a binary value of 0 (0 V). The waveforms are shown in figures 3.11 and 3.12.

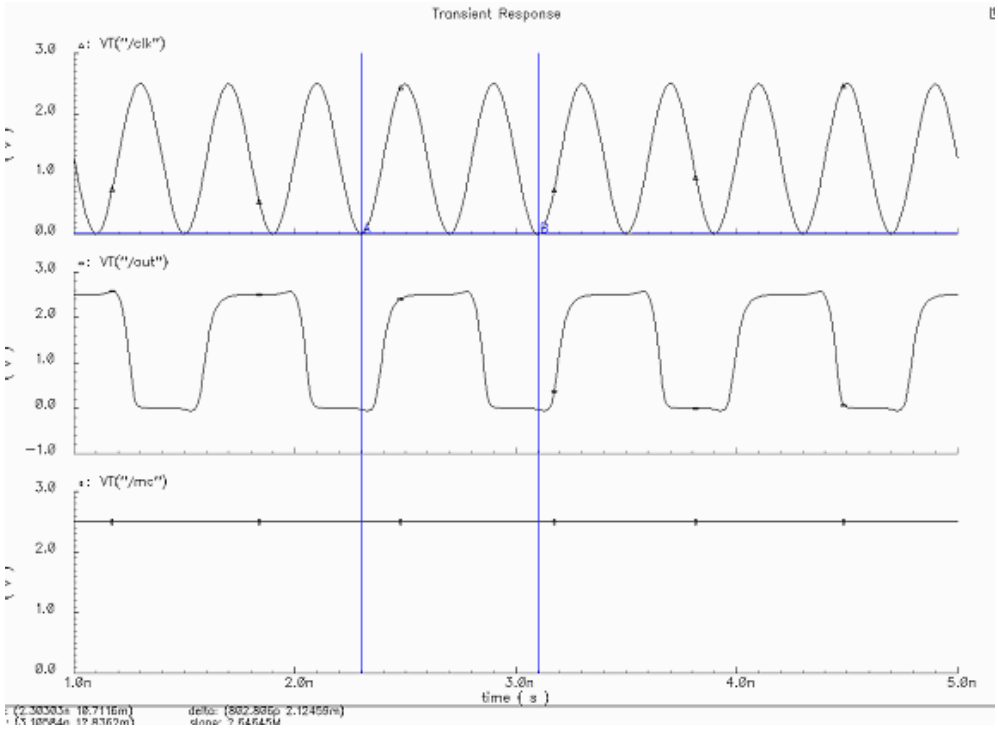


(a)

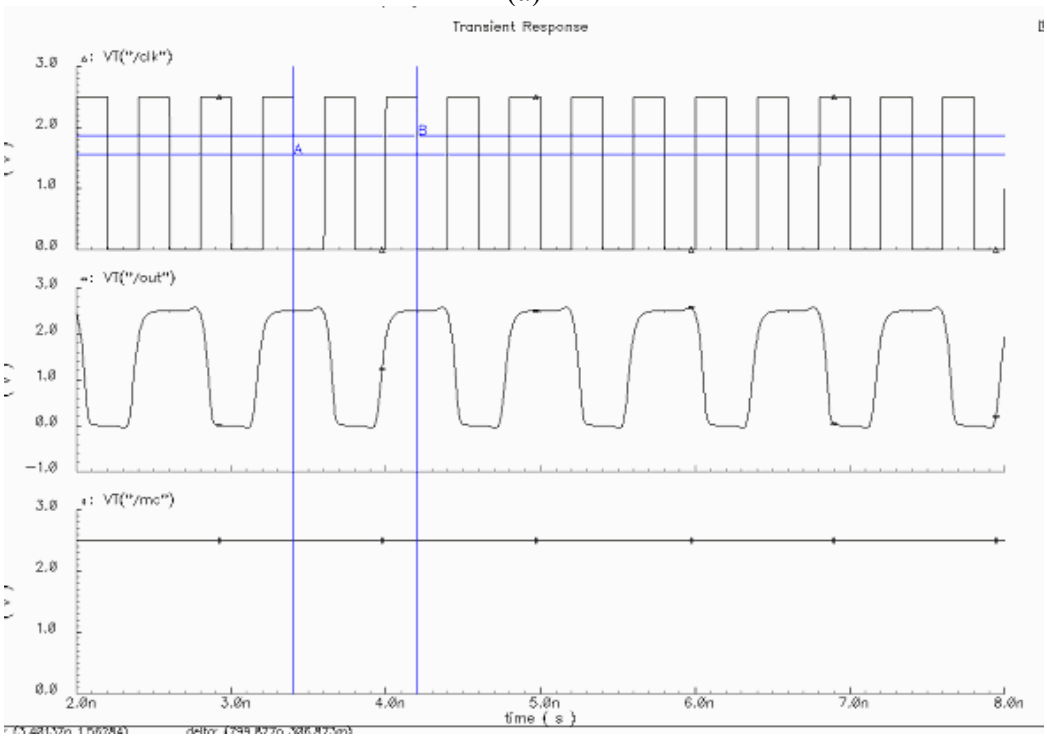


(b)

Figure 3.11 Transient response of divide-by-2/3 circuit with control input MC = 0, to (a) sine wave input and (b) square wave input



(a)



(b)

Figure 3.12 Transient response of divide-by-2/3 circuit with control input MC = 1, to (a) sine wave input and (b) square wave input

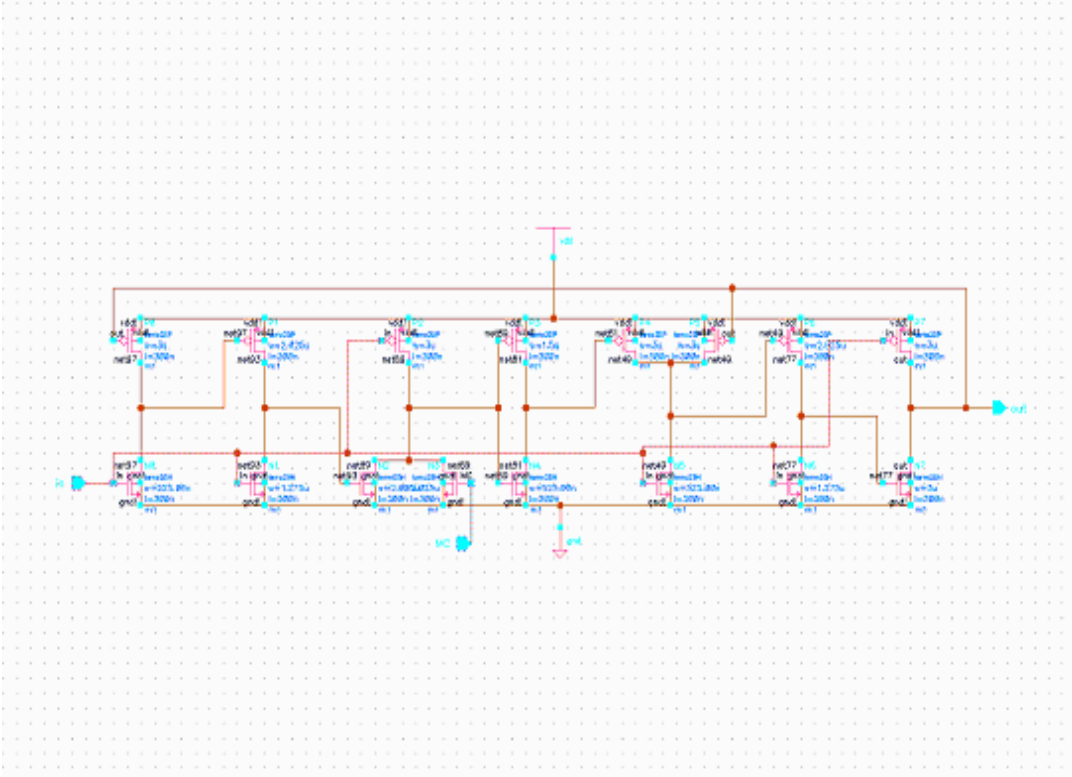
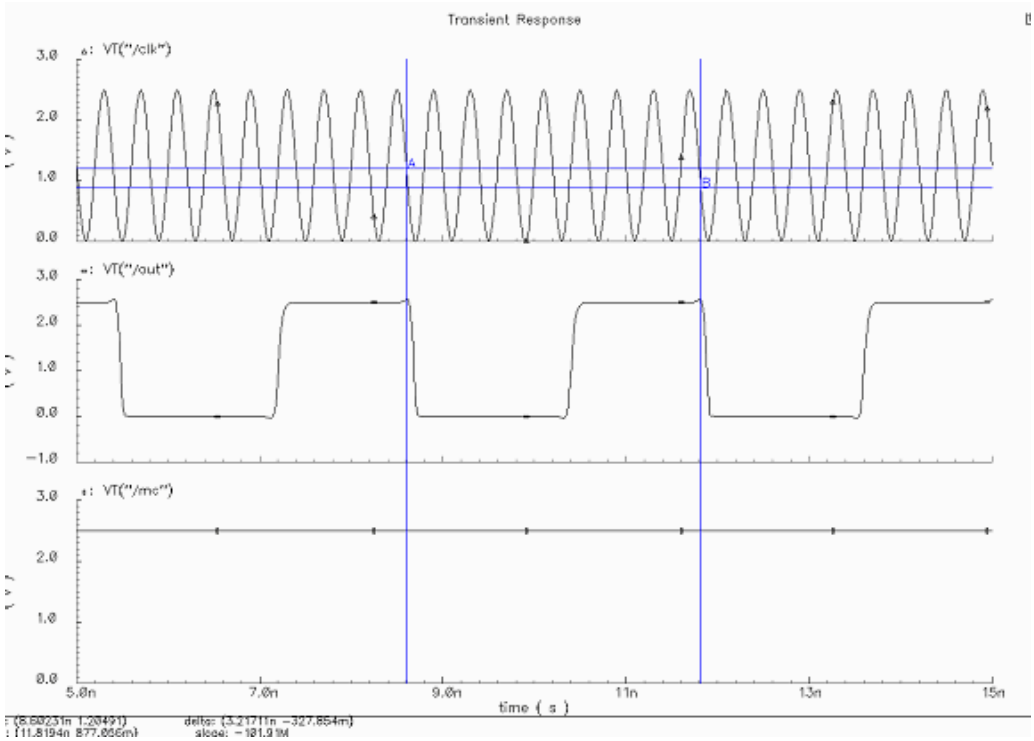
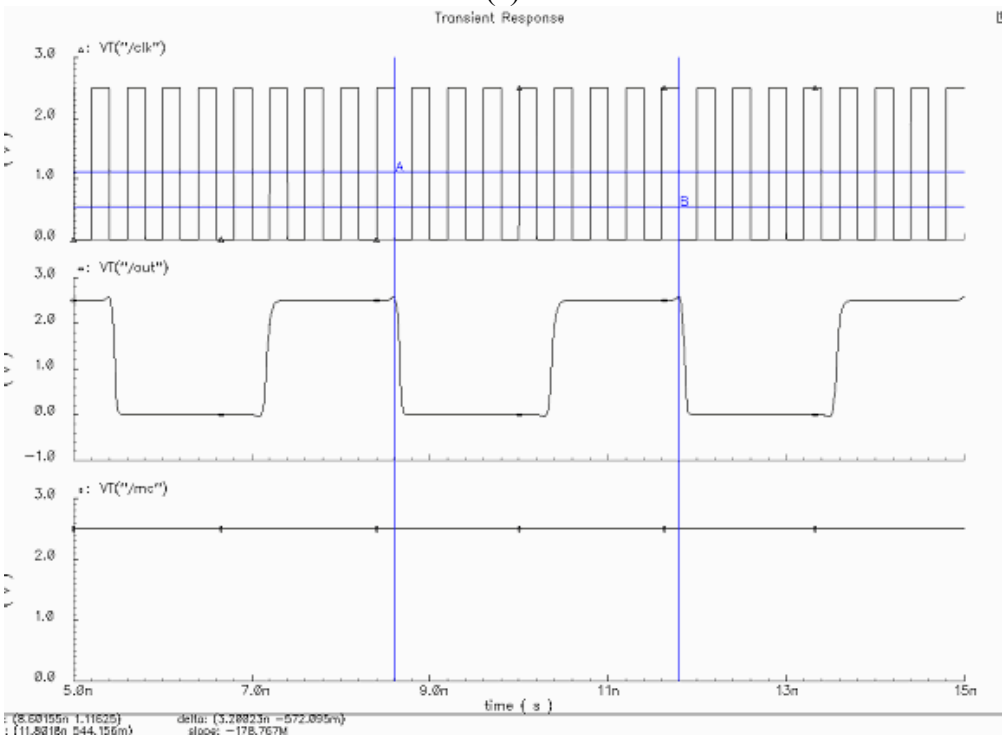


Figure 3.13 Cadence schematic of divide-by-2/3 circuit (refer figure 3.5)

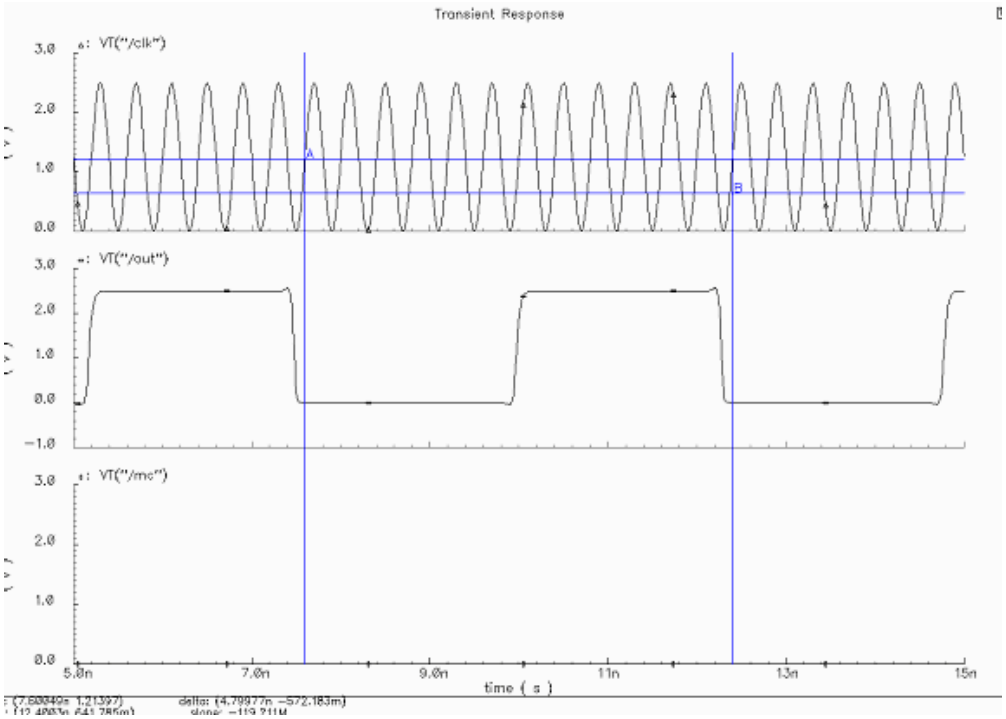


(a)

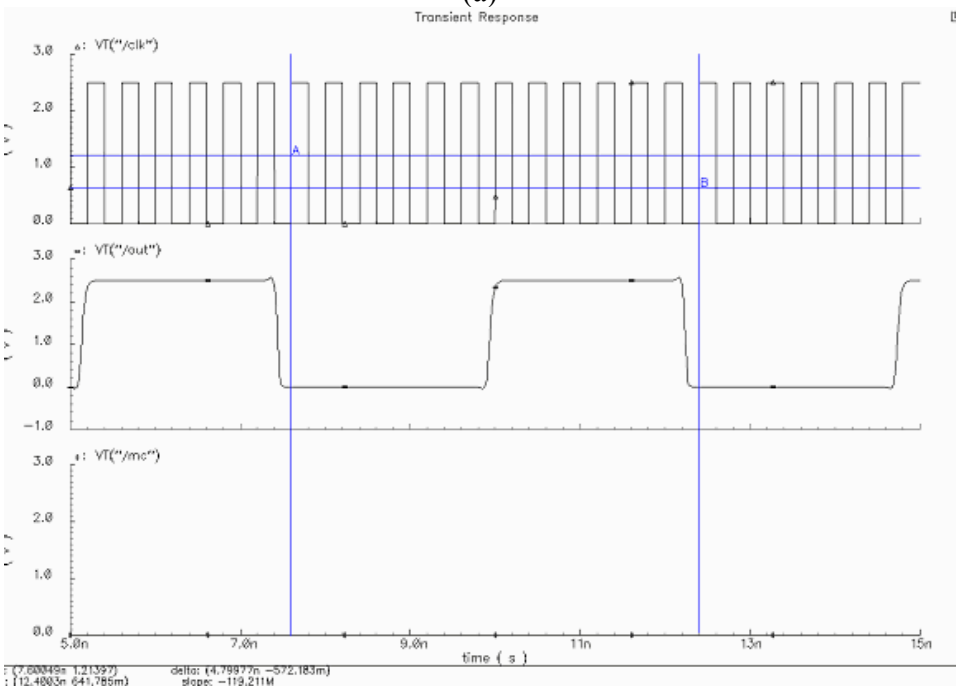


(b)

Figure 3.14 Transient response of divide-by-8/9 circuit with control input MC = 1, to (a) sine wave input and (b) square wave input



(a)



(b)

Figure 3.15 Transient response of divide-by-8/9 circuit with control input MC = 0, to (a) sine wave input and (b) square wave input

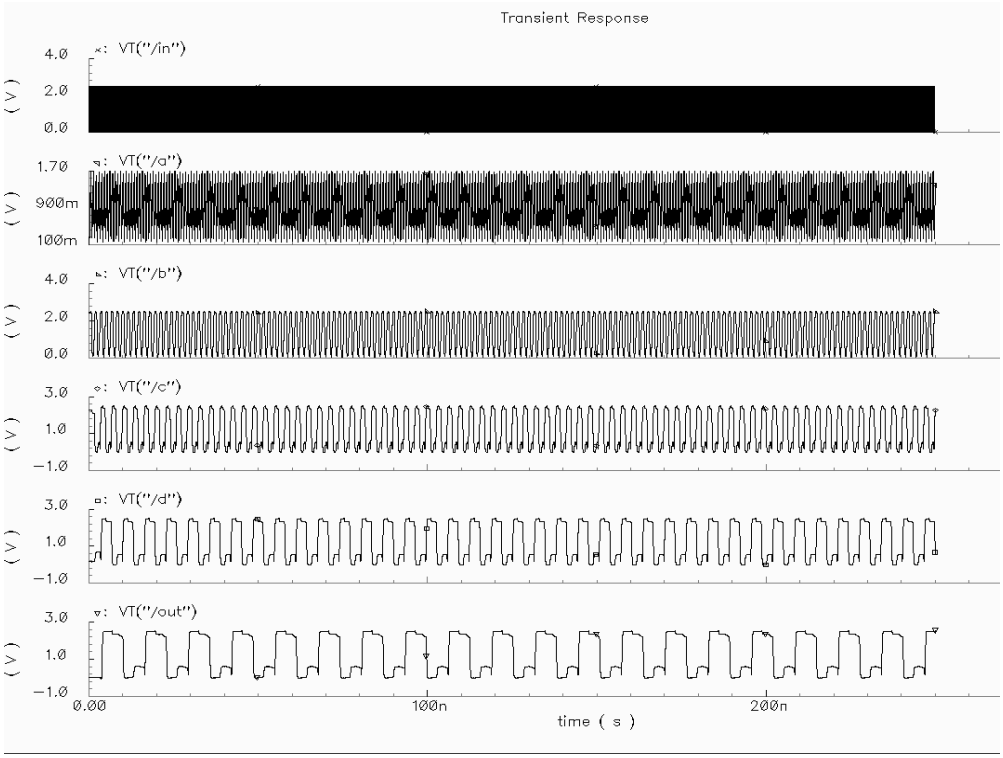


Figure 3.16 Waveforms at intermediate nodes in circuit

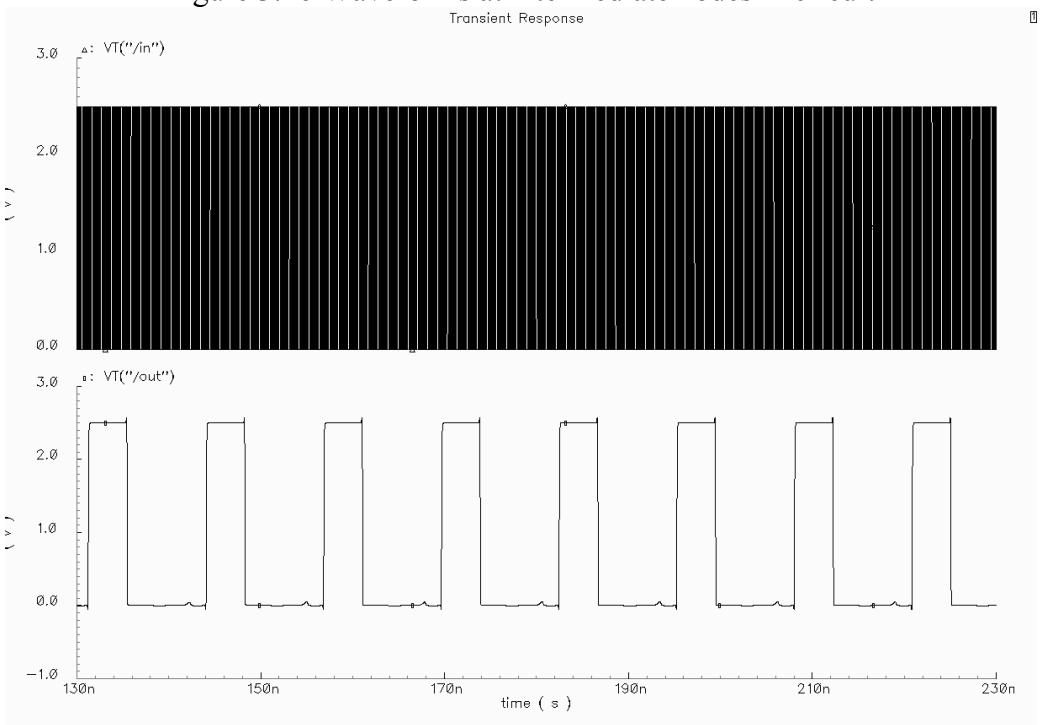


Figure 3.17 Waveform of complete circuit

3.5 Layout

A full custom layout of the divider shown in Figures 3.18 and 3.19 was designed to optimize for area and reduce interconnect parasitics. This helps to achieve greater speed of operation.

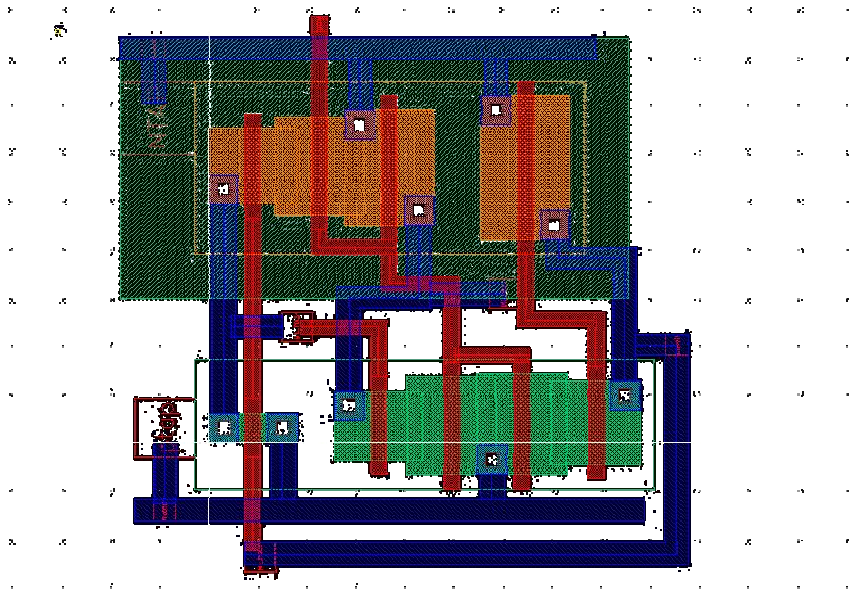


Figure 3.18 Layout of divide-by-2 circuit

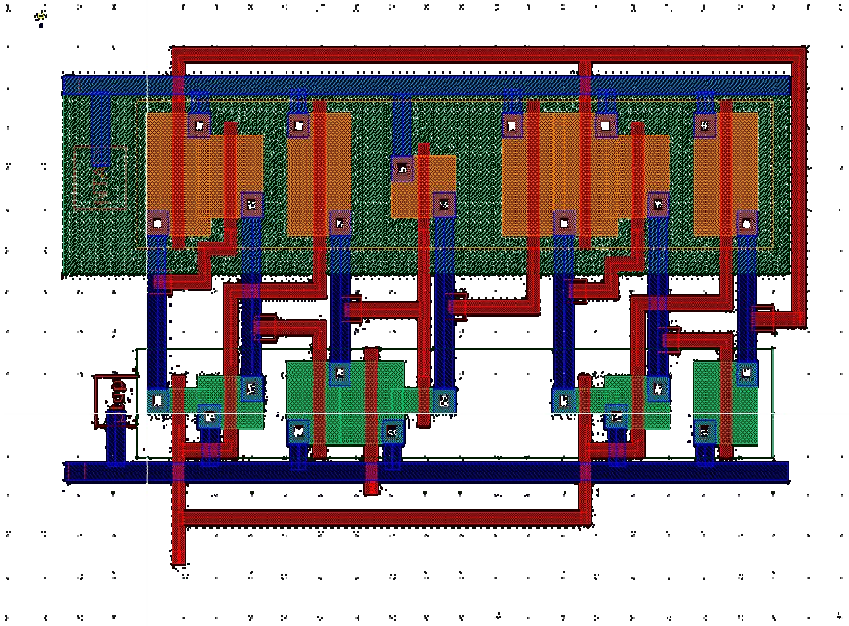


Figure 3.19 Layout of divide-by-2/3 circuit

The widths of the transistors used are shown in the table below. The length of all the transistors is kept at the minimum the technology allows which is 0.25 μm.

Table 3.2 Transistor Widths of Divide-by-2 Circuit

Transistor	**Width (W) in μm**
MP1	1.5
MP2	1.9
MP3	2.4
MP4	1.5
MN1	0.5
MN2	1
MN3	1.5
MN4	1.7
MN5	1.7

Table 3.3 Transistor Widths of Divide-by-2/3 Circuit

PMOS Transistor	**Width (W) in µm**	**NMOS Transistor**	**Width (W) in µm**
Mp1	3	Mn1	0.5
Mp2	2	Mn2	1.3
Mp3	3	Mn3	2
Mp3	1.5	Mn4	2
Mp5	3	Mn5	0.5
Mp6	3	Mn6	0.5
Mp7	2	Mn7	1.3
Mp8	3	Mn8	3

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

In this thesis the design of a new monolithic LC voltage controlled oscillator has been presented in 0.25 μm CMOS Technology. The VCO has been targeted to the 0.25 μm TSMC process. This VCO is unique in the sense that it does not make use of varactors in the design but instead relies on properties inherent in the circuit topology for frequency tuning. In this circuit changing the loop gain varies the frequency. By eliminating the use of varactors, the phase noise contribution due to varactors is absent.

To summarize, the designed VCO has a tuning range of 130 MHz around a center frequency of 5.70 GHz. It has a low simulated phase noise of –114 dBc/Hz at an offset of 1 MHz which is comparable to some of the best reported phase noise levels at this frequency. This is shown in table 2.2. The Q of on-chip inductors achievable today is a limit on the tuning range. Higher tuning range can be obtained with higher Q inductors. The core VCO consumes quiescent power of 6.25 mW from a supply of 2.5 V. This VCO can be used for 802.11a WLAN applications.

A comparison table has been provided (Table 4.1) to evaluate the performance of this work against other typical VCOs reported in recent years and operating in the same frequency range. All the papers listed in the table, make use of varactors in their VCO designs. In [8], the authors report a phase noise of -110 dBc/Hz at an offset of 1

MHz, from a VCO realized with varactors. In the same paper another design without making use of tail current is reported which achieves a phase noise of -117 dBc/Hz at the same offset but with higher power dissipation. A low power VCO design implemented in an SOI process is reported in [9], which achieves a phase noise of -110 dBc/Hz. The paper also reports the same design implemented in a CMOS process with better phase noise performance but much higher current consumption. Reference [10] reports a VCO designed with PMOS transistors to reduce 1/f noise contribution to the phase noise. The achieved phase noise is -116 dBc/Hz at 1 MHz offset. However this design makes use of varactors and also consumes higher current.

Table 4.1 5-GHz VCO Comparison

Design	Freq. (GHz)	VDD (V)	I_{tail} (mA)	Power (mW)	PN*
Ref [8] w/ tail	5.00	2.5	2	5	-110
Ref [8] wo/ tail	5.00	2.5	2.9	7.25	-117
Ref [9] VCO1	5.25	1.5	1.1	1.65	-110
Ref [9] VCO2	5.33	1.5	11.5	17.25	-126
Ref [10]	5.50	1.5	4.6	6.9	-116
Ref [11]	4.00	2.5	7.5	18.75	-117
This work (sim.)	5.68	2.5	2.5	6.25	-114

* Phase Noise in dBc/Hz @ 1MHz offset

[11] reports a novel MOS varactor design to improve phase noise performance of the VCO but the power dissipation is high. A similar scheme as used in this work is

reported in [7] where the design is implemented using BJT's in a Si bipolar technology. The reported VCO is designed for 1.8 GHz and achieves a phase noise of -88 dBc/Hz at an offset of 100 KHz. It also has a high power dissipation of 70 mW from a power supply of 5 V. In contrast, this work uses MOS transistors which helps to achieve higher operating frequencies and with much lower power consumption. The circuit performance as mentioned earlier, is comparable to the reported VCO designs.

The VCO design described in this thesis has been successful in satisfying the performance criteria for VCO's in WLAN transceivers, which are good phase noise performance, low power dissipation and high operating frequency. It has been shown here, through simulations that MOS transistors are better than BJT's to achieve the aforesaid criteria and that a high tuning range can be achieved even without using varactors in the design and this inturn could lead to improvement in phase noise performance.

As part of this thesis a frequency divider has also been designed, that operates at 5 GHz. The divider is formed by cascading a divide-by-2, divide-by-8/9 and divide-by-16 circuit. This design was undertaken to understand the design of high frequency digital circuits. The CMOS dynamic logic circuits operating on a single clock (TSPC technique) were used for all the flip-flops of the divider to reduce clock loading as well as eliminating clock skew problems. This part of the thesis contributes to outlining a design approach for high frequency dividers, but the programmability of the divider has not been undertaken in this work.

4.2 Future Work

The VCO and frequency divider presented in this work have been simulated with analytical spiral inductor models and generic transistors. So the next step would be to fabricate these designs and verify the results presented here.

Also the two circuits were evaluated in isolation. One proposal is to integrate control logic for modulus control of the divider to enable programmability. The second is to integrate the VCO and the frequency divider and evaluate the overall performance in terms of phase noise, switching characteristics and power dissipation.

APPENDIX A

MODEL PARAMETERS FOR 0.25 μm CMOS PROCESS

(Referenced for VCO design)

```
T4CS SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 27/05
* LOT: T4CS                  WAF: 7004
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 5.7E-9
+XJ      = 1E-7          NCH     = 2.3549E17       VTH0    = 0.3711459
+K1      = 0.4822794     K2      = 4.471019E-4     K3      = 1E-3
+K3B     = 3.6276844     W0      = 1E-7            NLX     =
2.348444E-7
+DVT0W   = 0             DVT1W   = 0               DVT2W   = 0
+DVT0    = 0.3667644     DVT1    = 0.5821305       DVT2    = -0.5
+U0      = 274.3844688   UA      = -1.653939E-9    UB      =
2.819096E-18
+UC      = 2.857558E-11  VSAT    = 1.181552E5      A0      = 1.8761843
+AGS     = 0.3235364     B0      = -3.933095E-8    B1      = -1E-7
+KETA    = -7.22467E-3   A1      = 4.984182E-4     A2      = 0.5672749
+RDSW    = 200           PRWG    = 0.4073997       PRWB    = 0.0417695
+WR      = 1             WINT    = 0               LINT    = 0
+XL      = 0             XW      = -4E-8           DWG     = -
2.178838E-8
+DWB     = 1.826441E-9   VOFF    = -0.0864567      NFACTOR = 1.5377422
+CIT     = 0             CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0             ETA0    = 4.251984E-3     ETAB    = -
8.430903E-5
+DSUB    = 0.0145709     PCLM    = 1.7379816       PDIBLC1 = 0.7224316
+PDIBLC2 = 3.890878E-3   PDIBLCB = 0.0893858       DROUT   = 1
+PSCBE1  = 5.77311E8     PSCBE2  = 2.162408E-5     PVAG    = 0
+DELTA   = 0.01          RSH     = 4.6             MOBMOD  = 1
+PRT     = 0             UTE     = -1.5            KT1     = -0.11
+KT1L    = 0             KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0             WLN     = 1               WW      = 0
+WWN     = 1             WWL     = 0               LL      = 0
+LLN     = 1             LW      = 0               LWN     = 1
+LWL     = 0             CAPMOD  = 2               XPART   = 0.5
+CGDO    = 5.85E-10      CGSO    = 5.85E-10        CGBO    = 1E-12
+CJ      = 1.790627E-3   PB      = 0.99            MJ      = 0.4646759
+CJSW    = 4.050666E-10  PBSW    = 0.99            MJSW    = 0.3400722
+CJSWG   = 3.29E-10      PBSWG   = 0.99            MJSWG   = 0.3400722
+CF      = 0             PVTH0   = -8.244259E-3    PRDSW   = -10
+PK2     = 3.408268E-3   WKETA   = 0.0137488       LKETA   = -
9.396848E-4    )
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 5.7E-9
+XJ      = 1E-7          NCH     = 4.1589E17       VTH0    = -
0.5483744
+K1      = 0.6457182     K2      = -1.223928E-3    K3      = 0
```

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+K3B     = 12.0016618     W0      = 1E-6           NLX     =
2.909056E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 3.3645707      DVT1    = 1              DVT2    = -
0.1084589
+U0      = 100            UA      = 8.639908E-10   UB      = 1E-21
+UC      = -1E-10         VSAT    = 1.315147E5     A0      = 0.9966156
+AGS     = 0.150024       B0      = 1.068252E-6    B1      = 5E-6
+KETA    = 0.0183269      A1      = 0.0424825      A2      = 0.3
+RDSW    = 1.78024E3      PRWG    = 0.0103173      PRWB    = -
0.0403102
+WR      = 1              WINT    = 0              LINT    = 3.28928E-
8
+XL      = 0              XW      = -4E-8          DWG     = -
3.962583E-8
+DWB     = 1.58796E-9     VOFF    = -0.1184864     NFACTOR = 1.1161098
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.274272       ETAB    = -
0.1247268
+DSUB    = 1.1713558      PCLM    = 1.3244603      PDIBLC1 = 4.93008E-
3
+PDIBLC2 = 1.315268E-8    PDIBLCB = -1E-3          DROUT   = 0.074962
+PSCBE1  = 3.85403E10     PSCBE2  = 1.667603E-8    PVAG    =
5.255732E-3
+DELTA   = 0.01           RSH     = 3.3            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 6.79E-10       CGSO    = 6.79E-10       CGBO    = 1E-12
+CJ      = 1.893734E-3    PB      = 0.9889579      MJ      = 0.4705132
+CJSW    = 3.124347E-10   PBSW    = 0.8            MJSW    = 0.2786992
+CJSWG   = 2.5E-10        PBSWG   = 0.8            MJSWG   = 0.2786992
+CF      = 0              PVTH0   = 6.560837E-3    PRDSW   = -
14.5007628
+PK2     = 2.349828E-3    WKETA   = 0.0302868      LKETA   = -
9.415202E-3    )
*
```

APPENDIX B

MODEL PARAMETERS FOR 0.25 μm CMOS PROCESS

(Referenced for Frequency Divider design)

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* LOT: n94s         WAF: 08
* Temperature_parameters=Default

.MODEL tsmc25N NMOS (                LEVEL=11  &
VERSION=3.1      TNOM=27       TOX=5.8E-9  &
XJ=1E-7      NCH=2.3549E17   VTH0=0.4308936  &
K1=0.3519429   K2=0.0298493   K3=1E-3  &
K3B=0.0592323   W0=1E-5      NLX=1.465901E-7  &
DVT0W=0       DVT1W=0       DVT2W=0  &
DVT0=0.0183405   DVT1=4.897584E-3  DVT2=-0.0252658  &
U0=455.3033362  UA=5.223592E-10  UB=1.104713E-18  &
UC=3.287888E-11  VSAT=1.050993E5   A0=1.2318623  &
AGS=0.3043334   B0=6.67749E-8   B1=5E-6  &
KETA=8.518046E-4  A1=0       A2=1  &
RDSW=509.5675851  PRWG=0.0227558   PRWB=-1E-3  &
WR=1       WINT=2.126497E-9  LINT=4.393474E-9  &
XL=-3E-8     XW=0       DWG=-3.409033E-9  &
DWB=2.794842E-9  VOFF=-0.1026054   NFACTOR=0.1344887  &
CIT=0       CDSC=1.527511E-3  CDSCD=0  &
CDSCB=0       ETA0=3.48737E-3   ETAB=4.557986E-4  &
DSUB=3.045473E-3  PCLM=1.0446257   PDIBLC1=0.1441952  &
PDIBLC2=4.513382E-4  PDIBLCB=-2.816756E-5  DROUT=0.4698725  &
PSCBE1=1.761109E10  PSCBE2=3.772916E-9  PVAG=0.0361824  &
DELTA=0.01      MOBMOD=1       PRT=0  &
UTE=-1.5      KT1=-0.11     KT1L=0  &
KT2=0.022     UA1=4.31E-9    UB1=-7.61E-18  &
UC1=-5.6E-11    AT=3.3E4     WL=0  &
WLN=1       WW=0       WWN=1  &
WWL=0       LL=0       LLN=1  &
LW=0       LWN=1       LWL=0  &
CAPMOD=2       XPART=0.4      CGDO=6.27E-10  &
CGSO=6.27E-10    CGBO=0       CJ=1.918655E-3  &
PB=0.9784049   MJ=0.4721729   CJSW=4.441595E-10  &
PBSW=0.9419636   MJSW=0.2871118   PVTH0=1.342985E-3  &
PRDSW=-61.8357222  PK2=-3.140724E-3  WKETA=7.512693E-4  &
LKETA=-6.144062E-3  )

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XJ=1E-7           NCH=4.1589E17      VTH0=-0.6158735 &
K1=0.4598379      K2=0.0399415      K3=0 &
K3B=8.7410723      W0=1E-6           NLX=1E-9 &
DVT0W=0              DVT1W=0              DVT2W=0 &
DVT0=0.6249485      DVT1=0.203296       DVT2=-0.0513763 &
U0=158.67524      UA=2.200024E-10   UB=4.457415E-18 &
UC=1.02138E-10    VSAT=1.85064E5      A0=1.3826397 &
AGS=0.4192977      B0=2.844099E-6    B1=5E-6 &
KETA=0.0208695      A1=0              A2=1 &
RDSW=968.5463       PRWG=-0.1026483     PRWB=-0.325 &
WR=1              WINT=2.748811E-8    LINT=8.71907E-9 &
XL=-3E-8          XW=0              DWG=-4.087585E-8 &
DWB=2.032008E-8    VOFF=-0.15          NFACTOR=1.5460516 &
CIT=0              CDSC=1.413317E-4    CDSCD=0 &
```

```
CDSCB=0               ETA0=0.3241245      ETAB=-0.1842 &
DSUB=1.0287138      PCLM=5.2654567      PDIBLC1=4.228338E-3 &
PDIBLC2=1.204519E-3    PDIBLCB=2.37525E-3     DROUT=0 &
PSCBE1=3.011456E10    PSCBE2=3.037042E-7    PVAG=8.9564294 &
DELTA=0.01           MOBMOD=1              PRT=0 &
UTE=-1.5           KT1=-0.11          KT1L=0 &
KT2=0.022          UA1=4.31E-9        UB1=-7.61E-18 &
UC1=-5.6E-11       AT=3.3E4          WL=0 &
WLN=1              WW=0              WWN=1 &
WWL=0              LL=0              LLN=1 &
LW=0              LWN=1              LWL=0 &
CAPMOD=2              XPART=0.4           CGDO=5.59E-10 &
CGSO=5.59E-10       CGBO=0              CJ=1.882857E-3 &
PB=0.9891317      MJ=0.4679789      CJSW=3.67186E-10 &
PBSW=0.9884654      MJSW=0.3562128      PVTH0=3.923756E-3 &
PRDSW=15.3953053     PK2=2.061759E-3    WKETA=4.10049E-3 &
LKETA=-0.0232426     LVSAT=1.257E5         )
```

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