CMOS OPTICAL TRANSIMPEDANCE AMPLIFIER DESIGN FOR PAM SIGNALING APPLICATION

by

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ABSTRACT

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APPLICATION

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The advent of Internet telephony and the surge in data communication field necessitate the use of broadband communication systems. The Optical communication systems has been suggested as an attractive solution to cope with the high speed data rate and large throughput bottleneck of the long haul communication systems due to their cheaper deployment cost. In the world of miniaturization, CMOS circuits have been widely used to develop the opto-electronic components. However, the intricacy involved in the design of high speed optical front-end is higher due to the poor noise performance of CMOS circuits compared to their bipolar counter parts. Despite their

noise performance, CMOS design facilitates high degree of integration of both analog and digital parts, lower power consumption, and high yield that lowers the fabrication cost.

In this thesis, a stand alone high speed differential trans-impedance amplifier serving the front-end of an optical receiver is designed using TSMC 0.18μm mixed-signal non-epi CMOS technology. The design meets the SONET OC-48 standard with 3 different multilevel signaling schemes. The overall trans-impedance gain of 77dBΩ is achieved with 3 post amplifier stages. The eye diagram measurement and power supply parasitic modeling is shown in the simulation.

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CHAPTER 1

INTRODUCTION

The Optical Communication system takes over the existing technology to satiate the demand of high speed, greater volume of transmission capacity for the telecommunication/ data communication networks. Compared with the conventional electrical communications, the communication using optical carrier waves are usually immune to electromagnetic interference and cross talks, offers immense bandwidth usage, provides low transmission losses, good overall system reliability and maintenance. Due to these reasons, the state of the art technology, Fiber Optics is realized for long-haul transmission, local area networks, video trunking, cable TV and sensors.

The Fiber Optics transmission schemes are governed by the Synchronous Optical Network (SONET) and Synchronous Digital Hierarchy (SDH) standard. It defines the technology for carrying information signals through a synchronous, flexible, optical hierarchy by means of a byte-interleaved multiplexing scheme. The basic transmission rate is 51.8 Mbps for the OC-1optical system and the higher rates are summarized in the Table 1.1 below. More information carrying capacity can be added on to the fiber by the Wavelength Division Multiplexing Scheme (WDM) which transmits many data streams on to the single fiber at different wavelength.

Table 1.1 Levels of SONET Signal Hierarchy and Electrical Equivalents

LEVEL	Equivalent electrical standard	LINE RATE(Mbits/s)
OC-1	STS-1	51.8
OC-3	STS-3	155.5
OC-9	STS-9	466.5
OC-12	STS-12	622
OC-24	STS-24	1244.1
OC-36	STS-36	1866.2
OC-48	STS-48	2488.3
OC-192	STS-192	9953.280
OC-768	STS-768	39813.120

A typical optical communication system comprises both electrical and optical discrete components like transmitter, optical source, driver circuitry, transmission fibers, optical detector and receiver circuit. For secure communications using optical fibers, CMOS circuits are mostly adopted because they to provide good compatibility of

all opto-electronic and digital system components to perform fair enough without affecting the overall system performance. On the other hand, the CMOS counterparts; GaAs MESFETs, AlGaAs/GaAs HEMTs, AlGaAs/GaAs HBTs, Si Bipolar transistors, or SiGe Bipolar transistors are still used for optical transceiver designs due to their higher speed and wider bandwidth capability. The process technology associated with these transistors can provide good quality of passive components like resistors and capacitors. However extensive research are conducted on CMOS optical systems because the high degree of integrity of CMOS design enables the fabrication of mixed signal functionality onto a single chip circuitry, offers low cost, low power consumption and high yield compared to different semiconductor technologies.

The optical communication system requires electrical to optical conversion in the transmitting end and the vice-versa on the receiver side for the further processing of obtained optical signals. The received optical signals are converted to current signal by the photo-detector located at the front end of the optical receiver followed by a preamplifier which converts the current signals to voltage levels for signal processing. The receiver design is more sophisticated in the overall optical communication system due to the mixed signal impediments of CMOS circuits like cross-talks and noise issues. Deliberate design tactics are needed especially for the front end preamplifier to resolve the noise issues of mixed signal parts and meet the data rate and bandwidth requirement of SONET standard.

The light wave traveling through the fiber usually undergoes considerable attenuation before reaching the photo-detector. This attenuation requires a subsequent

stage to detect and amplify the signal at an acceptable bit-error-rate (BER). Hence the Trans-impedance amplifier (TIA), the preamplifier, should cater both high overload tolerance and high input. To provide wide dynamic range to the received optical signals weakened by transmitter aging and/or long transmission distance, the TIA noise must be reduced to a minimum. On the other hand, a high overload tolerance is required to avoid bit errors caused by distortion in the presence of strong optical signals. Furthermore, to ensure stable operation and meet the bandwidth criteria, the gain can be optimized only within a narrow range. This limitation sometimes causes the output voltage that result from low-power optical signals to be insufficient for further processing. Therefore, a cascaded post amplifier often follows to amplify small TIA voltages.

Although the WDM scheme described above provides large data throughput, there are some technology limitations in providing a number of wavelengths, for instance due to channel broadening effects, non-ideal optical filtering and the channels must have minimum wavelength spacing for the desired performance. Wavelength range, accuracy, and stability are extremely difficult to control. In addition, this system requires the expensive and high quality optoelectronic and electrical devices to handle the high speed data transmission because the input speed will be limited by the speed of a WDM.

In this thesis, multilevel signaling schemes are used instead of WDM scheme to increase the spectral efficiency. Here 2^n bits can be represented in each unit interval by amplitude modulating the signal. As the semiconductor device technologies mature, more advanced communication technique such as multilevel signaling is needed to

further improve the performance of optical fiber system as well as developing semiconductor devices. By improving spectral efficiency, we can achieve higher data throughput in the optical communication system. By decreasing the symbol rate, resistance to uncompensated chromatic dispersion and polarization-mode dispersion can be controlled, and also utilize lower-speed electronics. Compared to binary signals, multilevel optical signals have longer symbol duration and have narrower spectra both in the optical domain and in the electrical domain, after detection at a receiver. These attributes of multilevel signals increase immunity to ISI, increase spectral efficiency, and relax the bandwidth requirements However, there are many restrictions in the design of a multi-level signaling transmitter to achieve high reliability and equal level spacing of output signal because the multi-level signaling scheme is more sensitive to the non-linearity and noise than the binary schemes.

Lastly, in this thesis, section 2 provides a background of optical communication system. Different types of preamplifier and the importance of trans-impedance amplifiers are also discussed. Section 3 describes the modeling of power supply parasitics associated with packaging and bonding wire. Section 4 describes the design intricacy of single ended TIA with post amplifier stages to improve the overall gain and the simulation results are discussed. In section 5, design of differential feedback TIA with the post amplifier stages along with output buffer driving 50Ω load impedance are discussed. The detailed simulation results showing the noise analysis, eye diagram measurement along with the transient responses of the multilevel signals (PAM signals) are included. Results including the power supply parasitics from the PCB board are

also simulated. Finally, in section 6, the summary of overall design and analysis of simulation results are discussed. Important performance characteristics such as Input Referred Noise and the optical receiver sensitivity calculations are shown.

CHAPTER 2

BACKGROUND AND DESIGN CONSIDERATION

2.1 Background

With the prolific growths of data being transported in the backplane communication and with the rise in the speed of microprocessor and memory devices have, rekindled the demand for faster and lower cost communication channels operating in Giga hertz range. The optical communication systems have been a promising candidate to overcome the speed and data throughput bottleneck of long- haul telecommunication systems. The search for lower cost has goaded a trend towards monolithic integration of optical and electronic components, called OEICs (Opto-Electronic Integrated Circuits), to achieve improved functionality and performance, with significant cost reduction. Parallel to the development of high speed long-haul point-to-point telecommunication systems, it is the fact that optical fiber systems are finding acceptance in many other application areas such as local area networks, video trunking, data buses, distribution, sensor etc [1]. As a result, the optical system has to satisfy many different requirements based on the applications. These requirements are often conflicting and hence careful attention should be paid for the optical receiver design to overcome the trade offs.

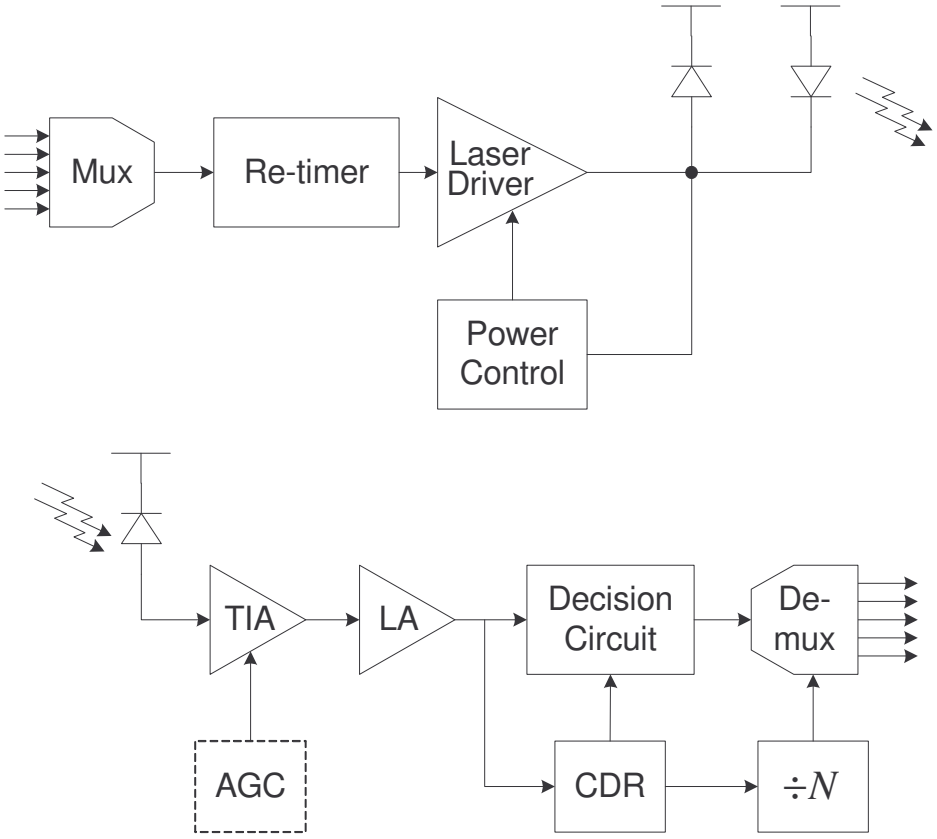


Figure 2.1: Optical communication system

The typical interface of an optical data link shown in Figure 2.1. It includes multiplexer, de-multiplexer, laser driver, transimpedance amplifier (TIA), post amplifier, clock and data recovery (CDR) and phase-locked loop (PLL), along with the other opto-electronic components. In the transmitter, a number of slow channels are multiplexed into a high-speed data stream. This data stream is retimed and applied to a laser driver, and the optical output is delivered to the fiber. The phase-locked loop (PLL) generates clocks for both the multiplexer and the retiming circuit. Also, because

the power of the laser output varies with temperature and aging, a power control circuit continuously adjusts the output level of the driver. In the receiver, the photo-detector (PD) converts the received light to a signal current, and the signal swing is amplified to logic levels by the TIA followed by the voltage amplifier. Subsequently, the CDR performs timing and amplitude-level decisions on the incoming signal, which leads to a time and amplitude regenerated data stream. The result is then de-multiplexed, thereby reproducing the original channels.

The receiver circuit entails severe design problems to meet the overall system requirements because, the photo-detector must exhibit high sensitivity to the input, as the light traveling through the fiber undergoes considerable attenuation before it reaches the detector. Further the electrical signals generated by the photo-detector must be amplified with low noise, so that the receiver can detect the signals with acceptable BER performance. Apart from this, the noise, gain, and bandwidth of the TIA and the post amplifier directly impact the speed and sensitivity of the receiver, raising additional issues as the supply voltage scales down. Hence the performance of the receiver is often characterized by the input sensitivity, bandwidth, and detection method employed in the receiver [2]. Bandwidth is usually determined by the total capacitance contributed by the PD, the preamplifier, and other parasitic elements present at the optical front-end.

2.2 Photodetector

The photo-detector converts the light carried by the fiber into electrical signal current by the property of optical absorption. The electrons in the valence band gets stimulated and rise to the conduction band, when the light falls on the P-N junction of the detector. Electron-hole pairs are generated (Figure 2.2) in response to the absorption of incident photons, when the band gap energy of the photons exceeds that of the material. The performance criteria of the detector are characterized by the wavelength, speed and responsivity. The wavelength determines the materials used for fabricating the photo-detector. Usually Si or GaAs materials are used for short distance application (0.85µm) and compound semiconductors like InGaAs or InGaAsP are used for 1.3µm/1.55µm long wavelength detector.

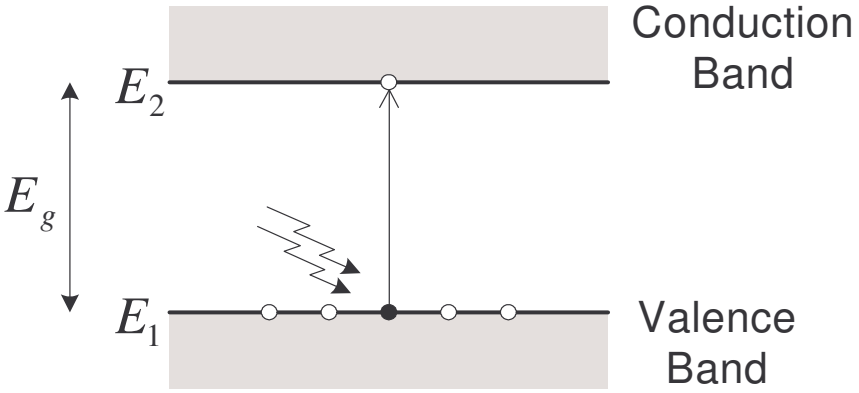


Figure 2.2: Electron-hole pair generation

The speed of the photo-detector is mainly detected by either the photo-detector capacitance or the carrier transit time. The structure and depletion region of the

detector, which enhances the photo-detection action, directly determines the detector capacitances. The three different types of photo-detectors are P-i-N, avalanche and Metal- Semiconductor-Metal (MSM) photo-detectors. A good photo-detector should posses, low dark current, low capacitance and high sensitivity. Among the different types, MSM detectors offer, capacitances as low as 20fF [3]. The responsivity of the detector evaluates how much electrical current it can produce based on the amount of optical power incident on them. Its value ranges from 0.5 to 1.2 A/W. A photo-detector with high responsivity should be selected as it directly affects the overall receiver sensitivity.

2.3 Importance of Transimpedance amplifier

The photocurrent generated by the photo-detector is very small; hence a preamplifier is required at the front end of the receiver to amplify the weak current signals with a minimum amount of added noise, to a usable signal for further processing. Since it converts the current signal into useful voltage signal, they are commonly known as transimpedance amplifier (TIA). A larger signal swing may be obtained by widening a light reception window to increase responsivity, but this larger signal swing then comes at a cost of an increased response time. Hence, the preamplifier is used at the front stage of amplification has great impact on determining the overall data rate and sensitivity that can be achieved in an optical communication system. There are two major factors which characterize the performance of preamplifier; bandwidth and sensitivity. The bandwidth of the preamplifier is indeed determined by the RC time constant at the input of the amplifier. These time constants are contributed

by the detector stray capacitance and input resistance and input parasitic capacitances of the preamplifier. It is important to choose a best topology to meet the system requirement, while finding an optimum trade off between the bandwidth and input receiver sensitivity.

There are three major types of preamplifier designs based on their biasing detector resistance value, namely; low impedance open loop amplifier, high impedance open loop amplifier and transimpedance feedback loop configuration. Each configuration has its own merits and demerits, which allow the designers to choose the topology, based on the specific design applications.

2.3.1 Low impedance open loop amplifier

Its simple known fact that, for converting the weak signal current generated by the photodiode to voltage, all we require is a resistance connected to the photo diode in parallel. Such a simple structure at the front end of the receiver design yields stringent design rules to meet the bottleneck of system standards. Some of the issues are discussed in this section. The structure of low impedance open loop amplifier is shown in Figure 2.3. In the figure, R represents the detector biasing resistor, R_{in} is an effective small signal input resistance of the amplifier and CT denotes the total capacitance including, phototodiode (C_{pd}), parasitic (C_s) and amplifier input gate capacitances (C_{gs}+C_{gd}). The transfer function, bandwidth and noise current of this structure is determined by the following equations.

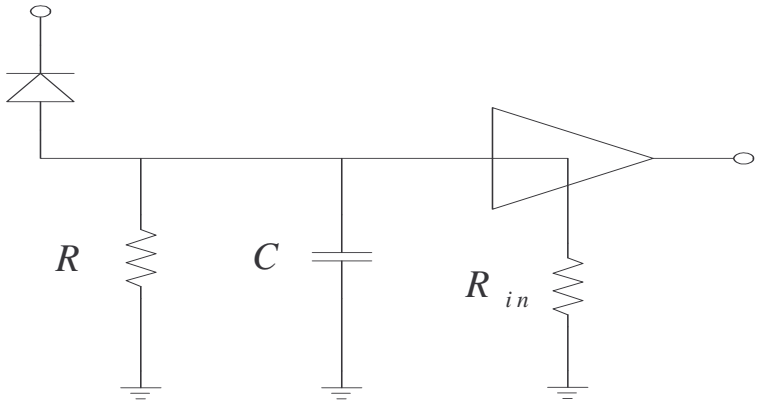


Figure 2.3: Low impedance open loop amplifier

$$\left|H(f)\right|^2 = \frac{R^2}{1+(\omega CR)^2} \tag{2.1}$$

$$f_{-3db} = \frac{1}{2\pi RC} \tag{2.2}$$

$$\overline{I_{n,in}^2} = \frac{KT}{R^2 C} \tag{2.3}$$

Thus by looking at the equations (2.1-3), we infer that the low impedance open loop preamplifier offers wide bandwidth and good dynamic range the cost of increased input noise current. Further the detector capacitance which plays an important role in the overall design is depends on process characteristics and device physical size, thus changing the bias resistor R is the only option to obtain wider bandwidth. Thus it is widely suggested that the diode/resistor network is ill-suited to high-performance applications, since it places tight design restrictions between bandwidth and receiver sensitivity.

2.3.2 High impedance open loop amplifier

The main design goal of high impedance structure shown in Figure 2.4 is to make the value of resistive component seen by the photo-detector as high as possible, so as to reduce the noise. Thus, if a high value of bias resistor R_b is used, it gives lowest noise level and hence the highest detection sensitivity. This type of preamplifier is called high impedance type amplifier. Due to the high load impedance at the front end, the dynamic range of the amplifier is limited along with, frequency bandwidth limitation by the RC time constant at the front end. Thus this type of preamplifier usually requires an equalizer [4] immediately after the amplifier output in order to boost up the gain and extend the receiver bandwidth to the desired range [5].

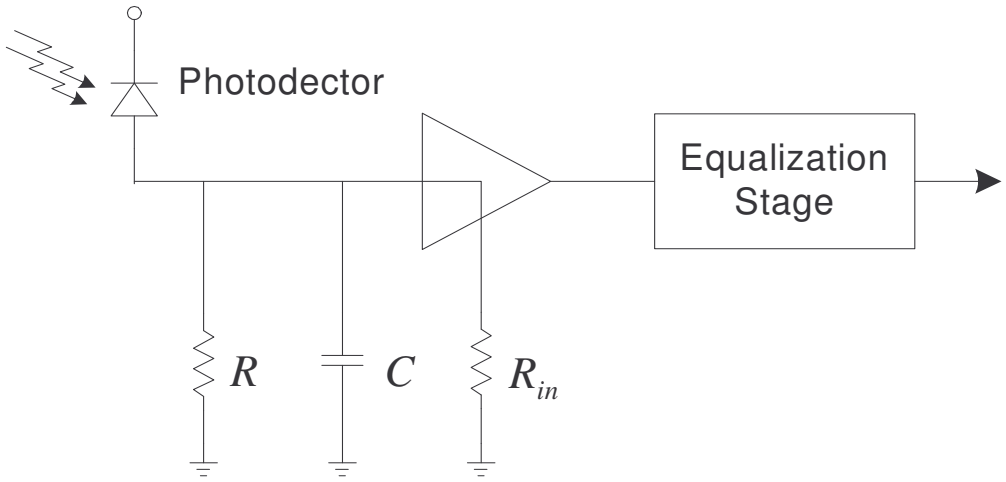


Figure 2.4: High Impedance open loop amplifier

The simplest structure of an equalizer takes the form of a parallel resistance and capacitance in series between the amplifier output and next stage input as shown in

Figure 2.5 [6]. This structure acts like a high pass filter, which attenuates the low frequency signal components and restores the flat transfer function to the system. This requirement adds complexity to the receiver design due to additional constraint of matching the poles of the amplifier frequency response to the zero of the equalizer. Since the total capacitance is the resultant of parasitics, it is hard to predict the exact value for the compensation technique.

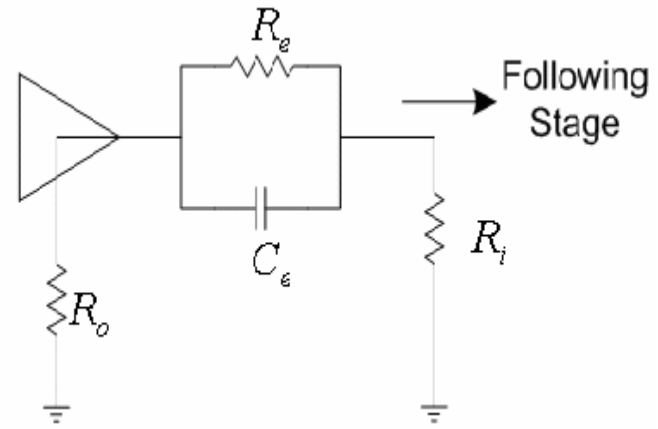


Figure 2.5: Equalization stage

In the Figure 2-5, Ro represents the output resistance of the amplifier and R_i is input resistance of the following amplification stage. The total power transfer function of the optical receiver is given by,

$$|H(f)|^2 = \left[\frac{R}{R_e}\right]^2 \cdot \left[\frac{R_i^2}{1+(\omega C_e R_e)}\right] \tag{2.4}$$

With the assumption of,

$$\frac{1+(\omega C_e R_e)^2}{1+(\omega CR)^2} \approx 1 \tag{2.5}$$

Thus the bandwidth of the high impedance preamplifier type is determined by R_e and C_e of the equalizer stage and is independent of R and C of the input stage. But the values of R and C cannot be ignored as they can affect amplifier noise performance.

2.3.3 Transimpedance feedback type preamplifier

Feedback type transimpedance amplifier offers medium complexity between the low and high impedance open loop type receiver configuration. The transimpedance amplifier design is a popular approach to avoid the dynamic range problem [7]. In addition, it is normally designed to take advantage of the negative feedback effect so that the amplifier bandwidth is extended to the desired value. Thus, this configuration doesn't require equalization circuitry.

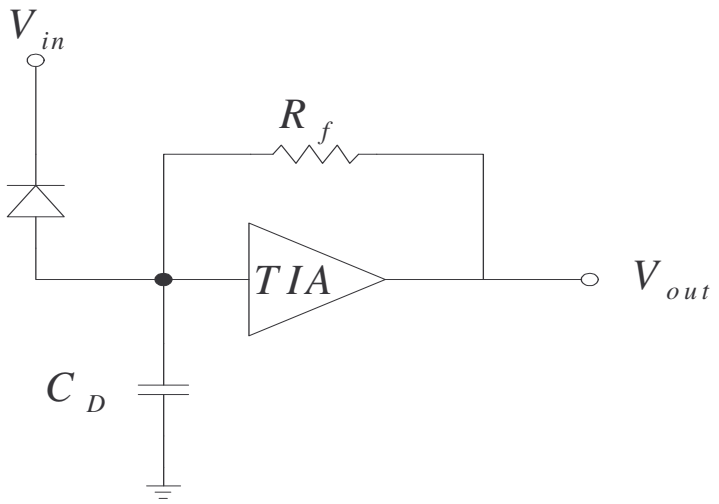


Figure 2.6: Feedback Transimpedance amplifier

However the receiver noise level is higher due to the thermal noise of the feedback resistor as shown in Figure 2.6. Hence the receiver sensitivity is also somewhat lesser compared to high impedance type. In principle, the receiver sensitivity

degradation of the transimpedance design can be kept negligible value by keeping the feedback resistance as large as possible [7]. For a desired bandwidth value, this can be achieved by increasing the amplifier open loop gain. However, the maximum open loop gain is restricted by the propagation delay and phase shift of the amplifying stages within the feedback loop. The transfer function of the circuit is given by

$$\left|H(f)\right|^2 = \frac{R^2}{1+\left[\frac{\omega RC}{A}\right]^2} \tag{2.6}$$

Thus the bandwidth of the transimpedance amplifier is dependent on the feedback resistance R, detector capacitance and the amplifier gain. Thus the freedom of design is relaxed to the feedback resistors which then, ease the stringent design requirements. Hence typically, the transimpedance amplifier is required to be able to accommodate wideband data extending from dc to high frequencies to avoid inter-symbol interference (ISI). At the same time, it is also desirable to maintain a reasonable signal gain, in-band noise, ripple, and phase distortion to improve the sensitivity [8]. As performance indicators, BERs are used to determine the bandwidth and the sensitivity, and eye diagrams can be visual aids to estimate or trouble-shoot sources of noise and other limiting factors.

2.4 Design Requirements

2.4.1 Receiver sensitivity and Bit error rate

In optical communication system, sensitivity is a measure of how weak an input signal can get with an acceptable performance. Sensitivity can be expressed as measure of average incident optical power in dBm. Therefore a receiver is said to be more sensitive if it achieves the same performance with less optical power incident on it. The launched optical power is therefore an important parameter, because it indicates how much light is arriving at the surface of the photo detector.

The signal uses digital discrete modulation of optical field. The receiver recovers a sequence of binary digits from the incoming optical signal field, thus, the technique used to specify a digital receiver's sensitivity is different from that used for an analog receiver. The primary measure of the performance of such systems is to quantify the probability that the receiver will make an incorrect decision. Therefore, the BER is defined as the ratio of number of incorrect identifications to total number of bits received by the decision circuit of the receiver. For example, a BER of $1x10^{-9}$ corresponds to on average of one error per billion bits. Measuring BER and simultaneously varying the amount of optical power received yields a bath-tub shaped plot similar to Figure 2.7.

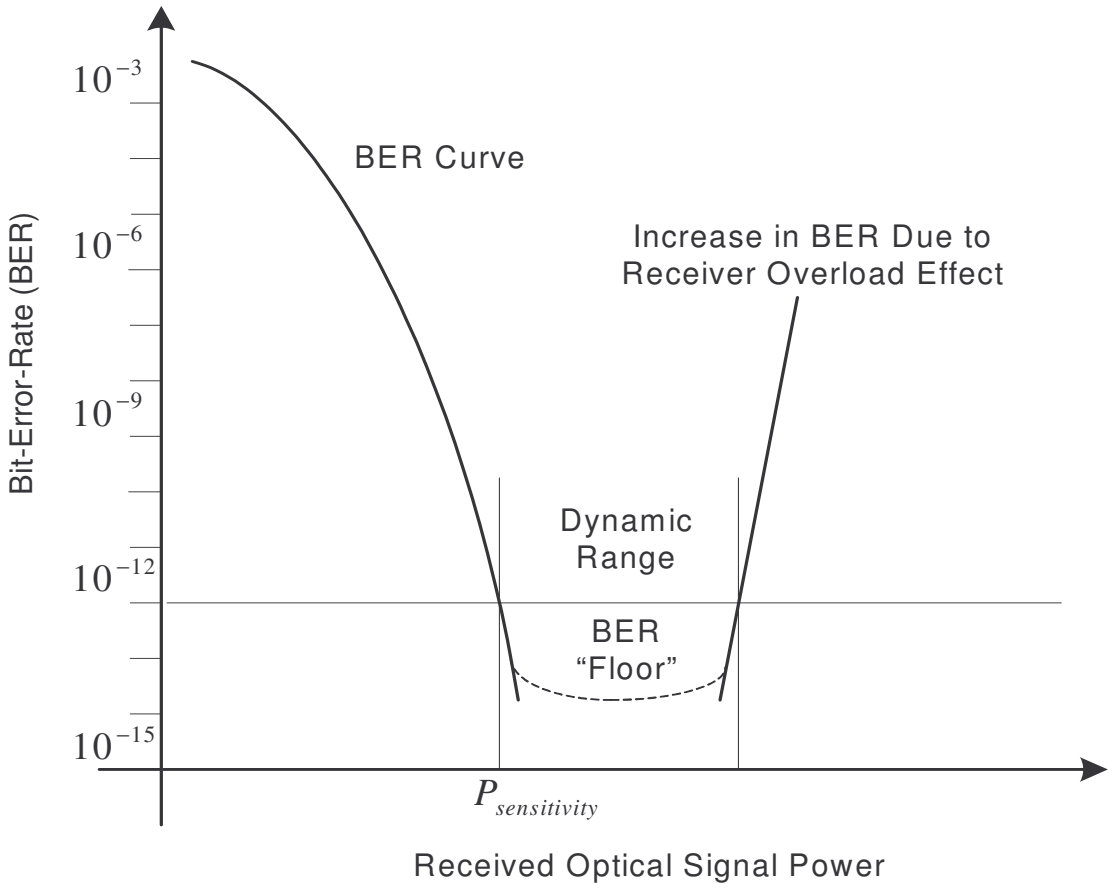


Figure 2.7: Relationship between BER and Receiver optical power

At low levels of the received optical power range, the error rate will be relatively high. As the received optical signal power increases, the probability of making a bit-error decreases. In a correctly designed link, a point will be reached that satisfies the user's quality-of-service requirements for BER. At higher received optical signal power levels, the BER will usually continue to decrease and the system will become error-free. However, it is possible for a BER "floor" to be observed in some

systems. These are usually caused by subtle receiver degradations that are independent of the amount of received optical signal power. Some forms of interference, clock jitter, data pattern dependence, and setup and hold-time violations in digital circuit designs can cause the occurrence of BER floors. Ultimately, if the received power continues to increase, the receiver will eventually overload and the error rate will rise [9]. The difference between the point at which there is just enough received optical signal power to meet the desired BER and the point at which receiver overload causes the BER to rise to unacceptable levels is the receiver dynamic range. In other words, the receiver has to operate not only at the minimum detectable power but also at optical power levels that are sometimes significantly larger. The receiver dynamic range is the difference (in dB) between the minimum detectable power levels and the maximum detectable power level.

Maximum allowable input-received power levels can be determined when the amplifier output starts to be affected by nonlinear dynamic effects, which is a function of either the bias resistor or of the feedback resistor. As the bias resistor decreases, the maximum allowable received optical power increases. Thus, dynamic range is increased. However, a reduction in the resistor value results in an increase in the amplifier noise level. Therefore, a trade-off is required between high receiver sensitivity and wide dynamic range. For the optical communication system, the bit error rate of less than 10-9 is recommended.

2.4.2 Eye diagram

Since the inter-symbol interference (ISI) effects manifests itself differently for different bit patterns, long sequence of random waveforms must be examined for ISI effects which is a tedious tasks. ISI can be occurred when the signal passes through the dispersive system. In optical interconnect system, dispersion is associated with the fiber, coupler, the transmitter circuitry, and the receiver circuitry. ISI is that the pulses corresponding to any one-bit smear into adjacent bits and overlaps. So, if ISI is large enough, this might trigger a false detection in the adjacent time slot. As a result, an increasing number of errors may be encountered as the ISI becomes more pronounced. To overcome this critical issue and to evaluate the system performance, the eye diagram is a simple method to visualize the non-idealities in digital transmission systems [10].

When observing data transmitted by optical driver on the oscilloscope, there is a visual method that is often used to qualitatively measure the properties of a recovered data waveform. If the pulse stream is applied to the vertical input and the sampling clock is applied to the external trigger, a waveform looking like a human eye is obtained. This is called an eye-diagram due to its similarity of shape to a human eye. An eye diagram is easily generated using an oscilloscope that is triggered by the symbol-timing clock and keeping the curve trace for certain duration of time. The eye diagram is a composite of multiple pulses captured with a series of triggers based on data-clock pulse fed separately into the scope. The scope overlays the multiple pulses to form the eye diagram.

Usually, long pseudo-random data patterns are often used when generating eye diagrams to guarantee that the eye-diagram is representative of virtually all possible symbol transitions. By measuring the width of the eye opening both in the vertical and in horizontal directions, the information about the system's ISI, noise, and jitter is obtained as shown in Figure 2.8.

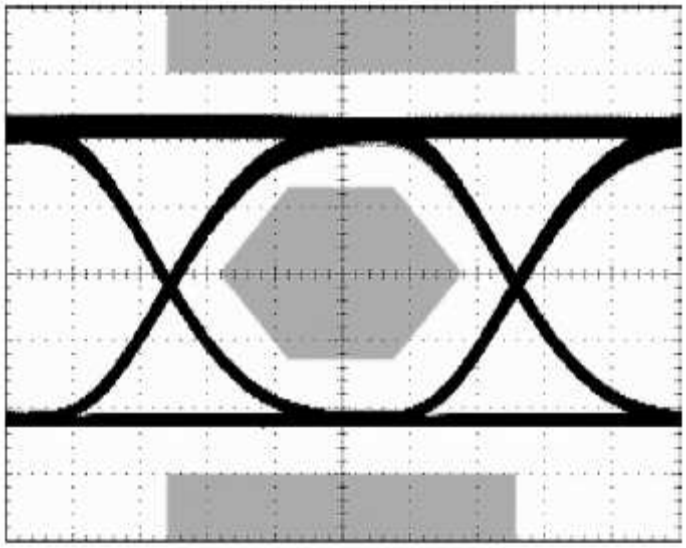


Figure 2.8: Eye diagram

The jitter, which is due to variations in the pulse duration or the accuracy of the symbol clock, will cause the eye closing in the horizontal direction. Noise and ISI are indicated by the vertical width of eye diagram. The ideal decision sampling point occurs at the time of maximum vertical opening. This point corresponds to the time when the signal-to-noise ration is at its maximum. Also, the size and shape of the eye diagram changes depending on the data rate. After the signal is displayed in the form of eye diagram in oscilloscope, the signal should meet the certain criteria to ensure the proper performance of the system. Therefore, eye pattern mask is defined and employed

measuring the eye diagram. As an example of eye mask, the SONET specifications provide a mask inside and around the eye diagram with required parameter values that can sustain the system link BER as shown in the Figure 2.9 according to the Bellcore's technical report [11].

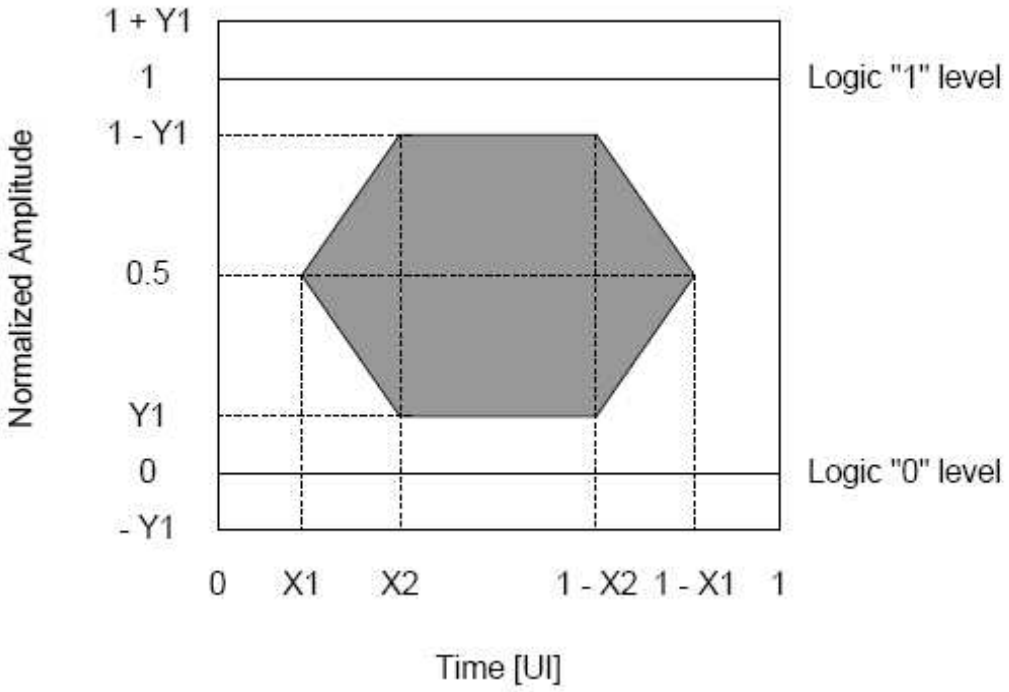


Figure 2.9: Eye Mask

2.4.3 Effect of Noise

The Random data propagating through the optical fibers experiences considerable amount of attenuation. A low- cost plastic fiber exhibit losses as high as 3dB/m [12]. Thus the noise of the receiver can significantly affect the detection of the data. Since noise directly trades with bandwidth, gain and power dissipation, it is important to detect the maximum tolerable noise for the given bit error rate (BER).

In direct-detection optical systems, the receiver is composed of a PD, amplifier circuit, and a CDR circuit. Generally, a semiconductor PD receives binary coded optical pulses representing "1" and "0" bits and converts them into electrical currents while the detection circuit identifies bits as either "1" or "0" depending on the signal amplitude. Hence the accuracy of the decision circuit depends heavily on the SNR of the electrical signal detected by the PD and the subsequent amplifier. As mentioned in the previous section, sensitivity, which is defined as the minimum average received optical power for which the optical receiver can achieve a certain BER, is the major parameter that characterizes receiver performance. Sensitivity is related to the SNR, which in turn depends on various noise sources that corrupt the desired signal. The photo-detection process itself introduces some noise even in a perfect noiseless receiver, which is often called a quantum-noise-limited receiver. In fact, such an ideal receiver does not exist because as many other noise sources degrades the SNR considerably beyond the shot-noise limit. In addition to noises introduced by receivers, the optical signal launched by the transmitter may have inherent intensity and phase fluctuations and chromatic dispersion of the optical fibers may contribute additional noise.

Therefore, receiver sensitivity is determined by the cumulative effect of all possible noise mechanisms as well as by the bit rate of the data because some noise sources are related to signal bandwidth.

2.5 Performance parameters

There are several performance parameters that trade off with each other, in the design of transimpedance amplifier. This section discusses some of the general considerations which influence the TIA design.

2.5.1 Input referred noise current (IRN)

For noise calculation of TIA, the noise must be referred to the input so that it does not depend on the gain. The Input-referred noise is the value that, if applied to the input of the equivalent noiseless circuit, produces an output noise equal to that of the original, noisy circuit. It is a factious quantity which cannot be observed in the circuit. The input referred noise current, I_{in} of the TIA determines the minimum amount of signal current generated by the photo-detector, that yields a given bit error rate. The total input-referred noise current is determined by total integral output noise voltage divided by the transimpedance gain. This is because; in order to obtain meaningful noise effect due to increase to frequency range, the output noise voltage should be integrated over the overall bandwidth.

$$\overline{I_{n,in_{rms}}} = \frac{\sqrt{\overline{V_{n,out,tot}^2}}}{Transimpedance \quad gain} \tag{2.7}$$

Where, $\overline{V_{n,out,tot}^2} = \int_0^\infty \overline{V_{n,out}^2} df$ (2.8)

The total noise current of high-performance TIA typically fall in the range of 0.5 to $2\mu A_{rms}$. The stringent TIA noise requirements limit the choice of circuit topologies and in particular the number of devices in the signal path.

2.5.2 Bandwidth limitation

As discussed above, the bandwidth and noise of transimpedance amplifier, trades off with each other. It is suggested that the bandwidth of TIA must be minimized so as to reduce the total integrated noise. However, on the other hand, limitation in bandwidth introduces inter-symbol interference (ISI) in the random data; resulting in vertical and horizontal eye closure. Hence in order to achieve a fair compromise between the bandwidth, ISI and noise, the speed of the circuit should be sacrificed a little, because in high speed application, bandwidth also trades with gain and power dissipation. The following discussion would quantify a relationship between all those parameters.

When the signal bandwidth is reduced, a periodic binary data would undergo a finite rise and fall delays due to low pass filtering effect at their output as shown in Figure 2.10. But when a random data is transmitted, the output magnitude of long 'run length' droops down making it difficult to define a decision threshold. This effect is known as 'dc wander' or 'baseline wander effect' as the dc level of the output keeps drifting [13]. This indeed leads to misinterpretation by the receiver, because such a small magnitude is susceptible to noise. This effect is known as inter-symbol

interference as the step rise of random data shows exponential response at output, there by corrupting the levels produced for subsequent bits.

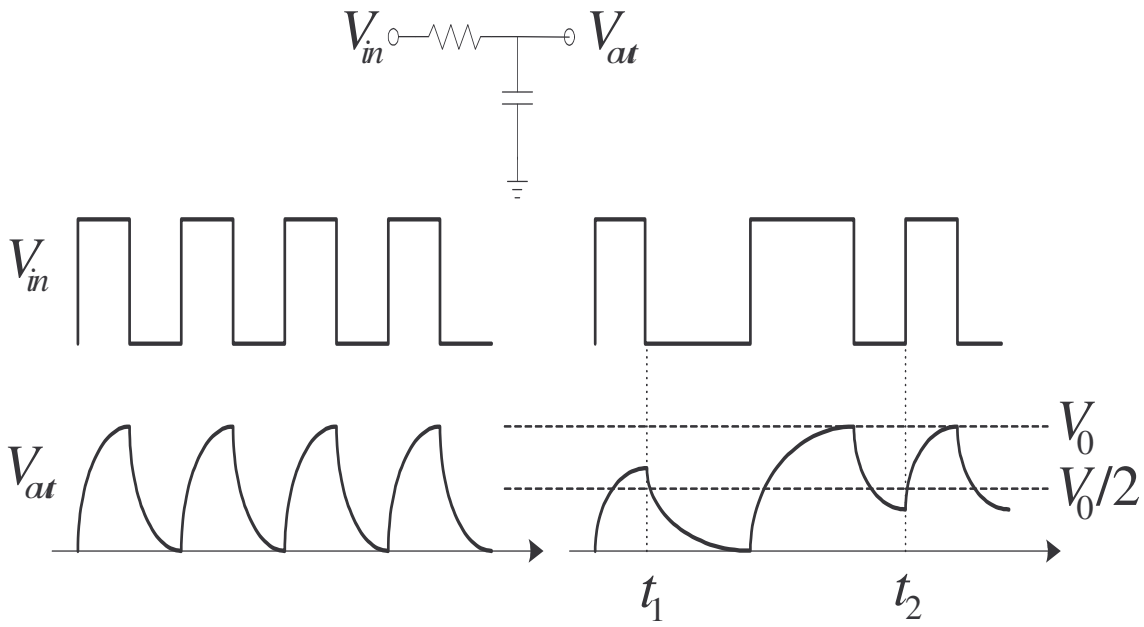


Figure 2.10: Effect of bandwidth limitation

The settling time of each bit is given by

$$V_{out}(t) = V_0\left(1 - \exp\frac{-t}{\tau}\right) \tag{2-9}$$

where $\tau = RC$. The error between V_{out} at $t=T_b$ and the final value is equal to

$$\begin{aligned} V_0 - V_{out}(T_b) &= V_0 \exp\left(\frac{-T_b}{\tau}\right) \\ &= V_0 \exp\left(\frac{-2\pi f_{-3dB}}{R_b}\right) \end{aligned} \tag{2-10}$$

where $f_{-3dB} = (2\pi RC)^{-1}$ and $R_b = 1/T_b$.

Thus the error grows exponentially with the bit rate. To achieve a compromise between bit rate and bandwidth, the f_{-3dB} is chosen to be 0.7Rb for less ISI effect [45]. Also, the photo-detector capacitance limits the TIA bandwidth.

2.5.3 Transimpedance gain

The transimpedance gain of TIA must be large enough to overcome the noise of the subsequent stage, typically a post amplifier or a 50Ω driver. Since the gain trades with bandwidth and voltage headroom, the two stages should be designed together so as to optimize the overall performance. At high speeds, (eg, 2.5Gbps) and low supply voltage (eg, 1.8V), the gain of the TIA may be limited to a few hundred ohms, making the design of the following stage quite difficult.

2.6 Multilevel signal optical receiver

In the proposed system, multilevel signaling schemes are used to minimize the bandwidth for the given data rate. In this design, 4, 8 and 16 level Pulse amplitude modulation signals as shown in Figure 2.11 are used as inputs. By comparing with the binary signal of same bit rate, the multilevel signal bandwidth is lower by the factor of $1/\log_2(M)$, where M is the number of levels. In other words, the Multilevel signal transmits $\log_2(M)$ times as much data as binary signaling on the same bandwidth. In addition the spectral efficiency is increased by the factor of $2\log_2(M)$ [13] and there is an increase in the dispersion-limited fiber distance. Thus the multilevel signaling scheme lessens the impact of bandwidth limitation (ISI), by reducing the width of the operating bandwidth required. While we do incur an SNR penalty, this penalty is

relatively insignificant given the high SNR of the channel. At the data rates we are targeting, the ISI increases even more as one tries to force more bandwidth through the channel.

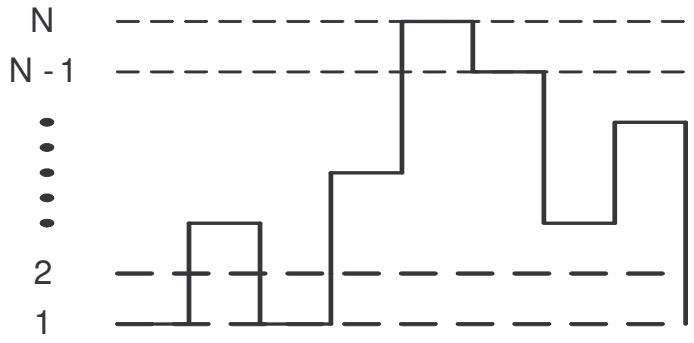


Figure 2.11: N level PAM signaling

The SNR penalty is the cost for squeezing more bits through a given bandwidth. Simply put, the SNR penalty (dB) comparing binary to N-level signaling is in the case where both schemes have the same data throughput rate.

$$\Delta SNR(N) = 10 \times \log_{10}\left(\frac{[N-1]^2}{\log_2 N}\right) \tag{2-11}$$

Using this formula, we see that the penalty for 4-level modulation is 6.5dB, for 8-level modulation, it is 12.13dB, and for 16-level modulation, it is 17.5dB. Also, careful design tactics are needed as the increase in signal levels give rise to linearity problem and noise issues.

The following table shows the lists of recent technology related with optical receiver using digital CMOS process.

Table 2.1: List of recent optical receiver technology

Reference	Technology	BW	Power consumption	Z_T (Ω)	Sensitivity/ Noise
[46]	0.18µm CMOS	2.5 GHz	100mW	531	0.80µArms (integrated to 2Ghz)
[47]	Si-Bipolar	10.5GHz	450mW	1000	12pA/√Hz (integrated to 7.5GHz)
[48]	Si-Bipolar	8.1GHz	280mW	615	10.5pA/√Hz (integrated to 8.1GHz)
[49]	Si-Bipolar	9.0GHz	215mW	710	10pA/√Hz

CHAPTER 3

PACKAGING PARASITIC CONSIDERATION

3.1 Introduction

The signal degradation due to the presence of the parasitics associated with packages and bonding wires has been a crucial factor; since then the, proliferation in the demand of higher data rate and density requirement by the telecommunication industry [14]. Modern ASIC chips can draw many amperes of transient current from the on-chip power supply rails in just a few hundred picoseconds. Depending on the function of the on-chip circuitry, such current may flow to the on-chip V_{ss} rail, or may flow through off- chip signal transmission wires to other parts of the system. To some extent that this current would require to be drawn from the impedance (parasitics) of the power supply line and transient voltage collapse will occur. These parasitics causes switching noise known as delta-I noise. Simultaneous switching or delta-I noise originates when the drivers switch current from power distribution systems [15],[16],[17]. This noise degrades edge rate of digital signal, reduces noise margins, and finally results false switching of digital logics causing error in the system. Therefore, packaging parasitics should be included in the design of the drivers.

To date, silicon CMOS drivers for bit rates up to several gigabits per second for low cost, low power consumption implementations have been reported. Also, delta-I noise has been analyzed and investigated by many researchers [18],[19],[20]. However,

the parasites of the package and bonding wires have not been considered in the design of this transimpedance amplifier driver circuitry due to the lack of efficient methods and models, although they are bonded into a package.

In this research, an equivalent circuit model of parasitics containing bonding wires and packages are developed. The equivalent model is included in ADS simulation of the overall amplifier and the effects of the parasitics are shown.

In order to solve the parasitic problem, the differential topology can be selected instead of single-ended topology, which stabilizes the bias current; since it has symmetric but opposite current flowing path to the power supply lines [21]. However, the effect of the parasitics cannot be eliminated fully due to the device mismatch in the differential pairs and different delays in the current path, although it has better bias current stabilization compared with single-ended version. Thus, use of a decoupling capacitor is also suggested to eliminate the effects of packaging parasitics [22],[23],[24],[25],[26]. In the simulation of the amplifier circuitry, actual equivalent model of capacitors is included to predict the precise effect of decoupling capacitor.

3.2 Background

In a single chip package and printed circuit board (PCB) system, voltage fluctuation named, simultaneous switching noise or delta-I noise has tremendously increased and have affected the performance of integrated circuits, as the circuit transition time is increased. The delta-I noise is caused by the parasitic inductance of the power supply lines in the package and an abrupt current change in the switching circuits.

To describe the mechanism of delta-I noise; a simple inverter with parasitic inductance is shown in Figure 3.1. When the input signal of the inverter (V_{in}) switches state from low-to-high or high-to-low, it causes an abrupt current change to the power supply distribution system through the interconnections. This results in a voltage drop in the power supply (V_p) in the presence of the parasitic inductance (L_parasitics) as explained in

$$V_{noise} = L\frac{dI}{dt} \tag{3.1}$$

The magnitude of the delta-I noise is proportional to the parasitic inductance and power supply current variation. If the magnitude of the voltage drop becomes too large, it results in decision error of the system. Therefore, the current variation should be reduced to minimize the voltage drop and it can be achieved by choosing differential topology in circuit design. Another way of reducing the delta-I noise is to minimize the parasitic inductance with carefully selecting package and PCB. However, the delta-I noise is not fully eliminated but partially reduced; since the inductance always has a

finite value in bonding wires as well as in the package and PCB. Therefore, by placing the decoupling capacitor near the internal power supply to provide charge during switching, delta-I noise can be effectively reduced as illustrated in Figure 3.1.

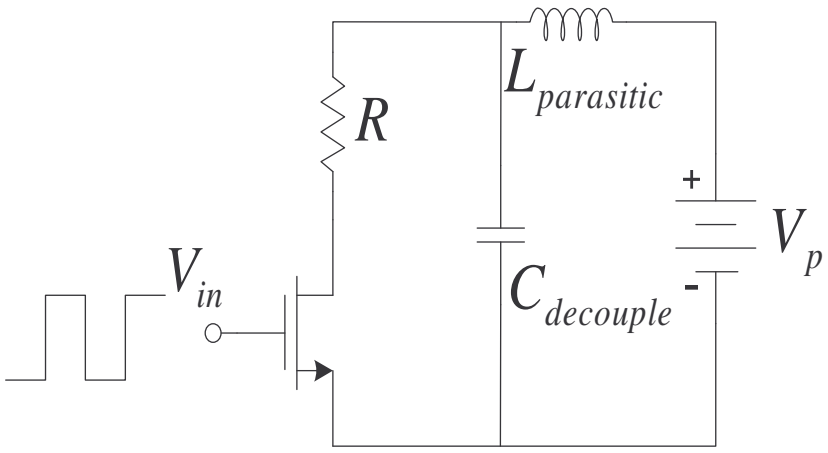


Figure 3.1: The example of the delta-I noise in a circuit.

3.3 Decoupling capacitors

The current ripple, caused by delta-I noise cannot be eliminated fully although the differential topology is employed. Thus decoupling capacitors are required to reduce the effect of the parasitics maintaining the constant dc power supply levels. The effectiveness of the decoupling capacitors can be expressed by the simple equation,

$$I = C\frac{dv}{dt} \tag{3.2}$$

$$\frac{dv}{dt} = \frac{I}{C} \tag{3.3}$$

Equation (3.2-3) states that the voltage fluctuation in power supply line can be suppressed by the capacitors. Therefore, by adding an additional proper decoupling capacitance, the noise can be effectively reduced to the desirable level. In the ideal case of capacitors, it is manifest that the improvement can be increased by using higher capacitance according to equation (3.2-3). However, the value of decoupling capacitor should be optimized since the real capacitors include a parasitic series resistance and an inductance which is called the equivalent series resistance (ESR) and the equivalent series inductance (ESL). In the presence of parasitics in the capacitor model, it also causes voltage fluctuation although the magnitude is much smaller than that of the case of the packaging parasitics. In addition, it causes resonance that gives the signal attenuation because of the parasitic LC in the capacitor model. Therefore, the value and the type of the decoupling capacitor for suppressing the delta-I noise should be chosen

carefully since some type of capacitors contains the higher parasitic inductance than others.

3.4 Modeling of the parasitics

A lumped-element equivalent model (RLC) for the packaging parasitics is developed to predict and analyze the behavior of the parasitics in the overall amplifier design. The model includes package bonding wire impedance, PCB metal line impedance, and bias wire impedance. The model and the values of the PCB impedance were generated and extracted from Advanced Design System (ADS) design tool. And the inductive impedance of bonding wires and bias wires were calculated [94] by

$$L = \frac{\mu_{ol}}{2\pi}\left(\ln\left(\frac{4l}{d}\right) + \mu_r\delta - 1\right) \tag{3.4}$$

where μ_o is the permeability of free space, μ_r is the relative permeability of the bonding wire material, d is diameter of the boding wire, l is the length of the bonding wire, δ is the skin effect factor give by

$$\delta = 0.25\tanh\left(\frac{4d_s}{d}\right) \tag{3.5}$$

And the skin depth of the bonding wire material is given by

$$d_s = \sqrt{\frac{\rho}{\pi f \mu_r \mu_0}} \tag{3.6}$$

where ρ is the resistivity of the bonding wire material and f is the frequency. The resistive impedance of bonding wires is ignored since the length of bonding wires is very short which means the associated resistance is very low.

To calculate the values of bonding wire impedance, the parameter values are shown in Table 3.1. The material of bonding wires is gold.

Table 3.1: The parameter valued for the model of bonding wires

Parameter	Value	Unit
μ_0	$4\pi\times10^{-7}$	H/m
μ_r	1	H/m
ρ	2.44×10^{-8}	Ohms/m
1	3	mm
d	0.0363	mm

The PCB is specially designed and built for the driver testing. The board should be designed as small as possible to minimize the parasitics. However, the board has parasitic impedance in itself that should be modeled for realistic prediction of the signal behavior. The size of the board is assumed as 4.5 cm × 4.5 cm. The model of metal strips in the board can be constructed in ADS with five-ladder structure. In the board, the metal strip is partitioned into five parts as illustrated in Figure 3.2 for modeling since the metal strip is tapered to fit SMA connectors and bonding wires.

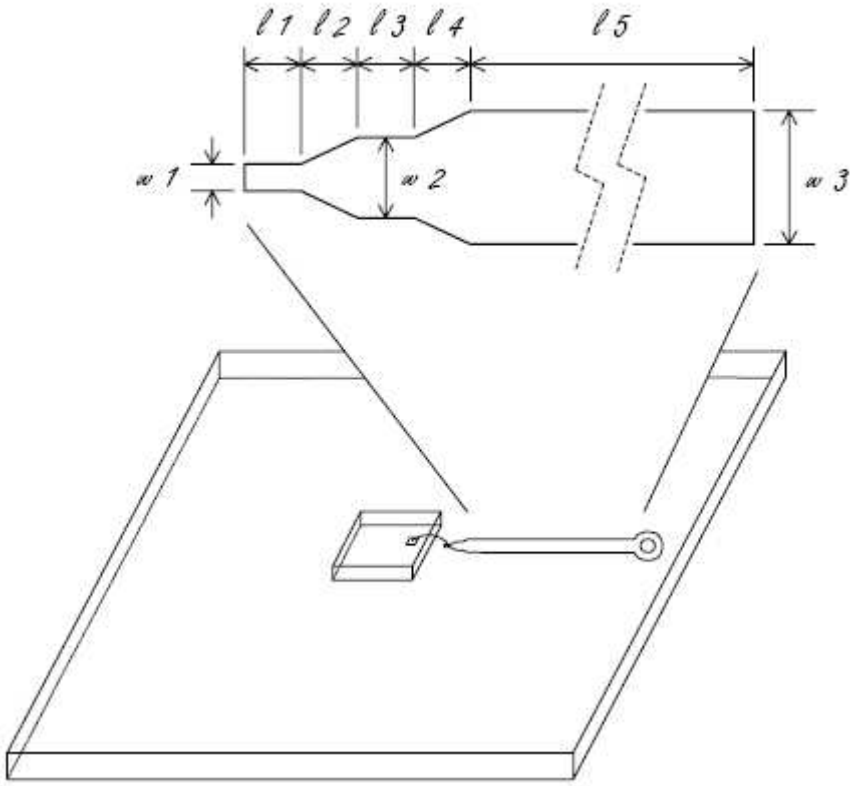


Figure 3.2: The diagram of metal strip in PCB

To extract the values of the board impedance, the lengths and widths are shown in Table 3.2. The material of the metal strip is tin.

Table 3.2: The length and width of metal strips in PCB

Parameter	l_1	l_2	l_3	l_4	l_5	w_1	w_2	w_3
Value	59.421 mil	16.745 mil	21.33 mil	27.735 mil	620.18 mil	10.01 mil	29.981 mil	49.894 mil

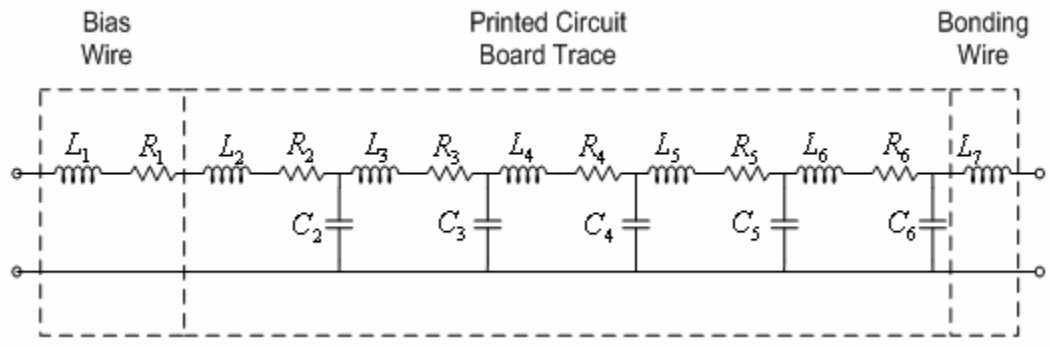


Figure 3.3: The final equivalent model of packaging

The final equivalent model of packaging is shown in Figure 3.3. It consists of bonding wire, board line, and bias wire parasitics. The value of parasitic impedance in the model is given in Table 3.3.

Table 3.3: The value of parasitic model

Parameter	Value	Parameter	Value
L_1	10.5 nH	C_4	0.367874pF
L_2	1.38664 nH	C_5	0.367874pF
L_3	1.38664 nH	C_6	0.367874pF
L_4	1.38664 nH	R_1	0.0280365 Ω
L_5	1.38664 nH	R_2	0.0280365 Ω
L_6	1.38664 nH	R_3	0.0280365 Ω
L_7	3.996 nH	R_4	0.0280365 Ω
C_2	0.367874 pF	R_5	0.0280365 Ω
C_3	0.367874 pF	R_6	0.0280365 Ω

CHAPTER 4

SINGLE ENDED TRANSIMPEDANCE AMPLIFIER DESIGN FOR PAM SIGNALING

4.1 Introduction

In recent years, the demand for fiber optics in data transmission is increasing rapidly; since then the integration of optoelectronic devices, interface circuitry, and other digital VLSI circuits in a single chip is gaining more attention. In most optical-to-electrical interface circuits, the front-end of the receiver consists of a photo-detector followed by a preamplifier, and this front-end traditionally designed in bipolar, GaAs and InGaAs compound semiconductor technologies. However, due to low-level of integration with other digital ICs, the receiver design using these technologies are limited to short range applications. On the other hand, their CMOS counter-part can be used for high- level integration of circuits together, especially for the mixed signal application, even though they have not shown enough performance to survive in such a noisy environment without sacrificing other important attributes such as gain, bandwidth, and large parasitic capacitances.

In this thesis various aspects that affect the performance of the optical receiver front-end are investigated, and a wideband differential CMOS transimpedance suitable for PAM application has been designed. Issues that arise from the submicron CMOS

technologies, such as low substrate resistance, high junction capacitance, low trans-conductance, and low supply voltage, are considered and addressed carefully in the design phase.

4.2 Design of Transimpedance amplifier

To ameliorate the tight trade off offered by the low and high impedance preamplifier, various TIA topologies has been considered here, as it lessens the design intricacies. Few performance parameters are lime- lighted before going into the design of single-ended transimpedance amplifier. In designing an optical receiver front-end, two major factors must be considered. These are the bandwidth of an amplifier and the input sensitivity. The bandwidth of the overall optical receiver is usually determined at the first stage, and it can be estimated by its RC time constant contributed by photo-detector stray capacitance, feedback resistance and other parasitic capacitance. Hence to meet the required SONET standard, a photo-detector with less detector capacitance should be chosen. In this design, MSM detector capacitance of 100fF is included in the simulation. The noise that affects the sensitivity is primarily related to the preamplifier input impedance. Hence it is crucial to choose the appropriate circuit topology that gives an optimal trade-off between bandwidth and input signal sensitivity for given system requirements. Atypical front-end optical receiver structure is shown in the Figure 4.1

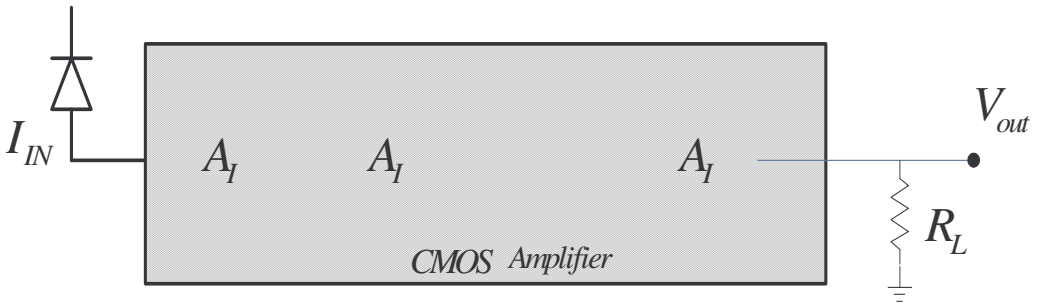


Figure 4.1: Front-end Optical receiver structure

4.2.1 Single-ended TIA structure

Single- ended TIA design is widely used because the current produced by the photo-detector is single ended. The structure utilized here is the most commonly used shunt-shunt feedback topology, where the negative feedback network senses the voltage at the output and returns a proportional current to the input. This type of feedback is chosen because it lowers both the input resistance; there by increasing the bandwidth and allowing the amplifier to absorb the photodiode current, and the output resistance; there by yielding better drive capability. Several researches on single ended TIA have been performed. [27],[28],[29],[30],[31],[32],[33][34] The single-ended TIA shown in the Figure 4.2 is designed to meet the OC-48 SONET standard.

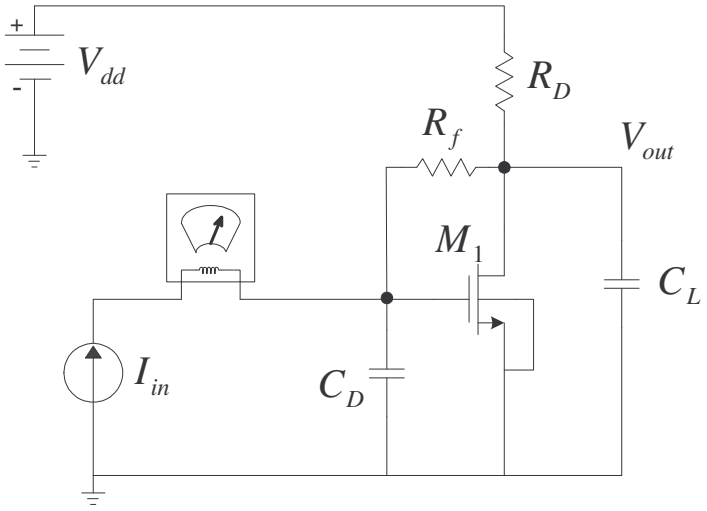


Figure 4.2: Single ended Transimpedance amplifier

The single ended TIA shown in the Figure 4.2 is designed to work for 4-PAM, 8-PAM and 16 level PAM signaling. The simulation results are discussed later in the chapter. As illustrated in the figure, the detector capacitor is modeled as $C_{D.}$ The gain and bandwidth of the preamplifier is adjusted by varying the load resistor and feedback resistor respectively.

4.2.2 Gain and amplifier bandwidth

The gain and bandwidth of the single-ended design is mainly characterized by the feedback resistance and the parasitic capacitance from the detector. The transimpedance gain of the single ended structure is given by

$$\frac{V_{out}}{I_{in}} = -\frac{A}{A+1}\frac{R_F}{1+\frac{R_F C_D}{A+1}s} \tag{4.1}$$

As given by Equation (4.1), the feedback amplifier provides a midband transimpedance gain of approximately R_f but with a time constant of $R_fC_D/(A+1)$.

The -3-dB bandwidth is thus equal to

$$f_{-3dB} \approx \frac{1}{2\pi}\frac{A}{R_F C_D} \tag{4.2}$$

Where, A is the amplifier gain.

4.2.3 Noise analysis

It is instructive to study the noise behavior of the single ended circuit. Modeling the input referred noise of the amplifier by a voltage source $\overline{V_{n,A}^2}$, the overall output noise voltage of the circuit is given by,

$$\left(V_{n,out} + \frac{V_{n,out}}{A} - V_{n,A} - V_{n,RF}\right)\frac{1}{R_F} = \left(-\frac{V_{n,out}}{A} + V_{n,A}\right)C_D s \tag{4.3}$$

$$V_{n,out} = \frac{V_{n,RF} + \left(R_F C_D s + 1\right)}{1 + R_F C_D s / A} V_{n,A} \tag{4.4}$$

The input-referred noise current is given by

$$\overline{I_{n,in}^2} = \frac{\overline{V_{n,RF}^2} + \overline{V_{n,A}^2}}{R_F^2}$$

$$= \frac{4kT}{R_F} + \frac{\overline{V_{n,A}^2}}{R_F^2} \tag{4.5}$$

Here, the noise voltage of R_F is directly referred to the input; the noise voltage of A is divided by R_F. The significance of feedback topology is that, feedback resistor R_F, need

not carry a bias current and its value does not limit the voltage headroom. The overall input-referred noise current should be obtained by integrating the total output noise voltage over the noise bandwidth to obtain meaningful effect.

4.3 Post amplifier design

Single-ended TIA designed, cannot amplify the weak current signals produced by photo-detector to large magnitude voltage signal; desired to meet to the specifications of the industry optical communication protocols FDDI and SONET. The target bandwidth of the amplifier should be greater than 2.5Gbps. In order to obtain such a high operating speed and to boost the voltage gain, design optimization yields a cascaded single-ended, low-gain-per each stage design as shown in Figure 4.3. The common source amplifiers are used as post amplifiers. As shown in the figure below, a resistive load amplifier are used, so as to achieve higher gain at the cost of using passives in the circuit and the dependence of gain on the resistive load results in non-linearity.

Assuming that the overall transimpedance gain is A_T, and a bandwidth of f_T, the best overall design for the amplifier would be that which minimizes the power dissipation. Assuming that each stage is identical and has one dominant pole and that the power dissipation of each stage is proportional to the gain-bandwidth product (GBW), then the power dissipation of the amplifier is proportional to the sum of GBW of each stage.

The normalized single stage gain-bandwidth product is defined by NGBWs, and is given by

$$\text{NGBWs}=\frac{GBWs}{A_T f_T} \tag{4.6}$$

GBWs is the gain-bandwidth product of individual stage and given by

$$\text{GBWs} = \frac{f_T}{\sqrt{2^{1/n} - 1}} \cdot A_T^{1/n} \tag{4.7}$$

The overall gain of the cascaded transimpedance amplifier is given by

$$A_T = A_I^{\,4} \cdot R_L \tag{4.8}$$

where A_I is the gain of individual stage and R_L is the output load resistance.

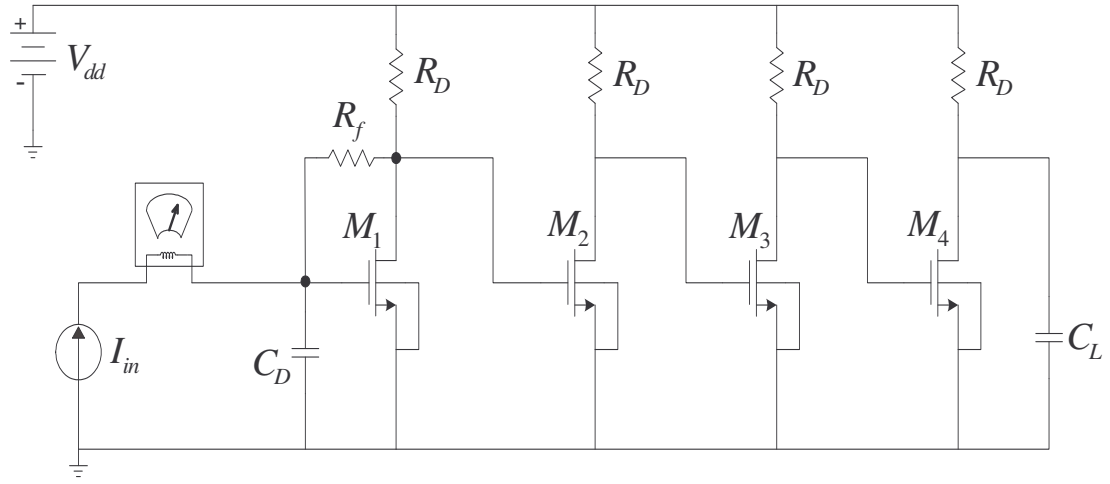


Figure 4.3 Single ended- TIA followed by post amplifier

In this design, the final amplifier consists of 3 post-voltage amplifier stages followed by the TIA. If too many stages are cascaded, a DC offset problem can occur since all stages are dc coupled and, in practice, the bandwidth decrease due to the accumulated effect of the parasitic capacitance associated with each amplifier stage. Thus an amplifier with about 4 stages is the optimal design for this application. The overall gain and bandwidth of the amplifier are included in the Table 4.1.

Table 4.1: Performance Analysis

Parameters	**TIA**	**PostAmp1**	**PostAmp2**	**PostAmp3**
Output Swing (mV)	31.5	56	97	172
Tran impedance Gain (dB)	47	52	57	62
3-dB Bandwidth (GHz)	4.024	3.63	3.3	2.85
Power Consumption = 27.36 mW				

4.4 Simulation

The design simulation is carried out in Advanced Design System (ADS) tool using TSMC 0.18μm CMOS technology with a maximum supply voltage of 1.8V at a gate length of 0.18 μm. In the design, a photo-detector stray capacitance is included to perform a realistic simulation. Usually the detector capacitor ranges from 0.1pF to 10pF. The detector capacitor greatly affects the speed of the front-end circuit. In order to meet the OC-48 SONET standard and achieve an overall speed of 2.5Gbps, a photo-detector with minimal capacitance should be chosen. Hence in this design, MSM

photo-detector with a capacitance of 100fF is modeled and included in the circuit simulation.

4.4.1 AC and noise analysis results

The AC analysis result of the overall amplifier is shown in the Figure 4.4. Even though the speed of the amplifier falls at each stage due to the accumulation of parasitics from the MOS transistors, the final overall achieved speed still meets the required standard. But the output magnitude level of around 172 mV is not sufficient enough for further signal processing. Increase in number of post amplifiers would result in falling of speed; there by making the single ended amplifier ill-suited for high speed optical receiver especially for PAM application.

The noise analysis is also illustrated in the figure below and input referred noise current is plotted for sensitivity calculation.

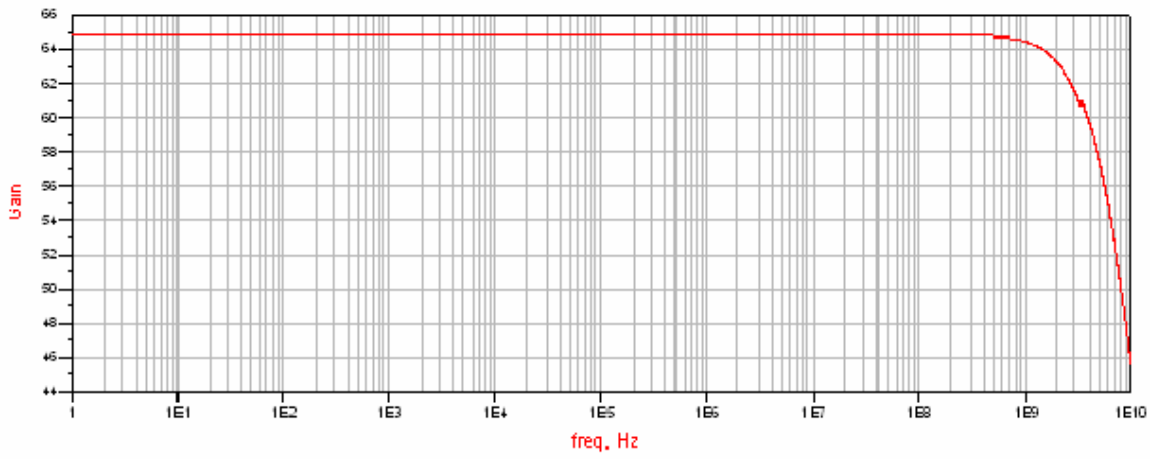


Figure 4.4: AC analysis of overall cascaded single ended stage

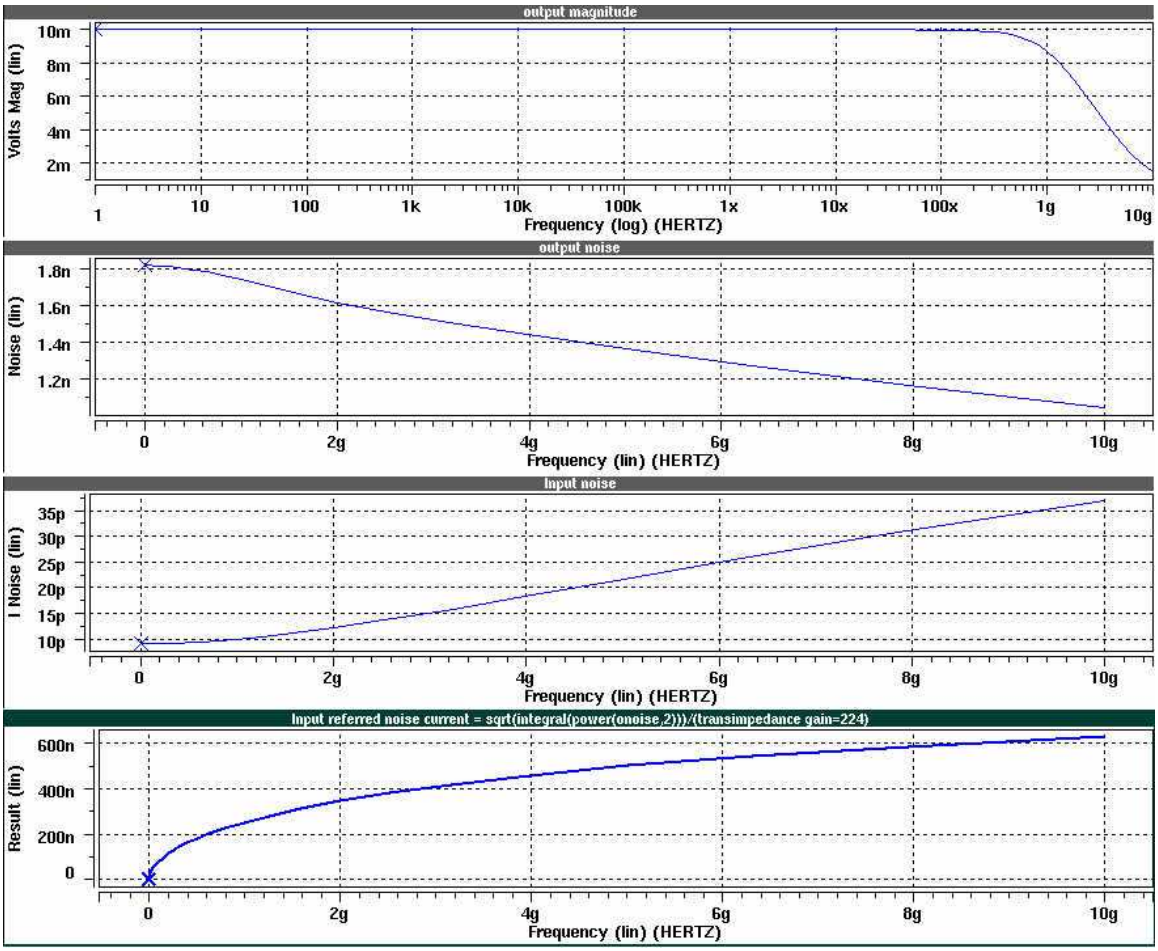


Figure 4.5: Noise analysis of the single ended transimpedance amplifier

4.4.2 Generation of multilevel PAM signal

An M-ary ASK optical intensity signal can be obtained by applying an M-ary electrical signal to a power combiner at the half power point of its transfer characteristic. Generating a 4-ary electrical signal from two binary tributaries at Gbit/s rates can be accomplished using the circuit shown in Figure 4.6. The multilevel signals with a operating speed of 2.5Gbps are generated using optical backplane communication tool, VPI transmission maker. The data source is included in ADS simulation using VPI link utility tool available in ADS. By comparing the M-ary signal bandwidth to a binary

signal of the same bit rate, the M-ary signal bandwidth is lower by a factor of $1/\log_2(M)$ where M is the number of levels. In other words, the M-ary signal transmits $\log_2(M)$ times as much data as binary signaling on the same bandwidth. In addition, the spectral efficiency is increased by a factor of $2\log_2(M)$ [13].

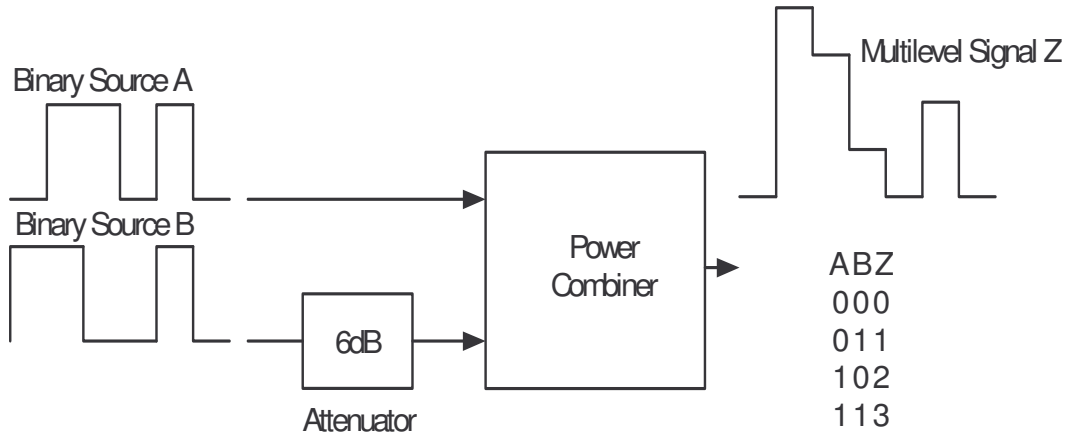


Figure 4.6: Generation of PAM signals

4 level, 8-level and 16-level PAM signals generated in VPI tool are shown in the figure below.

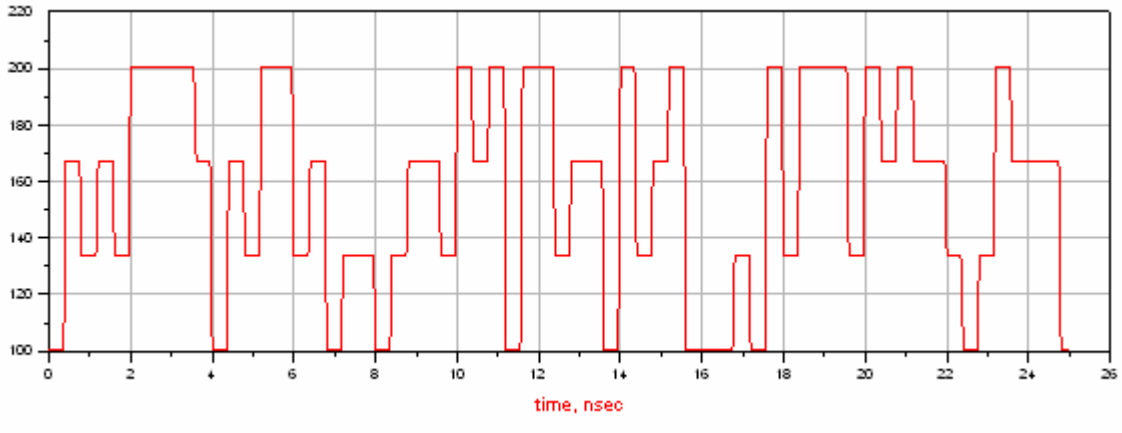


Figure 4.7: 4 –Level PAM signal

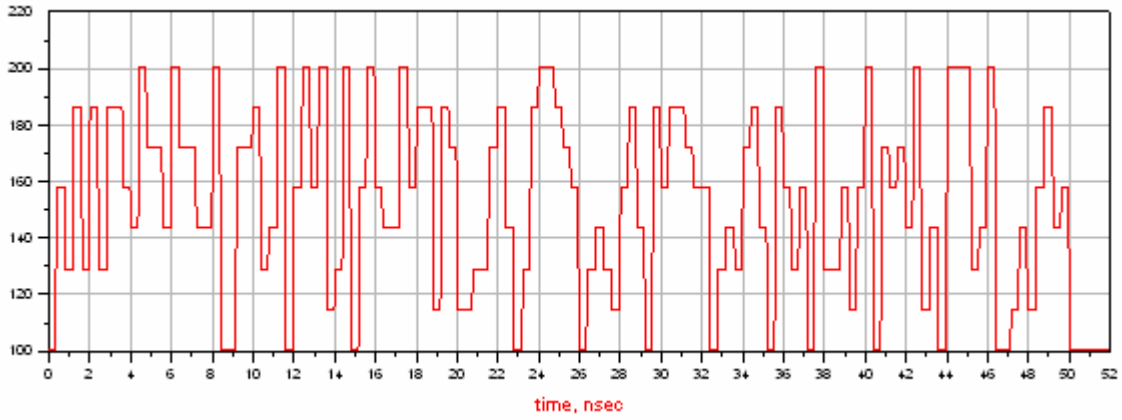


Figure 4.8: 8 –Level PAM signal

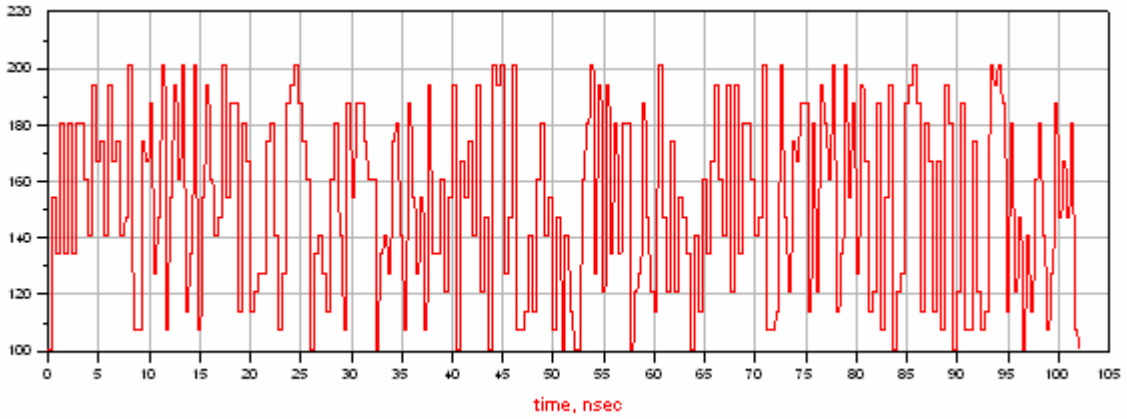


Figure 4.9: 16- Level PAM Signal

4.4.3 Transient and eye diagram analysis

The transient response of all the 3 different PAM schemes is included in the Figure 4.10 below. The output magnitude of 172mV is obtained with the operating speed of 2.5Gbps. The top trace shows the transient analysis result and the bottom one displays the corresponding eye diagram.

To visualize the effects of inter-symbol interference (ISI) effects, which manifest it differently for different bit patterns, long sequence of random waveforms must be examined. Eye diagram of all the PAM signaling is obtained in order to trace the ISI effects. The results are shown in the figure below. Cleaner the eye, better the performance of the system. The eye opening in wider and all the levels are obtained without any non-idealities like nonlinearity issue. The eye diagram mask meets the OC-48 SONET standard.

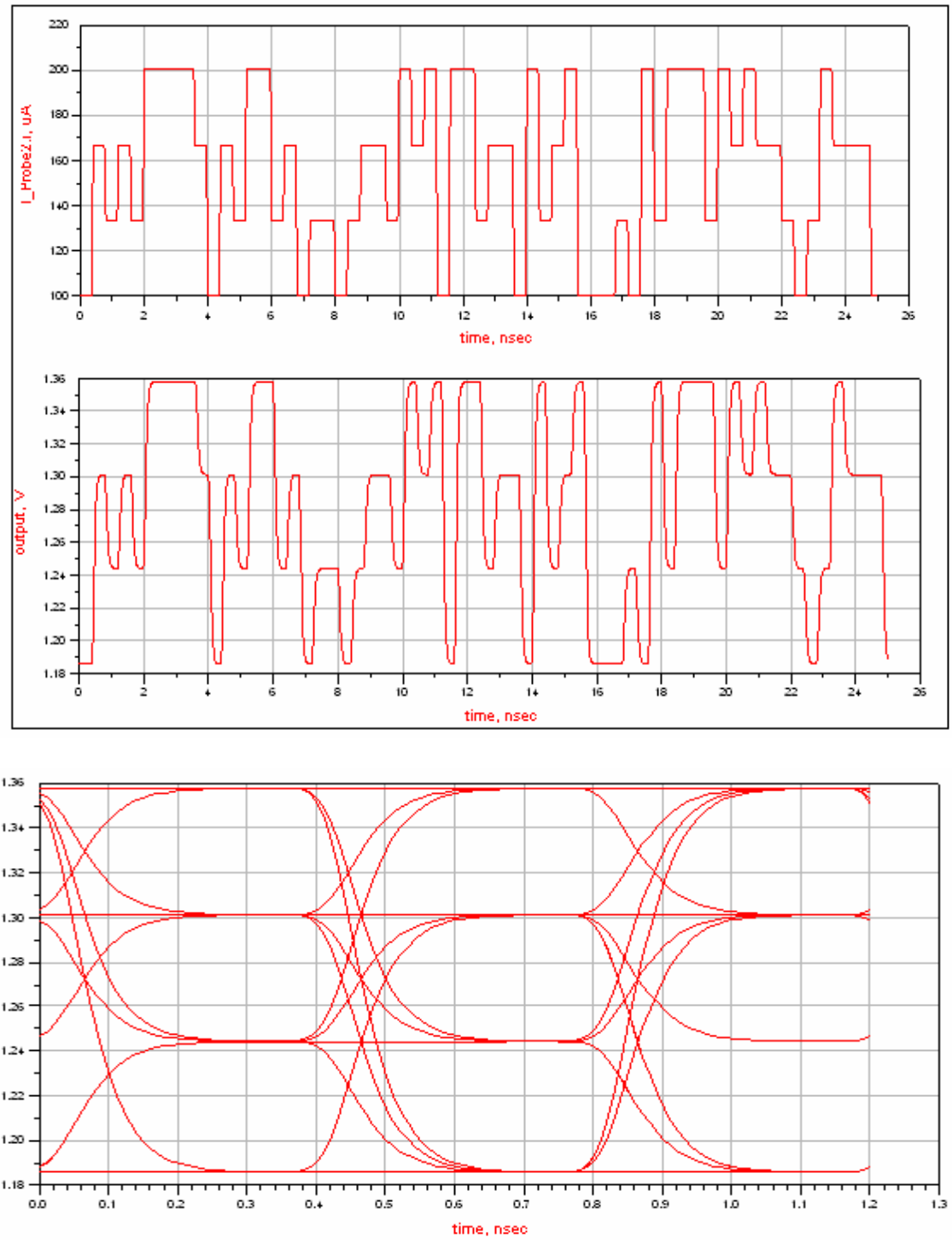


Figure 4.10: Top trace: Transient response of 4 levels PAM with operating speed of 2.5Gbps. Bottom trace: Eye diagram of the overall single ended TIA design

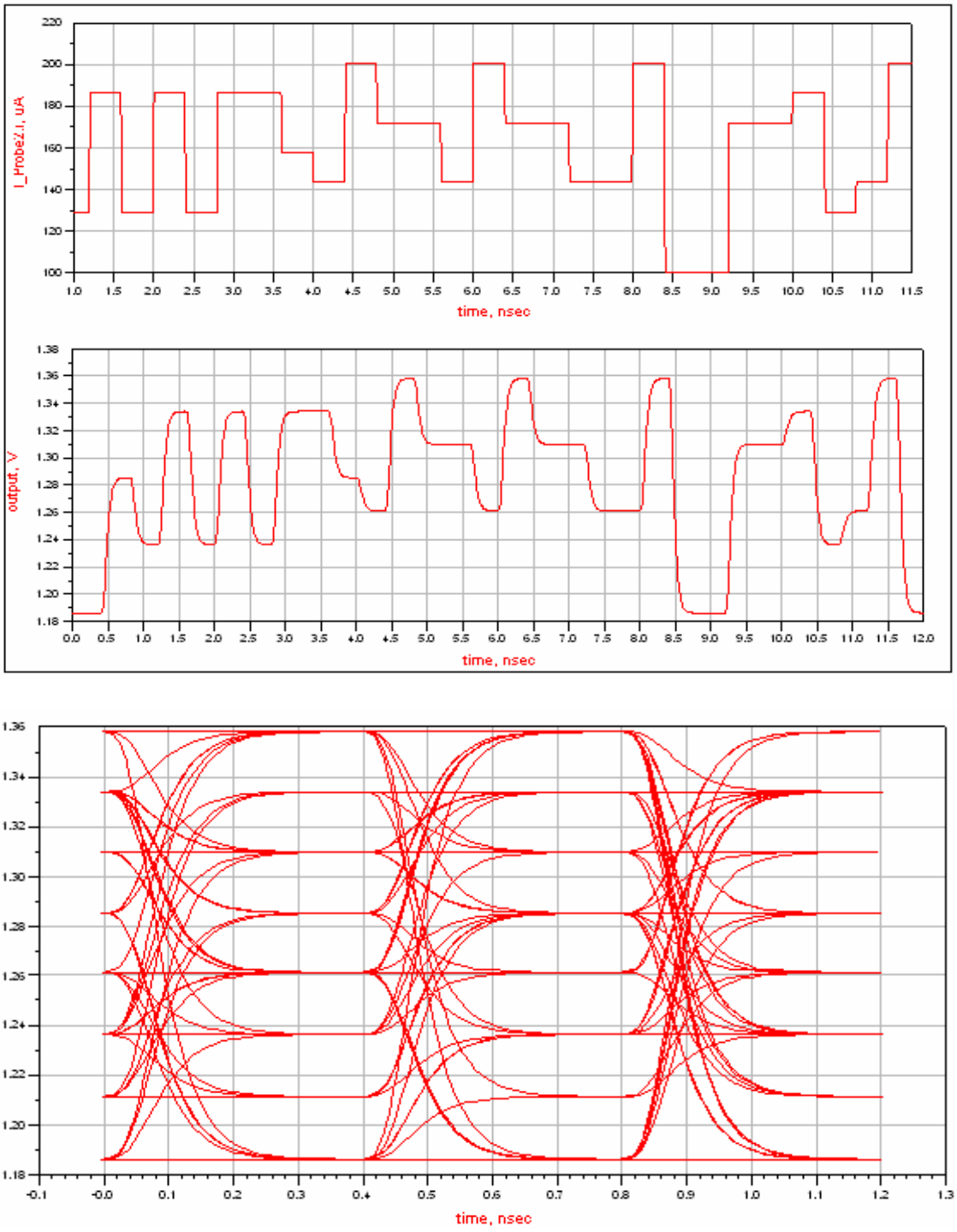


Figure 4.11: Top trace: Transient response of 8 levels PAM with operating speed of 2.5Gbps. Bottom trace: Eye diagram of the overall single ended TIA design

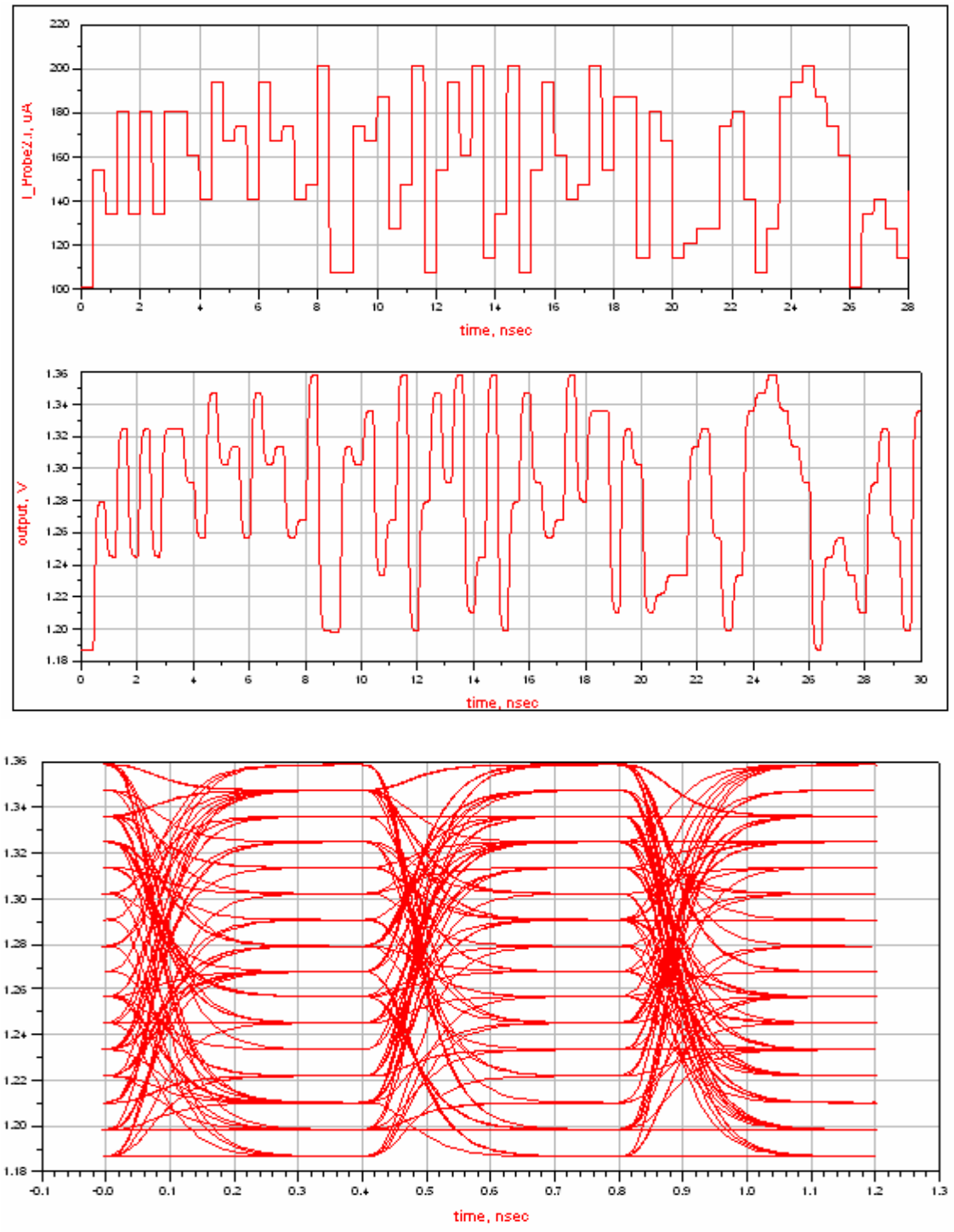


Figure 4.12: Top trace: Transient response of 16 levels PAM with operating speed of 2.5Gbps. Bottom trace: Eye diagram of the overall single ended TIA design

4.4.4 Effect of packaging parasitics

As discussed earlier in the previous chapter, in order to include the power supply parasitics caused by the package, bonding wire and PCB board, a realistic extraction of all these parasitics are included. The model shown in chapter 3 are included in the V_{dd} and V_{ss} power supply rails as shown in figure below and the simulation is carried out to observe the effects of those parasitics.

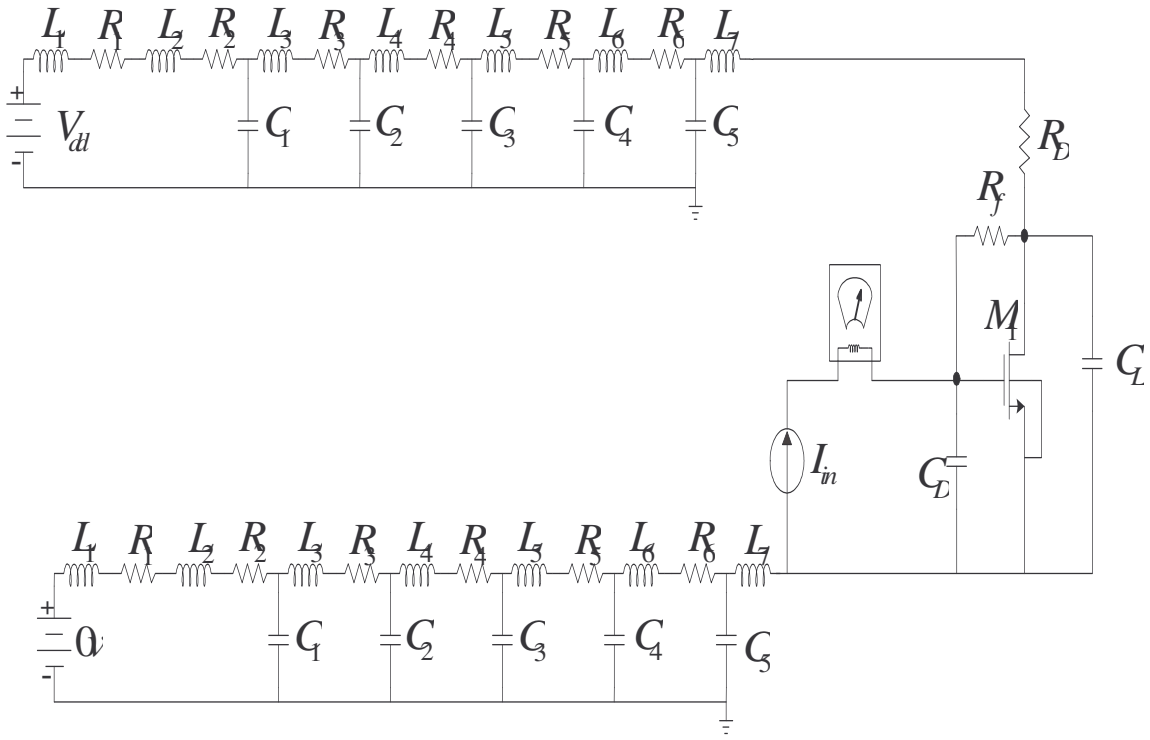


Figure 4.13: Effects of packaging parasitics in the power supply rails

The main drawbacks of single ended receiver designs are; they have no mechanism to remove noise picked up from the surrounding environment. In addition, single ended designs can produce noise because of large change in supply currents. To illustrate the risks associated with not a using a fully differential topology, the single ended transimpedance amplifier design has been simulated in the presence of large

digital noise at the input. The Figure 4.14 shows the receiver input and output signal when the substrate noise from parasitic model reaches the input node of the receiver. The output signal has been highly corrupted by the digital noise and thus becomes highly impractical for the high speed application.

To illustrate the noise production problem associated with single ended designs, the power supply current of the amplifier is simulated in ADS. The following figure shows

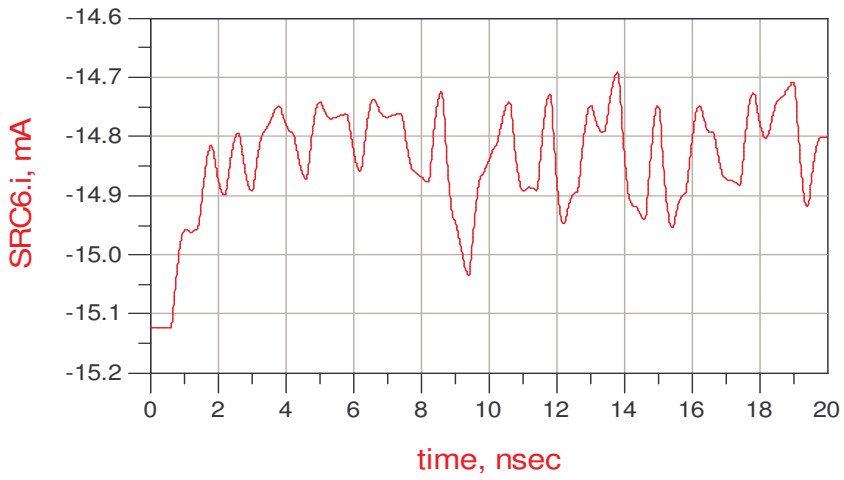


Figure 4.14: Change in power supply current of single-ended TIA due to substrate noise

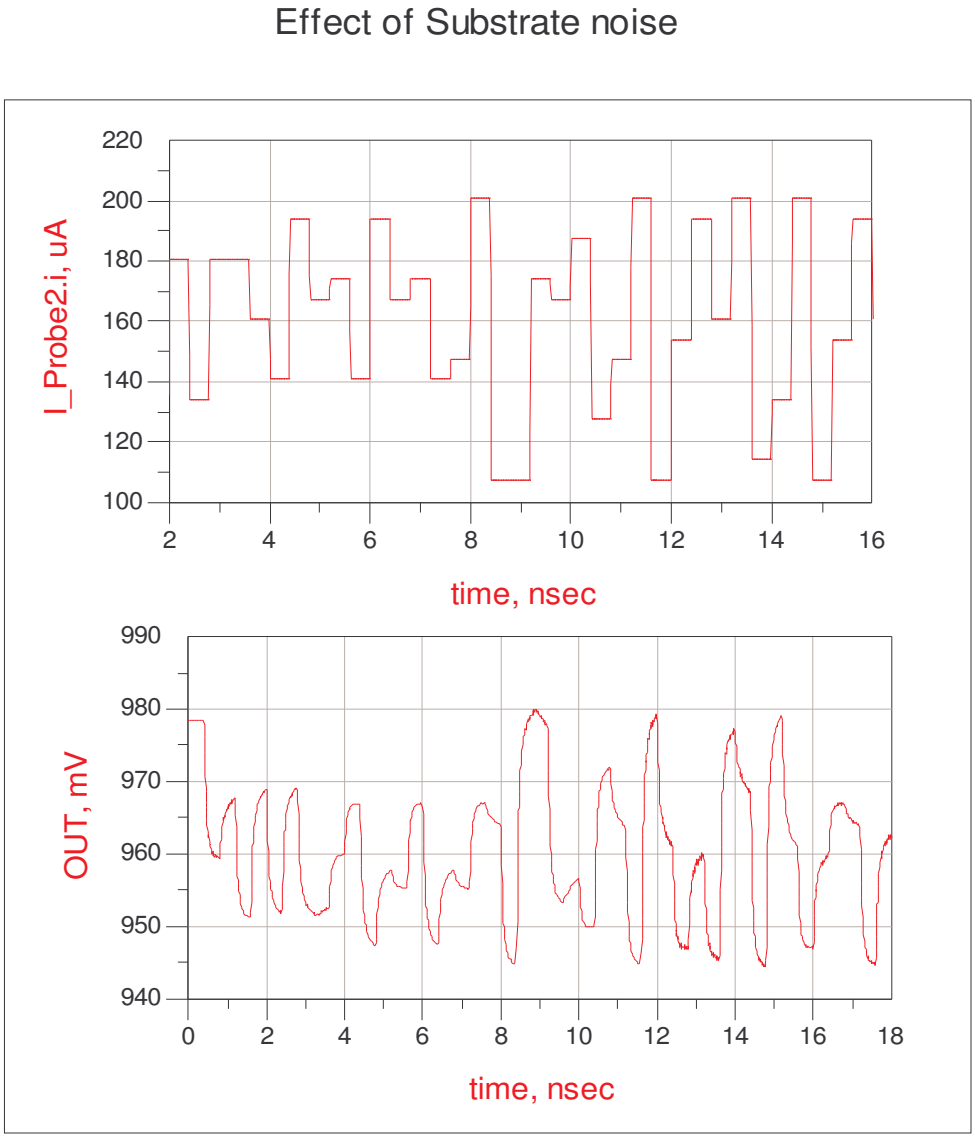


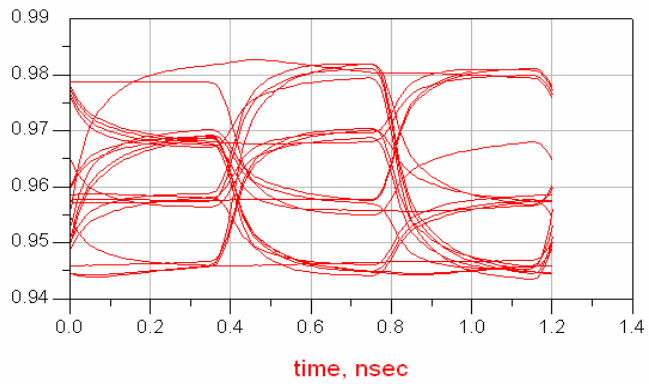
Figure 4.15: The noise-free 16 level PAM input signal current to the receiver with about 100 micro amp peak to peak.

that; there is around 0.5 milliamp change in the supply current in less than 1ns. This current can produce 5 millivolts of noise in a 5-10nH bond wire inductance maximum. It's numerically given by

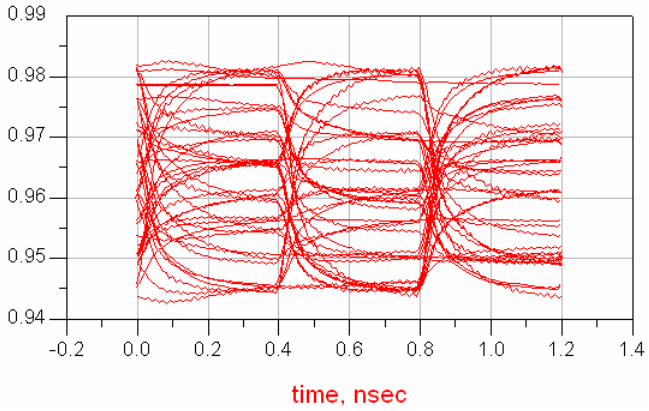
$$L \times \frac{di}{dt} = 10\text{nH} \times \frac{0.5mA}{1ns} = 5\text{ mV} \tag{4.9}$$

This noise voltage magnitude is comparable to the input voltage magnitude found on the receiver, which will result in oscillations (noise problem) due to output feedback in this amplifier.

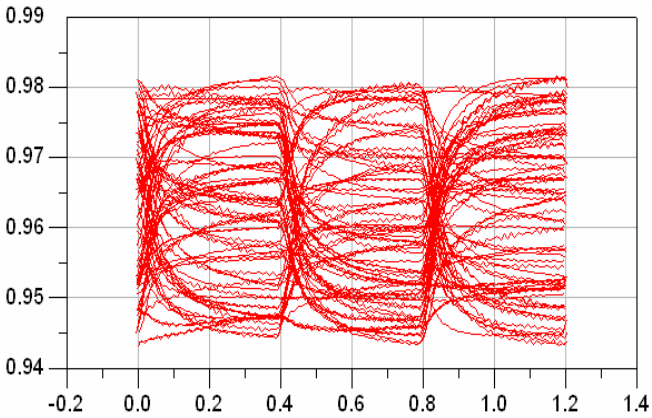
The effect of substrate noise can be better visualized using the eye diagram measurement. The following Figure 4.16 shows the eye diagram measurement of 4-level, 8- level and 16- level PAM signaling.



(a)



(b)



(c)

Figure 4.16: Eye diagram of 4, 8 and 16 level PAM signaling showing the ringing effect caused by the line impedance and parasitic capacitance of the power supply line. (a) 4 level (b) 8 level (c) 16 level

From the above analysis, it is observed that, eye opening is totally getting closed when number of levels for PAM signaling is increased, especially in the 16-level case, the eye diagram and the levels are totally ruined. This is mainly because; the total overall magnitude of the output voltage signal is divided equally among the 16 PAM output levels with smaller amplitudes. The substrate noise gets accumulated on the smaller output levels and thereby corrupting the transient response of the multi-level signals. Thus resulting in false detection of the transmitted data format, at the optical receiver.

Other than this, the step response exhibits ringing due to the over-damped time response, both creating ISI and corrupting the high and low levels of the data. The 'ringing effect' is caused due to the power supply impedance and large device parasitics which resonates at higher frequencies. The ringing effect of the output voltage levels are observed in the eye diagram analysis. To alleviate the supply dependence of single-ended TIA, a decoupling capacitor of 4nF is included between the power supply lines to eliminate the effect of substrate noise. However the ringing effect is still noticed in the Figure 4.17-4.19, even though the eye opening and the output levels are restored properly. Furthermore, if the decoupling capacitor acts as a short circuit for the broadband system, then it fails to reject the supply noise frequencies in the region of interest.

Thus due to these major drawbacks, single-ended TIA design is undesired for high- speed SONET standard application. Therefore we propose a fully differential topology for transimpedance amplifier design in the next chapter, which are highly

unaffected by the substrate noise due to their differential signaling compared to single-ended signaling. Apart from this, differential topologies are recommended for high speed application [12] due to higher bias current requirement.

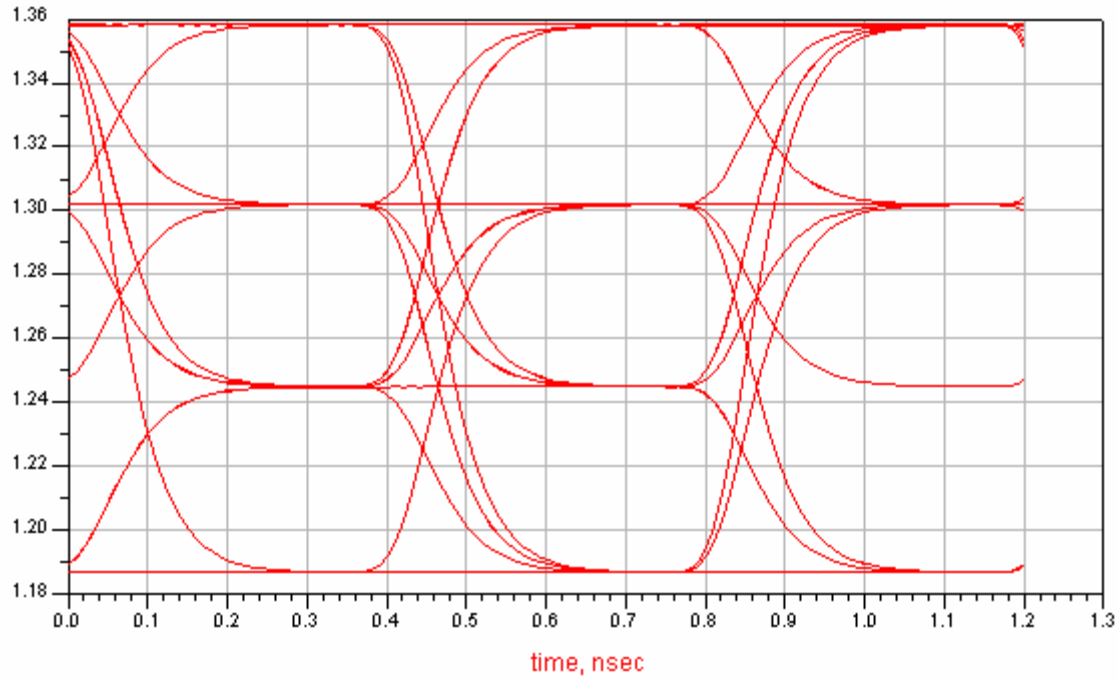


Figure 4.17: Effect of including decoupling capacitor with 4nF to eliminate the substrate noise in 4-level PAM signaling.

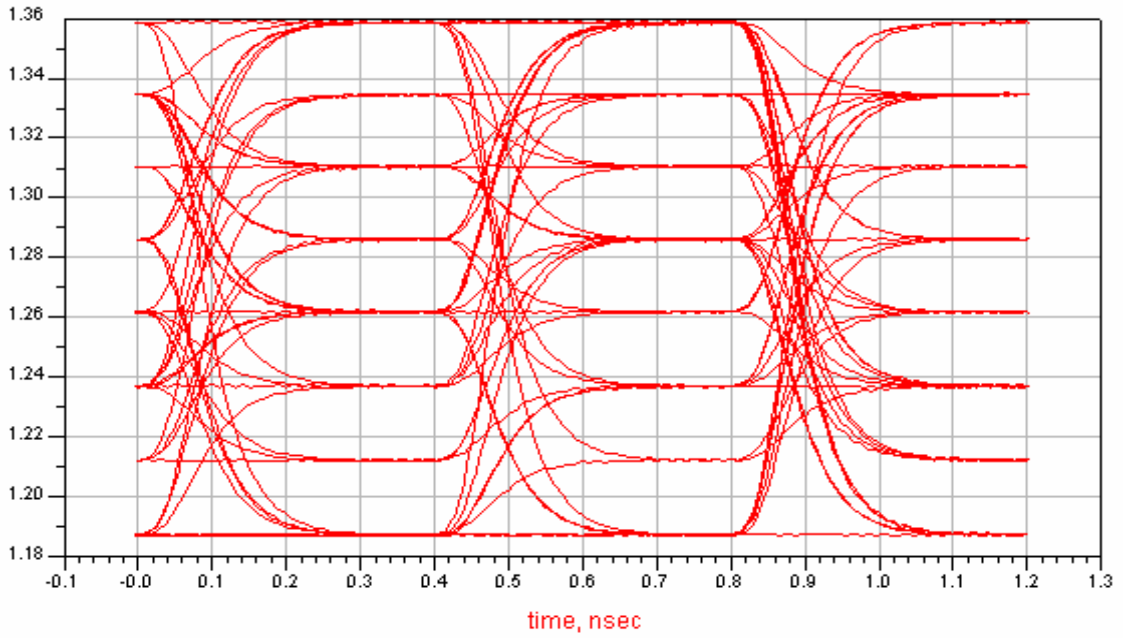


Figure 4.18: Effect of including decoupling capacitor with 4nF to eliminate the substrate noise in 8-level PAM signaling.

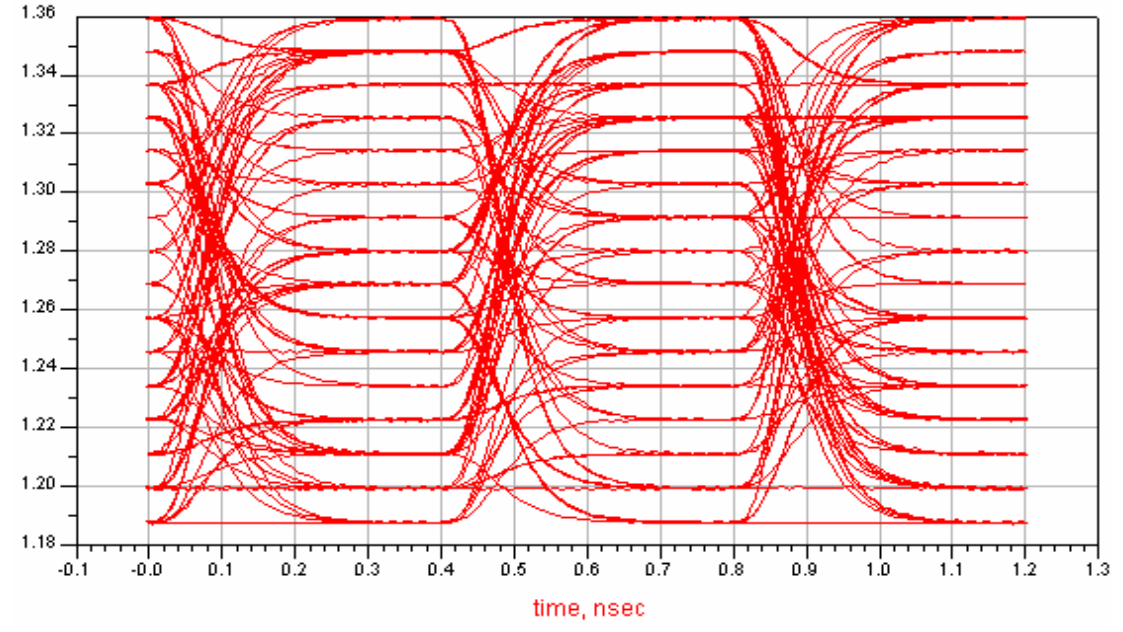


Figure 4.19: Effect of including decoupling capacitor with 4nF to eliminate the substrate noise in 16-level PAM signaling.

CHAPTER 5

PROPOSED FULLY DIFFERENTIAL TRANSIMPEDANCE AMPLIFIER DESIGN FOR PAM SIGNALING

5.1 Introduction

As a demand for the use of fiber optics in computing increases, the complexity of electronic functions in computational systems that use optical interconnections, analog optoelectronic (OE) devices and the interface circuits must operate in the presence of digital processing circuitry which produces digital switching noise [19]. Single-ended transimpedance architectures, despite the advantages of having high-gain, high-bandwidth, and low-power consumption, are not suitable because they are very susceptible to switching noise and plagued by stability problems stemming from parasitic feedback paths. A large substrate cross-talk noise, when integrated with other digital circuitry, also may significantly deteriorate the performance of a receiver, especially when using a low-level input signal under low-supply voltage in the submicron CMOS [35], [36].

The primary methods used to alleviate the large supply noise present in a mixed digital and analog circuit environment are to keep the sensitive analog parts away from the noisy digital parts, or to block the noise transmission from the digital circuitry. Thus, in addition to careful layouts including separate power supply lines, shields, and epitaxial layers underneath the transistors, differential circuit architectures are inevitable

in designing optical receiver systems that are unsusceptible to substrate noise [37],[38],[18],[23],[39] . Differential receiver designs attempt to remove noise due to two main reasons. Firstly they try to eliminate noise from their inputs by using identical, parallel signal paths with a 180-degree phase difference in differential circuits due to their good Common Mode Rejection Ratio (CMRR). The differential signals are to pick up the same noises that will be subtracted during amplification processes, and thus prevent them by passing to the multiple amplifier stages. Secondly, the bias current stabilization using balanced topology prevents incoming noise components which have same harmonics as the signal. Therefore differential topologies are preferred from mixed-signal crosstalk and high-speed perspective. In this research, a fully differential transimpedance amplifier suitable for PAM signaling application has been designed. Multistage post voltage amplifiers have also been cascaded to improve the overall trans-impedance gain. An output buffer to drive the 50 Ω impedance of the transmission line has also been designed. The design is carried out in TSMC 0.18μm CMOS technology with an overall operating speed of 2.5Gbps. The noise immunity to mixed-signal digital switching noise of the differential amplifier has been shown to be good enough to generate 10^{-9} BER with a receiver sensitivity of -14dBm.

5.2 Significance of differential signaling

The performance of the IC is limited by the packaging technology. To overcome the packaging restriction, the differential topology can be used so as to greatly minimize the current ripples in power supply lines. The Figure 5.1 shows the effect of differential signaling on power supply noise. In single ended and differential case, the V_{DD} changes by ΔV and the output voltage also approximately changes by the same amount, which implies that output is quiet susceptible to the noise on supply lines. However in differential circuit, due to symmetric topology, the noise on V_{DD} affects V_x and V_y but not in the differential output (V_x-V_y). Hence they are more robust to power supply noise and results in reduction of delta-I noise.

Secondly differential amplifiers are highly immune to environment noise. When two adjacent lines in a circuit carry a small, sensitive signal and large clock waveforms, due to capacitive coupling of between the lines, the transitions on line L2 corrupt the signal on the line L1. However in presence of difference signals, the common mode noise is rejected due to equal and opposite phase transitions. Finally, it is also beneficial to employ differential distribution for noisy lines. Apart from highly immune to all kinds of noises, differential signaling also helps in achieving high linearity and maximum output voltage swings compared to the single ended structures.

However, since photodiodes produce a single-ended current and since their cathode is connected to high voltage to allow high quantum efficiency, the input signal is not differential, leading to several design difficulties. Furthermore, the numerous

advantages of differential operation by far outweigh the possible increase in area and the single-ended current of the photodiodes.

5.3 Design of differential transimpedance amplifier

Figure 5.1 depicts the block diagram of the differential optical receiver front end, which is composed of a transimpedance stage with a single-loop resistive feedback, a post amplifier, and a 50Ω driving buffer. The goal of the research for this thesis is to design a PAM signaling based high-speed optical differential transimpedance amplifier compatible for short-reach optical links, which limits the target distance and there by lowering of requirements for preamplifier gain and noise because a lot more optical power is available at the input. The circuit was realized using TSMC 0.18μm CMOS technology and simulated along with the small signal model of photo-detector to measure the overall optical front-end performance.

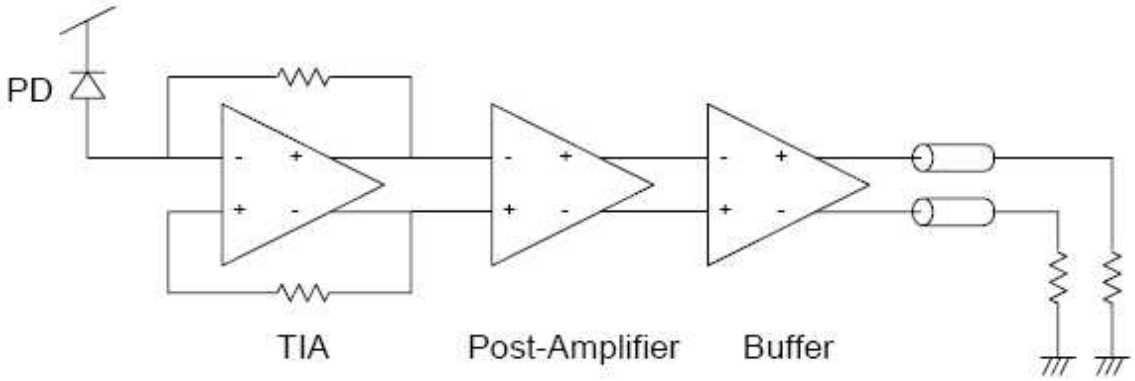


Figure 5.1: Differential TIA structure

5.3.1 Differential TIA design

In this research, a wideband optical receiver having a resistive feedback differential transimpedance amplifier is designed. This front end circuit converts the current produced by photo-detector into voltage signal. The resistive feedback reduces the both input and output impedance. Thus it provides wider bandwidth and good drive capability. Further the controllable feedback resistors help optimization of input sensitivity for a given bandwidth with stabilized bias current. In this design, a resistive load is used to provide higher transimpedance gain.

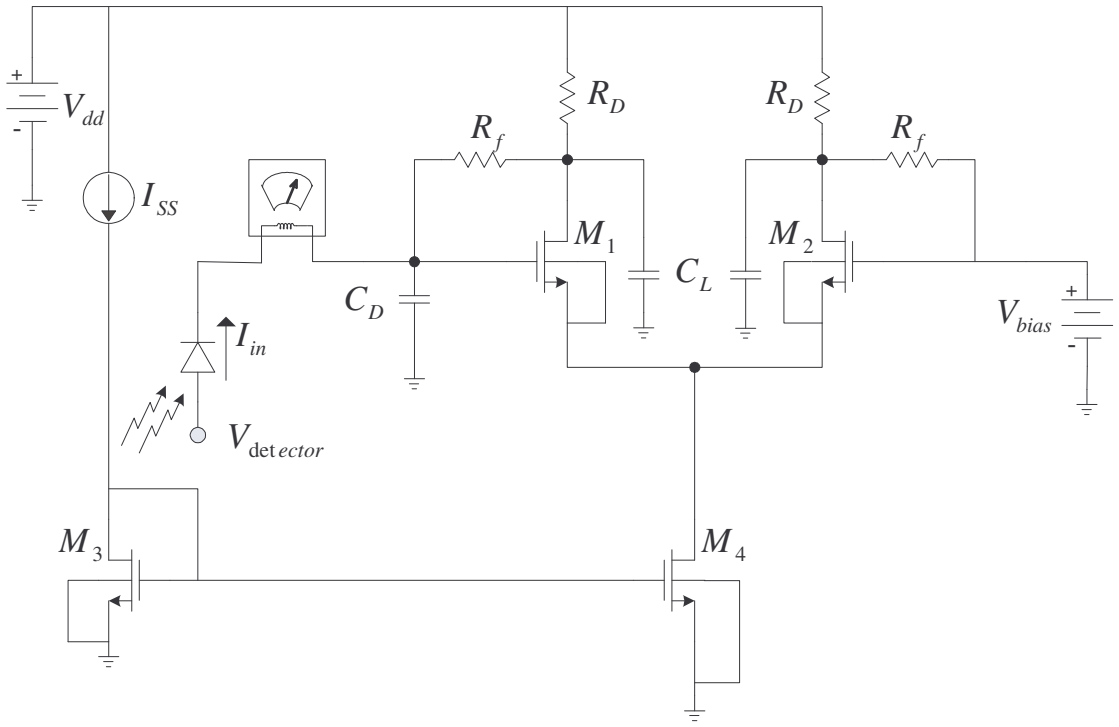


Figure 5.2: Proposed Differential Transimpedance amplifier

Multilevel input current of 100μA is utilized. Since the current produced by the photodiode is single ended, the other side of differential amplifier is biased separately

by a voltage source to obtain the similar input common mode level. The tail current of the differential pair is provided by the transistors M3 and M4 forming the current mirror. The input common mode level should is adjusted by the drain voltage of M4 in such way that the input transistors M1 and M2 are in saturation to provide maximum output voltage swing. The values of load and feedback resistors are carefully chosen, so that wide bandwidth is obtained at the front-end with acceptable transimpedance gain.

Table 5.1: Design Goal of Differential Transimpedance amplifier

Specification	Desired Goal of Design	Standard
Speed	2.5Gbps	SONET OC-48 standard when driving 50Ω termination load.
Transimpedance Gain	>60 dB	
Output swing	> 100mV	
Receiver Sensitivity	-11dBm with 100 μA	

5.3.2 Device intrinsic noise

The noise, intrinsic to devices in all electronic circuits fall into three major categories: shot noise, thermal noise and flicker noise [40],[41]. First, shot noise is generated when a current flows across a potential barrier, the random fluctuation of the current above and below its average value results in shot noise. This occurs in vacuum tubes and in semiconductor devices. In semiconductors, it is due to the random diffusion of holes and electrons through a p-n junction and to the random generation and recombination of hole-electron pairs. Shot noise is generally modeled with the device as a parallel noise current source, and the Norton equivalent noise current source is given by

$$I_{sh} = \sqrt{2qI\Delta f} \tag{5.1}$$

Second, thermal noise is generated when thermal energy causes free electrons to move randomly in a resistive material, and the equivalent noise current source is given by

$$I_t = \sqrt{4kT\gamma g_m \Delta f} \tag{5.2}$$

$$It = \sqrt{\frac{4kT\Delta f}{R}} \tag{5.3}$$

Equation 5.2-5.3 represents the thermal noise for MOSFETs and resistor, respectively, where k is Boltzmann's constant, T is the absolute temperature, R is the resistance, and g_m is the trans- conductance. The last noise source, flicker noise, is caused by the imperfect contact between two conducting materials when the conductivity is fluctuating in the presence of DC current, or, in the case of MOSFET, the drain bias

current. This noise source is also modeled as a noise current source in parallel with the device and given by

$$I_f = \sqrt{\frac{K_f I^m \Delta f}{f^n}} \tag{5.4}$$

where 1< m <3.

5.3.3 Relationship between BER and SNR

To derive a relationship between SNR in an analog system and BER in binary optical communication system, two separate SNRs associated with the high and low levels of the signal need to be combined into a single quantity. The error probability of the two-level digital signal can be expressed in terms of probabilities of "1", P(1), and "0", P(0). Also, the conditional probabilities of error are P(1|0) and P(0|1). Hence the definition of the probability of error, P, as Gaussian noise that will cause the signal plus noise at the decision instant to cross the threshold level to the opposite side from the signal alone is given by equation 5.5

$$P = P(1|0)P(0) + P(0|1)P(1) \tag{5.5}$$

and illustrated in Figure 5.3

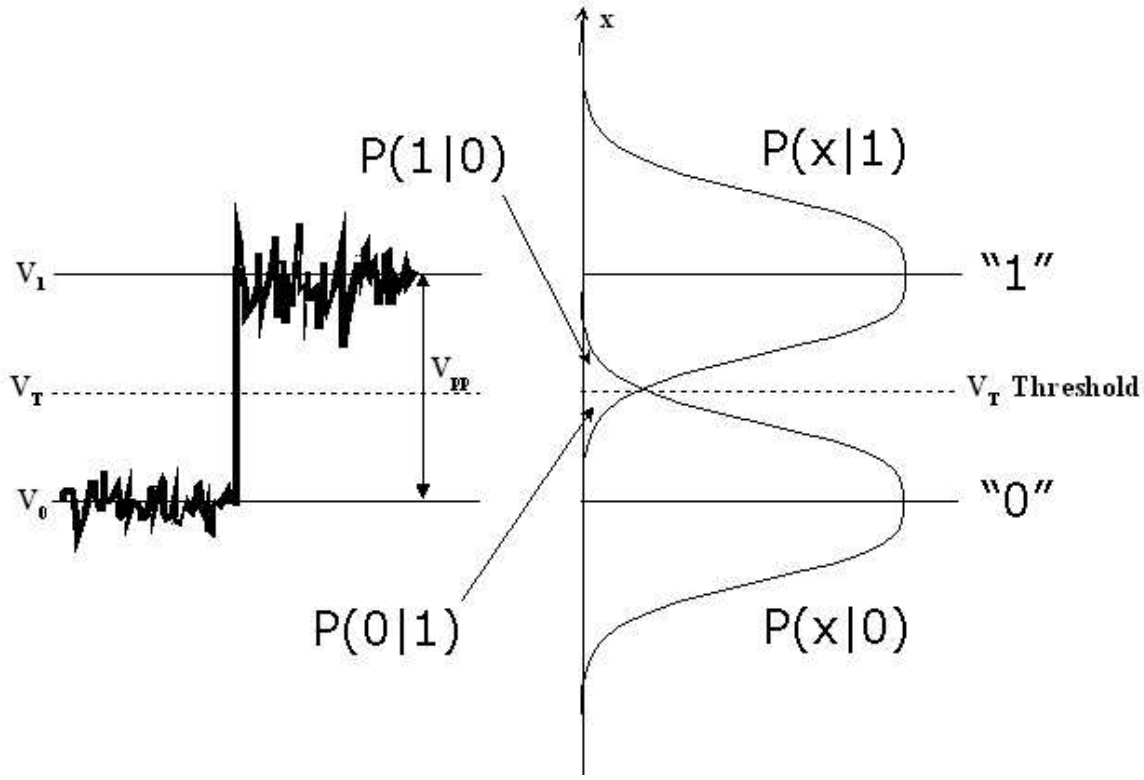


Figure 5.3: Probability of error of binary coded signal

Assuming the conditional probabilities are equal, and if ones and zeros are equally probable, the probabilities P(1) and P(0) are both 0.5, and the above equation becomes

$P = 0.5[P(1|0) + P(0|1)]$,

$= P(1|0)$

$= p(x)dx$ (5.6)

by symmetry. The definite integral will have a lower limit equal to half the peak-to-peak value, Vpp/2, and an upper limit of infinity. Because the distribution is Gaussian, the right-hand side of the equation can be expressed as

$$\begin{aligned} P(1|0) &= \frac{1}{\sigma\sqrt{2\pi}} \int_{V_{pp}/2}^{\infty} \exp\left(-\frac{x^2}{2\sigma^2}\right) \\ &= \frac{1}{2} erfc\left(\frac{V_{pp}}{2\sigma\sqrt{2}}\right) \end{aligned} \tag{5.7}$$

where *erfc* stands the complementary error function, defined as

$$erfc(x) = \frac{2}{\sqrt{\pi}} \int_{x}^{\infty} \exp(-y^2) dy \tag{5.8}$$

Hence the probability of error is given by

$$P = \frac{1}{2} erfc\left(\frac{Q}{\sqrt{2}}\right) \tag{5.9}$$

where

$$Q = \frac{V_{pp}}{2\sigma} = \frac{V_1 - V_0}{\sigma} \tag{5.10}$$

The probability of error in the binary coded digital system is commonly called the BER. The parameter Q [12] represents *SNR*s of the high and low levels of the digital signal, and is the ratio of the peak-to-peak signal to the RMS value of associated noises. The maximum input noise level to acquire a certain level of BER can be derived mathematically by the above equation, and their relation in terms of Q is

$$Q^2 = \frac{I_{signal}^2}{I_{noise}^2} \tag{5.11}$$

where Q is a power SNR, I_{signal} is the current signal converted by a PD, and I_{noise} is the total input-referred noise power. Therefore, the I_{noise} requirement can be obtained because the I_{signal} is a known value and can be obtained from the optical input power incident to the PD, and the sensitivity requirement of the receiver amplifier for a certain BER can be estimated from the following relationship given by Equation 5.12.

$$BER \approx \frac{1}{Q\sqrt{2\pi}} \cdot \exp\left(-\frac{Q}{2}\right) \tag{5.12}$$

The following table shows the relationship between BER, Q and SNR

Table 5.2: Relationship between BER and Q Value

BER	Q	SNR
10^{-6}	4.75	13.53
10^{-7}	5.20	14.32
10^{-8}	5.61	14.98
10^{-9}	5.99	15.55
10^{-10}	6.36	16.07
10^{-11}	6.71	16.53
10^{-12}	7.03	16.94

5.3.4 Receiver sensitivity

In optical communication system, receiver sensitivity is a figure of merit of the receiver. It is a measure of how weak an input signal can get with an acceptable BER performance. For SONET standard, BER of less than 10^{-9} is specified. The photo-detector and the transimpedance amplifier are the portion of receiver contributing most noise in the system. The sensitivity of the receiver is usually measured as average power (P_{AVG}) in dBm or as optical modulation amplitude (OMA) in W_{pp}. The sensitivity is the minimum OMA or P_{AVG} at which the maximum BER can be maintained.

The OMA of the receiver is given by,

$$OMA_{MIN} = \frac{i_n SNR}{\rho} \tag{5.13}$$

Where i_n, is the RMS input referred noise and it directly depends on the photodiode capacitance and ρ is the responsivity of the photo-detector expressed in amp/watts. The average optical power is given by

$$P_{AVG} = \frac{OMA(r_e + 1)}{2(r_e - 1)} \tag{5.14}$$

Where r_e is the extinction ratio of logic-one power level (P1) relative to logic-zero power level (P0). It is expressed in dB. It is given by

$$r_e = 10\log\left(\frac{P_1}{P_0}\right)(dB) \tag{5.15}$$

The Signal-to noise ratio is expressed in terms of peak-to-peak signal to that of RMS value of input-referred noise.

$$SNR = \frac{Signal_{(pp)}}{Noise_{(RMS)}} \tag{5.16}$$

The overall sensitivity of the receiver is given by

$$Sensitivity = 10Log\left(\frac{i_n SNR(r_e + 1)}{\rho(r_e - 1)2}1000\right)dBm \tag{5.17}$$

The designed differential TIA offers receiver sensitivity of -14.4dBm with an input magnitude of 50μA, responsivity and extinction ratio of 0.85A/W and 10dB respectively.

5.4 Post voltage amplifier

A large-value feedback resistor may be preferred for good sensitivity, but the integration of the signal because of the input capacitance will follow, because in practice the open-loop gain cannot be increased indefinitely. Cascading amplifiers within the feedback loop may also lead to additional phase-shift, which likely causes ringing or instability problems [43]. Hence the voltage swing produced by preamplifiers at the minimum light intensity is usually less than adequate to be further processed in the following stages. These issues are more prominent in CMOS technologies in which the supply voltage and trans-conductance are typically limited [44], [45].

The noise contribution from the later stage is negligible compared with that from the first transimpedance stage, and differential voltage-mode amplifiers are good candidates for post amplification. The fact that, unlike the first stage, the post amplifier and the output buffer can receive balanced input signals is another advantage, because ideal tail current sources used in differential pairs do not exist in practice. Hence the primary reason for post amplification and buffering is to boost the output signal swing of the TIA to an acceptable level so that it can be detected by an LA without adding a considerable amount of noise.

A cascade of *n* identical gain cells is one of the widely used methods to build a high-speed amplifier especially when one cannot achieve an enough gain from a single stage amplifier. The overall gain of the *n*-staged amplifier is given by

$$A_{total} = A^{n}_{cell} \tag{5.18}$$

where the overall bandwidth is

$$BW_{total} = BW^{n}_{cell}\sqrt{2^{\frac{1}{n}} - 1} \tag{5.19}$$

5.4.1 Post amplifier design

The goal of a designed post-amplifier composed of cascaded differential amplifiers is to boost a signal swing that could not be obtained sufficiently in the transimpedance stage. A three-stage cascaded amplifier has been chosen to minimize the noise, and the transistor level detail is shown in Figure 5.4. The biasing at the input of one stage is provided by the previous stage because AC coupling between stages cannot be used because of the wide-band nature of the application.

The difficulties lie in the fact that these gain cells also function as a pre-driver of the following 50Ω buffer that has wide transistors. Hence large transconductance with a small load (gain-bandwidth trade-off) was needed because the opposite combination may increase the time constant at the output node. Either a large tail current or a wide input transistor can be used to ensure sufficient transconductance. The designed amplifier produces an overall gain of around 66dBΩ.

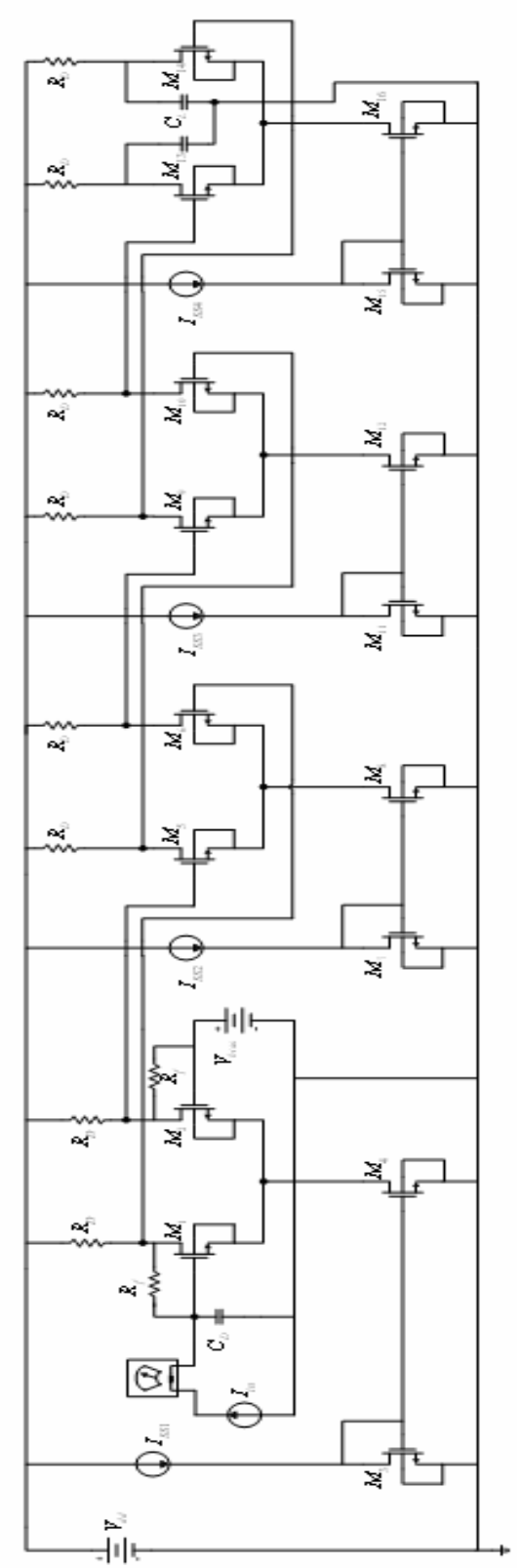


Figure 5.4: TIA cascaded with post amplifier

5.5 Output buffer

To achieve a high voltage gain with limited supply voltage, the load impedance must be as large as possible. If such a stage is to drive a low impedance load, then a buffer must be placed after the amplifier so as to drive the load with negligible loss of the signal level. To drive 50Ω output termination and capable of producing at least 200mV output swing, big output driver is required. A simple source follower circuit which has almost unity gain and high input impedance is designed as a buffer stage. The output buffer has bigger transistor size to handle the bigger current which will flow back and forth towards the pad.

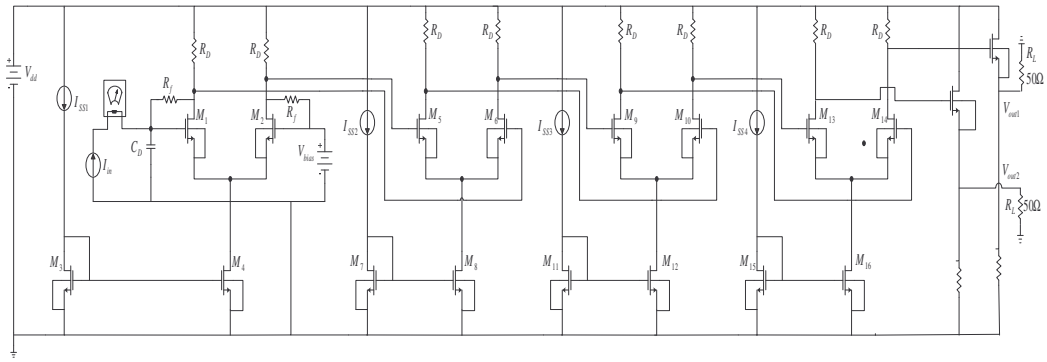


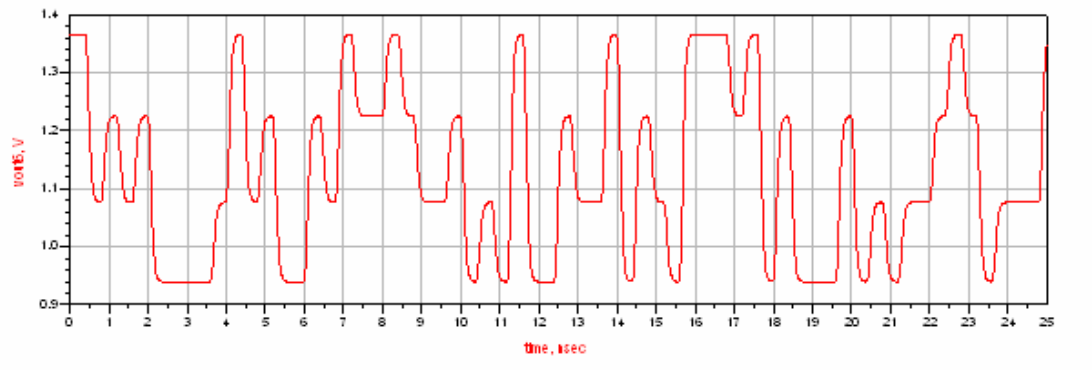
Figure 5.5: The source follower used as output buffer driving the 50Ω output termination.

5.6 Simulation

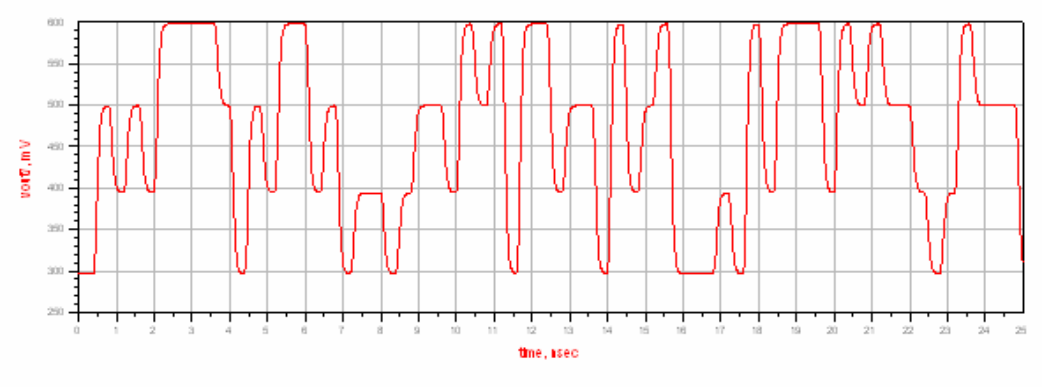
5.6.1 Transient Simulation of the overall amplifier with 3 different PAM signaling

The ADS simulation on the overall amplifier structure has been performed using TSMC 0.18um technology. The figure below shows the transient simulation results of 2.5Gbps signal with 4-PAM, 8-level PAM and 16-level PAM signal. The transistor sizes are optimized to obtain the desired result.

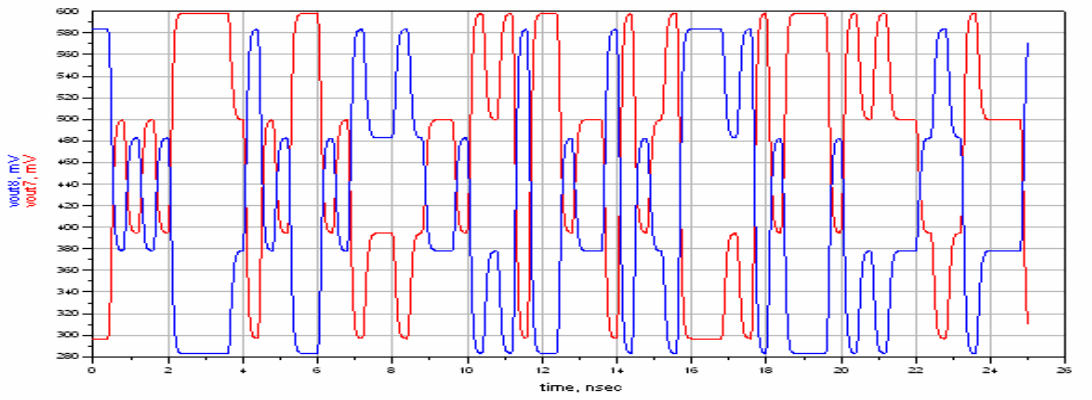
The transient response of overall amplifier including the output buffer is simulated and shown in the figure below. The overall output amplitude of around 300mV is obtained with the 50 Ω load.



(a)

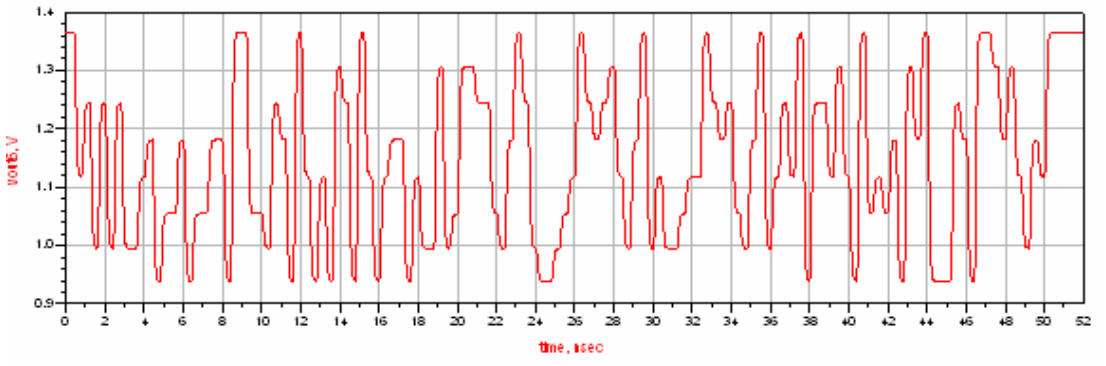


(b)

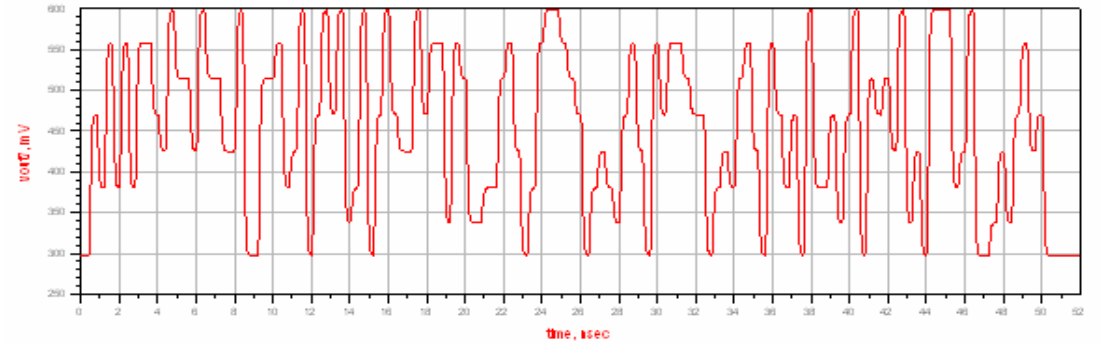


(c)

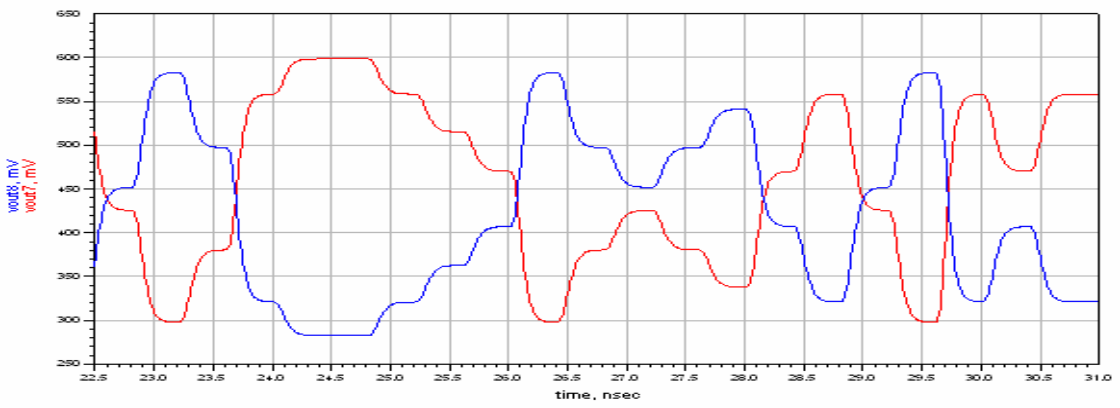
Figure 5.6: Transient response of 4 Level PAM signal at the end of post amp (a) Output at post amp. (b) Inverted output at post amp. (c)The overall amplitude level after including the load impedance of 50 Ω



(a)

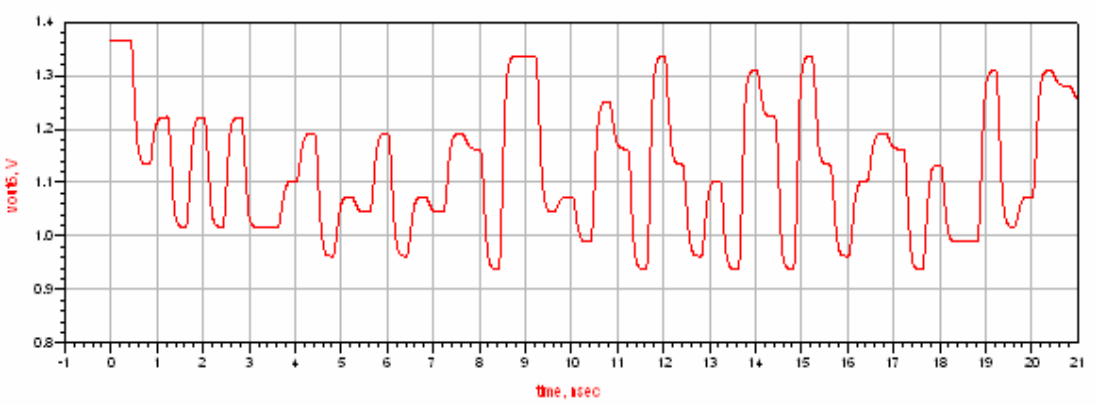


(b)

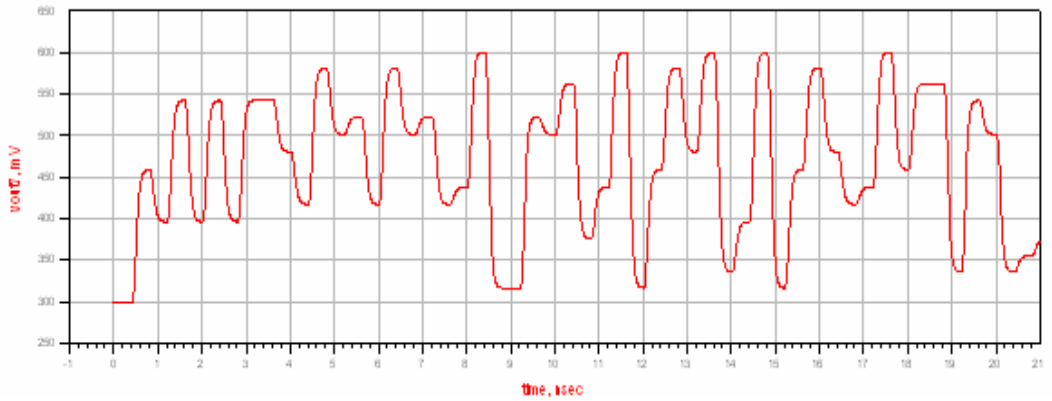


(c)

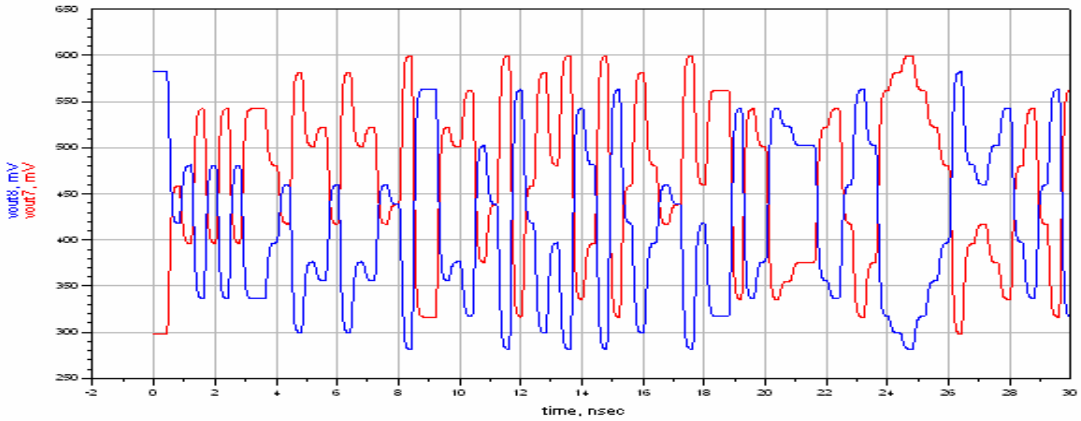
Figure 5.7: Transient response of 8 Level PAM signal at the end of post amp (a) Output at post amp. (b) Inverted output at post amp. (c)The overall amplitude level after including the load impedance of 50 Ω



(a)



(b)



(c)

Figure 5.8: Transient response of 16 Level PAM signal at the end of post amp (a) Output at post amp. (b) Inverted output at post amp. (c)The overall amplitude level after including the load impedance of 50 Ω

Eye diagram analysis all the 3 different PAM signaling operating at a speed of 2.5Gbps is also performed. The results are shown below. The results are taken at the output of the buffer stage. The figure 5.9-5.11 illustrates that the eye opening is wider for all 3 types of PAM signaling. Furthermore, no effect of non-linearity is observed from the simulation result. Thus the designed differential optical receiver front-end can be used for OC-48 standard.

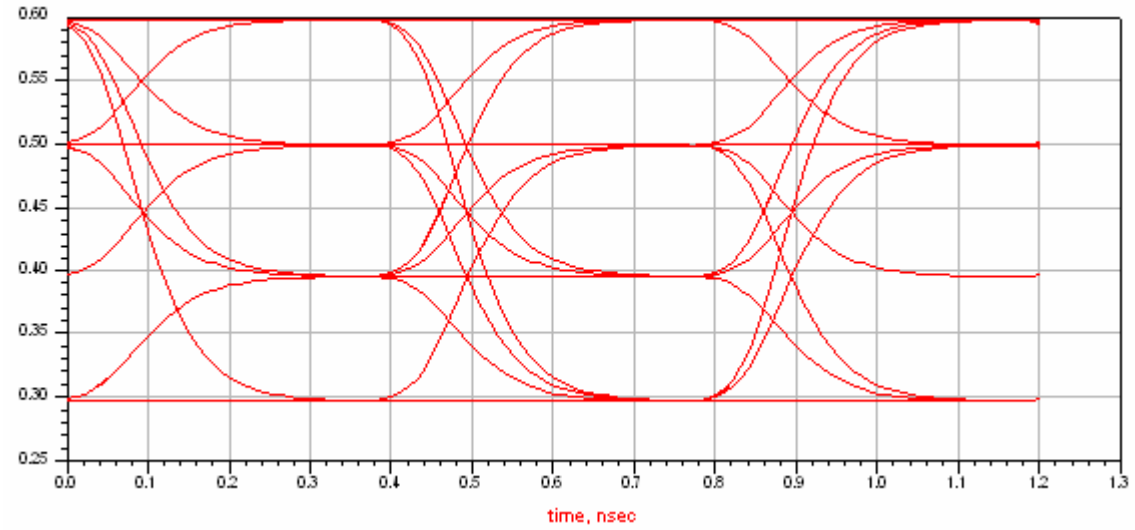


Figure 5.9: Eye diagram measurement at the output buffer stage for 4-level PAM

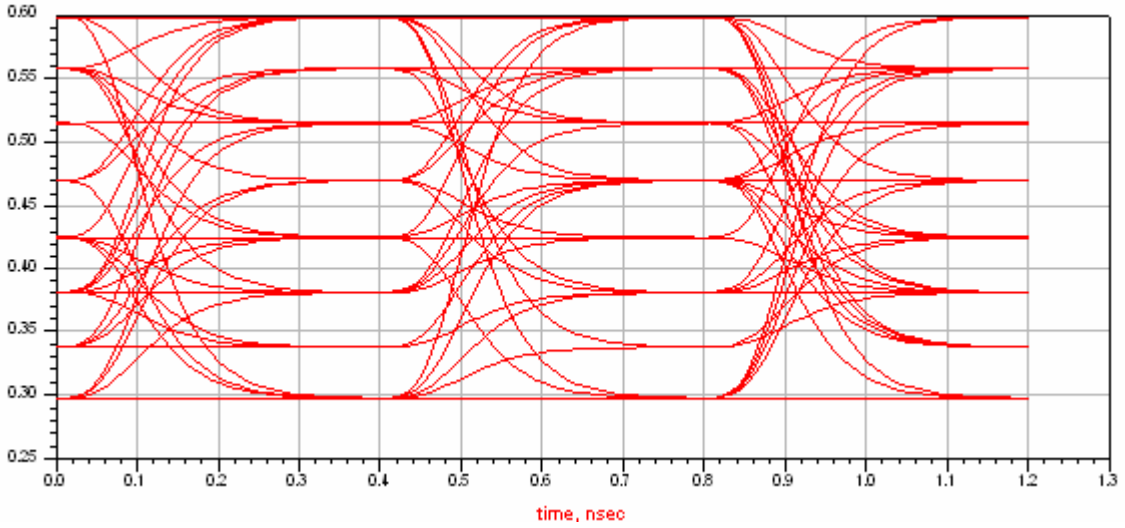


Figure 5.10: Eye diagram measurement at the output buffer stage for 8-level PAM

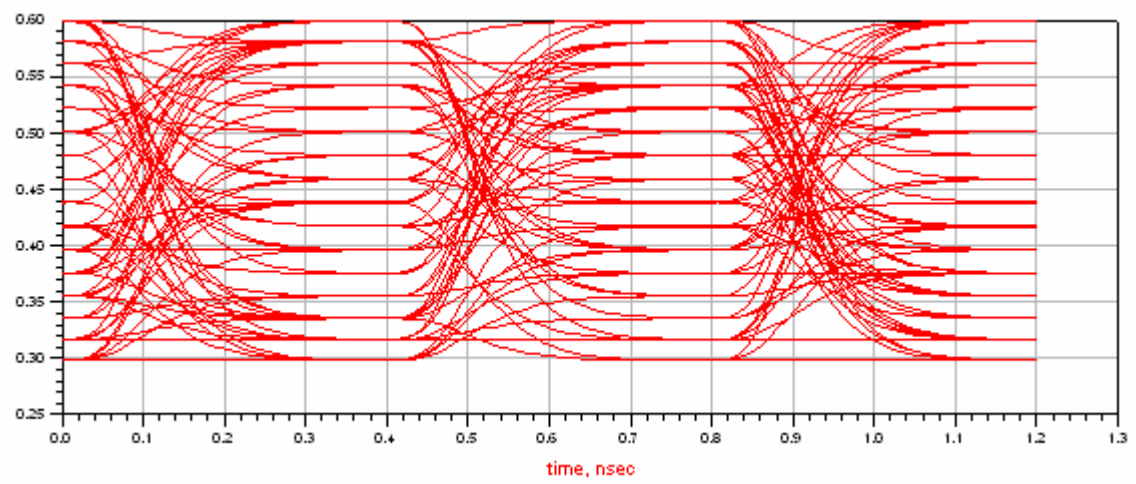


Figure 5.11: Eye diagram measurement at the output buffer stage for 16-level PAM

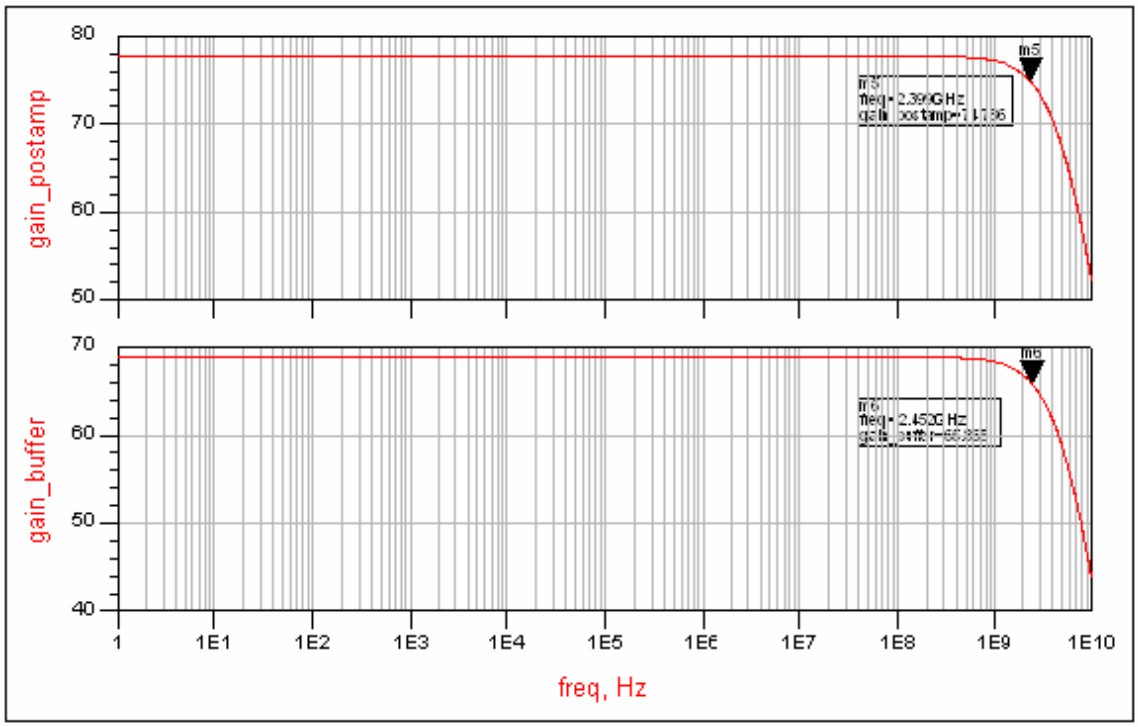
5.6.2 AC analysis and noise simulation

The following figure illustrates the ac analysis of the overall amplifier including the output buffer driving the 50 Ω termination loads. As expected the overall transimpedance gain is dropped 66dB in order to drive the wide transistors at the output stage.

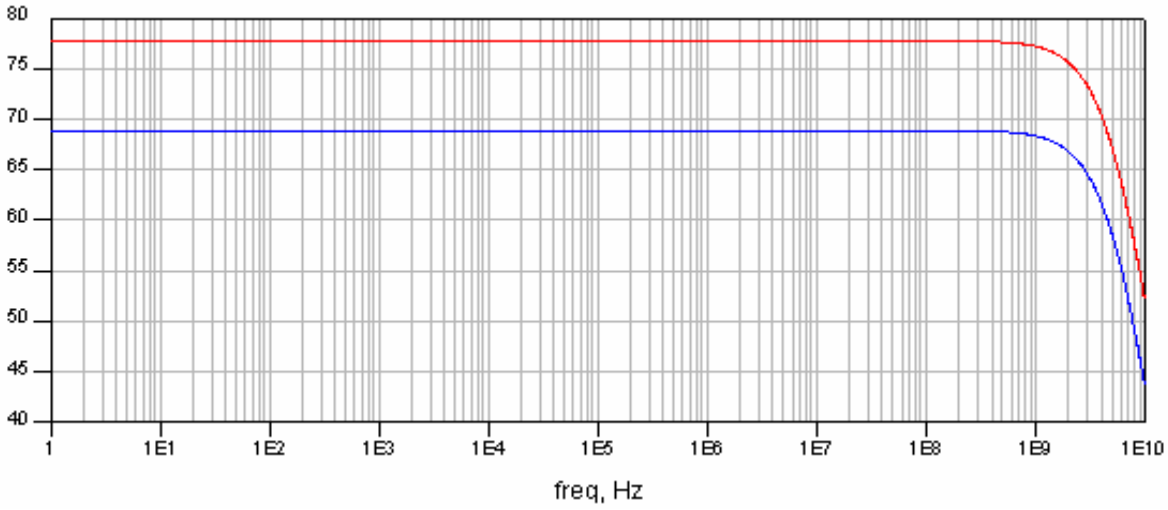
The low frequency gain of the front-end differential receiver is around 1995 Ω with the 3dB bandwidth of 2.43GHz. The following table lists the gain and bandwidth at the each stage with photo-detector capacitance of 0.1pF.

Table 5.3: Comparison of Performance parameters at each stage of the receiver

Parameters	TIA		PostAmp1		PostAmp2		PostAmp3	
Output Swing (mV)	49		120		292		853	
	22	27	60	60	145	146	426	427
Transimpedance Gain (kΩ)	0.35		0.86		2.03		5.5	
3-dB Bandwidth (GHz)	4.1		3.3		2.6		2.4	
Power Consumption = 148 mW (including the output stage driving 50 Ω load)								



(a)



(b)

Figure 5.12: (a) The gain plot of the final post amplifier and of the output buffer stage (b) Plot showing the drop of gain in order to drive resistive load of connectors

The noise analysis is performed using HSPICE simulation tool. The input referred noise current, which is the major important performance parameter affecting the receiver sensitivity is calculated based on the equation given in Chapter 2. The sensitivity of the receiver with 100 μA_{pp} is calculated to be around -11.3 dBm.

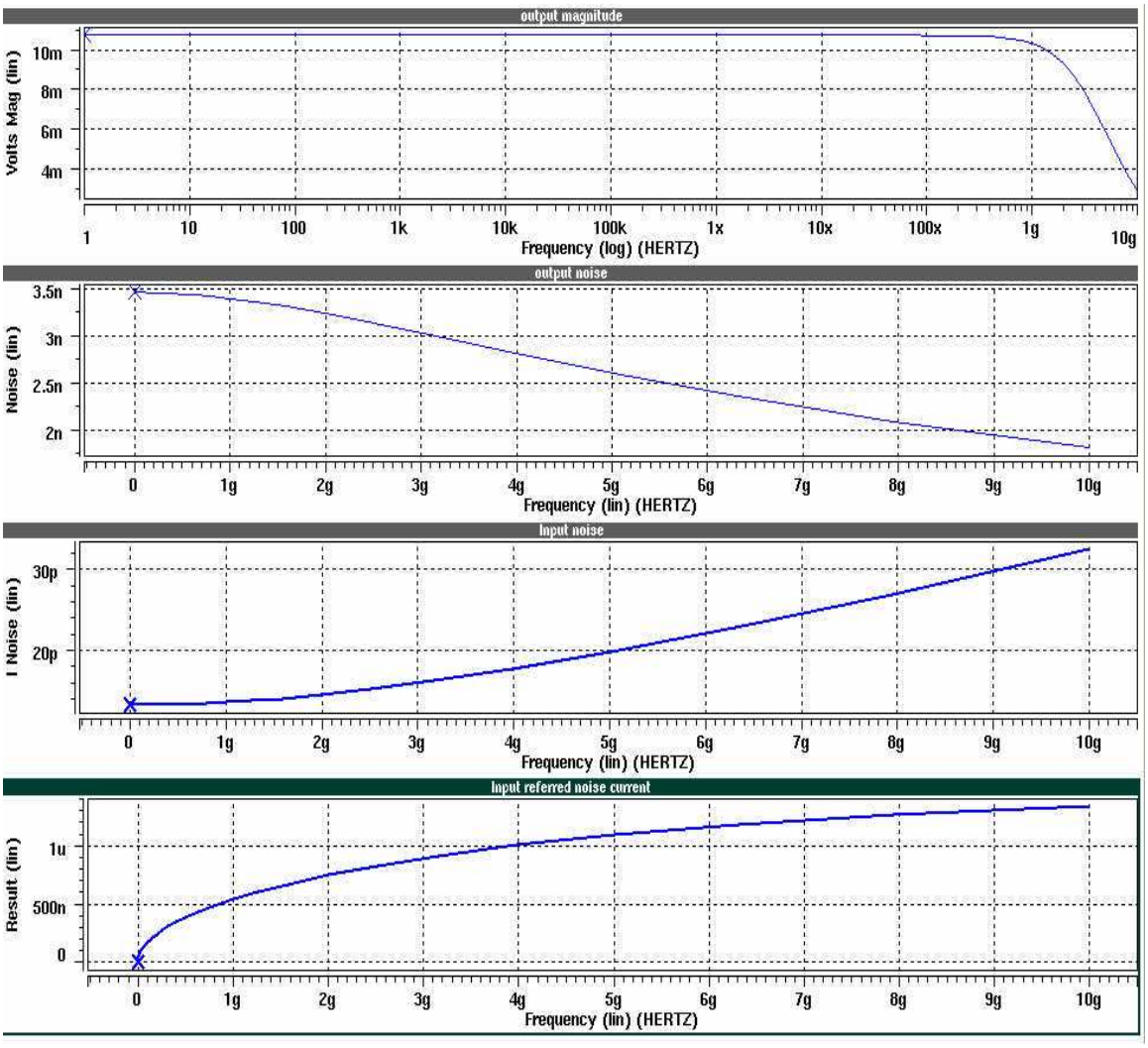


Figure 5.13: Noise analysis with 0.1pf detector capacitance.

The input referred noise current is found to be around 1.4$\mu A_{rms.}$ With a input current of magnitude 50μA_{pp}, the sensitivity of the receiver is found to be -14.4dBm.

5.6.3 Effect of packaging parasitics

Packaging inductance can play a major role in degrading the quality of the amplifier output signal, thus successful optical front-end design demands careful attention to the sources and effects of parasitic inductance due to bond wires, die pads, etc. As discussed earlier in this chapter, about the advantage of using differential signaling for substrate noise, a realistic model including the parasitics caused by the package, bonding wire and PCB board are included. The model shown in chapter 3 are included in the V_{dd} and V_{ss} power supply rails as shown in figure below and the simulation is carried out to observe the effects of those parasitics. The model values are estimated approximately or provided by the manufacturing company.

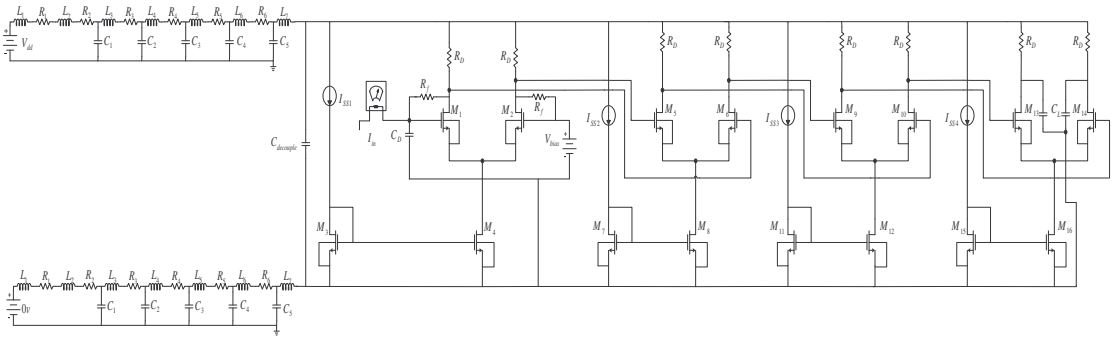


Figure 5.14: Inclusion of packaging parasitics between the power supply rails

Due to differential signaling, the noise production problem associated with differential designs are lesser compared to the single-ended design, the power supply current of the amplifier is simulated in ADS. The following figure shows that; there is around 15 to 20 micro amp change in the supply current in less than 1ns compared to 1milliamp change in supply current. This lower current produces lesser ripples compared to the single ended design.

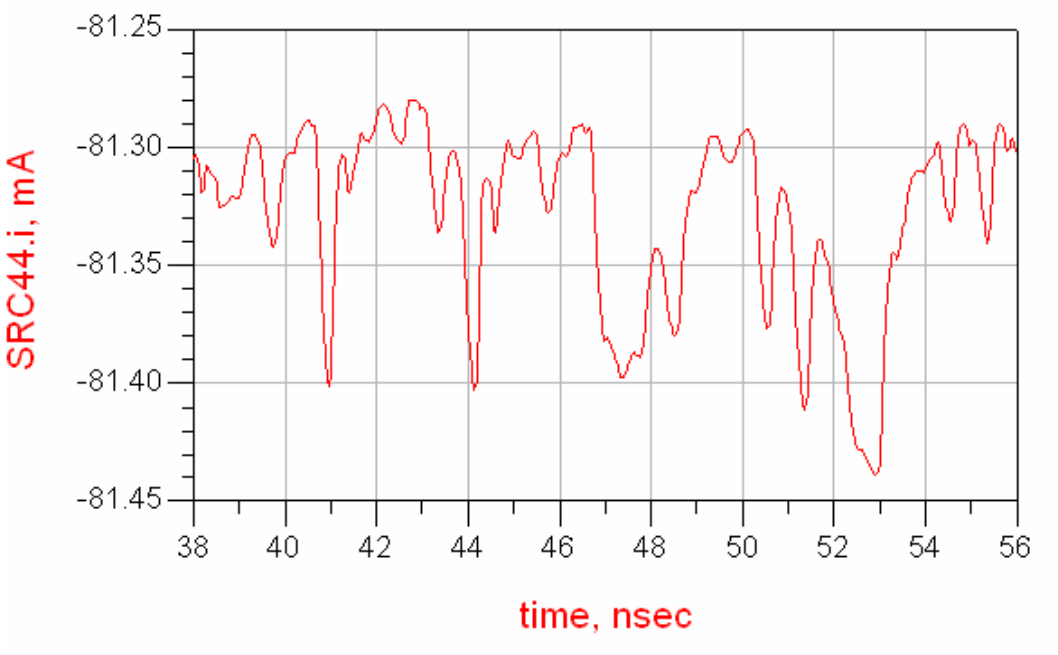


Figure 5.15: Supply current variation in 16-level PAM due to power supply parasitics

The effect of parasitics on the transient response of amplifier is illustrated in the Figure 5.16. The top trace shows the 16-level PAM signal current with peak-to-peak value of 100μA and their corresponding transient response of the output magnitude at the end of buffer is shown.

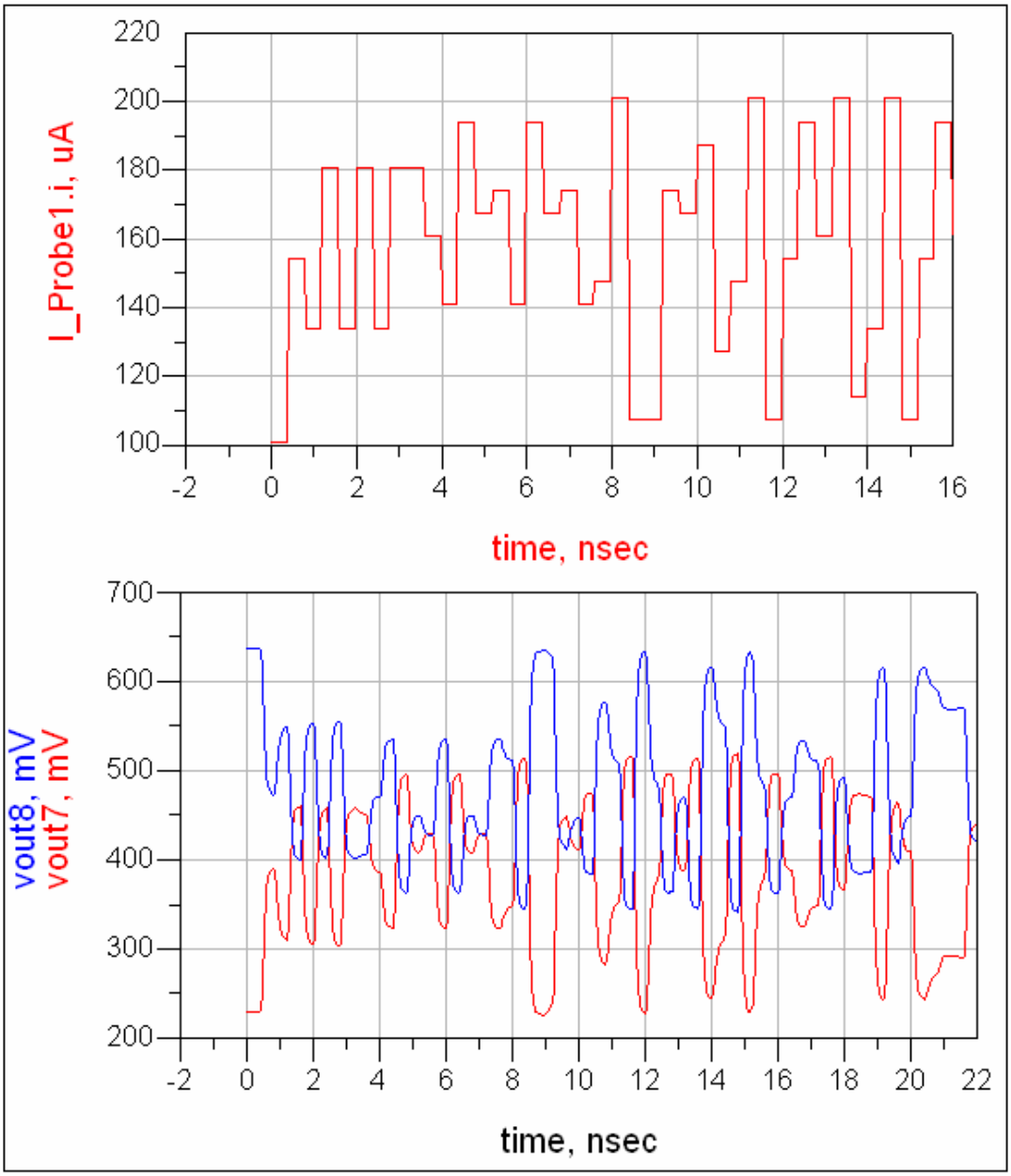


Figure 5.16: Top trace: 16-Level PAM signaling input current of $100\mu A_{pp.}$
Bottom trace: Effect of packaging parasitics on the differential output signal

The eye diagram analysis shown in the following figures shows better visualization of the power supply parasitics. The results are included for 4-PAM, 8-PAM and 16-PAM signals respectively.

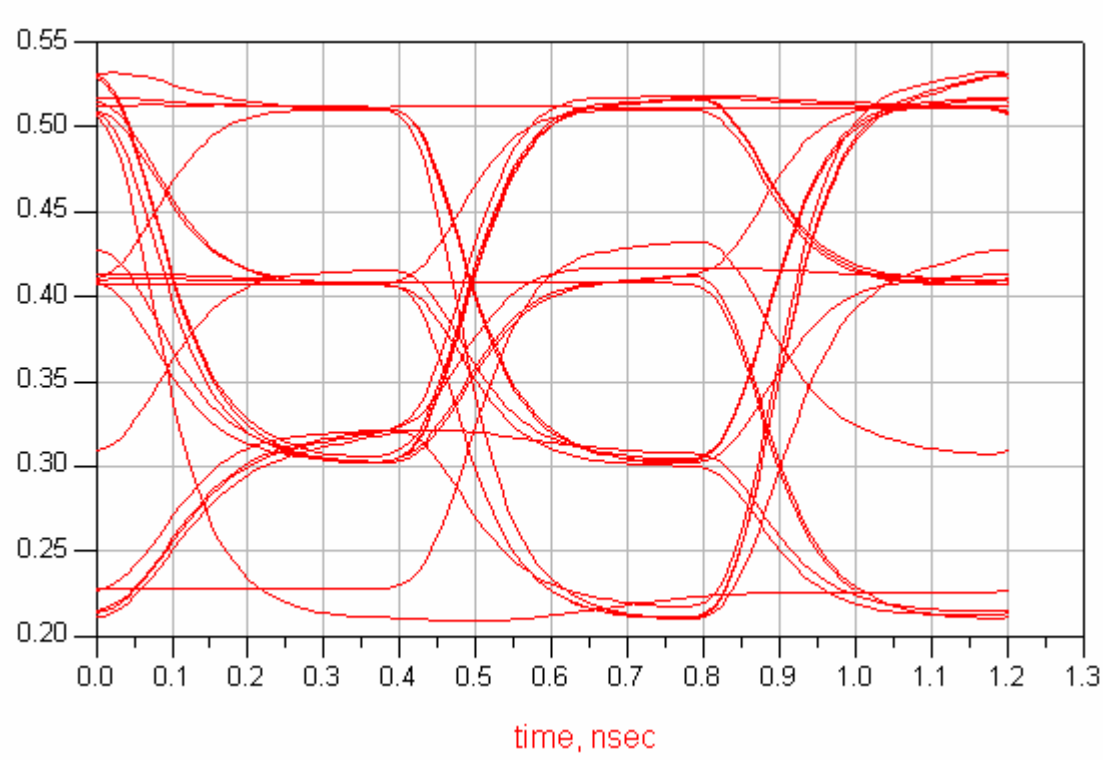


Figure 5.17: Eye diagram analysis of 2.5Gbps 4-PAM signal with packaging parasitics.

It is observed that, the eye opening of 4 PAM signals are shows acceptable performance. However there is some signal degradation seen in each level. In the case of 8 level and 16 level PAM signals, the packaging parasitics slows down the speed of overall amplifier and there by yielding higher ISI and eye closure. The result is worsen especially for the 16 level signals with their smaller magnitude of each level and there by corrupting the overall data transmission due to false detection at the optical receiver.

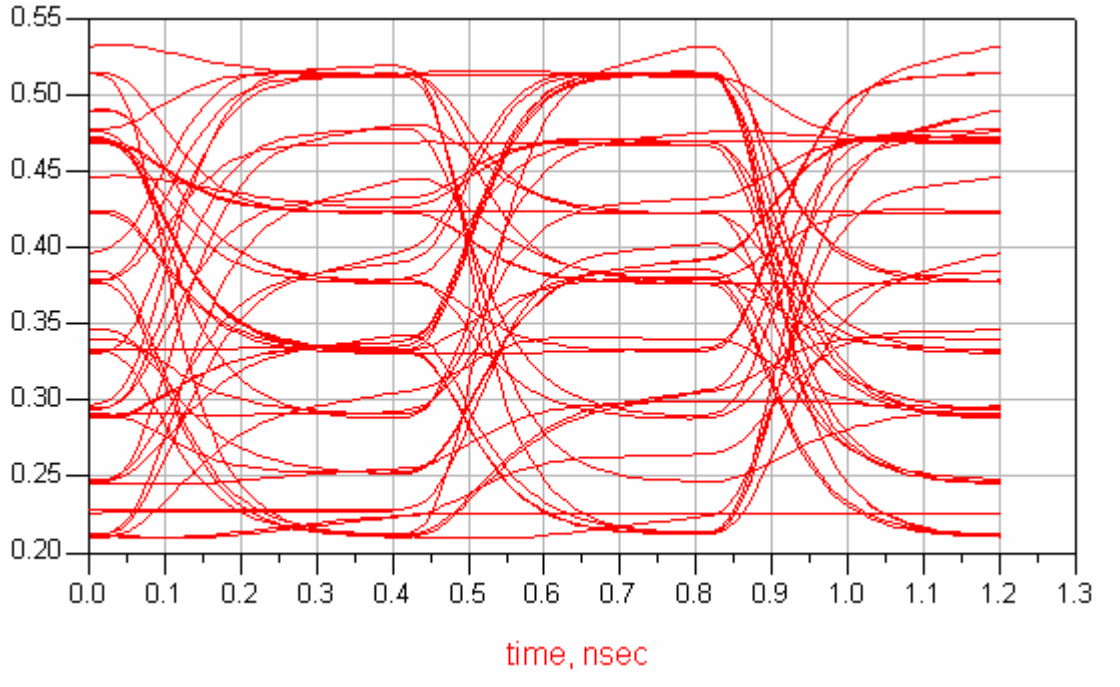


Figure 5.18: Eye diagram analysis of 2.5Gbps 8-PAM signal with packaging parasitics

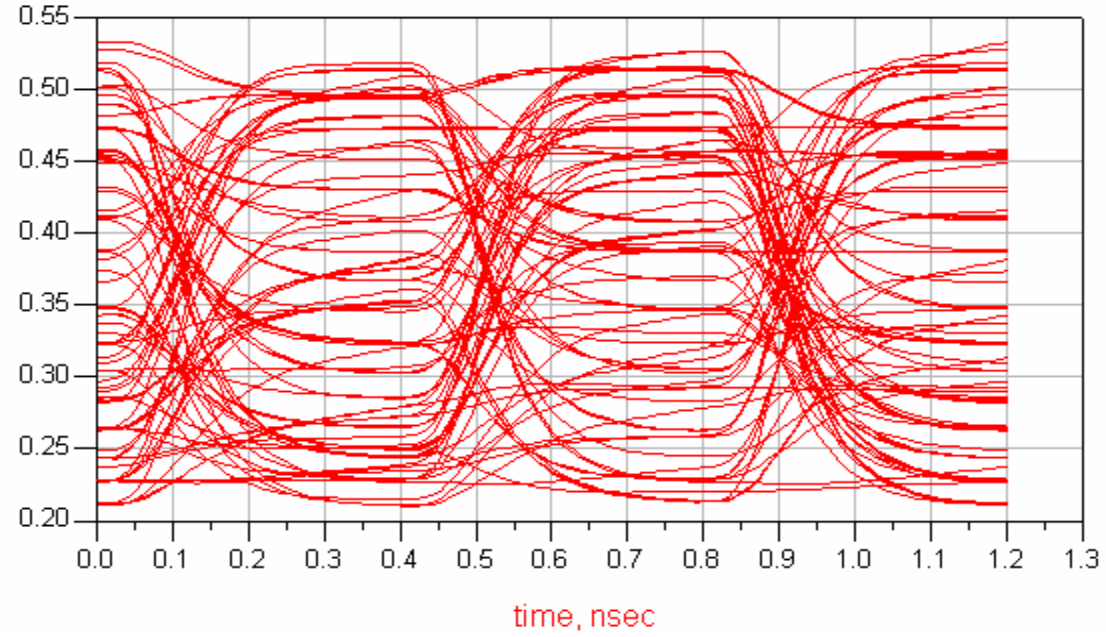


Figure 5.19: Eye diagram analysis of 2.5Gbps 16-PAM signal with packaging parasitics

A simple, yet effective way to suppress the finite packaging parasitic effect is to place decoupling capacitors between the power supply lines and the ground. In general, the more decoupling capacitors the better the power is regulated by providing the circuit enough charge until the switching noise settles down. However, because of the area constraint in the physical layout in practice, the optimum size and placement of those capacitors must be calculated. Hence a power supply parasitics model including package bond wires, PCB lines, and other biasing wires needs to be taken into consideration in the design phase. Considering the area of large decoupling capacitor, here a small decoupling capacitor of 4nH is connected between the power supply rails.

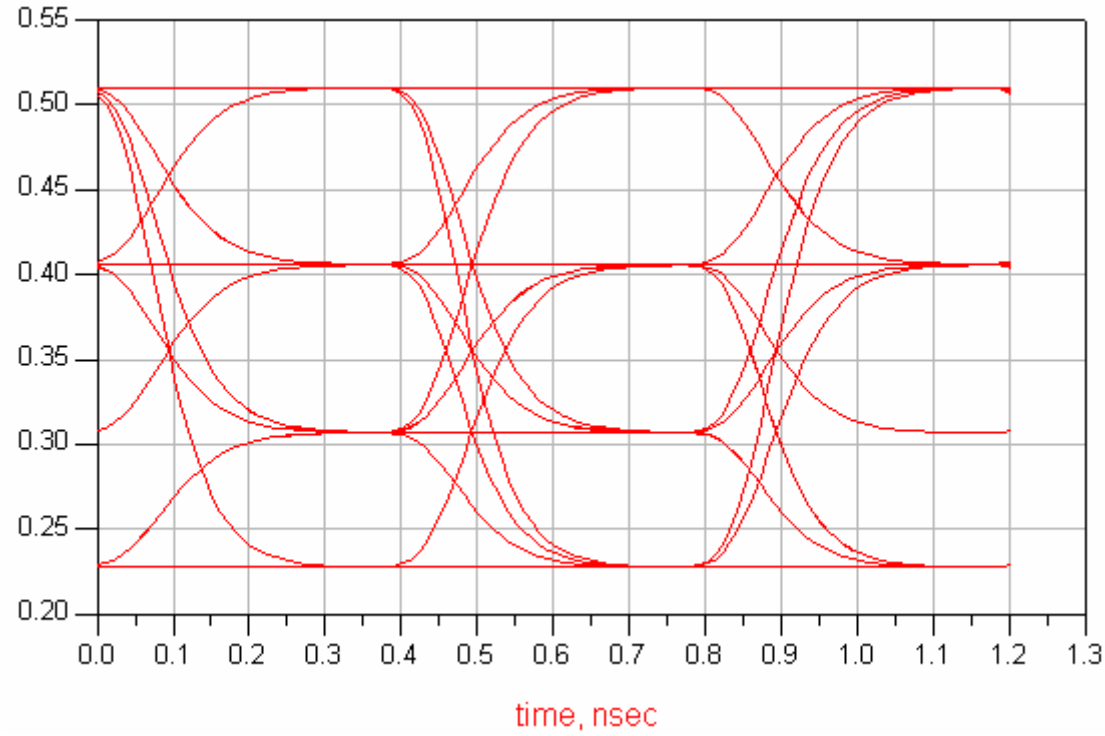


Figure 5.20: Effect of including decoupling capacitor of 4nH to lessen the power supply parasitics in 4-PAM signal.

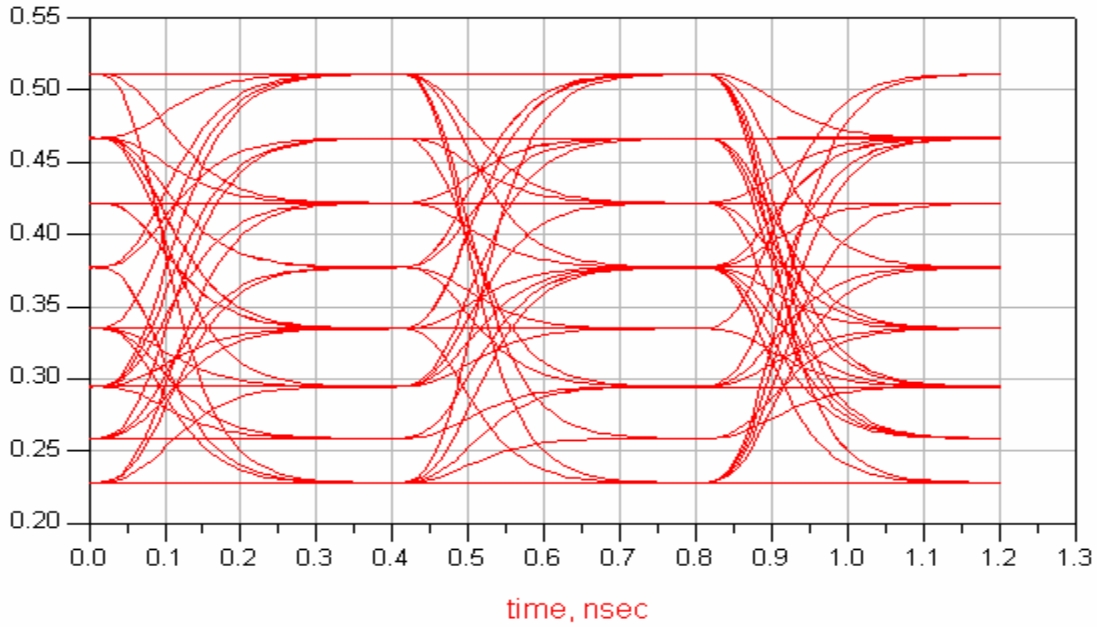


Figure 5.21: Effect of including decoupling capacitor of 4nH to lessen the power supply parasitics in 8-PAM signal.

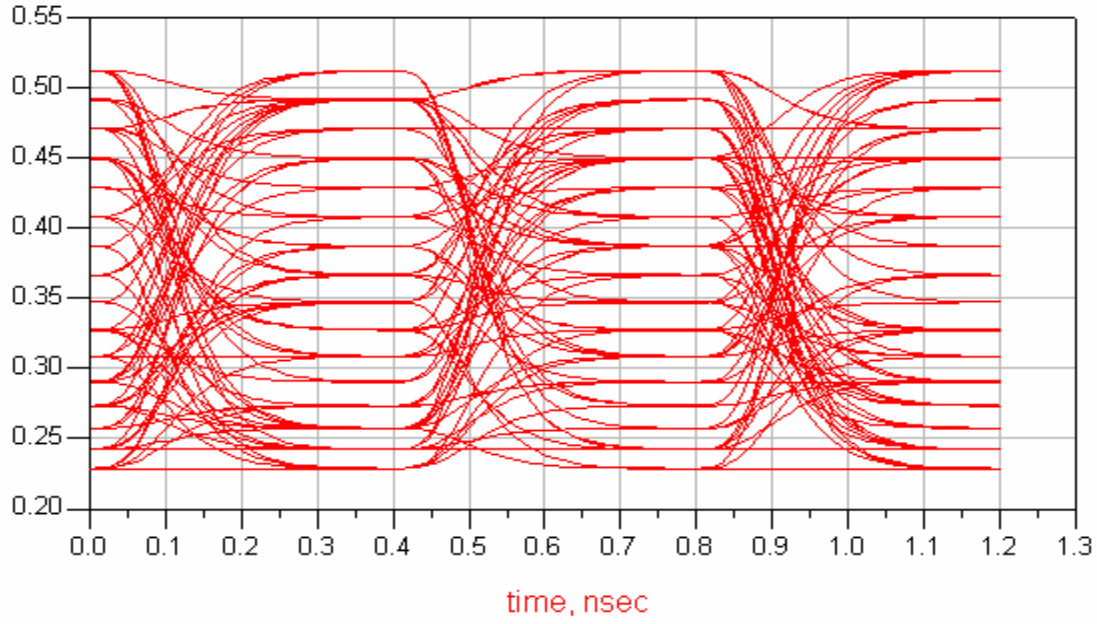


Figure 5.22: Effect of including decoupling capacitor of 4nH to lessen the power supply parasitics in 16-PAM signal.

Thus the analysis shows that, using decoupling capacitor, the effect of packaging parasitics can completely eliminated which is observed in the eye diagram analysis. The eye opening of all the levels is wider and level is seen clearly without any non-linearity.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

A differential transimpedance amplifier suitable for pulse amplitude modulation signaling scheme (PAM) was designed by using a front stage feedback loop, multi-stage post amplifier to boost the weak signal produced by the TIA. The designed TIA works well with 3 different PAM schemes; 4 levels, 8 levels and 16 level signal. The designed transimpedance amplifier, preceded by a photo-detector usually forms the front end of the optical receiver. The design is carried out using TSMC 0.18μm CMOS technology. ADS and HSPICE circuit simulator has been used for the design and simulation. The multilevel signaling scheme results in increase of data throughput without sacrificing serial data rate. Transmission of 16 level signals provides a data throughput of 10Gbps at a data rate of 2.5Gbps.

In chapter 2, theories and background supporting the operation of optical receiver are included. The performance measure of receiver such as eye diagram and BER requirement of SONET OC-48 standard are highlighted. The importance of using a transimpedance amplifier at the front-end of receiver and their performance parameters are also discussed prior to the actual design. Use of multilevel signaling scheme for the optical communication lessens the impact of bandwidth limitation (ISI), by reducing the width of the operating bandwidth required to half compared to the

binary signals. It also helps in the improvement of dispersion-limited fiber distance. The SNR penalty of the multilevel signaling is insignificant when compared to the targeted data rate, as the ISI increases even more as one tries to force more bandwidth through the channel.

In chapter 3, the power supply parasitics associated with packaging and bonding wire are modeled for the desired PCB dimension using the HSPICE net list extractor available in ADS. The parasitic model is included in the simulation of the circuits in order to obtain the realistic results observed in testing of chip, which are usually unnoticed in the circuit simulation.

In chapter 4, the performance optimization of different topology of front end optical receiver based on bandwidth, noise and gain is done and the transimpedance feedback amplifier structures has been recommended. The design of single-ended transimpedance amplifier topology optimized between their performance parameters such as input referred noise, transimpedance gain and bandwidth; with the given detector capacitance is discussed. The overall speed and the output voltage magnitude obtained at the end of three-stage cascaded post amplifiers, drops down due to the gain-bandwidth trade off at each stage. Inclusion of packaging parasitics for the multi-stage, single-ended design totally ruins the eye opening. The decoupling capacitor used to eliminate the power supply noise restores the eye opening at the cost of ringing effect. The ringing effect produces oscillation, which is highly undesired in the case of higher data rates. Thus it is recommended that multi-stage, single-ended transimpedance amplifier is unsought for the SONET OC-48 standard especially with PAM signaling.

In chapter 5, 4-stage differential, wide band transimpedance amplifier has been designed and simulated in ADS using TSMC 0.18μm CMOS technology to support the 2.5Gbps data rate essential for OC-48 standard. The overall design includes low-transimpedance gain front end TIA followed by 3 stage post amplifiers to boost the gain of the output magnitude suitable for further processing. The design is optimized for low input referred noise current and wide bandwidth with an acceptable overall transimpedance gain of 66dBΩ. An output buffer driving 50Ω termination load is also added to the design. Furthermore, the simulation results proves that use of decoupling capacitor can completely eliminate the power supply parasitics effect in the case of differential transimpedance amplifiers. The simulation results are included in the table below.

Table 6.1: Final simulation results obtained with PAM signaling scheme

Specification	Obtained simulation result	Standard
Speed	2.5Gbps	SONET OC-48 standard when driving 50Ω termination load.
Input current	$100\mu A_{pp}$	
Transimpedance Gain	66dB (~2KΩ)	
Output magnitude at each node	300 mV	
Receiver Sensitivity	-11.4 dBm	
Bandwidth	2.4 GHz	
Power Consumption	148mW	

6.2 Future Work

Our future work would be the goal of designing the complete multi-level signaling optical receiver system consisting of frond-end transimpedance amplifier followed by post amplifiers, comparators, and clock and data recovery circuit, detection circuitry. The CDR and detection circuitry is being researched and designed by the other members of our lab.

The next step would be moving on to the fabrication of entire chip and for the same, the layout of this circuitry will be performed near soon, and the final design would be sent to the fabrication company, MOSIS. When we receive the fabricated chip from MOSIS, the bare chip will be tested with a probe-station and other testing equipments.

The final goal is basically building a whole optical communication system chip for multilevel signaling scheme. This research is very challenging and proposes a lot of motivation to students because currently, the development of optical communication system in a single chip has been an interesting and challenging job for their extensive commercial applications.

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