THERMAL ENHANCEMENT OF STACKED DIES USING THERMAL VIAS

BY

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ABSTRACT

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Following Moore's law, the number of transistors on a die continues to rise and has recently exceeded a billion on high end processors. In light of the convergence of technology, power requirements is becoming a serious concern even on low density interconnect systems such as cellular phones and personal digital assistants. Also, in order to minimize foot prints, the recent trend in packaging is stacking. The stacking, however, creates challenges in cooling and especially if one is to include logic in the stack. The primary heat flow path for stacking is through the substrate and as the number of stacks increase, the cooling problem is amplified. Thermal vias are emerging as a viable technology for transferring heat and in effect creating a thermal short circuit from individual die to the substrate.

This thesis focuses on enhancement of thermal vias in different stacked die architectures for flash semiconductor products. Three different die stacking architectures were drawn as follows: spacer stacked, rotated stacked and pyramid stacked die.

Geometries were drawn by using Pro-Engineer Wildfire 2.0 as a Computer-Aided-Design tool and imported to Ansys Workbench 10.0, where meshed analysis was conducted. There are different number thermal vias every packaging. So, this thesis compares the junction temperature and heat flux as number of thermal vias.

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CHAPTER 1

INTRODUCTION

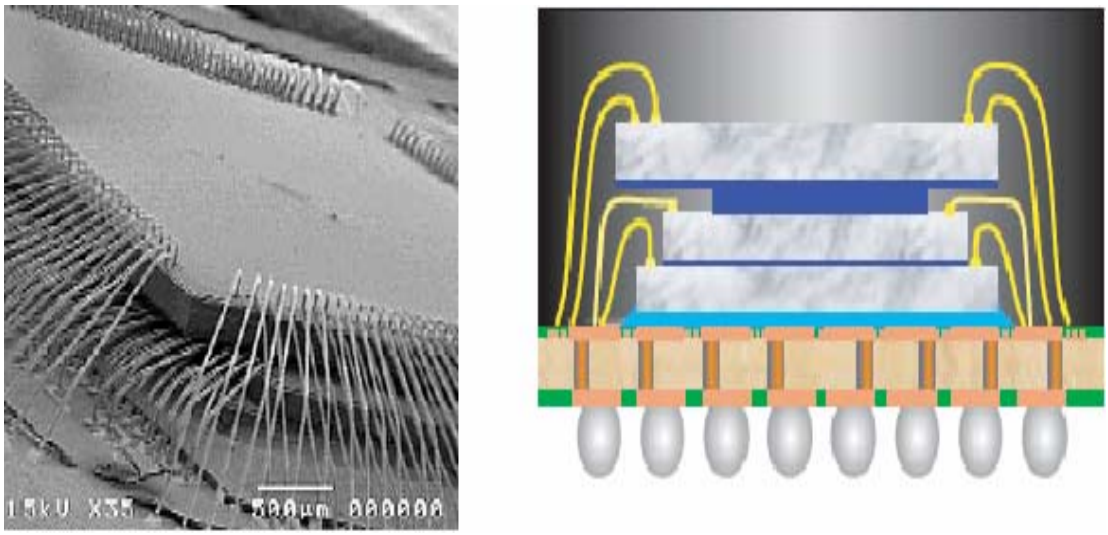
1.1 Package Technology

1.1.1 3D packaging technology

3-dimensional (3D) packaging technologies reclaim the third or more many dimension packaging to produce a volumetric packaging solution for higher creation and efficiency. Consumer organization demand in smaller, lighter, lighter products, so 3D packaging has grown critical to integrating the multi-media features. Consequently, this increasing functional structure requires higher memory capacity in more complex and efficient memory architectures. Figure 1.1 shows 3D packaging architectures. New product designs as digital handbook, cell phones, digital cameras, PDAs and music players request that these features be led in innovative technical form factors and architectures. Figure 1.2 shows example of using in 3D packaging technology. Now days, 3D packaging is undergoing new applications and high growth by delivering the highest level of silicon integration and area efficiency at the lowest cost, smallest size and best performance.

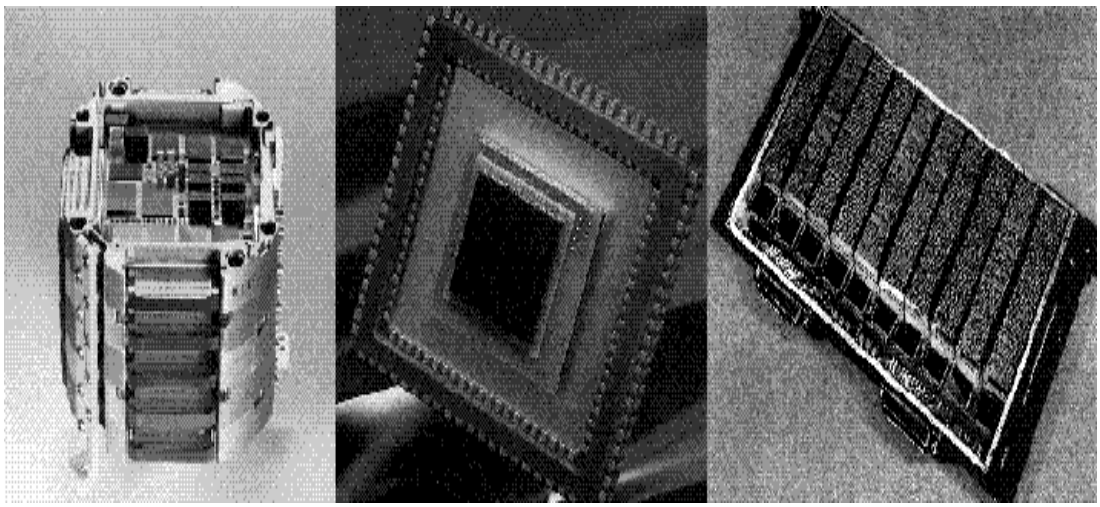
Since 1995, 3D packaging technology has been grown and provided high architectures at low cost. Because 3D packaging technology have the benefits such as reduced packaging costs, size and weight through more semiconductor functions, enables more geometry freedom to make innovative new form factors and variety

through stacked die packaging approach and enables higher electrical efficiency through shorter interconnect structure with stacked die.



(a) (b)

Figure 1.1 Example of 3D Packaging architecture
(a) Real picture; (b) Paint picture



(a) (b) (c)

Figure 1.2 Example of 3D Packaging Technology:
(a) The Aladdin parallel processor; (b) Irvine's 3D smart sensor; (c) TI 1.2 Gbit Solid state recorder [17]

1.1.2 Flip chip technology

A flip chip technology is one type of semiconductor apparatus devices, such as Integrated Circuit chips, which have no any wire bonds. In generally, there are two ways in the flip chip connection, one is solder balls, another is conductive adhesive on the chip pads intead of wire bonds. Flip chips will remain an underfill process that will cover the sides of the die, similar to the packaging process. Underfill is a specially made epoxy that encapsulates the area between the die and the carrier, surrounding the solder contact. It can take in the stress and reduce strain on the solder contact. Figure 1.3 shows wire bond BGA packaging and figure 1.4 shows flip chip BGA packaging. Both two figure shows difference of wire bond technology and flip chip technology. In a word, flip-chip packaging enables the creation of high-pin out, high-speed designs that are not achievable in a standard wire bond package. By using the flip chip technology, we can get a number of possible advantages. First, by using the entire surface of the die for establishing interconnect, package size can be reduced. Because flip chip packaging need not have spacer for wire, or in utilizing higher density substrate technology. [3] Second, the inductance of the signal path is extremely reduced, because of short distance of the interconnect inductance and capacitance. This is an important requisite high speed connection and switching devices. Third, using flip chip interconnect extremely decreases the noise of the core power, improving performance of the silicon, because power can be brought directly into the core of the die. The fourth, flip chip packaging can hood up exceedingly larger numbers of interconnects on the same die size. It can be possible to get high signal density. [17]

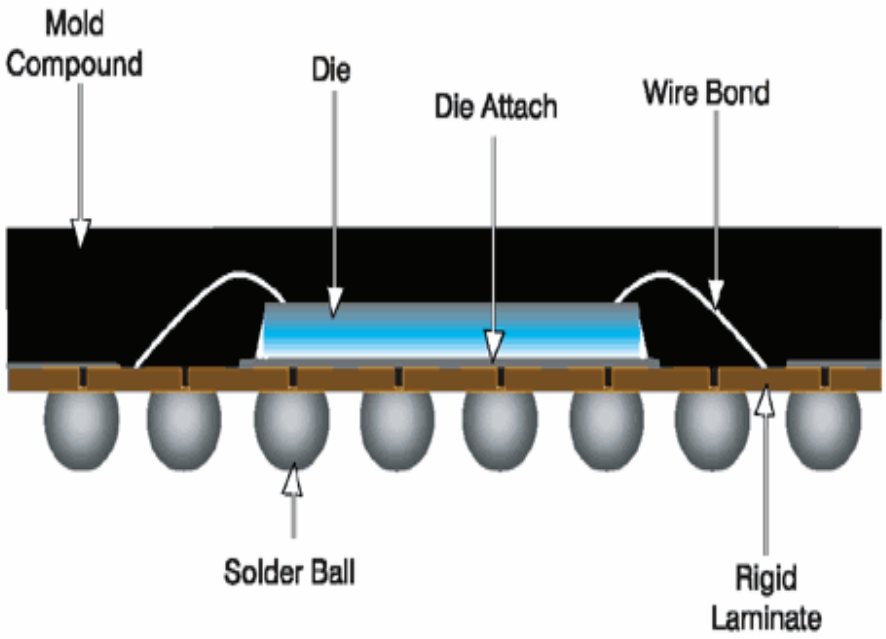


Figure 1.3 Amkor's Wire bond BGA section

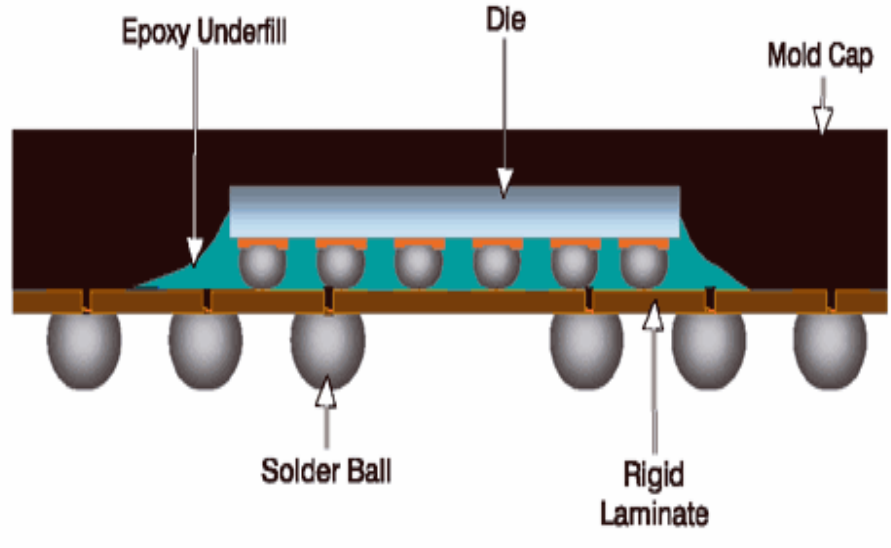


Figure 1.4 Amkor's Flip Chip BGA section

1.1.3 System in packaging technology

System in Package contains multiple die that are traditionally found on the system mother board. For instance, System in Package is a combination of one or more wire bonded or flip-chip dice with one or more passive components attached to a standard formal microelectronic package. Figure 1.5 shows general system in packaging. The important capacity of System in Packaging is the ability to bring together many package assembly and Inter Circuit. System in packaging and system on chip provide a key point that is smaller size with increased functionality. However, system in packaging gives faster time to market, lower research and development cost, more integration adaptability and lower product cost than system on chip. System in packaging includes implementations that need for low cost higher density substrates and high speed simulation tools for mechanical and electrical analysis. Figure 1.7 and figure 1.8 show System in packaging memory trends in SDRAM and FLASH. [16]

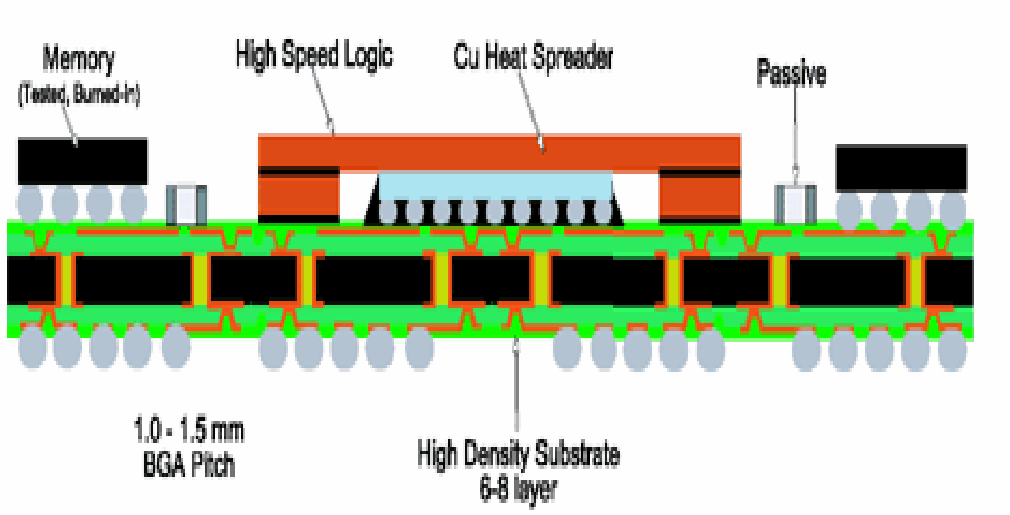


Figure 1.5 Amkor's System in Packaging section

System in packaging has emerged as the fastest growing packaging technology segment as the solution to facilitate the needs of these market demand which is cellular phones, laptops, cameras and commercial products. In 2004, 1.89 billion systems in packaging were assembled. By 2008, this quantity is expected to reach 3.25 billion, growing at an average rate of about 12% per year.[4] There are three factors, cost, size and performance, for driven by the material selections within the package. Figure 1.6 shows some of the variables and mutual relations on cost, size and performance as the function of the packaging, substrate and assembly methodology. The first 20% of the development phase determined the 80% of the cost of the product. This means that the choice of technology will determine the cost of the function. [16]

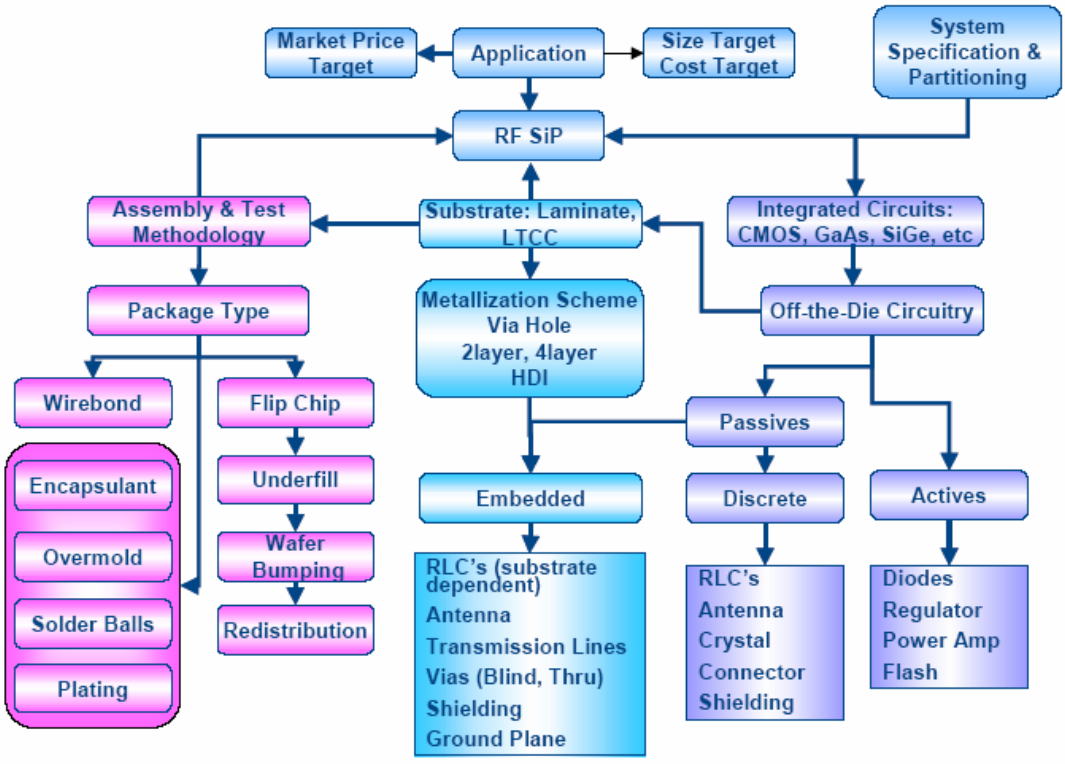


Figure 1.6 Mutual relations in Cost, Size and Performance [16]

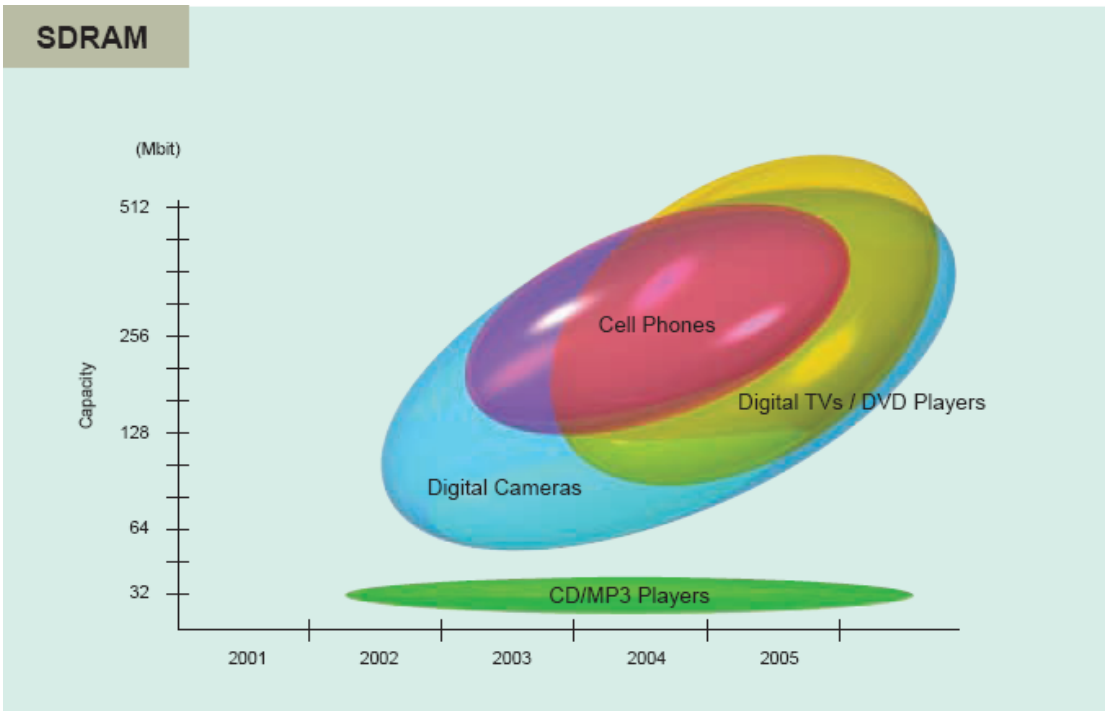


Figure 1.7 System in packaging memory trends in SDRAM [Toshiba Catalog]

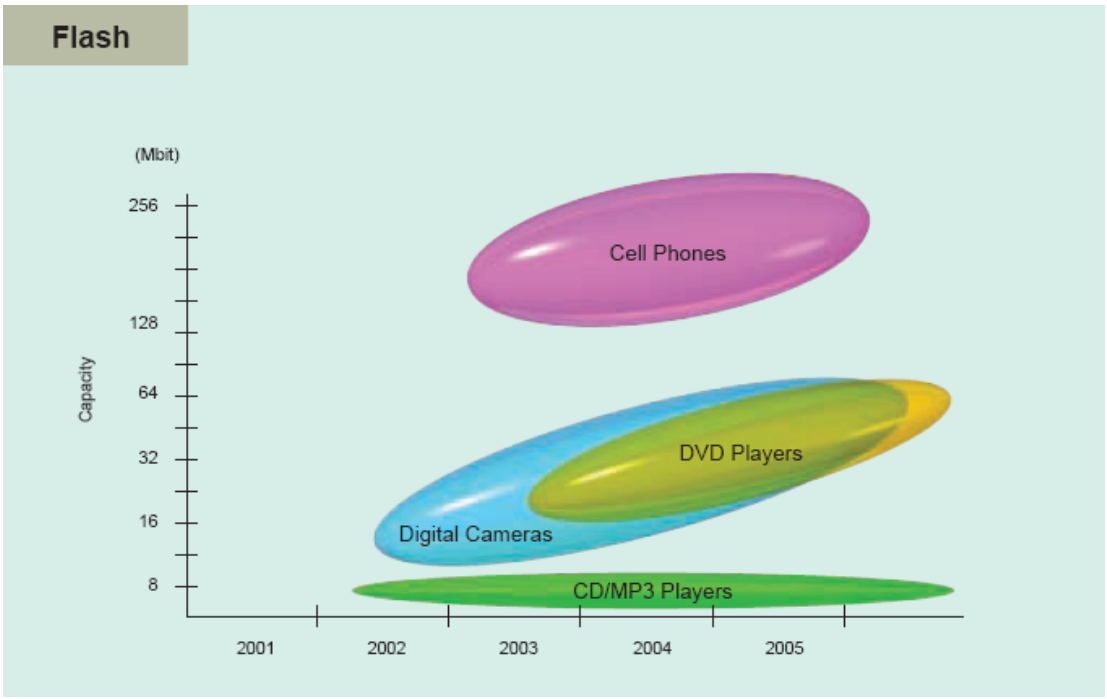


Figure 1.8 System in packaging memory trends in FLASH [Toshiba Catalog]

1.1.4 Wafer level packaging technology

Wafer level packaging is completed immediately on the wafer by dicing for the assembly in a flip chip fashion. Packaging with a few connects can be processed on the complete wafer before separation which is done when the package is already formed on the wafer and separation becomes the last process step. All wafer level packages are real chip size rather than chip scale due to the wafer level processing. By looking figure 1.9, we can understand all steps of wafer level packaging. By redistributing technology, wafer level package is to enlarge the pad pitch of standard ICs. The important advantages of wafer level packages are that the die and package in wafer level packaging are manufactured and inspected on the wafer, prior to outstanding product. It can down the cost of the wafer level packaging as the wafer size increases and as the die shrinks, unlike other packaging techniques that are assembled after singulation of the die from the wafers. There are three technologies, redistribution technology, encapsulate technology and flex tape technologies, for compete in market. [17]

1.1.5 Packaging on packaging technology

Packaging on packaging are improved performance and memory density, while reducing mounted area, designed for products requiring efficient memory architectures including multiple buses. Useful electronic products such as mobile phones, digital cameras, portable players, gaming and other mobile applications can benefit from the combination of packaging on packaging. By looking figure 1.10, we can understand advantage of packaging on packaging.

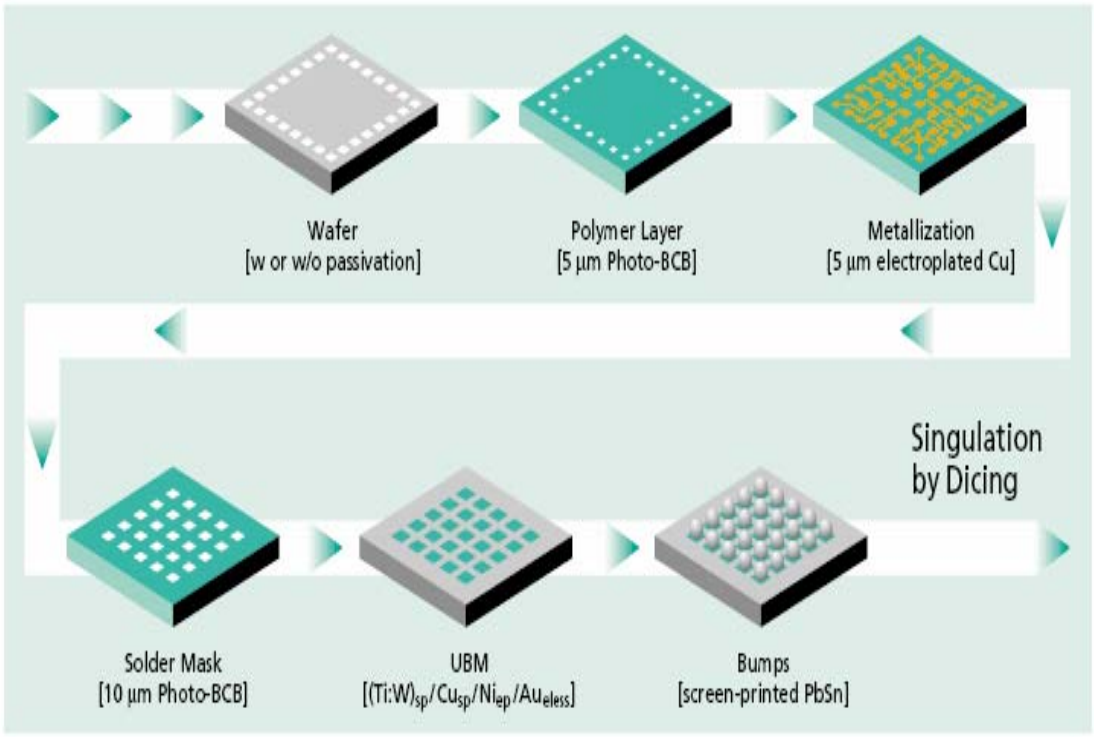


Figure 1.9 All steps of wafer level [17]

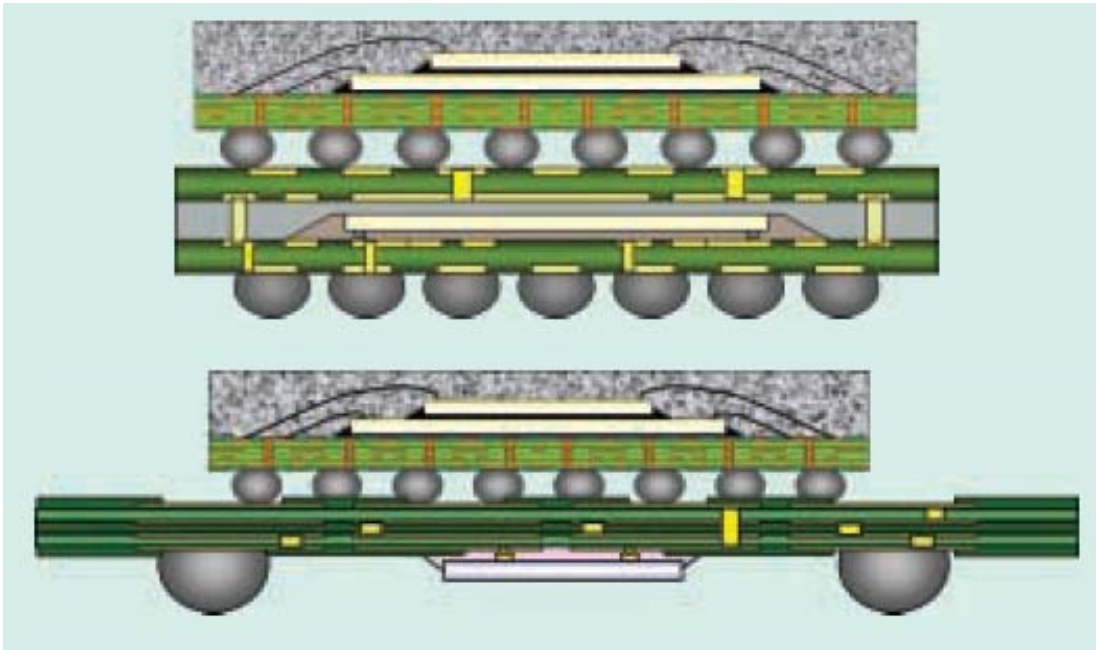


Figure 1.10 Amkor's packaging on packaging

1.2 New packaging technology

Various types of packaging technologies have been appeared in recent years. New packaging technology growth that is silicon through-via chip stacks and packages begin to develop or substitute conventional interconnection and packaging, such as advanced wire-bond chip stack packages and ceramic or organic chip carriers. The use of silicon carrier with silicon through-via provides a means of tightly integrating different chip technologies. Silicon carriers with through-vias can support heterogeneous semiconductor technologies, provide passive or active circuits and high-density I/O wiring interconnections with electro-optic technology, and support three-dimensional circuit integration. System on packaging within silicon-via technology can provide both high performance and low cost packaging solutions, extendible with advances in semiconductor lithography. [ibm]

1.2.1 Thermal Vias

The using of thermal vias has two different methods in the packaging. One is that one end of via attached to the bottom substrate, and the other attached to the top substrate with through to the substrate as shown figure 1.11. The other is that one end of via attached to the top die, and the other attached to the bottom die with through to the die as shown figure 1.12. In this thesis will examine through to the die such as figure 1.12. Figure 1.11 and figure 1.12 explain the heat flow between the top area of the die and the underside of the lower copper plane for a small region centered about one of the vias. The heat is created uniformly on the area of the die and intercepted by the top metal plane. Because the copper have the high thermal conductivity, the most of the

heat will concentrate to the vias location, flow along the length of the vias, and then diverge upon reaching the bottom metal plane. A few portion of the heat will flow directly from the top plane to the bottom one through the substrate.

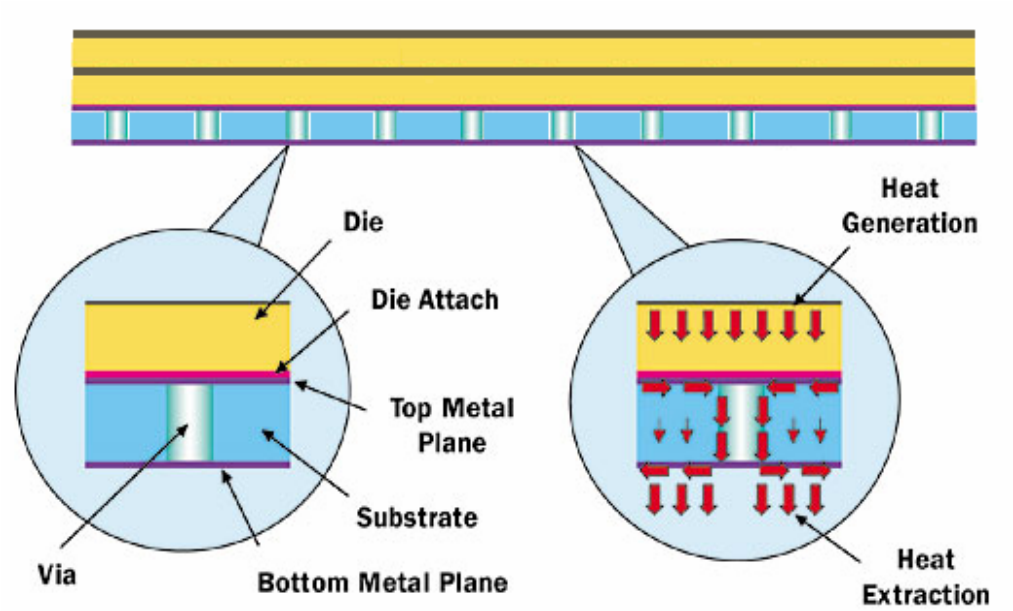


Figure 1.11 Diagram of thermal vias through to substrate with via array and heat flow [18]

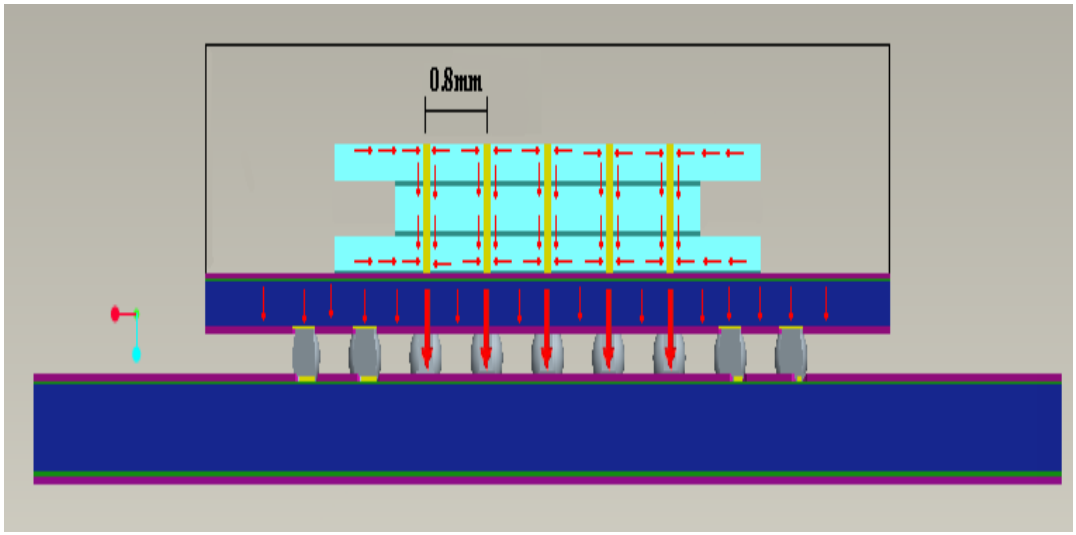


Figure 1.12 Diagram of thermal vias through to die and heat flow

The heat is emitted from the bottom metal layer with a thermal efficiency that would be representative of an array of solder balls covering 20% of the surface of the bottom layer. This is represented in the model as an effective heat transfer coefficient applied to the bottom area. [18]

1.2.2 Relation of the thermal vias and thermal resistance

Thermal solution of vias relate to thermal resistance. The various via configurations of table1.1 lists included in the analysis. All of the vias arrays are arranged to be on a regular pitch on a matrix pattern. The vias matrices vary from no vias (0 x 0) to a large 11 x 11 array and the vias numbers vary from 0 to 121. As shown table 1.1, although the thermal resistance for the no vias situation is 15.9°C/W, thermal vias can reduce by 90% of thermal resistance at the largest via array evaluated at 11 x 11 array vias. [18]

Table 1.1 Result of FEA calculations of effect of vias

Matrix	Number of vias	Via pitch (mm)	Thermal resistance	
			(℃/W)	% Reduction
0 x 0	0	N / A	15.9	0%
1 x 1	1	10.0	14.2	10.8%
2 x 2	4	5.0	10.5	34.3%
3 x 3	9	3.3	7.3	54.3%
4 x 4	16	2.5	5.2	67.5%
5 x 5	25	2.0	3.8	75.8%
6 x 6	36	1.7	3.0	81.1%
7 x 7	49	1.4	2.5	84.6%
8 x 8	64	1.3	2.1	86.8%
9 x 9	81	1.1	1.8	88.4%
10 x 10	100	1.0	1.7	89.6%
11 x 11	121	0.9	1.5	90.4%

Figure 1.13 shown relationship of number of vias and thermal resistance. Figure show that the relation of vias and thermal resistance is an inverse proportion. However, after a certain point, adding additional vias becomes a matter of diminishing returns. For instance, the 25 vias achieve 90% of the thermal reduction obtained with the 121 vias.

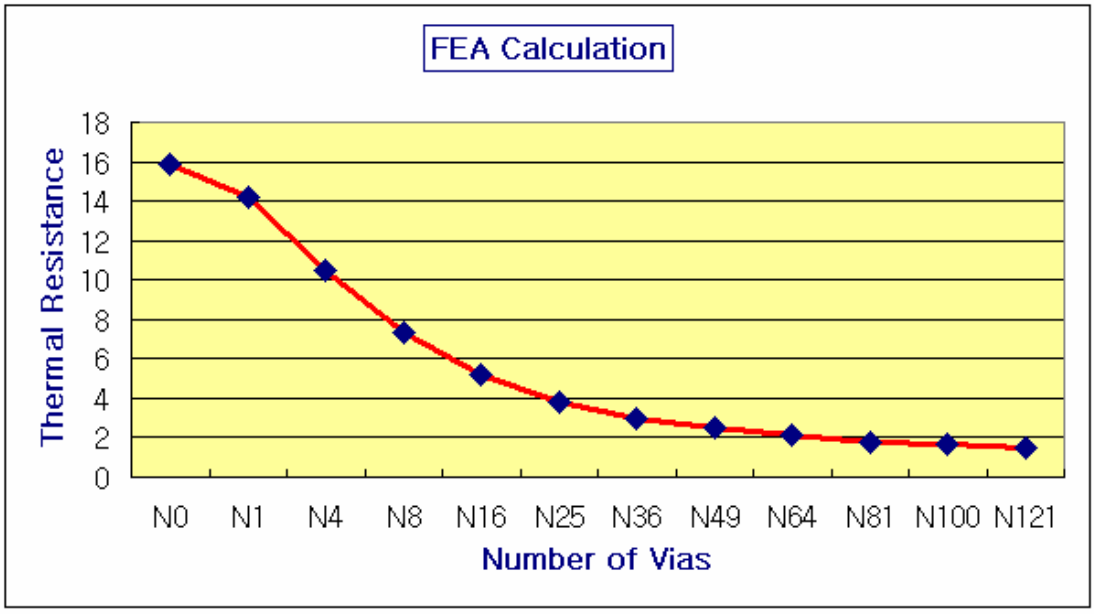


Figure 1.13 FEA thermal solutions

CHAPTER 2

LITERATURE REVIEW

2.1 Thermal Vias

Many different packaging papers have been published since the late 1990s, but three-dimensional packaging technology with through-vias has been receiving increasing attention recently. This attention stems partly from the technology's promise of making modules that are smaller, lighter, have fewer boards and other pares, and are cheaper than current modules. The following papers show present an overview of vias technology and new packaging technologies.

Kazumi (2005) evaluated optimization for chip stack in 3-D packaging. The structure was optimized for successful connection in a chip stack without degrading the features of the chips. Using this structure enabled a stable and rigid connection, a four-layer chip stack assembled on a ceramic substrate exhibited adequate thermal cycle performance. Their paper discusses how the structure of terminals was optimized for chip stacking. A finished package assembled from static random access memory with through-type electrodes was confirmed to operate and exhibit normal functioning.

Ricky (2005) presents a new package design for multi-chip modules. Chips are assembled on a silicon chip carrier with eutectic solder joints. A through-silicon via hole is made at the center of the silicon chip carrier for optional underfill dispensing. The whole multi-chip module is mounted on the printed circuit board by the standard surface mount reflow process. The Underfill material is dispensed through the center

through-silicon via hole on the silicon chip carrier to encapsulate the solder joints and four smaller chips.

Spiesshoefer (2005) describe that the formation of a through-silicon via. Following their paper, through-silicon via enables three-dimensional interconnects for chip-stacking applications that will be especially important for integrating heterogeneous devices. They include many processing steps such as via formation, deposition of via insulation, barrier, Cu seed films, Cu electroplating for via-fill and backside processing. Their paper discusses the process flow and integration of the processes useful in through-silicon via technology. By reading this paper, we can know processes of the through-silicon via.

Mccoy (2004) published paper about performance evaluation and reliability of thermal vias. They establish a high-yield design approach for surface mount power packages utilizing PWB thermal vias, elastomer material and heat-sinks. A feasibility study proved that the thermal via concept could be implemented to meet cooling and producible requirements. This paper is useful to understand the function of the thermal via.

Seongjoon (2003) described the details of the process for the fabrication of high density, high aspect ratio through-wafer electrical interconnect that includes deep dry etching hole through the substrate, depositing an insulation layer and depositing a conductive layer. Papers show the two different processes. One is that through-wafer electrical interconnect is fabricated after the fabrication of MEMS devices, another is that through-wafer electrical interconnect is fabricated before the fabrication of MEMS

device. This paper demonstrated the through-wafer electrical interconnect can be made after the MEMS devices are first fabricated based on the post-process sequence presented in that paper, the pre-process would be a favorable choice unless the fabrication of MEMS devices must precede the through-wafer electrical interconnect creation.

Marc (2002) published about the high performance thermal vias in low temperature co-fire ceramic substrates. New developments in low temperature co-fire ceramic (LTCC) have allowed the fabrication of highly thermally conductivity vias arrays. Following this paper, the introduction of high-density thermal via arrays in LTCC technology provides a low thermal resistance path for thru substrate applications. Thermal vias with 80% via density and internal spreader layers have been demonstrated. Typical via arrays with area fractions of less than 20% will be able to provide adequate heat transport through the substrate for near-future anticipated thermal loads. This will require the use of enhanced via arrays with high area fractions over 50%, with through-plane effective thermal conductivity over 100W/m-k.

Yasuhiro (2001) describes the thermal characteristics of three dimensional modules where four bare-dies with Cu through-vias are vertically stacked and electrically connected through the Cu-vias and the metal bumps. To realize more accurate thermal analysis for the 3D-modules in the earlier stage of the process development, a series of simple thermal resistance measurements by Laser-flash method and parametric numerical analyses have been carried out. This paper confirmed that the Cu-vias in dies are not so effective to thermal performance, while bumps between dies

can function as thermal vias effectively. At the same time, the thermal effect of the die thickness is not negligible. Die-thinning is a minus effect from the viewpoint of thermal management.

Li (2000) presents a simple analytical model that provides an efficient approach for analysis of thermal via pads. Heat flow across the substrate thickness in the vias cluster is much more significant than the heat spreading effect in the lateral direction. So it means that predominantly one-dimensional heat conduction allows analytical simplification by modeling the thermal via as parallel networks. Paper present the functional relationship between the thermal resistance and the via design parameters that can also serve as a design guideline for engineers to properly select design configuration by accommodating other factors such as reliability and manufacturability. Namely, thermal performance of via cluster depends on dimensionless design parameters. By reading this paper, we can know different function of thermal via as the dimensionless design parameters.

By reading all mentioned papers, it is useful for me to write my thesis. Now days, study focuses on the thermal management and resistance of vias on dies and substrate in 3D-packaging.

2.2 Thermal resistance and Thermal theory

Thermal properties of equipments can often be indicated as components in an electrical circuit as show figure 2.1. Power dissipation is designed as a current source, thermal resistance is designed as electrical resistance and temperature is designed as a voltage. The models provide easy steady-state evaluation of thermal problems using

familiar circuit analysis techniques. The model shown does not apply to transient thermal resistance. In the figure 2.1, θ_{JA} is thermal resistance between junction and ambience given in ℃/W. The θ_{JA} specifies the increase in junction temperature (T_J) above ambient temperature (T_A) for every watt of power. Mathematically θ_{JA} is given as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} = \frac{T_J - T_A}{P_D} \text{°C/W} \tag{2-1}$$

Also in the figure 2.1, θ_{JC} is thermal resistance between junction temperature (T_J) and case temperature (T_C). θ_{CA} is thermal resistance between case temperature (T_C) and ambient temperature (T_A).

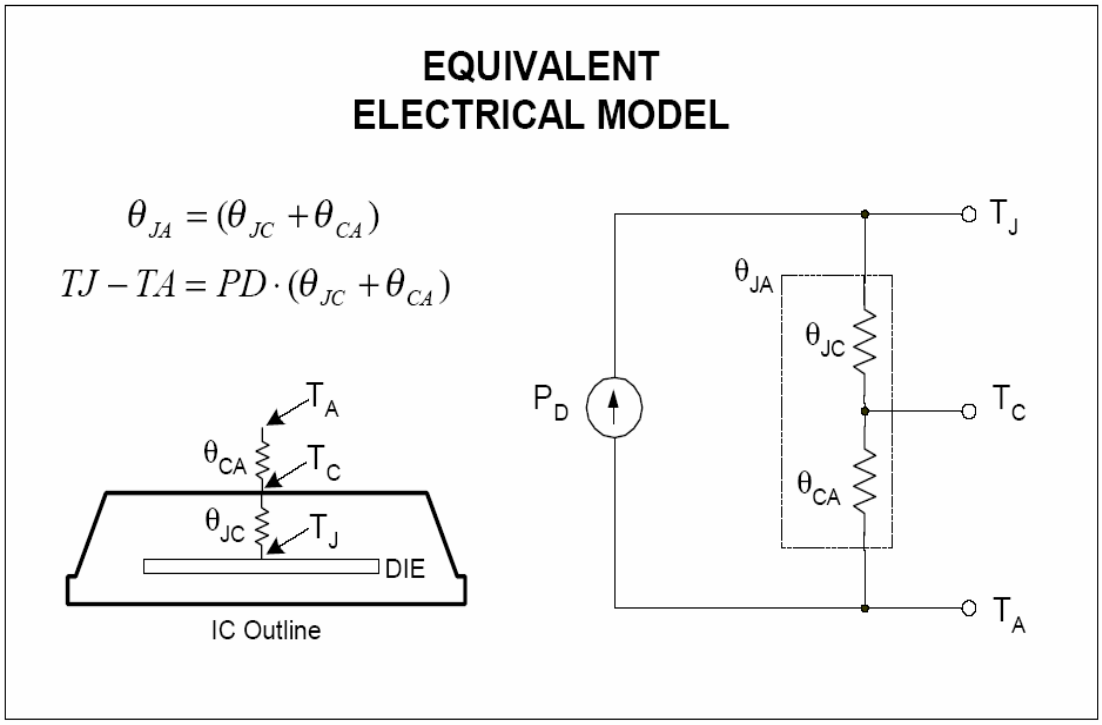


Figure 2.1 Equivalent electrical model

As show the figure 2.2, maximum continuous power that can be dissipated at the junction of the IC by the package. The value is specified at a given temperature with a particular factor (1/ θ_{JA}) calculated from specific test conditions. It simply states how much power can be dissipated by the package, and is not representative of the power of the die. If operation is performed above the specified temperature (T_{Amas}), the package is unable to dissipate the maximum continuous power rating and must be diminished. Maximum junction temperature is highest temperature of the junction before damage or increased failure rate occurs in figure 2.2.

The thermal resistance of an IC is affected by many parameters, some of which can be changed by a system designer to obtain improved heat transfer characteristics. Other parameters have a direct relation to the IC package. θ_{JC} is derived from specific characteristics of the IC package such as die size, lead frame material/design and package body material. θ_{CA} is directly related to system level variables. Forced-air cooling, package mounting, trace width, external heat sinks and many other variables all affect the total thermal resistance of an IC. The combined thermal resistance of θ_{JC} and θ_{CA} is known as θ_{JA}. This helps in understanding the scope of the θ_{JA} value when evaluating IC packages. θ_{JA} should be used as a relative number when evaluating the thermal dissipation performance of an IC package. [12]

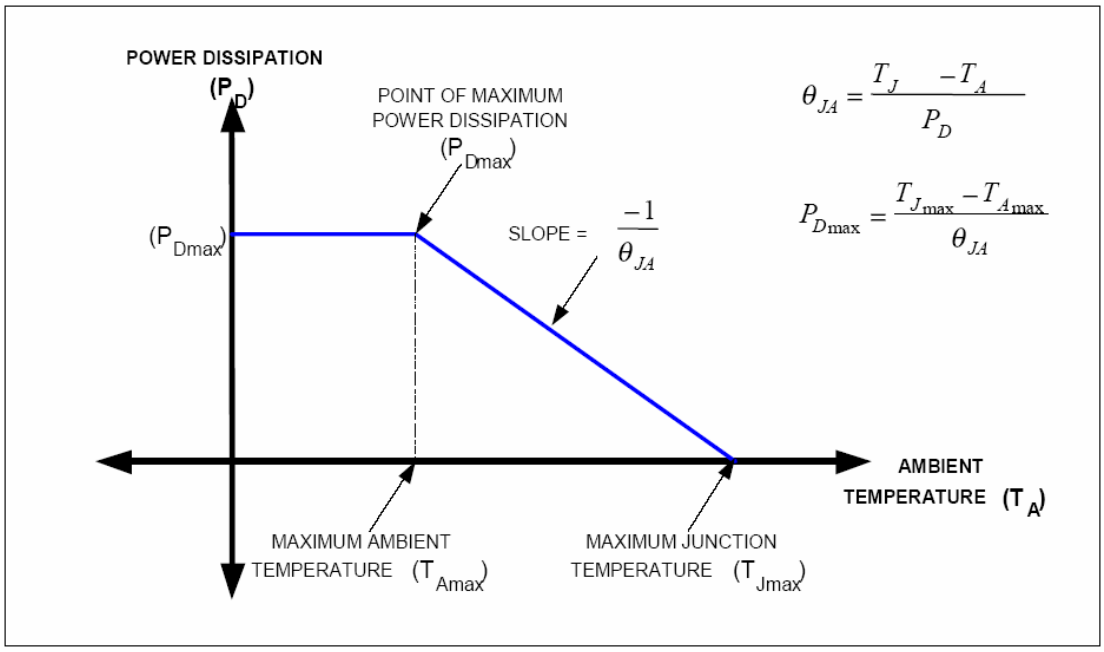


Figure 2.2 Power dissipation vs. Ambient temperature [12]

CHAPTER 3

OBJECTIVES AND SUMMARY

3.1 Summary in study

Figure 3.1 summarizes the methodology of this study. First, the geometry excluding the vias (including the material property) is created using pro/engineer wildfire 2.0. Second, thermal vias is created. Thirdly, pro/e model of the entire geometry and properties is imported to Ansys workbench. Boundary conditions are then implemented in Ansys. The end result of the simulation is the comparison of the heat transfer with and without vias.

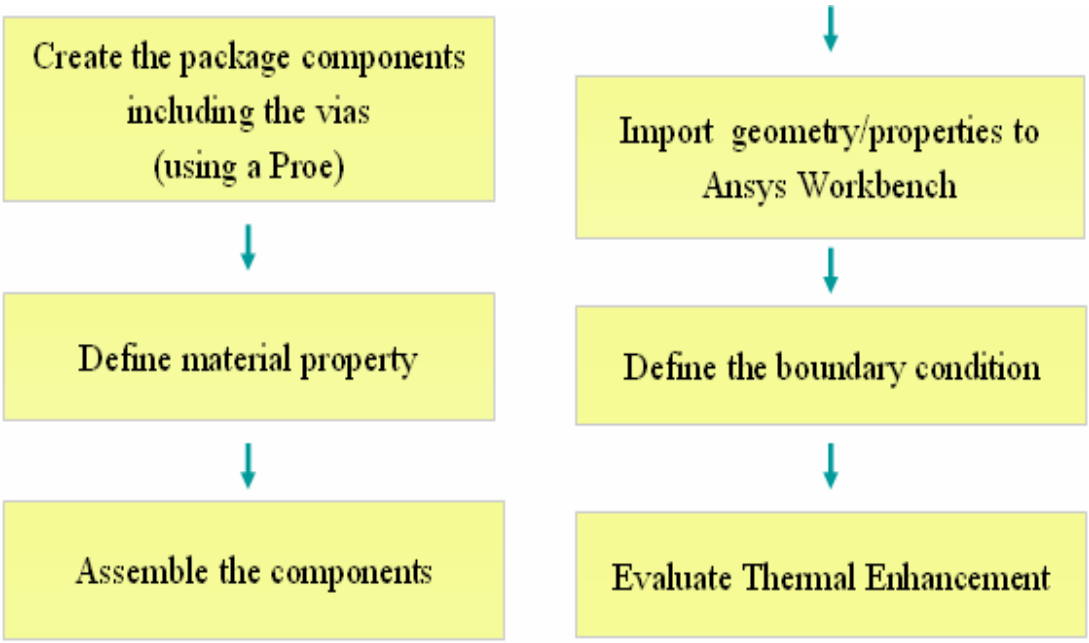


Figure 3.1 Summary of this thesis

3.2 Objectives

This study focuses on how reduce temperature by using of thermal vias. There are several approaches to implementation of thermal vias. One approach is to have a thermal die that thermally connects each die to the substrate. Thermal vias can possible the heat flow between the top area of the die and the underside of the lower copper plane for a small region centered about one of the vias. The heat from each die is conducted either through the die attach or the vias. Since the vias have copper, they provide a path of least resistance and a heat is transferred through the vias in a proportion much greater than the area of the vias. Vias can also provide both electrical and thermal path. In this thesis, only the thermal enhancement of vias is discussed. Three different stacking architectures were evaluated, stacking with spacers, pyramid stacking and rotated stacking die. Based on the maximum junction temperature, thermal management strategies that involve increasing heat transfer co-efficient on top of the package, increasing the PCB core thermal conductivity, and use of copper heat spreader are presented.

CHAPTER 4

GEOMETRY MODELING

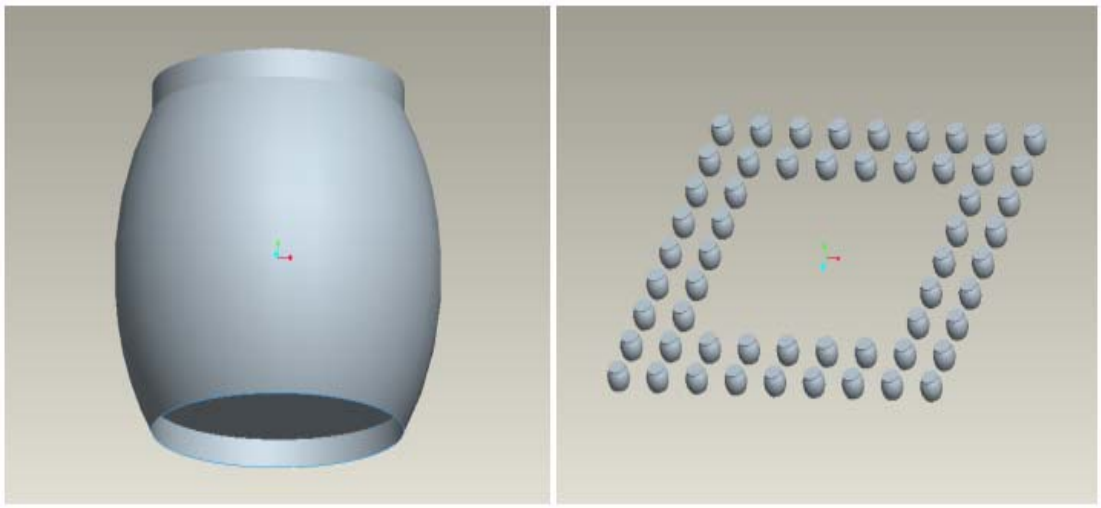
4.1 Package and Dimension

Every elements of packaging were modeled using Pro/Engineer Wildfire 2.0 as a CAD tool. Each element saved UDF library with material property. Then, by using assembly function, packaging geometries were created for each of the stacking architectures. Figure 4.7 shows process of assembly. Dimensions of all elements were parameterized. It can help in creation of different models which are uses to get solution multi-design variable optimization problems, a capability that exists in Ansys Workbench. Now days, Pro/Engineer used in variety industry because it has many advantages as following. [ptc.com]

- Complete 3D modeling capabilities enable any body to exceed any product quality and time-to-market goals
- Maximum production efficiency through automated generation of associative tooling design, assembly instructions, and machine code
- Ability to simulate and analyze virtual prototypes to improve product performance and optimize product design
- Ability to share digital product data seamlessly among all appropriate any people
- Compatibility with myriad CAD tools — including associative data exchange — and industry standard data formats

In this work, the two stages of assigning material properties and dimensional parameterization are completed during the geometry modeling. Then, geometry that modeled in Pro/Engineer import to Ansys Workbench for simulation.

9mm x 9mm substrate on a 1-layer PWB is adopted in the model of this study. The substrate has a 0.3mm thickness. PWB have 32mm x 24mm and 0.6mm thick. The mold cap is 1.2mm thick and has the same dimensions as the package substrate. Solderball geometry is modeled closely approximating the real solderball as show figure 4.1(a). In solderball geometry, mid diameter is 0.43mm, and top and bottom diameter is 0.33mm, with a height of 0.34mm. Solder ball of 56 numbers arrange is same as figure 4.1 (b).

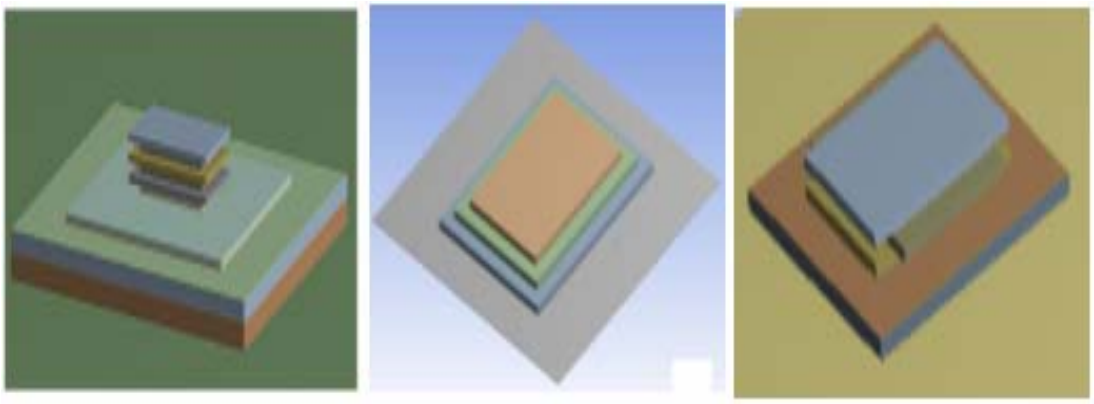


(a) (b)

Figure 4.1 Die stacking configurations:
(a) Solderball architecture; (b) Arrange of Solderball

Three different package architectures were modeled; (a) spacer stacked die; (b) pyramid stack die; (c) rotated stack die as show Figure 4.2. In the spacer die, all dies have 6.4mm x 4.8mm with a thickness of 0.2mm. Paste is same as die dimension with a thickness of 0.02mm. All dies was placed parallel. In the rotated stack die, all dies have 6.4mm x 4.8 mm with a thickness of 0.25mm. Paste is same as die dimension with a thickness of 0.025mm. Die 2 was paced at 90° to die 1 and die 3 as show figure 4.2(c).

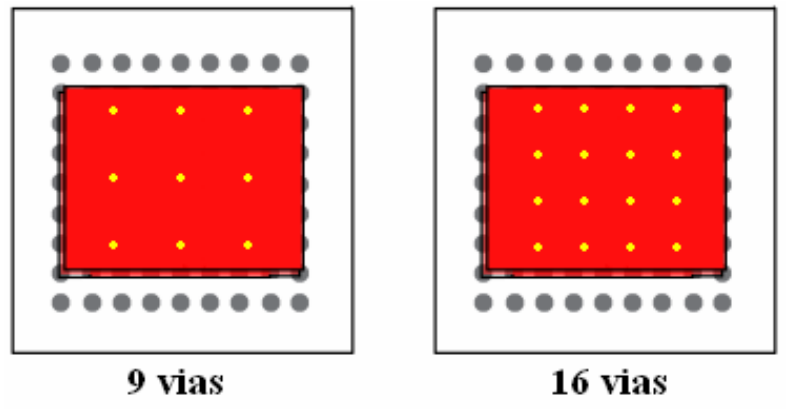
In the spacer stacked die, thermal vias have diameter of 0.12mm and thickness of 0.86mm. In the rotated stacked die, thermal vias have diameter of 0.12mm and thickness of 0.825mm. Thermal vias was placed 9 vias and 16 vias in the each package. It can compare to maximum junction temperature as number of vias. Arrange of thermal vias is same as figure 4.4 and figure 4.6. One end of via attaches to the top substrate, and the other attaches to a top die as show figure 4.3 and figure 4.5.



(a) (b) (c)

Figure 4.2 Die stacking configurations:
(a) Spacer stacked die; (b) Rotated stacked die; (c) Pyramid die

Figure 4.3 Thermal vias in spacer die



(a) (b)

Figure 4.4 Arrangement of vias in spacer die: (a) 9vias; (b) 16 vias

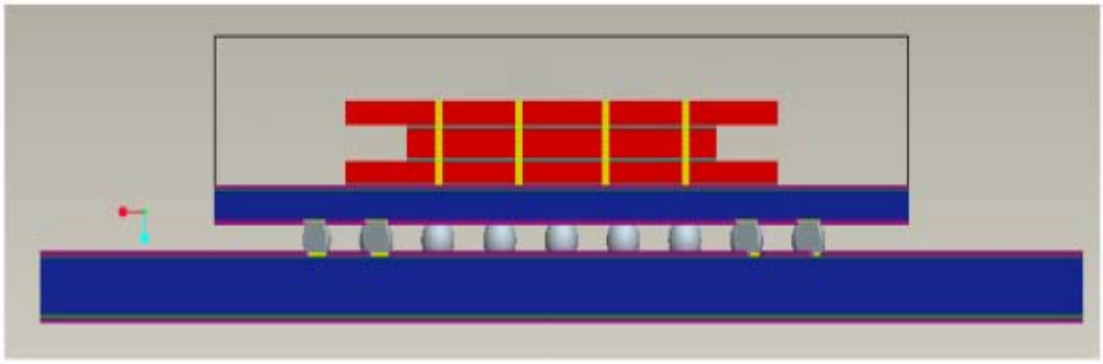
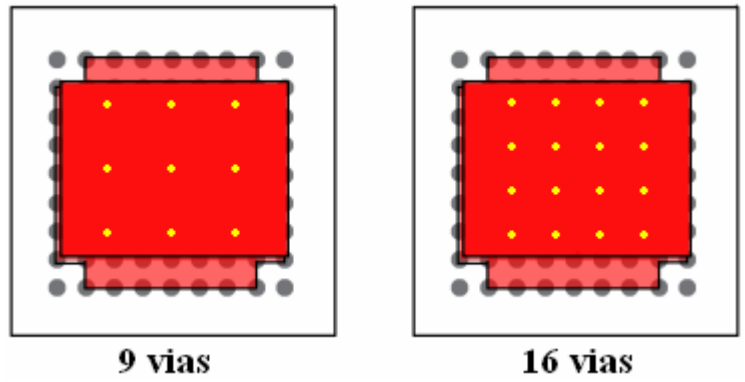


Figure 4.5 Thermal vias in rotated stacked vias



(a) (b)

Figure 4.6 Arrangement of vias in rotated stacked die: (a) 9 vias; (b) 16 vias

Table 4.1 shows the package dimensions.

Table 4.1 Dimensions of packaging

	Spacer Die (mm)	Pyramid Die(mm)	Rotated Die (mm)
Die	6.4 x 4.8 x 0.2	6.4 x 4.8 x 0.25 6 x 4.4 x 0.25 5.6 x 4 x 0.25	6.4 x 4.8 x 0.25
Paste	6.4 x 4.8 x 0.02	6.4 x 4.8 x 0.25 6 x 4.4 x 0.25 5.6 x 4 x 0.25	6.4 x 4.8 x 0.025
			4.8 x 4.8 x 0.025
Dummy die	5.6 x 4.0 x 0.08	-	-
Dummy die paste	5.6 x 4.0 x 0.02	-	-
Substrate	9 x 9 x 0.3	9 x 9 x 0.3	9 x 9 x 0.3
PCB	32 x 24 x 0.6	32 x 24 x 0.6	32 x 24 x 0.6
Mold compound thickness	1.2	1.2	1.2
Solder ball	Td=0.33 Md=0.43	Td=0.33 Md=0.43	Td=0.33 Md=0.43
Thermal vias	D=0.24 T=0.86	D=0.24 T=0.825	D=0.24 T=0.825

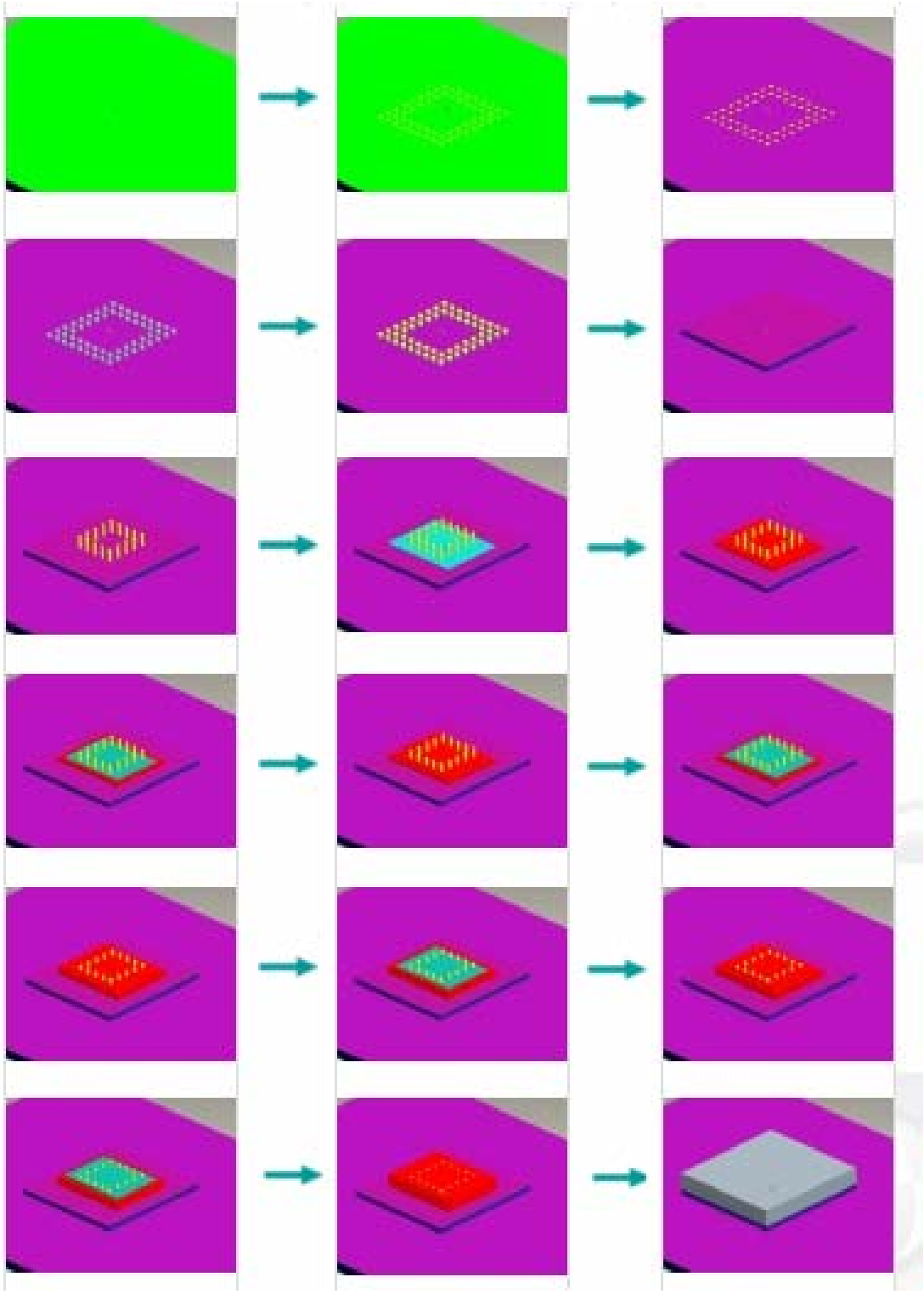


Figure 4.7 Process of assembly

4.2 Thermal Conductivity

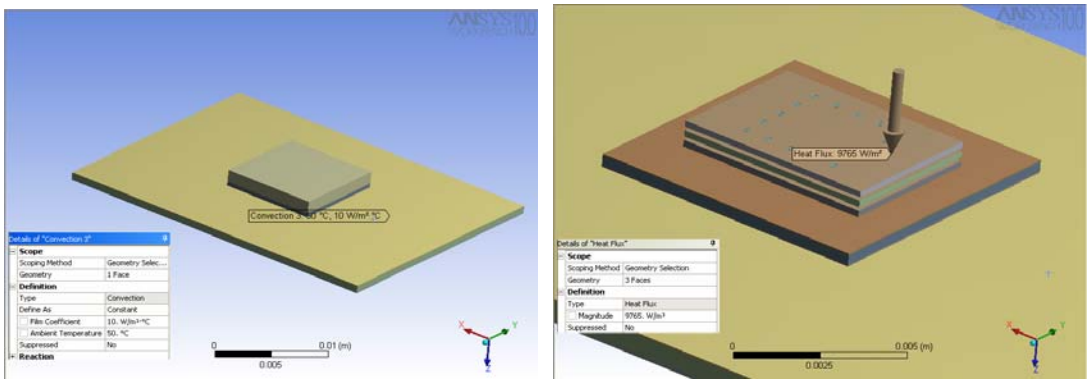
Heat transfer by conduction involves transfer of energy within a material without any motion of the material as a whole. The rate of heat transfer depends upon the temperature gradient and the thermal conductivity of the material. In other to get effect of thermal vias, we must use high thermal conductivity vias. But using high thermal conductivity vias such that thermal conductivity of diamond is 1000W/mK is very expensive. This study use copper vias. Table 4.2 shows the material thermal conductivity of the elements.

Table 4.2 Thermal conductivity of elements

Element	Thermal conductivity (W/m-K)
Solder ball	54
Die	120
Copper	380
Mold Cap	0.88
PCB	0.18
PCB resist	20
Die paste	0.48
Thermal vias	377

4.3 Simulation in Ansys Workbench 10

Pro/engineer geometries with material properties were imported into Ansys Workbench 10.0 to determine the maximum junction temperature. Material properties were already assigned during Pro/engineer modeling. Figure 4.8 shows boundary condition and heat flux. That is, film coefficient is 10W/m²℃ and ambient temperature is 50℃ on the all face of molding cap and bottom PCB. This thesis apply that power is 0.3W on the face of each die. By dividing area, we can get a heat flux, 9765W/m². Table 4.3 and 4.4 shows the boundary condition such as film coefficient, ambient temperature and power.



(a) (b)

Figure 4.8 Inserting of boundary conditions and uniform power

Table 4.3 Power in each die

Die 1	0.3 W (heat flux = 9765 W/m²)
Die 2	0.3 W (heat flux = 9765 W/m²)
Die 3	0.3 W (heat flux = 9765 W/m²)

Table 4.4 Boundary condition

Ambient Temperature	10 W/m²℃
Film Coefficient	50℃

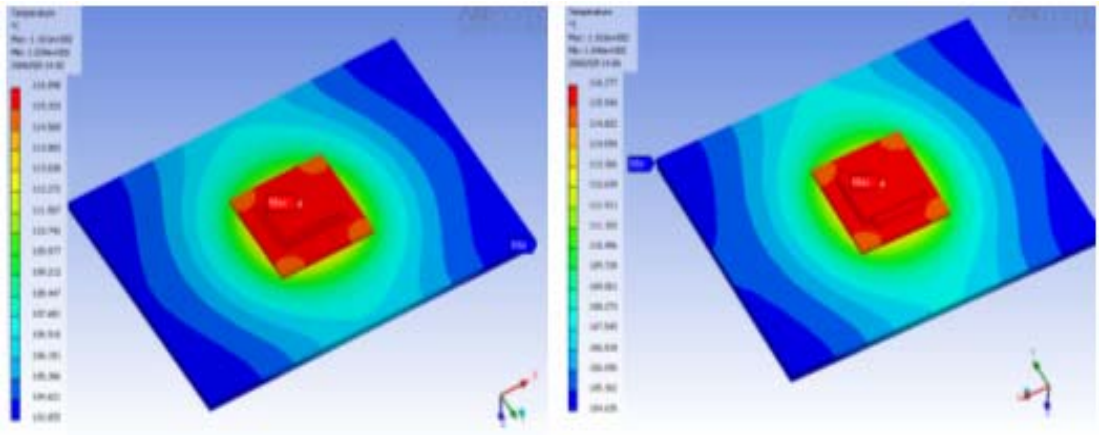
For the present context of thermal vias material properties were assigned in modeling tool i.e. Pro-e wildfire where the geometry was built and assembled as per the design. The simulation was carried as a baseline study in steady state conditions on the geometry with and without the vias to major focus on the advantage of the thermal vias attached. The simulation is done using different iterations of 9, 16 and no thermal vias at all and ended up with quite decent numbers.

CHAPTER 5

RESULT & DISCUSSION

5.1 Compare the max temperature of Die applied on uniform power

For the baseline simulation, an effective heat transfer coefficient of 10 W/m²-ºc with 50ºc ambient temperature was applied on the top of the mold cap, and the top and bottom surfaces of the circuit board. Every die applied 0.3W uniform power. The result was a junction temperature of 116ºc with no vias. When 9 vias were included, for the same heat transfer coefficient, the junction temperature was reduced to 111ºC, results in a decrease of around 3.6% of the maximum temperature in each of the architectures. By increasing the via count to 16 we got the junction temperature to 110ºc effectively reducing the junction temperature 4.49% of the maximum temperature in each of packaging.



(a) (b)

Figure 5.1 Maximum junction temperature:
(a) Spacer die; (b) Rotated die

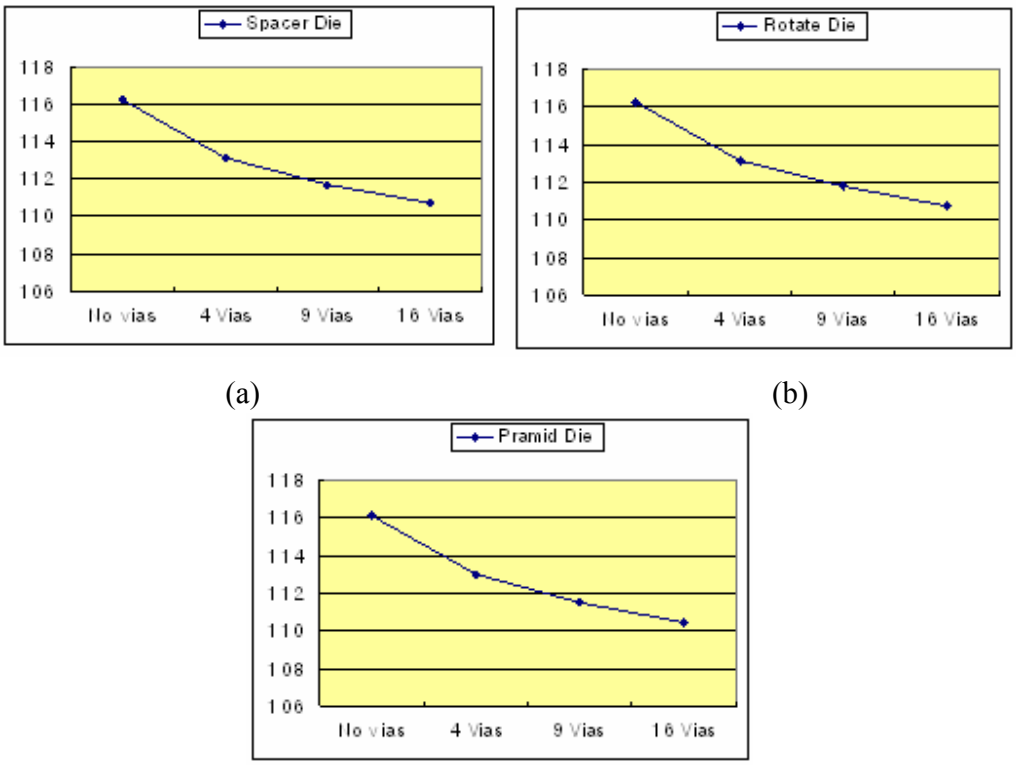


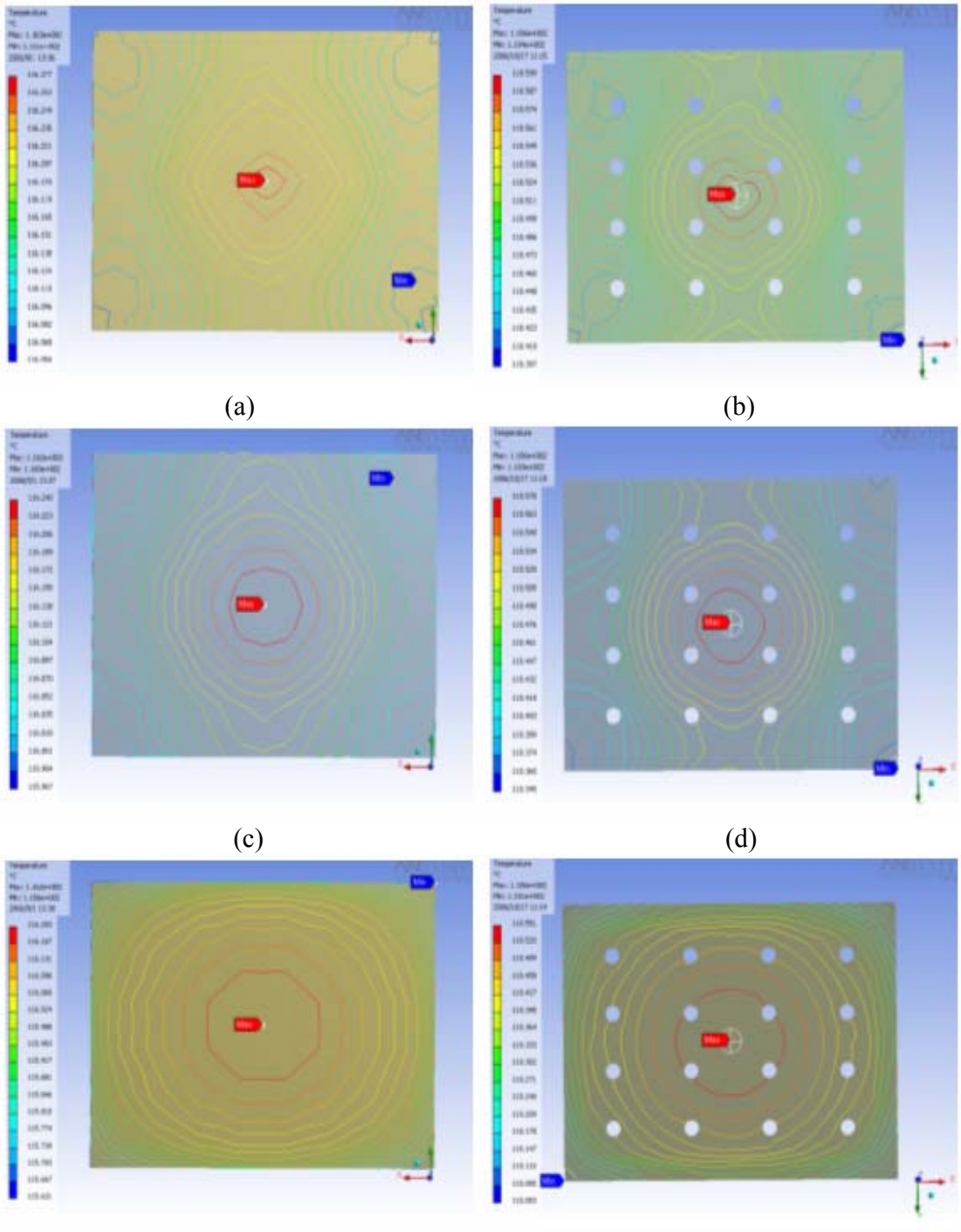
Figure 5.2 Graph of Maximum junction temperature:
(a) Spacer die; (b) Rotated die; (c) Pyramid die

From the figure 5.2 graphs and table 5.1 we can notice that rotated, pyramid and spacer dies all show the similar behavior when it comes to the junction temperature and thermal vias. That is, when the number of thermal vias increases the junction temperature goes down. This shows that as you provide more paths for heat outlet, it helps to bring down the temperature to a decent number.

Table 5.1 Result of Maximum junction temperature in uniform power

	Spacer die	Rotated die	Pyramid die
No vias	116.27 ºC	116.27 ºC	116.09 ºC
4 vias	113.12 ºC	113.11 ºC	112.98 ºC
9 vias	111.71 ºC	111.76 ºC	111.54 ºC
16 vias	110.60 ºC	110.71 ºC	110.48 ºC

The figure 5.3 which shows the isolines of die-geometry without and with vias in ANSYS Workbench clearly mention that the temperature near the thermal via location is high and the isolines are dense. As the heat concentrates more in the thermal vias area the temperature of the isolines surrounding the vias location is hotter when compared to other area. We can also observe that the contours at the vias are clearer. In the heat flux picture figure 5.4 of this die we can see that most of the heat gathers more at the thermal vias location and easily dissipates away from the die.

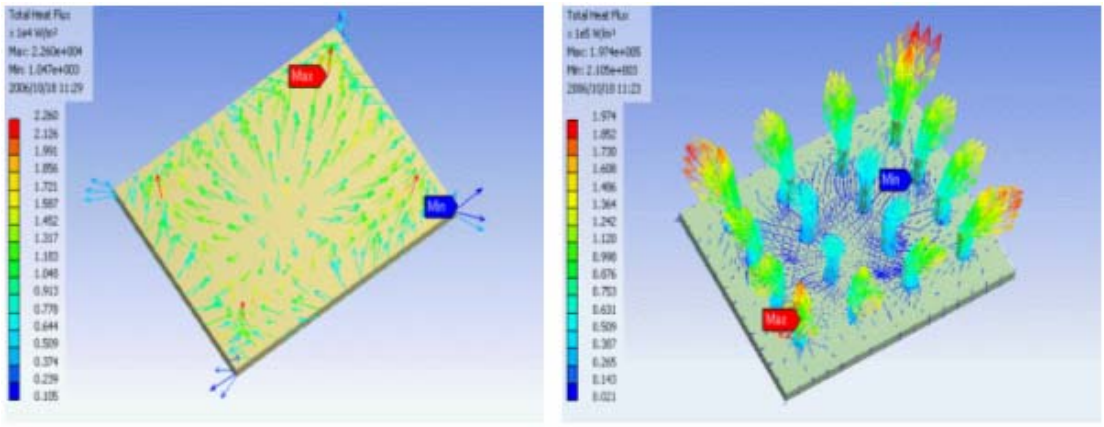


(a) (b)

(c) (d)

(e) (f)

Figure 5.3 Distribution of max temperature with and without vias in uniform power: (a) Top die without vias; (b) Top die with vias; (c) Mid die without vias; (d) Mid die with vias; (e) Bottom die without vias; (f) Bottom die with vias



(a) (b)

Figure 5.4 Heat flux arrows in Spacer die: (a) no vias; (b) with vias

The main objective behind this study is providing a smooth and effective heat transfer path. Due to the high thermal conductivity of the copper i.e. the thermal vias, a proportion of the heat much greater than the surface area of the vias will be transferred. Figure 5.4 explains the proportional vector plot of heat flux in ANSYS® Workbench™ 10.0 where we can see the heat flow path which densely collects at the via location. This heat flux is a negative heat flux where heat is transferred from the respective die directly to the substrate. Comparing the heat flux Figures 5.4 (a) and (b), it is clear that the vias provide a significant heat flow path and thus reduce the amount of heat that has to traverse through the entire stack.

5.2 Different location of thermal vias for optimized results

Figure 5.5 and table 5.2 show different locations of thermal vias and the vertical and horizontal distances between the thermal vias.

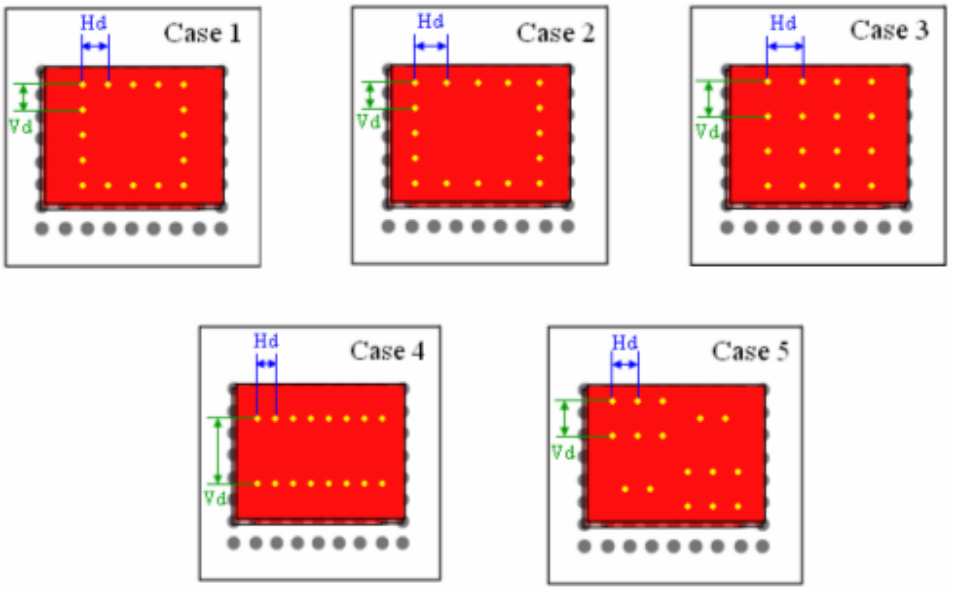


Figure 5.5 Different locations of Thermal vias

Table 5.2 The vertical and horizontal distances between the thermal vias

	Case 1	Case 2	Case 3	Case 4	Case 5
Hd	0.8 mm	1.1 mm	1.5 mm	0.7 mm	0.8 mm
Vd	0.8 mm	0.8 mm	1.2 mm	2.0mm	1.0 mm

Table 5.3 shows results of different locations of thermal vias. Though, there is not much difference in the temperature, Case 3 shows that such type of arrangement gives the lowest temperature than the other four.

Table 5.3 Results of different locations of thermal vias

	Case 1	Case 2	Case 3	Case 4	Case 5
Temperature	110.70 ºC	110.68ºC	110.60ºC	110.72ºC	110.67ºC
Heat flux	17.95w/cm²	18.25w/cm²	19.74w/cm²	17.19w/cm²	18.30w/cm²

5.3 Compare the max temperature of Die applied on non-uniform power

As devices such as microprocessors increase in functionality, the power distribution in die becomes an increasingly significant factor in determining the cooling capability of thermal solutions. [15] Thermal vias can also provide a means of customizing the heat transfer process for devices with a highly non-uniform power distribution. This is especially important for high density interconnects where the device has highly non-uniform power map.

5.3.1 2X2 Non-uniform power supply

Here the die area is been divided into four equal portions and non-uniform power distribution is supplied. In the below figure 5.6 show that the three dies are divided in four equal partitions and on one quarter part 8 vias are placed with a power of 0.15W and remaining three dies portions have two vias each with a power of 0.05W which makes the total power as 0.3W on each die. This process applied same on the top, mid and bottom die.

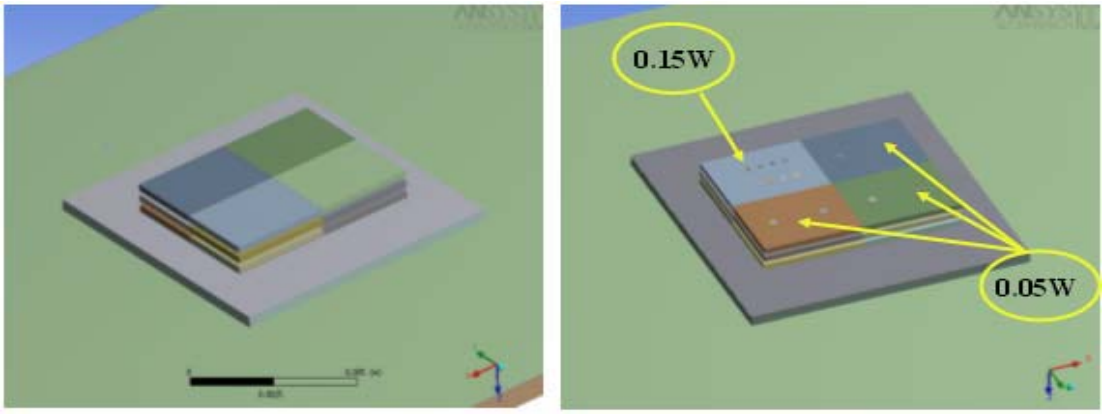
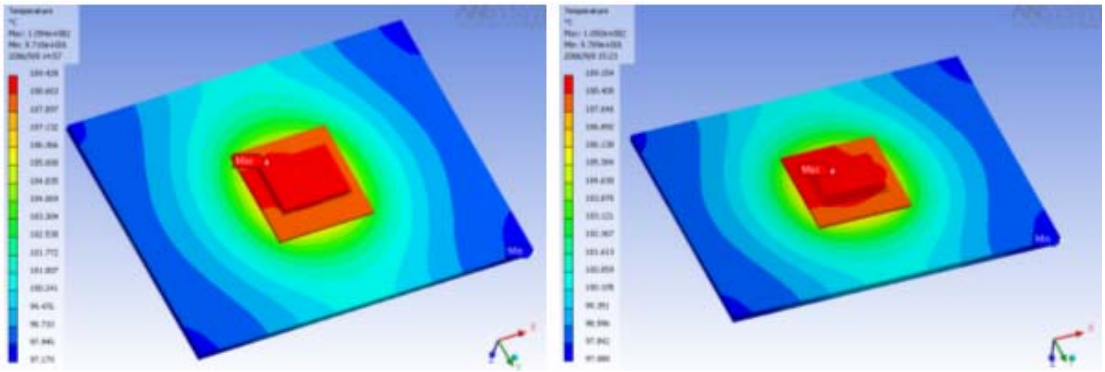


Figure 5.6 Simulation of Spacer stacking Die applied on non-uniform Power



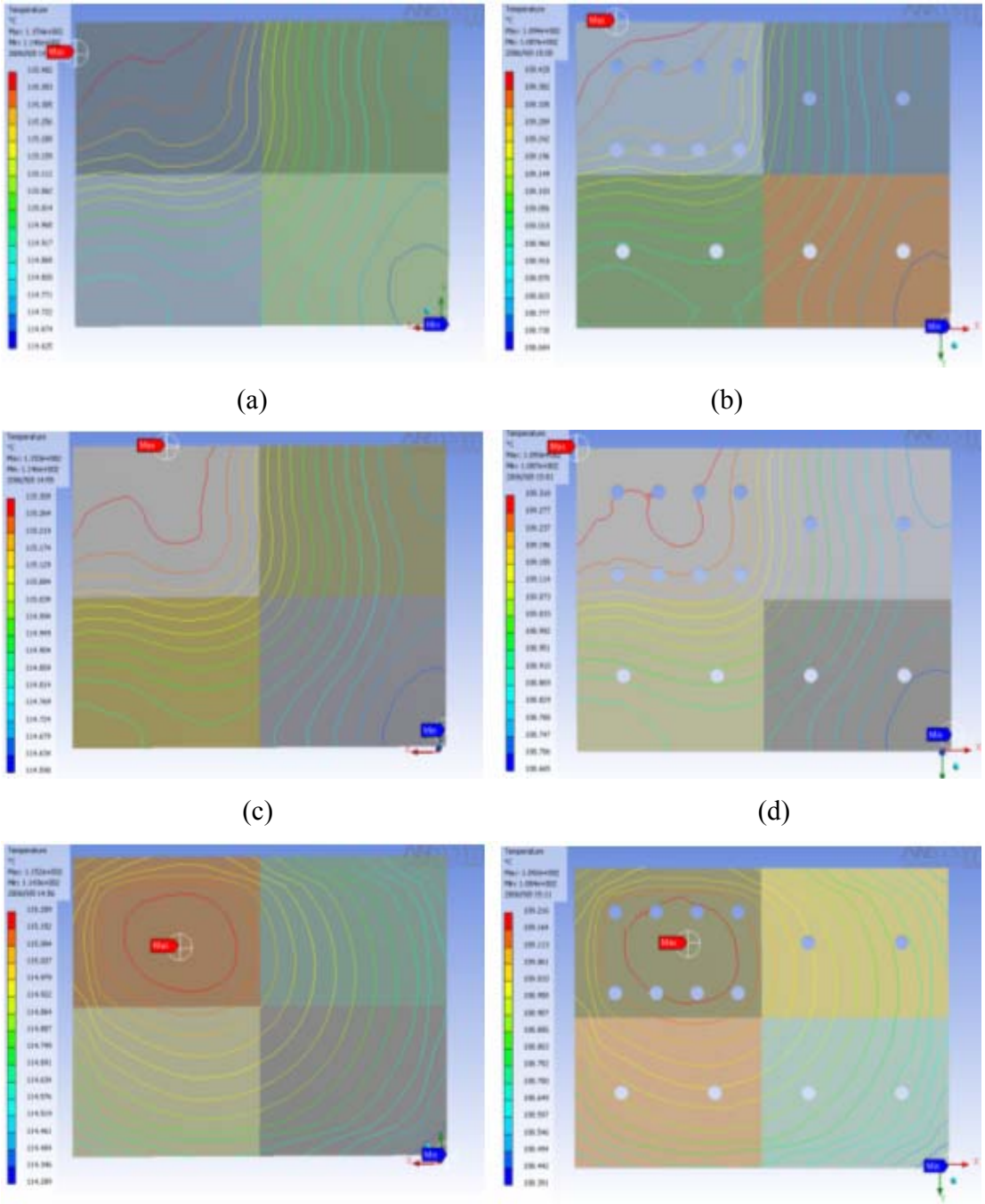
(a) (b)

Figure 5.7 Max junction temperatures die stacking: (a) spacer die; (b) pyramid die

Table 5.4 Maximum junction temperature 2x2 die applied on non-uniform power

	Spacer die	Pyramid die
No vias	115.402 ºC	115.325 ºC
with vias	109.428 ºC	109.154 ºC

When the higher power was applied on top left die the heat travels the path from the top die to bottom die. Figure 5.8 show that in the top die the isolines are scattered in the top left portion and in the bottom die the isolines concentrates on the top left segment. Where there are thermal vias, the temperature isolines show almost the same characters as without vias. But junction temperature is more decreased. At the die partition where 0.15W power applied on placed the temperature gradient lines are hot when compared to the other die partitions. Especially in the bottom die figure the lines are closely packed in the top left die leaving the remaining areas cooler than the die with 8 vias.

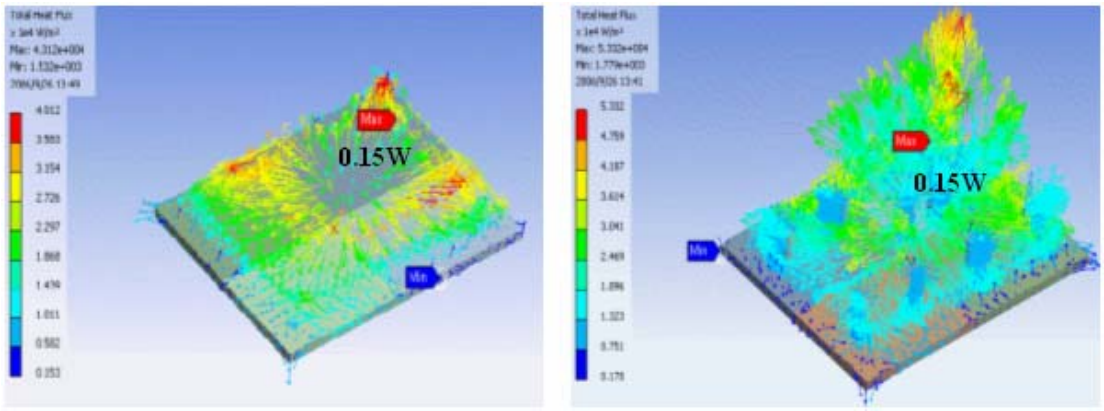


(a) (b)

(c) (d)

(e) (f)

Figure 5.8 Distribution of temperature with and without vias in 2x2 non-uniform power: (a) Top die without vias; (b) Top die with vias; (c) Mid die without vias; (d) Mid die with vias; (e) Bottom die without vias; (f) Bottom die with vias



(a) (b)

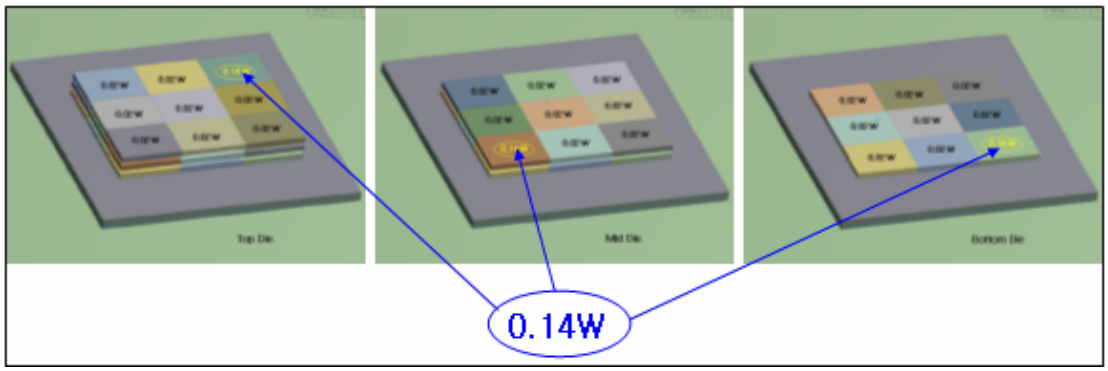
Figure 5.9 Heat flux arrow in 2x2 Spacer Die: (a) no vias; (b) with via

The flipped figure of the heat flux simulation model shows that there is maximum heat flow occurring at the area where more i.e. 8 vias are placed which explains that even in the non-uniform power distribution thermal vias plays a significant role in driving most of the heat away from the die or the hot spot area. The geometry and simulation limitations restrict us to place only 8 vias in the maximum power location which still could help in reducing the junction temperature both in uniform and non-uniform power distribution conditions. Figure 5.9 explain most of the heat developed is dissipated out from the thermal vias location where the max vias are placed. When there is no vias the heat flows through the die. With the vias placed most of the heat flows through the vias.

5.3.2 3X3 Non-uniform power supply

In case, the high power is applied at different location to spread the power on all directions of the 3 dies. The 3x3 structure of die geometry was applied by non-uniform power. Figure 5.10 shows that on the top die high power was applied on top right part,

on the mid die high power applied on bottom left portion and lastly on the bottom die high power was applied on bottom right part. And then, remaining 24 dies portions applied a power of 0.02W which makes the total power as 0.3W on each die. This procedure repeated when vias were used.



(a) (b) (c)

Figure 5.10 Die stacking configurations: (a) Top die; (b) Mid. die; (c) Bottom die

In the figure 5.11, the isolines show maximum temperature on the die portion where high power is applied. As the heat goes downward the bottom dies right most portions shows the hot spot area. The temperature i.e. 117 ºC is more than that of no-vias uniform because power is spread on all sides of the three dies.

Table 5.5 Maximum junction temperature 3x3 die applied on non-uniform power

	Uniform Power	Non-Uniform Power
No vias	116.2 ºC	117.4 ºC
with vias	111.7 ºC	109.9 ºC

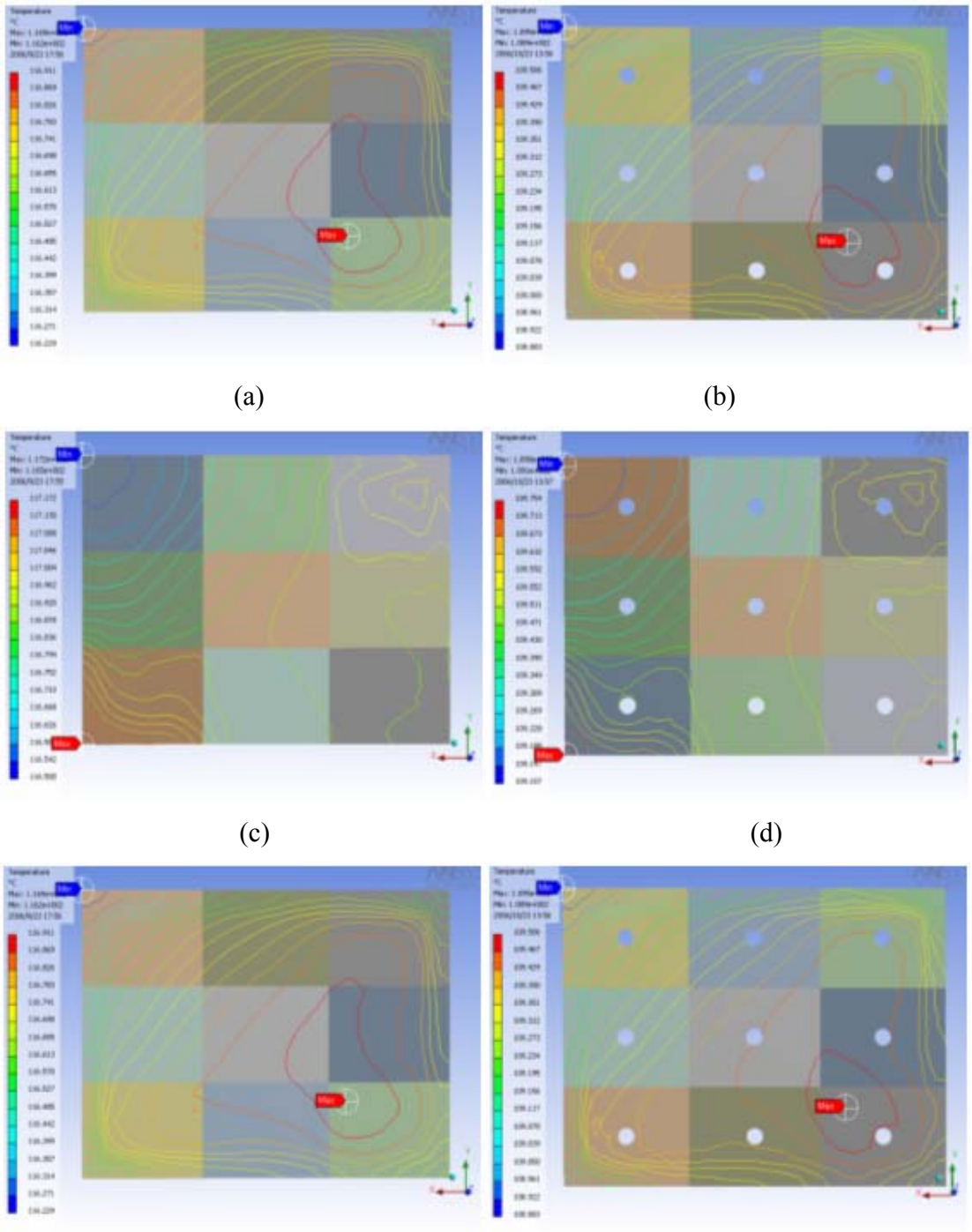


Figure 5.11 Distribution of temperature with and without vias in 3x3 non-uniform power: (a) Top die without vias; (b) Top die with vias; (c) Mid die without vias; (d) Mid die with vias; (e) Bottom die without vias; (f) Bottom die with vias

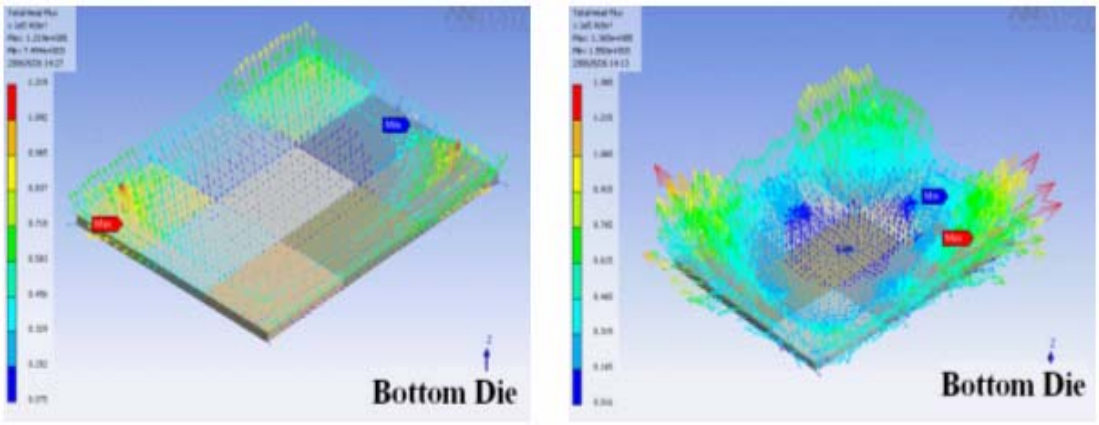


Figure 5.12 Heat flux arrows in 3x3 spacer die: (a) without vias (b) with vias

Table 5.6 Result of heat flux

	Top die	Mid die	Bottom die
No vias	10.31 W/cm²	11.26 W/cm²	12.19 W/cm²
With vias	11.15 W/cm²	11.60 W/cm²	13.65 W/cm²

Table 5.6 shows result of heat flux. The heat flux of the 3x3 model of the die without thermal vias is less than the heat flux with vias. The reason for this being, with vias, most of the heat finds definite path to dissipate. Compare bottom die maximum heat flux from figure 5.13 and table 5.6 is higher with vias than without vias.

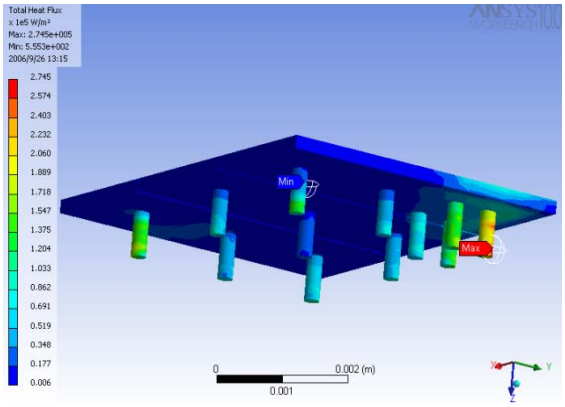


Figure 5.13 Heat flux in die and thermal vias

5.4 Conclusion & Summary

An efficient thermal via placed on the top of the die decreased the junction temperature of the package from 116ºc to 110ºc which is quite considerable. In this paper elaborate study has been done in analyzing the effect of thermal vias on the die and ways to bring down the junction temperature by reduce count.

Thermal enhancement has been achieved by running the thermal simulation with and without thermal vias. Temperature profiles of the entire stacked die geometry has been plotted in Ansys Workbench. The thermal enhancement study done in this paper focuses on the importance of thermal vias to a great extent.

Future study will focus on improved thermal conductivity via new material. In addition, the effect of using thermal vias to control non-uniformly powered devices will also be included. The vias will serve not just as effective thermal path but as a means of minimizing the ΔT on the die. The simulation models will be validated with experiments. The experimental work will be done in collaboration with industry. The simulation models are validated with measurements and found that simulation results agree with measurement results within 10 % accuracy. The printed circuit board substrate of the PBGA allows degrees of design flexibility in the form of features like the thermal vias, thermal bumps, and heat spreader planes within the substrate. These features when tied effectively to the motherboard planes allow superior thermal performance.

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BIOGRAPHICAL INFORMATION

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