THE SELF-HEATING EFFECTS OF BIPOLAR JUCTION TRANSISTORS ON THE FUNCTIONALITY OF A CURRENT FEEDBACK AMPLIFIER

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ABSTRACT

THE SELF-HEATING EFFECTS OF BIPOLAR JUCTION TRANSISTORS
ON THE FUNCTIONALITY OF A CURRENT FEEDBACK AMPLIFIER

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Self-heating effects strongly affect the performance of modern silicon-on-insulator (SOI) bipolar junction transistors. This research work does an extensive analysis of self-heating effects on large-signal behavior, small-signal behavior and transient operation of bipolar junction transistors. The two mechanisms in which device temperature affects large-signal behavior of a BJT transistor are investigated, i.e. the common-emitter (CE) configuration is to be driven by a constant base-emitter voltage and a constant base current. It is shown that the output characteristic of a BJT transistor is less sensitive to self-heating under a fixed base current than a fixed base-emitter voltage. A simple method of extracting the thermal resistance and the Early voltage is proposed. Self-heating effects on the BJT small-signal behavior are examined by investigating the two-port network parameters. It is shown that the gain of an amplifier and the output impedance of a current mirror can be affected significantly by self-heating effects. The mechanism of self-heating in transient operation is investigated and the transient operation of a high speed voltage buffer is analyzed. A method for estimating the thermal tail of a voltage buffer is presented.

An approach to analyze the contribution of each transistor to the overall thermal tail of current feedback operational amplifiers is presented. It is shown that the overall thermal tail of a

current feedback operational amplifier (CFOA) is a linear superposition of each individual transistor. Techniques to minimize the thermal tail are proposed. A cascode bootstrapped CFOA is designed and optimized to minimize the thermal tail. The overall thermal tail is reduced to 9 μV/V compared with 1032 μV/V of a classical CFOA when driving a 2 kΩ load in a unity gain feedback configuration. Also the common mode rejection ratio (CMRR) is greatly improved to 92 dB compared with 60 dB of the classical CFOA.

The Vertical Bipolar Inter Company (VBIC) model is used for all the simulations. Simulations are performed using Cadence and Advanced Design System (ADS).

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CHAPTER 1

INTRODUCTION AND ORGANIAZTION

Silicon-on-insulator (SOI) technology used in today's applications has many advantages over conventional bulk silicon, such as increased speed and simpler fabrication processes [1]. SOI-based devices differ from conventional silicon built devices in that silicon junction is above an electrical insulator, which is typically silicon dioxide. The dielectrically isolated process allows the creation of NPN and PNP transistors with highly complementary characteristics, yet isolated from each other by insulator sidewalls [2]. It also gives low parasitic capacitance because of full isolation and no P-N junction between the collectors and substrate or well. However, due to poor heat conductivity of silicon dioxide, the use of a buried silicon dioxide layer causes larger thermal spreading impedance which leads to more heat retention. This in turn increases the operating temperature of the device and thus affects circuit behavior. The thermal effect induced by the thermal spreading impedance is called the self-heating effect. The self-heating effect is typically restricted to the heat generated by the device itself. Self-heating effects can be significant for SOI-based bipolar junction transistors (BJTs) since the BJT performance is strongly temperature dependent.

The self-heating effect on large-signal behavior, small-signal behavior and transient operation of a bipolar junction transistor has been studied through analytical formulations and simulations in this research work. A simple method of extracting thermal resistance and the Early voltage has been developed based on the self-heating effects on large-signal behavior of a BJT. Self-heating effects on the fundamental blocks of current feedback operational amplifiers such as current mirror and voltage buffer has been studied. Based on this, a cascode bootstrapped circuit topology is proposed to minimize the self-heating effect.

Chapter 2 introduces the SPICE Gummel-Poon (SGP) model and the Vertical Bipolar Inter-Company (VBIC) model and conversions between these two models. Also the physics based SGP and VBIC model used in this research work is introduced.

Chapter 3 provides an overview of current feedback operational amplifiers (CFOAs). It presents the classical circuit topology of the CFOA, and the advantages and disadvantages of CFOAs. Important operational amplifier parameters such as Input offset voltage, input bias current, input noise, common mode rejection ratio, power supply rejection ratio, and common mode input range are discussed in this chapter.

Chapter 4 provides an approach to model the self-heating effect on large-signal behavior of BJT transistor. The two mechanisms in which device temperature affects large-signal behavior of BJT transistor are discussed, i.e. common-emitter (CE) configuration is to be driven by a constant base-emitter voltage and a constant base current. Also a simple method of extracting the thermal resistance and the Early voltage is presented.

Chapter 5 presents the BJT small-signal model with self-heating effects. Self-heating effects on BJT small-signal behavior are examined by investigating the two-port network parameters. Self-heating effects on the output impedance of a current mirror are the primary focus. Techniques to reduce self-heating effects are also discussed.

Chapter 6 provides an approach to model the self-heating effect in the transient operation of a transistor. The effect of self-heating on transient operation in the high speed voltage buffer is analyzed here.

Chapter 7 presents an approach to analyze the contribution of each transistor in an operational amplifier to the overall thermal tail of current feedback amplifiers. Various design techniques are suggested to develop self-heating tolerant CFOAs. A cascode bootstrapped CFOA is proposed that minimize the self-heating effect.

Chapter 8 presents the summary of the accomplishments and the suggestions for future work.

CHAPTER 2

The SPICE GUMMEL-POON AND VERTICAL BIPOLAR INTER-COMPNAY MODEL

The dielectrically isolated process allows the creation of NPN and PNP transistors with highly complementary characteristics, and isolated from each other by insulator sidewalls. It also gives low parasitic capacitance because of full isolation and no P-N junction between the collectors and substrate or well. Dielectrically isolated bipolar junction transistors can be used to design class AB output stages with very low quiescent current and high output drive in the analog circuits used in wired broadband applications [2]. However, because of the use of a buried oxide layer, it has large thermal resistance which causes heat retention which in turn leads to circuit behavior. To accurately predict and simulate circuit behavior, an accurate model is needed. While the widely used SPICE Gummel-Poon (SGP) model does not support the self-heating effect, the improved Vertical Bipolar Inter-Company model (VBIC) does. This chapter introduces the SGP model, VBIC model and conversions between these two models.

2.1 SPICE Gummel-Poon (SGP) model

The SPICE Gummel-Poon (SGP) model had been the industry standard bipolar transistor model for more than 20 years before the VBIC model was developed by McAndrew's group in 1995 [3]-[5]. The SGP model shown in figure 2.1 was an improvement to the Ebers-Moll model by modeling such second-order effects as the low-current effect (low-current drop in β), the base-width modulation and the high-level injection [5]. To improve low current effect modeling, two non-ideal diodes, D_{SE} and D_{SC}, are added to the Ebers-Moll model to represent the base-emitter and base-collector recombination effect respectively. The normalized majority base charge, q_b, is introduced to model the base-width modulation effect and high-level injection effect.

2.1.1 The Equivalent Circuit of the SGP Model and Related Parameters

Figure 2.1 shows the equivalent circuit of the SGP static model for the NPN bipolar transistor [3]. It contains three nodes, i.e. Base (B), Emitter (E) and Collector (C). The depletion capacitances, C_{je} and C_{jc}, model the incremental fixed charges Q_{je} and Q_{jc} stored in the base-emitter and base-collector junction depletion regions for incremental changes in the associated junction voltage respectively. The diffusion capacitances, C_{bc} and C_{be}, model the diffusion charges associated with the mobile carrier in the BJT. The three parasitic resistances, R_b, R_e and R_c, model the parasitic resistances at the base, emitter and collector respectively. Note R_b is a current dependent resistance modulated by the normalized base charge, q_b. The capacitance, Cjcx, is used to model the distributed base-collector capacitance.

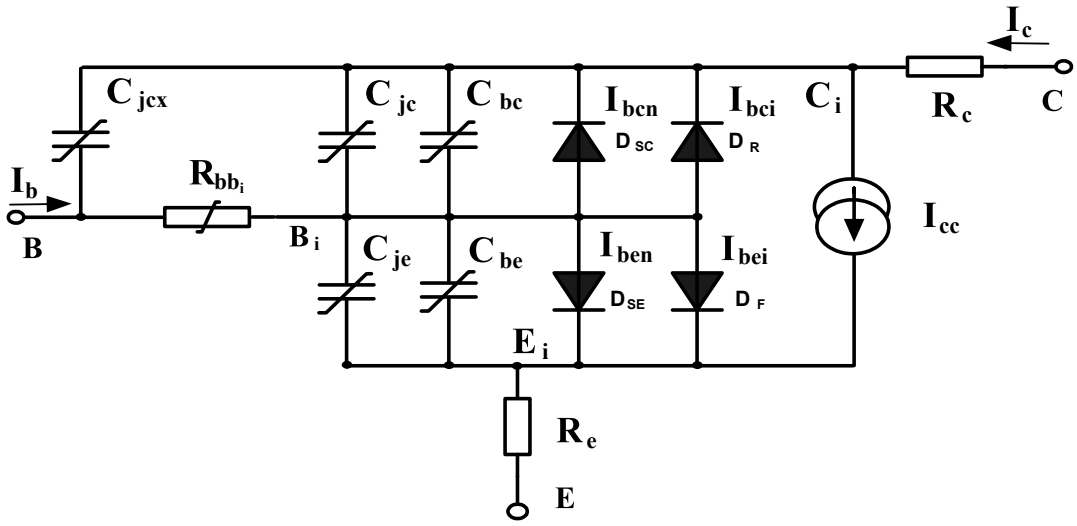

Figure 2.1 Equivalent circuit of SGP static model [3].

2.1.2 The SGP Model Formulation

2.1.2.1 The Collector and Base Currents of the SGP Model

The base current formulation considers the base-emitter and base-collector recombination effect in the low-current region. Thus it has four components, i.e. the ideal forward base-emitter diffusion current which flows through the diode, D_F, and has a saturation current, $I_{bei}=I_S/\beta_F$; the ideal reverse base-collector diffusion current which flows through the

diode, D_R, and has a saturation current, $I_{bci}= I_S/\beta_R$; the non-ideal base-emitter recombination current which flows through the diode, D_{SE}, and has a saturation current, $I_{ben}=I_{SE}$; the non-ideal base-collector recombination current which flows through the diode, D_{SC}, and has a saturation current, $I_{bcn}=I_{SC}$. It can be formulated as [11]

$$\begin{aligned} I_b = & \frac{I_S}{\beta_F}\left[\exp\left(\frac{V_{BE}}{N_F V_T}\right)-1\right] + I_{SE}\left[\exp\left(\frac{V_{BE}}{N_E V_T}\right)-1\right] \\ & + \frac{I_S}{\beta_R}\left[\exp\left(\frac{V_{BC}}{N_R V_T}\right)-1\right] + I_{SC}\left[\exp\left(\frac{V_{BC}}{N_C V_T}\right)-1\right] \end{aligned} \tag{2.1}$$

where I_S, I_{SE}, I_{SC} denote the transport saturation current, base-emitter leakage saturation current, base-collector leakage saturation current respectively, N_F, N_E, N_R and N_C are ideality factors, and β_F , β_R are the forward and reverse current gain.

The collector current has three components, i.e. the single current source, I_{cc}, between the collector and the emitter, which is a combination of the ideal forward diffusion current and the ideal reverse diffusion current; the ideal reverse base-collector diffusion current which flows through the diode, D_R; the non-ideal base-collector recombination current which flows through the diode, D_{SC}. It is formulated as [11]

$$\begin{aligned} I_c = & \frac{I_S}{q_b}\left\{\left[\exp\left(\frac{V_{BE}}{N_F V_T}\right)-1\right]-\left[\exp\left(\frac{V_{BC}}{N_R V_T}\right)-1\right]\right\} \\ & - \frac{I_S}{\beta_R}\left[\exp\left(\frac{V_{BC}}{N_R V_T}\right)-1\right] - I_{SC}\left[\exp\left(\frac{V_{BC}}{N_C V_T}\right)-1\right] \end{aligned} . \tag{2.2}$$

The charge, q_b, denotes the normalized base charge in equation (2.2) and is [11]

$$q_b = \frac{q_1}{2}(1+\sqrt{1+4q_2}), \tag{2.3}$$

$$q_1 = \frac{1}{1-\frac{V_{BE}}{V_{AF}}-\frac{V_{BC}}{V_{AR}}}, \tag{2.4}$$

$$q_2 = \frac{I_S}{I_{KF}}\left[\exp\left(\frac{V_{BE}}{N_F V_T}\right)-1\right]+\frac{I_S}{I_{KR}}\left[\exp\left(\frac{V_{BC}}{N_R V_T}\right)-1\right]. \tag{2.5}$$

The variables, V_{AF}, V_{AR}, I_{KF} and I_{KR}, are the forward Early voltage, the reverse Early voltage, the forward high-level injection knee current and the similar reverse current respectively. Note that q_1 models the effects of base-width modulation and q_2 models the effect of high-level injection.

2.1.2.2 Current Dependence of the Base Resistance

The base resistance consists of the external base resistance (R_b) and the intrinsic base resistance (R_{bm}). The external base resistance includes the contact resistance and sheet resistance. The intrinsic base resistance is a function of base current. The current dependence of this resistance comes from nonzero base region resistivity, which in turn precipitates non-uniform biasing of the base-emitter junction.

The total base resistance is [11]

$$R_{bb_i} = R_{bm} + 3\cdot\left(R_b - R_{bm}\right)\cdot\frac{\tan(z)-z}{z\cdot\tan^2(z)}, \tag{2.6}$$

$$z = \frac{-1+\sqrt{1+144 I_b/\pi^2 I_{rB}}}{\left(24/\pi^2\right)\sqrt{I_b/I_{rB}}}. \tag{2.7}$$

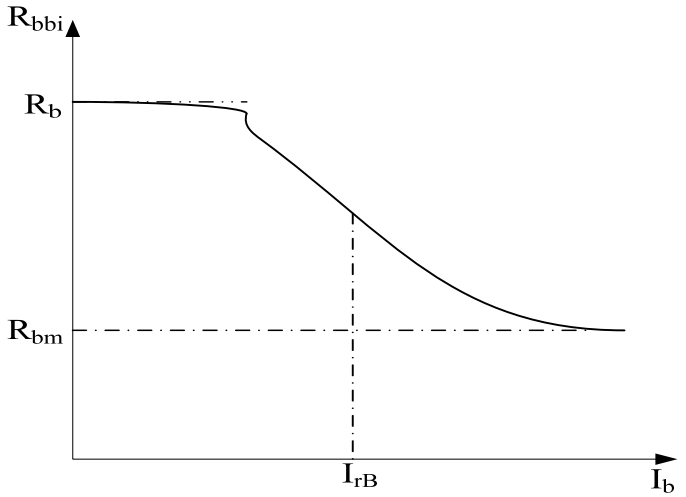

Figure 2.2 The variation of the total base resistance with base current

Figure 2.2 shows the typical curve of the variation of the total base resistance with the base current. The variable R_{bm} is the minimum base resistance that occurs at high currents, R_b is the base resistance at zero bias (small base currents), I_{rB} is the current where the base resistance falls halfway to its minimum value.

2.1.2.3 Temperature Mappings of the SGP Model

BJT electrical behavior varies with temperature, so the SGP model defines the temperature dependence for its model parameters. The saturation current depends on the intrinsic carrier concentration and the diffusion coefficient of electrons and holes. Temperature appears explicitly in the exponential terms of the equations of both the intrinsic carrier concentration and the diffusion coefficient. The temperature dependence of the transport saturation current is determined by [11]

$$I_S(T_2) = I_S(T_1)\left(\frac{T_2}{T_1}\right)^{XTI} \exp\left[-\frac{qE_g(300)}{kT_2}\left(1-\frac{T_2}{T_1}\right)\right]. \tag{2.8}$$

The variables, XTI and E_g, are the saturation current temperature exponent and the energy gap.

The effect of temperature on forward and reverse current gain is determined by [11]

$$\begin{aligned}\beta_F(T_2) &= \beta_F(T_1)\left(\frac{T_2}{T_1}\right)^{XTB} \\ \beta_R(T_2) &= \beta_R(T_1)\left(\frac{T_2}{T_1}\right)^{XTB}\end{aligned}. \tag{2.9}$$

The temperature dependence of the junction built-in potential, ϕ_J , is modeled as follows: [11]

$$\phi_J(T_2) = \frac{T_2}{T_1}\phi_J(T_1) - 3\frac{kT_2}{q}\ln\left(\frac{T_2}{T_1}\right) - \left[\frac{T_2}{T_1}E_g(T_1) - E_g(T_2)\right]. \tag{2.10}$$

2.2 Vertical Bipolar Inter-Company (VBIC) Model

The SPICE Gummel-Poon (SGP) model had been the industry standard for circuit simulation for over 20 years. However, the SGP model has some shortcomings, e.g. it is unable to model collector resistance modulation (quasi-saturation) and parasitic substrate transistor action. Improved BJT models have been presented over the years [6]-[7]. In 1995 a group of representatives from the IC and CAD industries defined the VBIC model to replace the SGP model. The complete source code for the VBIC model is accessible to the public. It was made to be as similar to the SGP model as possible.

2.2.1 The Equivalent Circuit of the VBIC Model and Related Parameters

Figure 2.3 shows the equivalent circuit for the VBIC model [3]. It contains five nodes, i.e. Base (B), Emitter (E), Collector (C), Substrate (S) and a temperature rise node that models self-heating (dT). The VBIC model includes a NPN transistor modeled by a complete Gummel-Poon model and a parasitic substrate PNP transistor modeled by a simplified Gummel-Poon model. A weak avalanche current I_{gc} is included for the base-collector junction. Quasi-saturation is modeled with the elements R_{ci}, C_{bcx}, and C_{bcq} [4]. The constant capacitance, C_{BEO} and C_{BCO}, are included to model capacitances associated with extrinsic base-emitter and base-collector overlap capacitance respectively. The intrinsic base resistance and parasitic base resistance, R_{bi}, and R_{bip}, are modulated by the normalized base charges, q_b and q_{bp}. The intrinsic collector resistance, R_{ci}, is modulated by V_{bci}. Two additional sub-circuits are included to model excess phase effect and self-heating effect. The excess phase effect is modeled by a second-order RLC network. Self-heating is modeled by the thermal power source I_{th} and a RC thermal network which includes the thermal resistance R_{th} and capacitance C_{th}. The thermal power source I_{th} couples the power generated in the transistor to the thermal network. The local temperature rise at node dT is linked to the electrical model through the temperature mappings of the model parameters.

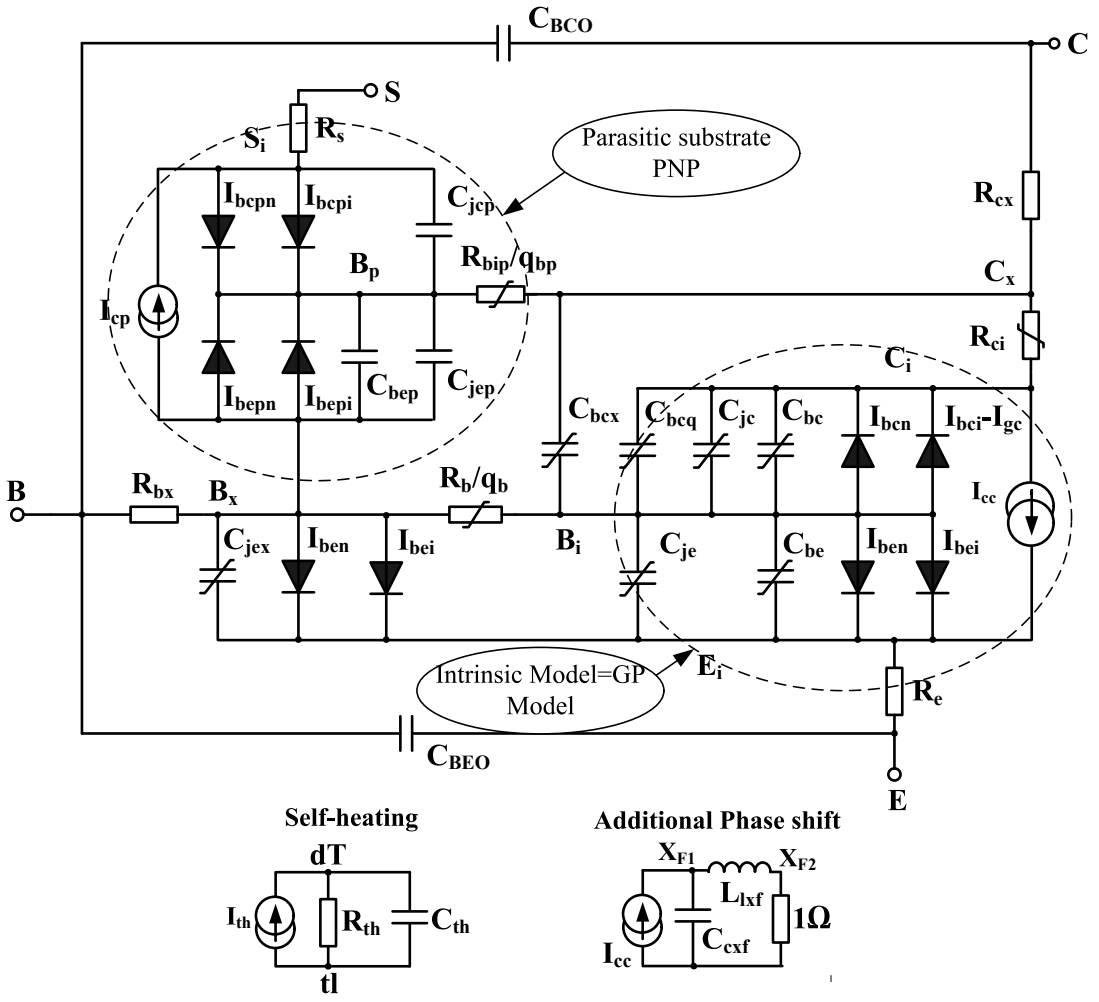

Figure 2.3 Equivalent circuit of VBIC Model [3].

Overall the VBIC model improves the deficiencies of the Gummel-Poon model in the following aspects [5]: the Early effect modeling, parasitic substrate PNP modeling, quasi-saturation modeling, weak avalanche modeling, constant parasitic overlap capacitance modeling, excess phase modeling, temperature dependency modeling and self-heating modeling.

Table 2.1 lists each parameter of the VBIC model and gives a short description of the function of the parameter.

Table 2.1 VBIC Model parameters and physical definition [12]

VBIC Parameters	Definition
	Main Collector Current Source
IS	Transport saturation current
NF	Forward emission coefficient
NR	Reverse emission coefficient
	Early Effect Modeling
VEF	Forward Early Voltage (0=infinity)
VER	Reverse Early Voltage (0=infinity)
	Webster Effect
IKF	Forward knee current
IKR	Reverse knee current
	Forward Base Current
IBEI	Ideal base-emitter saturation current
NEI	Ideal base-emitter emission coefficient
IBEN	Non-ideal base-emitter saturation current
NEN	Non-ideal base-emitter emission coefficient
WBE	Portion of I_{BEI} from V_{BEI}, 1-W_{BE} from V_{BEX}
	Reverse Base Current
IBCI	Ideal base-collector saturation current
NCI	Ideal base-collector emission coefficient
IBCN	Non-ideal base-collector saturation current
NCN	Non-ideal base-collector emission coefficient
	Weak Avalanche Current
AVC1	Base-collector weak avalanche parameter 1
AVC2	Base-collector weak avalanche parameter 2
	Parasitic Resistance
RE	Emitter resistance
RBX	Extrinsic base resistance
RBI	Intrinsic base resistance
RS	Substrate resistance
RBP	Parasitic base resistance
RCX	Extrinsic collector resistance
	Quasi Saturation
RCI	Intrinsic collector resistance
GAMM	Epi doping parameter
VO	Epi drift saturation voltage
HRCF	High current RC factor
QCO	Collector charge at zero bias
	Space Charge Capacitance
CJE	Base-emitter zero-bias junction capacitance
PE	Base-emitter grading coefficient
ME	Base-emitter junction exponent
AJE	Base-emitter capacitance smoothing factor
CJC	Base-collector zero-bias junction capacitance
PC	Base-collector grading coefficient
MC	Base-collector junction exponent
AJC	Base-collector capacitance smoothing factor

Table 2.1 – *Continued*

CJEP	Base-emitter extrinsic zero-bias junction capacitance
CJCP	Base-collector extrinsic zero-bias junction capacitance
PS	Collector-substrate grading coefficient
MS	Collector-substrate junction exponent
AJS	Collector-substrate capacitance smoothing factor
FC	Forward bias junction capacitance threshold
	Transit Time Modeling
TF	Forward transit time
XTF	Coefficient of TF bias dependence
ITF	Coefficient of TF dependence on I_{CC}
VTF	Coefficient of TF dependence on V_{BC}
QTF	Variation of TF with base-width modulation
TR	Ideal reverse transit time
	Excess Phase
TD	Forward excess-phase delay time
	Parasitic Capacitance
CBEO	Extrinsic base-emitter overlap capacitance
CBCO	Extrinsic base-collector overlap capacitance
	Parasitic Substrate Transistor
ISP	Parasitic transport saturation current
NFP	Parasitic forward emission coefficient
WSP	Portion of I_{CCP} from V_{BEP}, 1-W_{SP} from V_{BCI}
IBEIP	Ideal parasitic base-emitter saturation current
IBENP	Non-ideal parasitic base-emitter saturation current
IBCIP	Ideal parasitic base-collector saturation current
NCIP	Ideal parasitic base-collector emission coefficient
IKP	Parasitic current (0=infinity)
	Temperature Mapping
CTH	Thermal capacitance
RTH	Thermal resistance
TNOM	Nominal ambient temperature for characterizing
EA	Activation energy for I_S
EAIE	Activation energy for I_{BEI}
EAIC	Activation energy for I_{BCI}/$_{IBEIP}$
EAIS	Activation energy for I_{BCIP}
EANE	Activation energy for I_{BEN}
EANC	Activation energy for I_{BCN}/I_{BENP}
EANS	Activation energy for I_{BCNP}
XRE	Temperature exponent of emitter resistance
XRC	Temperature exponent of collector resistance
XRB	Temperature exponent of base resistance
XRS	Temperature exponent of substrate resistance
XVO	Temperature exponent of V_O
XIS	Temperature exponent of I_S
XII	Temperature exponent of I_{BEI}/I_{BCI}/I_{BEIP}/I_{BCIP}
XIN	Temperature exponent of I_{BEN}/I_{BCN}/I_{BENP}/I_{BCNP}
TNF	Temperature exponent of N_F
TAVC	Temperature exponent of A_{VC}
	Noise Modeling
KFN	Flicker noise coefficient

Table 2.1 – *Continued*

AFN	Flicker noise exponent
BFN	Flicker noise frequency exponent

2.2.2 The VBIC Model Formulation

2.2.2.1 Collector current and base current of VBIC model

The core of the VBIC model is the transport current model, which is similar to the SGP model. The collector transport current is related to the forward transport current (I_{tf}) and the reverse transport current (I_{tr}) and determined by [5]

$$\begin{aligned} I_{cc} &= (I_{tf} - I_{tr})/q_b \\ I_{tf} &= I_S\left(\exp\left(qV_{bei}/N_F kT\right)-1\right). \\ I_{tr} &= I_S\left(\exp\left(qV_{bci}/N_R kT\right)-1\right) \end{aligned} \tag{2.11}$$

The variables, V_{bei} and V_{bci}, are the voltage difference between node B_i and E_i and the voltage difference between node B_i and C_i in figure 2.3. Non-ideal factors N_F and N_R are included for forward and reverse components of I_{cc}, for compatibility with the SGP model.

The collector transport current of the VBIC model has the same form as the SGP model, but the normalized base charge, q_b, is modeled differently. For the VBIC model, the normalized base charge includes depletion and diffusion components. The normalized base charge is [5]

$$q_b = q_1 + \frac{q_2}{q_b}, \tag{2.12-a}$$

where

$$\begin{aligned} q_1 &= 1 + \frac{q_{je}}{V_{ER}} + \frac{q_{jc}}{V_{EF}} \\ q_2 &= \frac{I_S}{I_{KF}}\left[\exp\left(\frac{qV_{bei}}{N_F kT}\right)-1\right] + \frac{I_S}{I_{KR}}\left[\exp\left(\frac{qV_{bci}}{N_R kT}\right)-1\right] \end{aligned}. \tag{2.12-b}$$

The variables, V_{EF} and V_{ER}, are the forward and reverse Early voltage, while I_{KF} and I_{KR} are the forward and reverse knee currents. The Early voltage components model the base-width modulation effect and the knee current components model the high-level injection effect. The normalized base-emitter and base-collector depletion charges are [5]

$$q_{je} = q_j\left(V_{bei}, P_E, M_E, F_C, A_{JE}\right),$$
$$q_{jc} = q_j\left(V_{bci}, P_C, M_C, F_C, A_{JC}\right). \tag{2.13}$$

Here P_E, P_C and M_E, M_C are the built-in potentials and grading coefficients of the base-emitter and base–collector junctions respectively, while A_{JE} and A_{JC} are the capacitance smoothing factors of the base-emitter and base–collector junctions respectively. F_C is the forward bias junction capacitance threshold. The normalized depletion capacitance function for reverse and low forward bias is [5]

$$C_j(V,P,M,F_C,A) = \frac{\partial q_j(V,P,M,F_C,A)}{\partial V} \approx \frac{1}{(1-V/P)^M}. \tag{2.14}$$

If the depletion capacitance smoothing parameters A_{JE} and A_{JC} are less than zero, C_j limits its value to a constant for $V>F_CP$, otherwise C_j increases linearly just like the SGP model does in figure 2.4.

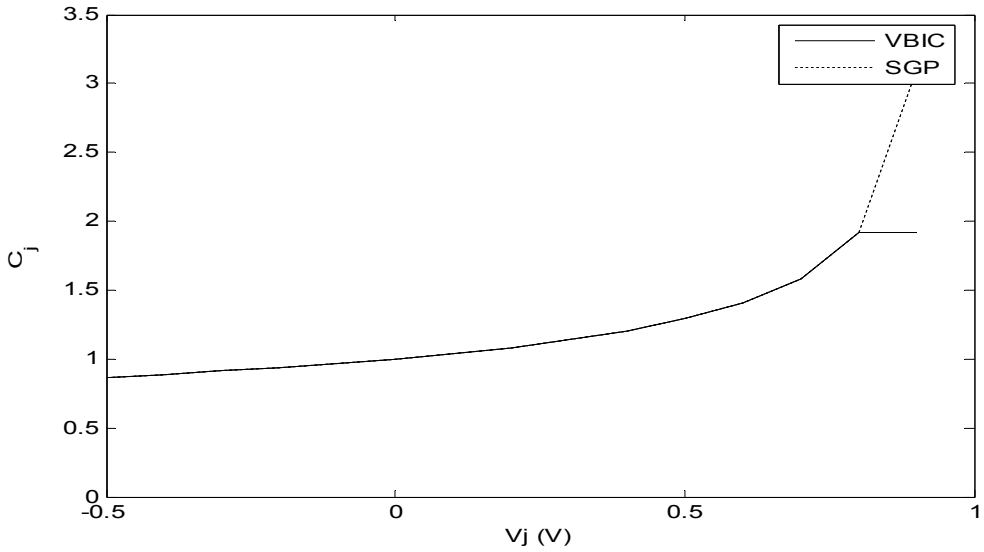

Figure 2.4 The variation of the normalized depletion capacitance with junction voltage [5].

Instead of linking base current and collector current by beta, the base current is modeled independently of the collector current in the VBIC model. The base current in the VBIC

model is also apportioned between the intrinsic and extrinsic components. The base-emitter component of the intrinsic transistor base current is modeled as [5]

$$I_{be} = W_{BE}\left(I_{bei}\left(\exp\left(qV_{bei}/N_{EI}kT\right)-1\right)+I_{ben}\left(\exp\left(qV_{bei}/N_{EN}kT\right)-1\right)\right). \quad (2.15)$$

Here I_{bei} and I_{ben} are ideal and non-ideal saturation currents, N_{EI} and N_{EN} are ideality factors. Usually N_{EI} is approximately equal to 1 and N_{EN} is approximately 2. The base-collector component is similarly modeled as [5]

$$I_{bc} = I_{bci}\left(\exp\left(qV_{bci}/N_{CI}kT\right)-1\right)+I_{bcn}\left(\exp\left(qV_{bci}/N_{CN}kT\right)-1\right). \quad (2.16)$$

The extrinsic base-emitter recombination current is determined by [5]

$$I_{bex} = \left(1-W_{BE}\right)\left(I_{bei}\left(\exp\left(qV_{bex}/N_{EI}kT\right)-1\right)+I_{ben}\left(\exp\left(qV_{bex}/N_{EN}kT\right)-1\right)\right). \quad (2.17)$$

The weak avalanche current, I_{gc}, is modeled as [7]

$$I_{gc} = \left(I_{cc}-I_{bc}\right)A_{VC1}\left(P_C-V_{bci}\right)\exp-\left(A_{VC2}\left(P_C-V_{bci}\right)^{ME-1}\right). \quad (2.18)$$

2.2.2.2 Quasi-Saturation

One of the major shortcomings of the SGP model is that it does not support quasi-saturation modeling. The VBIC model modifies the Kull-Nagel model [5] to avoid the negative output conductance problem at high V_{BE}. The VBIC model also includes an empirical model for modeling the increase of collector current at high V_{bci}. The intrinsic collector resistance, R_{ci}, is used to model quasi-saturation. The VBIC model gives the current in the modulated R_{ci} as [5]

$$I_{rci} = \frac{I_{epi0}}{\sqrt{1+\left(I_{epi0}\cdot R_{ci}/V_O\cdot\left(1+\frac{0.5\sqrt{0.01+V_{rci}^2}}{V_O\cdot HRCF}\right)\right)^2}}, \quad (2.19\text{-a})$$

where

$$I_{epi0} = \frac{1}{R_{ci}}\cdot\left(V_{rci}+V_{tv}\cdot\left(K_{bci}-K_{bcx}-\ln\frac{1+K_{bci}}{1+K_{bcx}}\right)\right)$$

$$K_{bci} = \sqrt{1+GAMM\cdot\exp\left(\frac{v_{bci}}{V_{tv}}\right)}, K_{bcx} = \sqrt{1+GAMM\cdot\exp\left(\frac{V_{bcx}}{V_{tv}}\right)}. \quad (2.19\text{-b})$$

Here V_{rci} = V_{bci} - V_{bcx} is the voltage across R_{ci}, HRCF is the high current R_C factor which accounts for the increase of collector current at high V_{bci}, GAMM is the collector doping factor parameter, and V_O is the epitaxial drift saturation voltage. Figure 2.5 shows how R_{ci} affects the output characteristics. It basically determines the slope of the saturated range. With the parameter GAMM, the effect of quasi-saturation is deferred to the higher currents as shown in figure 2.6. The epitaxial drift saturation voltage, V_O, determines the begin of velocity saturation. This means a smoothing at the high-end of the quasi-saturation as shown in figure 2.7 [12].

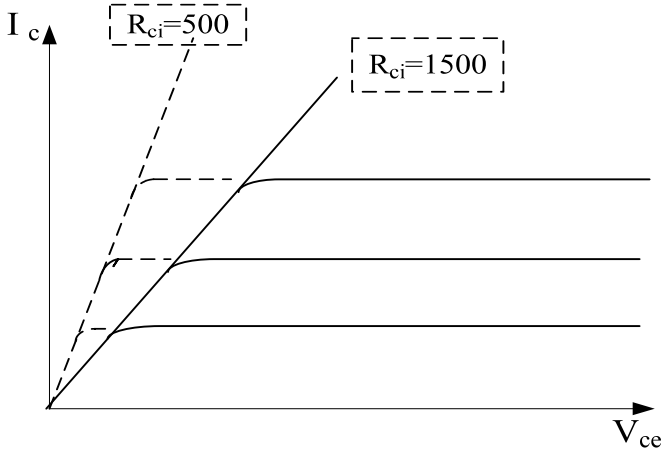

Figure 2.5 The effect of R_{ci} on quasi-saturation [12]

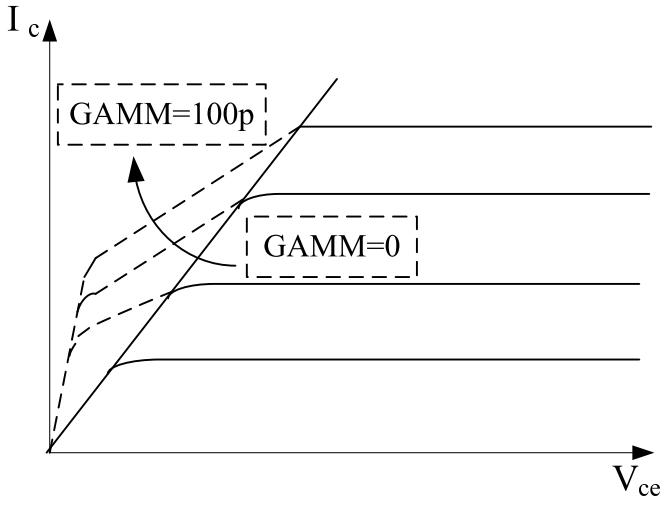

Figure 2.6 The effect of GAMM on quasi-saturation [12]

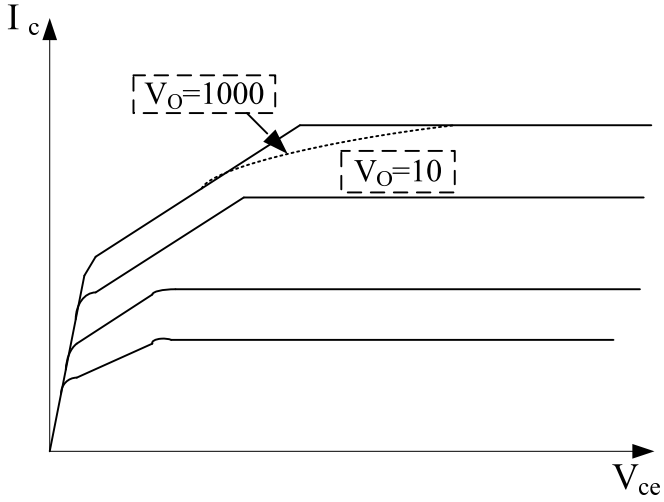

Figure 2.7 The effect of V_O on quasi-saturation [12]

2.2.2.3 Temperature Mappings of the VBIC Model

The temperature mappings of the VBIC model are similar to those of the SGP model. The temperature dependence of the transport saturation current is [5]

$$I_S(T) = I_S(T_{nom})\left(\frac{T}{T_{nom}}\right)^{XIS} \exp\left[-\frac{q \cdot EA}{kT}\left(1-\frac{T}{T_{nom}}\right)\right]^{1/N_F}. \tag{2.20}$$

Here XIS is the temperature exponent and EA is the activation energy.

Each saturation current has a separate temperature exponent and also an activation energy. The intrinsic base-emitter saturation current, I_{bei}, varies with temperature as [5]

$$I_{bei}(T) = I_{bei}(T_{nom})\left(\frac{T}{T_{nom}}\right)^{XII} \exp\left[-\frac{q \cdot EAIE}{kT_2}\left(1-\frac{T}{T_{nom}}\right)\right]^{1/N_{EI}}. \tag{2.21}$$

N_F, N_R and A_{VC1} are modeled as having linear temperature dependence [5], i.e.

$$N_F(T) = N_F(T_{nom}) + TNF \cdot (T - T_{nom}), \tag{2.22}$$

$$N_R(T) = N_R(T_{nom}) + TNF \cdot (T - T_{nom}), \tag{2.23}$$

$$A_{VC1}(T) = A_{VC1}(T_{nom}) + TNVC \cdot (T - T_{nom}). \tag{2.24}$$

The built-in potential P and zero bias junction capacitance C_j are modeled in a similar way as the SGP model, with a modification to avoid the built-in potential going negative for high temperature [9]. The built-in potential P varies with temperature as [13]

$$P(T) = \psi + \frac{2kT}{q}\ln\left(\frac{1+\sqrt{1+4\exp(-q\psi/kT)}}{2}\right), \tag{2.25}$$

where

$$\psi = \frac{2kT}{q}\ln\left(\exp\left(\frac{qP(T_{nom})}{2kT_{nom}}\right) - \exp\left(-\frac{qP(T_{nom})}{2kT_{nom}}\right)\right) - \frac{3kT}{q}\ln\left(\frac{T}{T_{nom}}\right) - EA\left(\frac{T}{T_{nom}} - 1\right). \tag{2.26}$$

The temperature dependence of the zero bias junction capacitance C_j is determined by [9]

$$C_j(T) = C_j(T_{nom})\left(\frac{P(T_{nom})}{P(T)}\right)^M. \tag{2.27}$$

The collector doping parameter, GAMM, is modeled over temperature as [6]

$$GAMM(T) = GAMM(T_{nom})\left(\frac{T}{T_{nom}}\right)^{XIS}\exp\left[-\frac{q\cdot EA}{kT}\left(1-\frac{T}{T_{nom}}\right)\right]^{1/N_F}. \tag{2.28}$$

The collector drift saturation voltage, V_O, is modeled over temperature as [5]

$$V_O(T) = V_O(T_{nom})\left(\frac{T}{T_{nom}}\right)^{XVO}. \tag{2.29}$$

2.3 Conversion of the SGP to the VBIC Model

The treatment of the Early effect is the major difference between the VBIC and SGP models. Thus most of the SGP model parameters can be converted to VBIC model parameters [3]. Table 2.2 lists simple mappings from SGP parameters to VBIC parameters as well as the empirical or optimized values used for the additional features in the VBIC model.

Table 2.2 Mappings from SGP parameters to VBIC parameters [3].

VBIC parameter	Mapping from SGP	VBIC parameter	Mapping from SGP	VBIC parameter	Mapping from SGP
IS	0.9*IS	NF	NF	NR	NR
RCI	RC*10	RCX	RC	RBX	RBM
RBI	RB-RBM	RE	RE	CJE	CJE
PE	VJE	ME	MJE	CJC	CJC*XCJC
CJEP	CJC(1-XCJC)	PC	VJC	MC	MJC
CJCP	CJS	PS	VJS	MS	MJS
IBEI	IS/BF	NEI	NE	IBCI	IS/BR
NCI	NR	IBCN	ISC	NCN	NC
IKF	IKF*0.9	IKR	IKR*0.9	TF	TF*0.25
XTF	XTF	VTF	VTF	ITF	ITF
TR	TR	TD	π*TF*PTF/180	EA	EG
EAIE	EG	EAIC	EG	EANE	EG
EANC	EG	XIS	XTI	XII	XTI-XTB
XIN	XTI-XTB	KFN	KF	AFN	AF
VEF	VAF*0.5	VER	VAR*0.5	WBE	1.0
AVC1	0.15	AVC2	20	GAMM	1E-10
VO	1.5	HRCF	33E-3	QCO	1E-9
AJE/AJC/AJS	-0.5	PC	0.9	QTF	0.3

2.4 Physics Based SGP and VBIC Model

The models developed by Kamal R. Sinha (in Appendix A) are used for analysis and simulation [10]. The procedure for obtaining the VBIC model parameters begins with the doping concentration of the emitter, base, collector and active emitter area. Then estimates of the SGP model parameters are done based on physics equations. The SGP model is converted to VBIC model with appropriate estimates [10].

Figure 2.8 shows the variation of an NPN transistor current gain with collector current. At low current, β_F decreases with collector current; at mid current, β_F is nearly constant; and at high current, β_F decreases because of high-level injection and the Kirk effect.

Figure 2.9 shows the variation of an NPN transistor transition frequency, f_T, with collector current. At low-current, the transition frequency decreases with I_C because of dominance of depletion capacitance. At mid-current, f_T reaches the peak, and f_T decreases at high-current also because of high-level injection and the Kirk effect.

Figure 2.10 and 2.11 illustrate how the current gain and transition frequency of a PNP transistor vary with collector current.

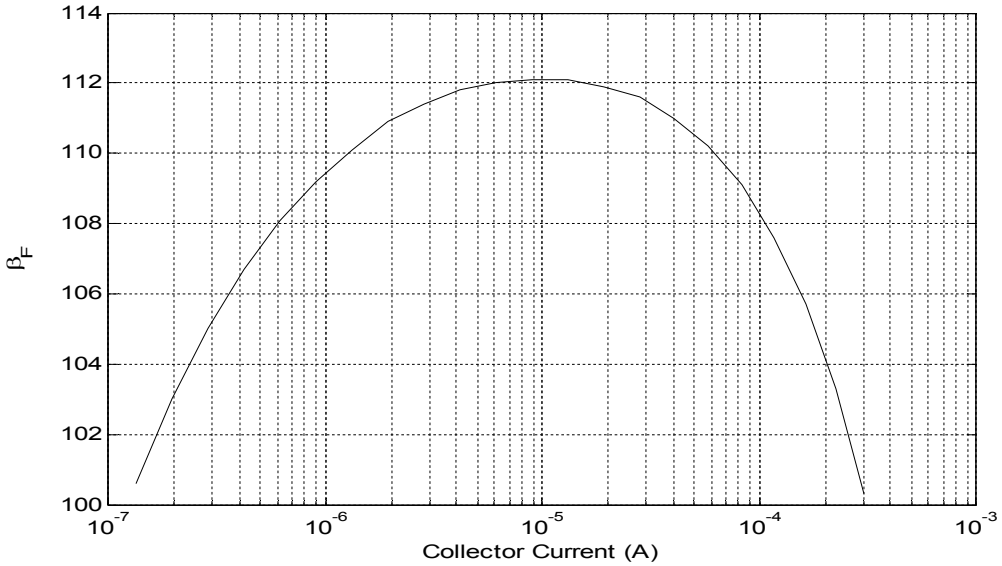

Figure 2.8 Current gain β_F versus I_C for an NPN transistor

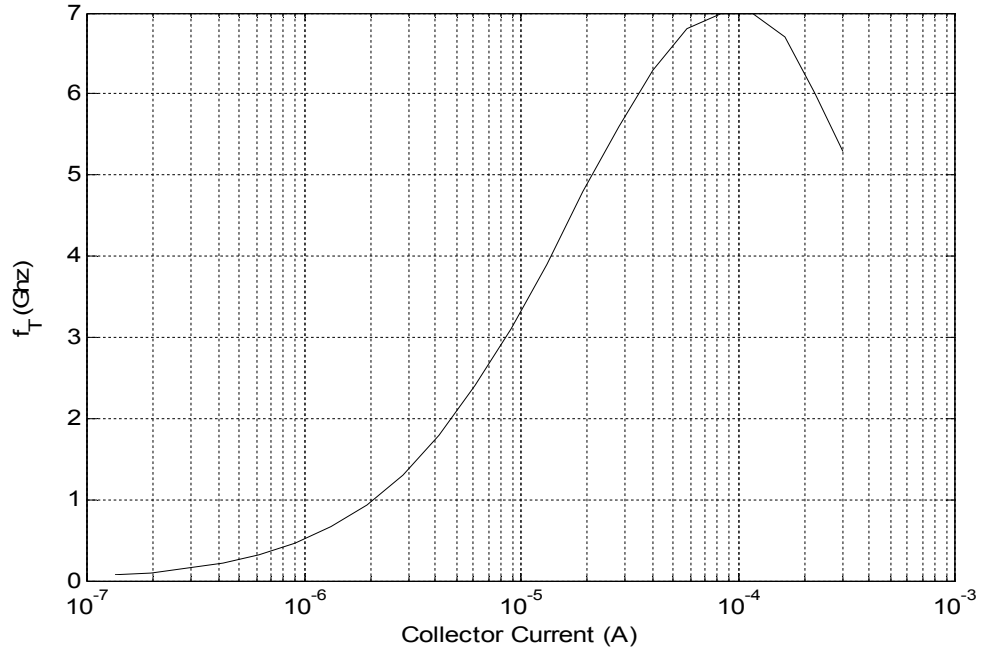

Figure 2.9 Transition frequency f_T versus I_C for an NPN transistor

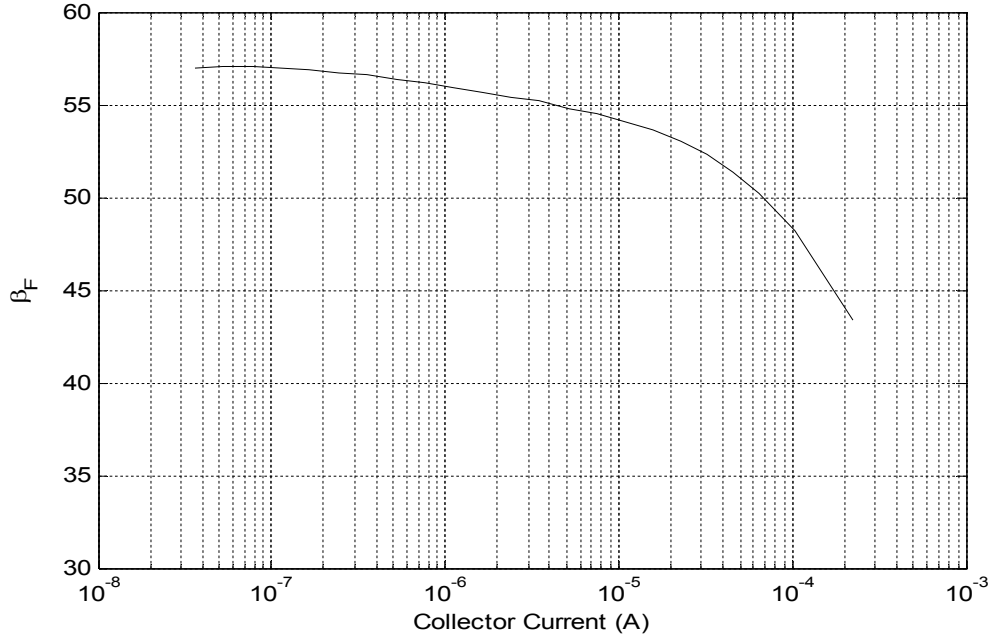

Figure 2.10 Current gain β_F versus I_C for a PNP transistor

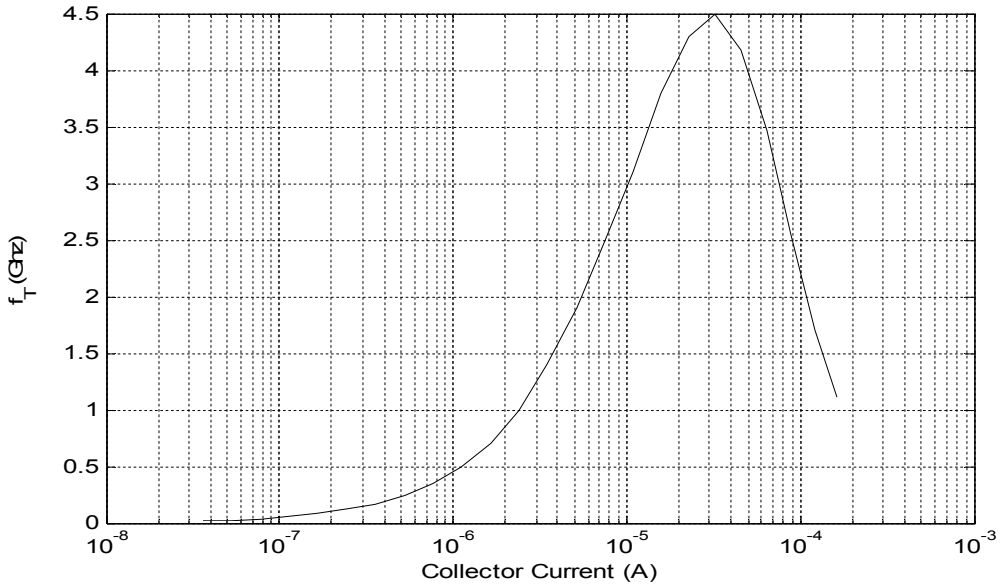

Figure 2.11 Transition frequency f_T versus I_C for a PNP transistor

2.5 Summary

The SGP model provides an improvement to the Ebers-Moll model in the areas of the low-current effect, the base-width modulation effect and the high-level injection effect. The VBIC formulation improves the SGP model in the modeling of the Early-effect, the self-heating effect, inclusion of the parasitic substrate PNP transistor, quasi-saturation, weak avalanche, excess phase and parasitic capacitance. The conversion between the SGP model and the VBIC model is presented because the VBIC model is as similar to the SGP model as possible apart from the improvements.

CHAPTER 3

THE CURRENT FEEDBACK OPERATIONAL AMPLIFIER

The Current Feedback Operational Amplifier (CFOA) is inherently faster than Voltage Feedback Operational Amplifier (VFOA) and has bandwidths that are almost independent of closed-loop gain. The CFOA achieves these advantages by employing current-mode operation. It is based on a transimpedance stage and two unity-gain buffers. It finds wide application in high-sampling rate analog to digital converter (ADC) drivers, high-resolution and high-sampling rate digital to analog converter (DAC) output buffers, high-speed, high-performance video signal processing circuits, automatic gain amplifiers and active filters [14] [15].

Although the Current Feedback Operational Amplifier (CFOA) has significant advantages over the Voltage Feedback Operational Amplifier (VFOA) in slew rate and gain-bandwidth product, it also suffers some disadvantages, e.g. worse noise and worse input offset voltage, worse power supply rejection ratio (PSRR), worse common-mode rejection ratio (CMRR), worse common mode input range (CMIR) and worse open loop gain. This chapter will provide a brief introduction to Current Feedback Operational Amplifier (CFOA) and discussion of its related important operational amplifier parameters.

3.1 Introduction to Current Feedback Operational Amplifier

3.1.1 Current Feedback Operational Amplifier Topology

A classical implementation of a current feedback operational amplifier is shown in figure 3.1 [15], [21], [24]-[25]. It is based on three stages: an input voltage buffer, an intermediate transimpedance stage and an output voltage buffer. The input buffer is made up of transistors Q_1 through Q_4. Transistors Q_1 and Q_2 form a low output-impedance push-pull stage, and Q_3 and Q_4 provide V_{BE} compensation as well as raising the input impedance. The input, V_p, and the output, V_n, of the input buffer (Q_1 through Q_4) constitute the non-inverting and inverting nodes of

the CFOA. Summing currents at the inverting node yields $I_n = I_1 - I_2$, where I_1 and I_2 are the push-pull transistors currents. A pair of current mirrors (Q_{13} ~ Q_{16}) forms the intermediate transimpedance stage. The transimpedance stage reflects the push-pull transistors currents (I_1, I_2) and recombines them at a common high-impedance node Z. The voltage formed at the high-impedance node, Z, is then transferred to the output via a second buffer. The output voltage buffer is made up of transistors Q_5 ~ Q_8 and provides low-output impedance for the external load. Transistors Q_9 through Q_{12} and Q_{17} through Q_{18} provide biasing circuitry for the input buffer and the output buffer respectively. Bias in the output stage is usually larger than that of the input to provide an adequate output drive to the load. Figure 3.2 summarizes the current-mode operation feature of a current feedback amplifier in a general block-diagram form.

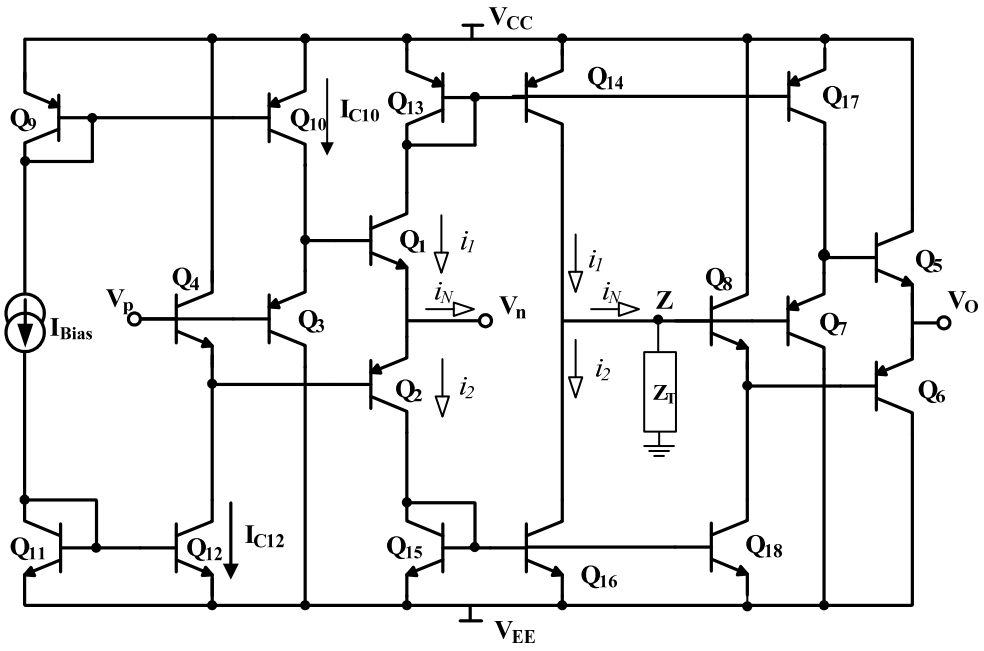

Figure 3.1 Classical simplified CFOA circuit [21].

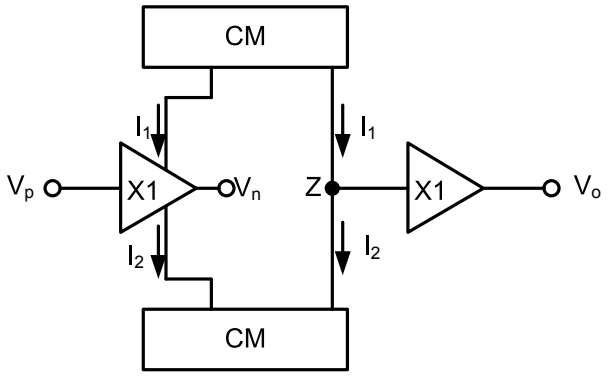

Figure 3.2 Simplified block diagrams of CFOA [25].

3.1.2 Bandwidth Independent of Gain

The current feedback operational amplifier is widely used in high-frequency analog signal processing, especially in the use of non-inverting amplifier configuration shown in figure 3.3 (a). One of the main advantages is that, unlike the constant Gain-Bandwidth product of the VFOA, the amplifier's closed-loop bandwidth is almost independent of its close-loop gain [21].

Figure 3.3 (b) shows the equivalent marco-model of a CFOA in the non-inverting amplifier configuration. The resistance, R_{oinv}, is the input buffer output resistance looking into the inverting node V_n of the CFOA. The summing current flowing out of the input buffer I_n, is replicated at the high-impedance node Z through a current controlled current source. Note that I_n is also the difference between the feedback current I_f and the current flowing through R_g (I_g). High Z node impedance is represented by R_t and C_t. The frequency, ω_{cm}, is the current mirror pole frequency due to the current mirror circuits showed in figure 3.2. Typically, the current mirror pole frequency is much higher than the pole frequency of a high Z node due to high impedance of node Z.

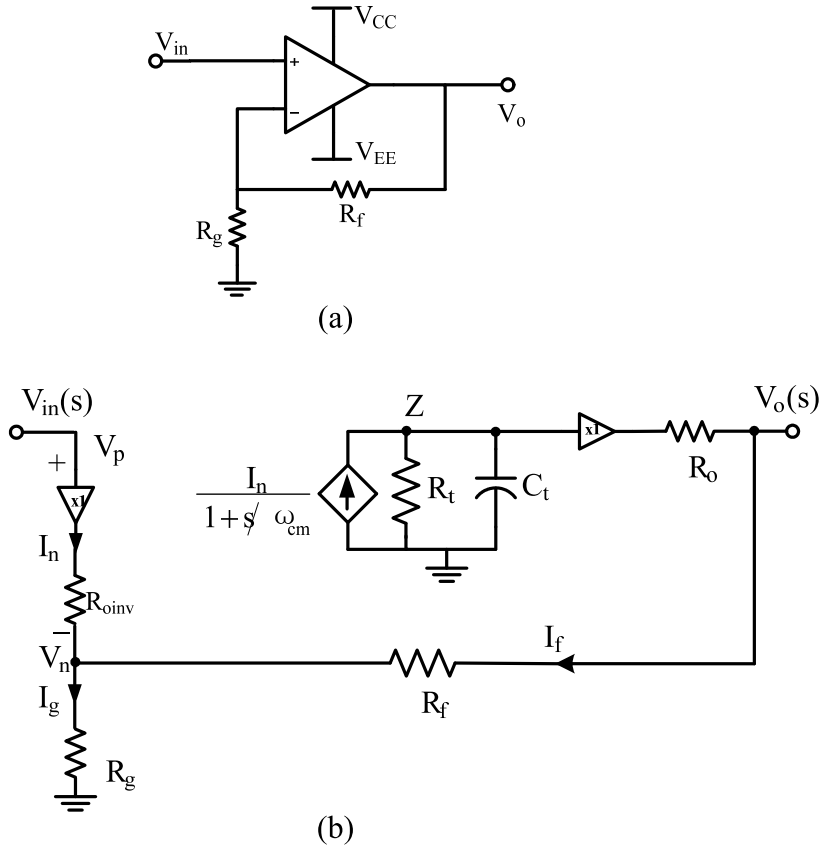

Figure 3.3 (a) Non-inverting amplifier configuration [21],
(b) Equivalent Macro-model of a CFOA in the non-inverting configuration [16].

By assuming $\omega_{cm} \rightarrow \infty$, the transimpedance Z_t (s) can be represented by the equivalent R_t, C_t circuit as

$$Z_t(s) = \frac{R_t}{1 + \frac{s}{\omega_t}}, \tag{3.1}$$

where $\omega_t = 1/(R_t \cdot C_t)$. The loop gain T (s) can be represented as follows

$$T(s) = \frac{Z_t(s)}{R_f}. \tag{3.2}$$

The voltage developed by high Z node in response of I_n is conveyed to the output through a voltage buffer, which gives

$$V_o(s) = I_n \cdot Z_t(s) \tag{3.3}$$

Noting that the input buffer keeps $V_{in}=V_p=V_n$, the Kirchhoff's Current Law (KCL) at the inverting node gives

$$I_n = V_{in}(s) \cdot \left(\frac{1}{R_f} + \frac{1}{R_g} \right) - V_o(s) \tag{3.4}$$

Thus the simplified transfer function of figure 3.3 (a) can be obtained by combining equations (3.3) and (3.4) as [21]

$$\begin{aligned} \frac{V_o(s)}{V_{in}(s)} &= \left(1 + \frac{R_f}{R_g} \right) \cdot \left(\frac{1}{1 + 1/T(s)} \right) \\ &= \left(1 + \frac{R_f}{R_g} \right) \cdot \left(\frac{R_t}{R_t + R_f} \right) \cdot \left(\frac{1}{1 + \dfrac{sR_t \cdot R_f C_t}{R_t + R_f}} \right). \end{aligned} \tag{3.5}$$

By assuming transresistance $R_t >> R_f$, the transfer function can be simplified as

$$\frac{V_o(s)}{V_{in}(s)} = \left(1 + \frac{R_f}{R_g} \right) \cdot \left(\frac{1}{1 + sR_f C_t} \right). \tag{3.6}$$

Equation (3.4) shows that the closed loop bandwidth is determined by $1/(R_f C_t)$, and the closed loop gain is determined by $1 + R_f / R_g$. Thus the gain and bandwidth can be independently adjusted by choosing the value of R_f and R_g.

3.1.3 Stability Criterion

If the current mirror pole frequency, ω_{cm}, is much greater than ω_t, but not ∞, then the transimpedance function Z_t (s) becomes

$$Z_t(s) = \frac{R_t}{\left(1 + \dfrac{s}{\omega_t} \right) \left(1 + \dfrac{s}{\omega_{cm}} \right)}. \tag{3.7}$$

The transfer function of CFOA becomes [16]

$$\frac{V_o(s)}{V_{in}(s)} = \left(1+\frac{R_f}{R_g}\right)\cdot\left(\frac{1}{1+1/T(s)}\right)$$
$$= \left(1+\frac{R_f}{R_g}\right)\cdot\left(\frac{\frac{R_t}{R_f}\cdot\omega_t\cdot\omega_{cm}}{s^2+\omega_{cm}\cdot s+\frac{R_t}{R_f}\cdot\omega_t\cdot\omega_{cm}}\right), \quad (3.8)$$
$$= \left(1+\frac{R_f}{R_g}\right)\cdot\left(\frac{\omega_p^2}{s^2+\frac{\omega_p}{Q}\cdot s+\omega_p^2}\right)$$

where $\omega_p = \sqrt{\frac{\omega_{cm}}{R_f C_t}}$ and $Q = \sqrt{\frac{1}{R_f C_t \omega_{cm}}}$.

Equation (3.6) is a classical two-pole characteristic equation. To avoid peaking, the value of Q should be chosen to be less than $1/\sqrt{2}$, and so R_f should be equal to or greater than $2/(C_t\cdot\omega_{cm})$. Hence a minimum feedback back resistance is required to ensure the stability of the non-inverting configuration of the CFOA [16], [18], [21].

3.2 Input Offset Voltage

The input offset voltage in a CFOA suffers from component mismatches much more than does a VFOA. Figure 3.4 shows the simplest implementation of the input stage of a CFOA. The main problem of this configuration is that the input offset voltage will be affected by mismatch between the NPN's and PNP's base-emitter voltage (V_{BE}). Assuming no mismatch of V_{BE} and Early voltage for the same kind of transistors, the input offset voltage is given by [22]

$$V_{os} = \frac{V_T}{2}\ln\left(\frac{I_2}{I_1}\right) + V_T\ln\left(\frac{J_{SP}}{J_{SN}}\right) + \frac{V_T}{2}\ln\left(\frac{A_2A_3}{A_1A_4}\right). \quad (3.9)$$

where V_T is the thermal voltage, I_1 and I_2 are the bias currents of the input stage, J_{SN} and J_{SP} are the saturation current density of the NPN and PNP transistor respectively, A_n is the emitter

area of Q_n. The second term will be the dominant contributor to the input offset voltage because of the configuration.

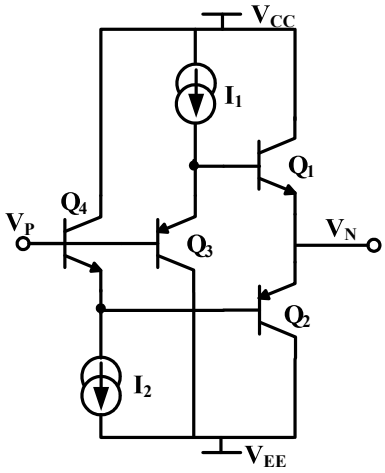

Figure 3.4 CFOA input buffer [21].

Another type of CFOA input stage is shown in figure 3.5 [21]. With the use of two diode connected transistors, this configuration allows matching between the same kinds of transistors. Therefore, it achieves better input offset voltage than the input stage in figure 3.4. However, the tradeoff is relatively low non-inverting input impedance, a high non-inverting input bias current, and noise.

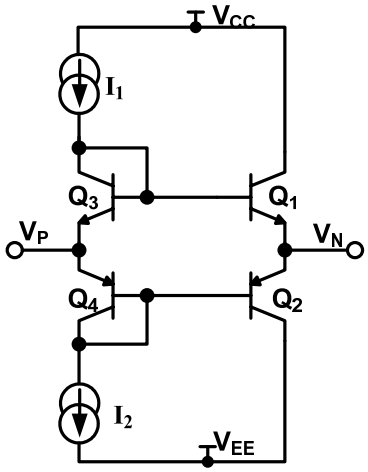

Figure 3.5 Alternative CFOA input buffer [21].

The eight transistors input stage configuration [23]-[24] shown in figure 3.6 has the advantage of high non-inverting input impedance, low non-inverting input bias current and low input offset voltage due to base-emitter voltage matching of the same kinds of transistors. On the other side, this configuration results in poor common mode input range due to the cascade of transistors, slew rate limitation, relatively higher inverting output impedance and hence relatively lower bandwidth for the CFOA.

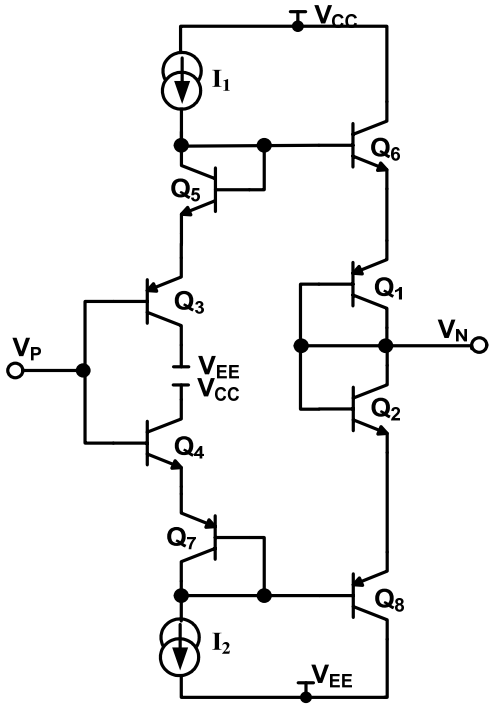

Figure 3.6 Eight transistors CFOA input buffer [24].

The analysis of the half circuit gives

$$V_{os} = V_P - V_N = V_{EBQ1} + V_{BEQ6} - V_{EBQ3} - V_{BEQ5}\,. \tag{3.10}$$

Assuming perfect matching between the same kinds of transistors and considering Early voltage effect, equation (3.8) becomes [23]-[24]

$$V_{os} = V_T \ln\left(\frac{V_{AN} + V_{CBQ\,5}}{V_{AN} + V_{CBQ\,6}} \cdot \frac{V_{AP} + V_{BCQ\,3}}{V_{AP} + V_{BCQ\,1}}\right). \tag{3.11}$$

3.3 Input Bias Current

The current feedback operational amplifier generally has higher input bias current than the voltage feedback operational amplifier. In the VFOA, the input bias currents are fairly well matched, while in the CFOA the input bias currents are not well matched as discussed in section 3.2. The non-inverting input error term (I_{bn}) which flows directly out of non-inverting terminal is usually a result of mismatch between the upper branch and the lower branch of the input buffer and mismatch of bias current (I_1 and I_2) [23]-[24]. The inverting input error item (I_{bi}) which flows directly out of the inverting terminal is usually a result of input offset voltage, feedback resistance R_f and R_g. The two mechanisms are not correlated.

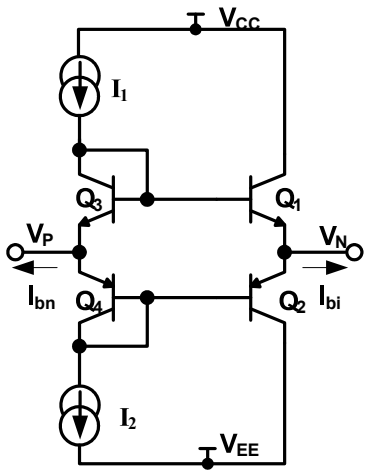

Figure 3.7 Input bias current of CFOA

3.4 Input Noise

Noise in a CFOA is higher than that of a VFOA. The I_{bn} shot noise in both a CFOA and VFOA is made up of base current, but in a CFOA there are usually two base currents due to the use of a complementary input stage compared to one base current in a VFOA. The I_{bn} shot noise in a CFOA is $\sqrt{2}$ times larger than that of a VFOA. For the I_{bi} noise, the CFOA and VFOA are totally different. The I_{bi} shot noise in the CFOA is dominated by the collector currents of the output transistors on the inverting side of the input buffer, which is a much larger current

compared to the base current generated I_{bi} shot noise in a VFOA. Generally the I_{bi} noise will be $\sqrt{\beta}$ times larger than I_{bn} shot noise [23]-[24].

The V_{os} noise in a CFOA is very similar to the V_{os} noise in a VFOA. The net input voltage noise of the CFOA in figure 3.8 is approximately half of the input voltage noise of a VFOA of two transistor input stage at the same bias current due to parallel connection of two sets of two devices in CFOA.

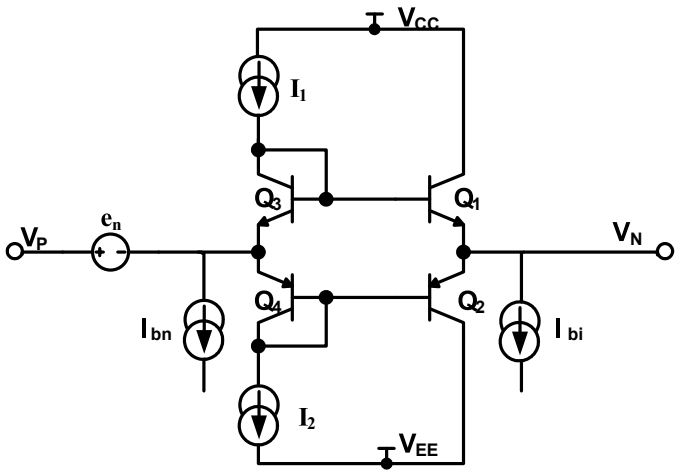

Figure 3.8 Input noise of CFOA [24]

3.5 Common Mode Rejection Ratio

The common-mode rejection ratio (CMRR) is defined as the ratio of the magnitude of the differential gain to the magnitude of the common mode gain, i.e. $CMRR=A_{dm}/A_{cm}$. To understand it better, the input stage of a classical CFOA shown in figure 3.1 is simplified to a small-signal equivalent circuit in figure 3.9 [17].

Assuming that $R_{\mu 1}= R_{\mu 2}>>r_{o1}= r_{o2,}\ r_{o10}= r_{o12}$, then

$$\left|A_{cm}\right| = \left|\frac{i_{out(cm)}}{V_{cm}}\right| \cdot \left|Z_T\right| \cong \left(\frac{2}{r_{o1,2}} + \frac{2}{r_{o10,12}}\right) \cdot \left|Z_T\right|, \tag{3.12}$$

$$\left|A_{dm}\right| = \left|\frac{i_{out(dm)}}{V_{dm}}\right| \cdot \left|Z_T\right| \cong g_{m1,2} \cdot \left|Z_T\right|, \tag{3.13}$$

$$\mathrm{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| \cong \frac{g_{m1,2}}{\frac{2}{r_{o1,2}} + \frac{2}{r_{o10,12}}}, \tag{3.14}$$

where Z_t is the high impedance at the high Z node, $i_{out(cm)}$ and $i_{out(dm)}$ are the output currents of the common mode and the differential mode, respectively, V_{cm} and V_{dm} are the input common-mode voltage and differential-mode voltage, respectively.

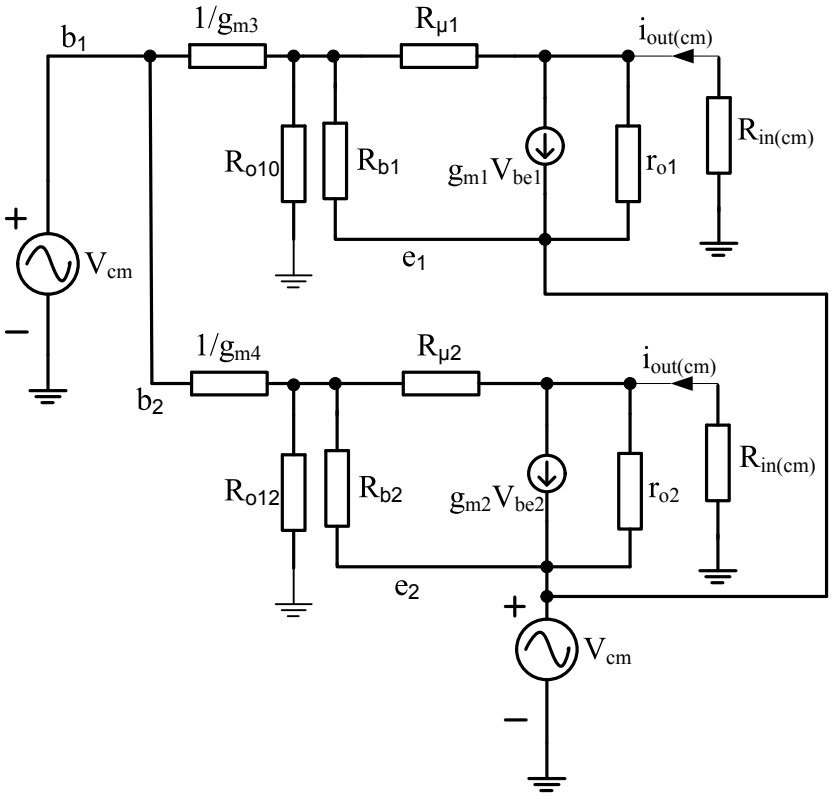

Figure 3.9 Small-signal equivalent input stage of the CFOA in figure 3.1 with a common-mode voltage applied [17].

The CMRR for the CFOA depends on the output resistances of the bias current mirrors (Q_9 through Q_{10} and Q_{11} through Q_{12} in figure 3.1) in the input stage and the output resistances of the power transistors (Q_1 and Q_2 in figure 3.1) of the input stage. The value of CMRR in CFOA is normally in the range of 60 dB, which is worse than 80 dB of a typical VFOA.

Another perspective is to use the alternative definition of CMRR [19], i.e. the ratio of an input CM voltage change (DM voltage input is zero) to the resulting input-referred offset voltage,

$$\mathrm{CMRR} = \frac{\Delta V_{cm,in}}{\dfrac{\Delta V_{os,out}}{A_{DM}}} = \frac{\Delta V_{cm,in}}{\Delta V_{os,in}}. \tag{3.15}$$

As discussed in section 3.2, the input offset voltage in a CFOA suffers from mismatches and Early voltage effects much more than a VFOA does. Hence the CMRR in CFOA is worse than a VFOA.

3.6 Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) is defined as the gain from the input to the output divided by the gain from the supply to the output [20]

$$\mathrm{PSRR}^{+/-} = \left| \frac{A_V(\Delta V_{cc} = 0)}{A_{CC,+/-}(\Delta \mathrm{V_{in}} = 0)} \right|, \tag{3.16}$$

where $A_V=V_o/V_{in}$, $A_{CC,+}=V_o/\Delta V_{cc}$, $A_{CC,-}= V_o/\Delta V_{ee}$, and ΔV_{cc} and ΔV_{ee} are the small signal voltages in the positive and negative power supply, respectively. The PSRR is worse in a CFOA than a VFOA. PSRR can be considered to be the ratio of a change in supply voltage to the resulting input-referred offset voltage change assuming the change in input bias current is small. As discussed in section 3.3, the changes in I_{bn} and I_{bi} in figure 3.8 can make the PSRR worse since they are large and uncorrelated. On the other hand, a change in V_{os} due to supply voltage change becomes worse due to errors caused by the Early voltage.

The unity gain configuration of a CFOA shown with zero input voltage in figure 3.10 can be used to simulate the positive and negative PSRR [20],

$$\mathrm{PSRR}^{+} \cong \frac{\Delta V_{cc}}{\Delta V_{out}}, \tag{3.17}$$

$$\mathrm{PSRR}^{-} \cong \frac{\Delta V_{ee}}{\Delta V_{out}}. \tag{3.18}$$

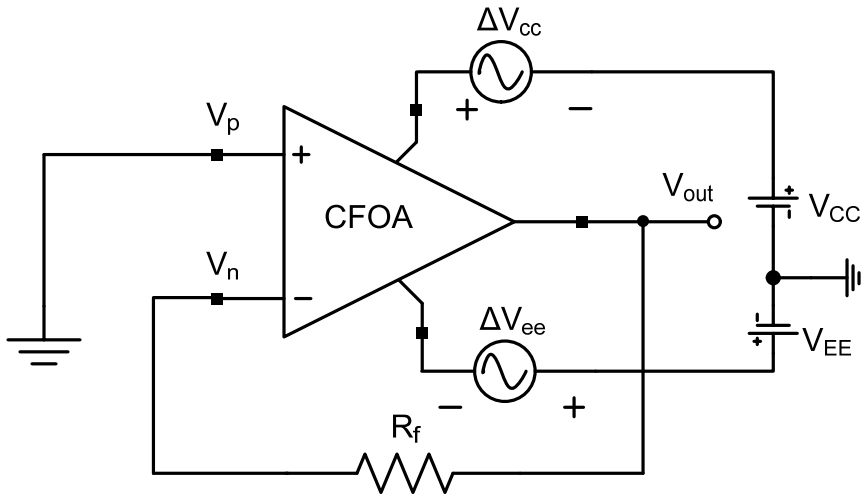

Figure 3.10 CFOA in unity-gain configuration for simulation of $PSRR^{+/-}$ [20]

3.7 Common Mode Input Range

Common mode input range (CMIR) is defined as the range of the common mode input voltage within which the OP-Amp operates as expected. Due to circuit topology limitation of input stage, the CMIR in CFOA is generally worse than a VFOA. The best CMIR that can be achieved in a CFOA is only within two diodes of either supply voltage, i.e. $-V_{EE}+V_{BE}+V_{CEsat} \leqq V_{ic} \leqq V_{CC}-V_{BE}-V_{CEsat}$ while the CMIR in a VFOA often includes one of the supply rails. Cascading the input stage to improve V_{os} will make the CMIR worse.

Figure 3.11 shows the circuit configuration for finding the CMIR [21]. The mechanism is that when the input voltage exceeds 2 times the lower limit or upper limit of CMIR, the output voltage, V_{out}, will reach a negative or positive rail, i.e. the CFOA no longer works as expected.

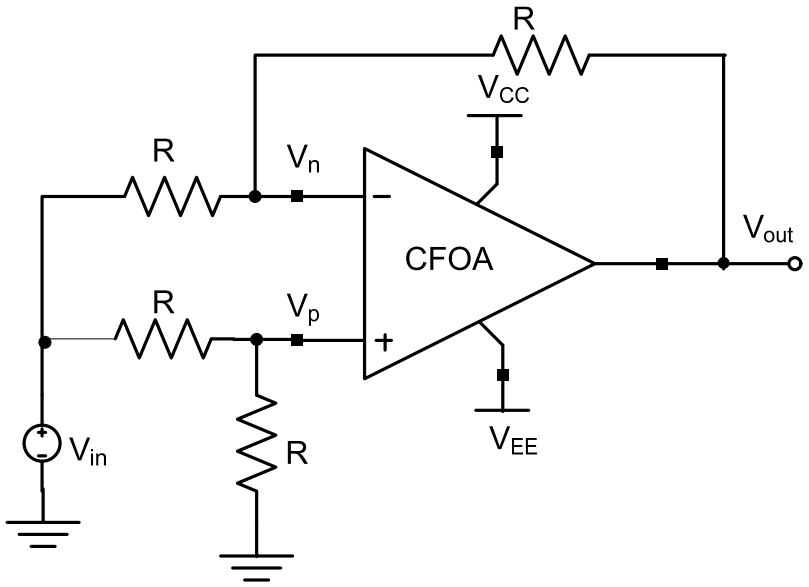

Figure 3.11 CMIR simulation configuration [21]

3.8 Summary

Current feedback operational amplifiers offer significant advantages and disadvantages. While having higher slew rate and bandwidth independent of gain, CFOAs also shows worse noise, input errors, power supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), common mode input range (CMIR) and open loop gain. Different topologies of the input stage of CFOAs are investigated. Topology selection should be based on specific application because there are always tradeoffs in different topologies.

CHAPTER 4

MODELING AND CHARACTERIZATION OF THE EFFECTS OF SELF-HEATING ON LARGE-SIGNAL BEHAVIOR OF A BJT TRANSISTOR

This chapter provides an approach for modeling the thermal effect of self-heating on large-signal behavior in a silicon-on-insulator (SOI) bipolar transistor. As illustrated previously, the strong dependence of collector current on temperature significantly affects the small-signal and large-signal behavior of BJTs. The effect of self-heating on the bipolar transistor in the common-emitter (*CE*) configuration driven by a constant base-emitter voltage or constant base current will be investigated.

First, the self-heating mechanism of a device will be examined to assess the device temperature dependency on the static device characteristics. Then two configurations in which device temperature affects large-signal behavior of a BJT transistor will be discussed, i.e. common-emitter (*CE*) configuration is to be driven by a constant base-emitter voltage and a constant base current. Analytical formulations will be developed to model and predict the large-signal behavior.

4.1 Thermal Effects of Self-Heating

The temperature increase of a transistor due to its own power dissipation is called self-heating. As a result, the collector current of the bipolar transistor will change due to device temperature changes. The static self-heating can be represented by an electro-thermal model [26]-[27] illustrated in Figure. 4.1.

In Figure 4.1, the variables I_B, I_C, V_{CE}, V_{BE}, T_A, and T_j are the large-signal base current, large-signal collector current, large-signal collector-emitter voltage, large-signal base-emitter voltage, circuit ambient temperature, and device operating temperature respectively. For the

SOI bipolar transistor, the operating temperature, T_j, is always higher than ambient temperature because of self-heating. The operating temperature of a device can be expressed as

$$T_j = T_A + P_{th} \cdot R_{th}, \tag{4.1}$$

where $P_{th} = V_{CE}I_C + V_{BE}I_B$ denotes static power dissipation in the device, and R_{th} is the thermal resistance of the transistor.

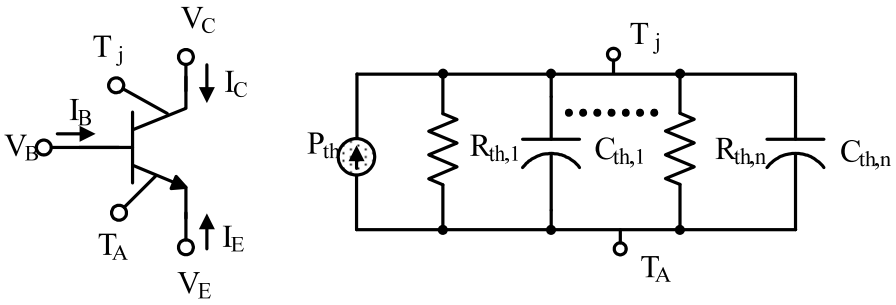

Figure 4.1 Electrothermal model for an SOIBJT.

Since collector current is a function of V_{BE} (base-emitter voltage) or I_B (base current), V_{CE} (Collector-emitter voltage) and device operating temperature such as

$$I_C = f(V_{BE} \text{ or } I_B, V_{CE}, T_j) \tag{4.2}$$

and V_{BE} (base-emitter voltage) generally decreases 2.0 mV/°C. Thus self-heating through power dissipation can affect the large-signal behavior of the BJT and consequently circuit behavior.

4.2 Large-Signal Behavior of BJT Transistor

4.2.1 Temperature Effects on the Model Parameters

The Ebers-Moll static model [11] shown in Figure 4.2 with thermal heating can be used to model the self-heating effect on the large-signal behavior of BJT transistors. The single Current source (I_{CT}) between the emitter and the collector can be expressed as follows,

$$I_{CT} = I_{CC} - I_{EC} = I_S \cdot \left(\exp\left(\frac{qV_{BE}}{kT} \right) - \exp\left(\frac{qV_{BC}}{kT} \right) \right). \tag{4.3}$$

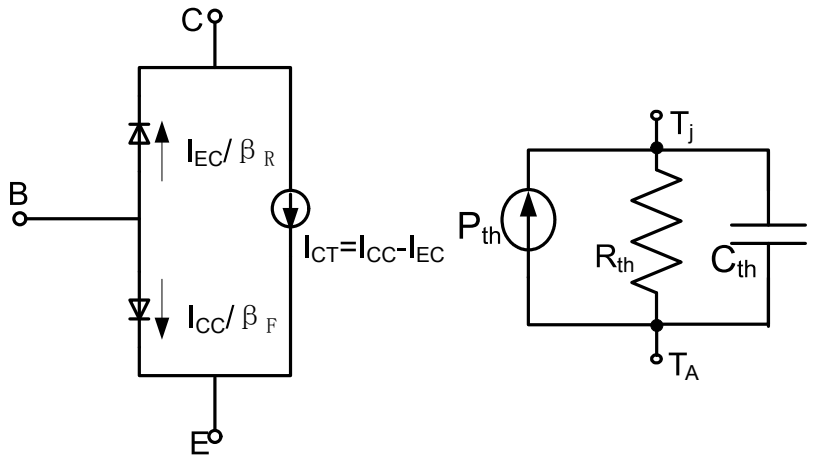

Figure 4.2 Ebers-Moll static model for an NPN ideal transistor: transport version [11] with thermal heating.

Taking the Early effect into account, the expression for I_{CT} becomes

$$I_{CT} = \frac{I_S}{1 + V_{BC}/V_A} \cdot \left(\exp\left(\frac{qV_{BE}}{kT} \right) - \exp\left(\frac{qV_{BC}}{kT} \right) \right), \tag{4.4}$$

where $I_S = \frac{qD_n n_i^2 A_J}{Q_B}$, D_n is the diffusion coefficient for electrons, A_J is the cross sectional area of the emitter, Q_B is the number of doping atoms in the base per area of the emitter and n_i is the intrinsic carrier concentration in silicon.

Although equation (4.3) contains the absolute temperature explicitly in the exponent, qV_{BE}/kT, the principal temperature dependence results from the extremely strong temperature dependence of the saturation current I_S.

The principal temperature dependence of the component of saturation current I_S, is related to the intrinsic carrier concentration, n_i^2 [11],

$$n_i^2(T) = C_1 T^3 \exp\left(\frac{-E_g(T)}{kT} \right) \tag{4.5}$$

where C_1 is a constant while the bandgap energy, E_g, is also function of temperature, according to the general relation [28]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T}. \tag{4.6}$$

For Si, experimental results give α =7.02 x 10^{-4}, β =1108, and $E_g(0)$ =1.16 eV.

Drift and diffusion are both manifestation of the random thermal motion of the carriers. Consequently, the mobility μ_n and the diffusion coefficient D_n are not independent. More precisely, they are related as follows: [11]

$$D_n = \mu_n \frac{kT}{q}, \tag{4.7}$$

$$D_p = \mu_p \frac{kT}{q}. \tag{4.8}$$

These equations are known as the Einstein relations.

The mobility is limited by two primary mechanisms, lattice scattering and impurity scattering. Lattice scattering is strongly temperature dependent due to thermal phonon vibration, while impurity scattering is relatively temperature insensitive. The balance of these two mechanisms is such that at doping levels greater than 10^{19} cm^{-3}, impurity scattering dominates, and the mobility is nearly a constant as a function of temperature. At doping levels lighter than 10^{19} cm^{-3}, lattice scattering becomes increasingly more prominent, and the mobility becomes increasingly more temperature dependent, its magnitude increasing with decreasing temperature [34].

Empirical relations for the temperature as well as doping dependence of the carrier mobility in silicon are available as well and are listed below [32],

$$\mu_n(N,T) = 88\left(\frac{T}{300}\right)^{-0.57} + \frac{4.37\cdot 10^{14}\cdot\left(\frac{T}{300}\right)^{-2.33}}{1 + \frac{N}{1.26\cdot 10^{17}\cdot\left(\frac{T}{300}\right)^{2.4}}\cdot 0.88\left(\frac{T}{300}\right)^{-0.146}}, \tag{4.9}$$

$$\mu_p(N,T) = 54.3\left(\frac{T}{300}\right)^{-0.57} + \frac{4.51\cdot 10^{13}\cdot\left(\frac{T}{300}\right)^{-2.23}}{1+\frac{N}{2.35\cdot 10^{17}\cdot\left(\frac{T}{300}\right)^{2.4}}\cdot 0.88\left(\frac{T}{300}\right)^{-0.146}}. \quad (4.10)$$

The temperature dependence of mobility in equation (4.9) and (4.10) can be fitted in power law as follows:

$$\mu_n(N,T) = \mu_n(300,N)\cdot\left(\frac{T}{300}\right)^{-n} = C_2 T^{-n}, \quad (4.11)$$

$$\mu_p(N,T) = \mu_p(300,N)\cdot\left(\frac{T}{300}\right)^{-m} = C_3 T^{-m}. \quad (4.12)$$

where C_2 and C_3 are constants, and m, n value depends on doping levels as showed in Figure 4.3 and Table 4.1.

Table 4.1 n and m corresponding to different doping level

N (cm^{-3})	n	m
4E+15	2.14	1.99
1E+16	2.05	1.94
2E+16	1.91	1.86
4E+16	1.69	1.72
1E+17	1.25	1.41
2E+17	0.86	1.07
4E+17	0.54	0.72
1E+19	0.44	0.43

Substituting equation (4.5) through (4.8) into equation (4.4), I_{CT} expression becomes

$$I_{CT} \cong CT^{4-n}\left[\exp\left(\frac{qV_{BE}-E_g(T)}{kT}\right)-\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\right]\cdot\left(1+\frac{V_{CB}}{V_A}\right) \quad (4.13)$$

where C is equal to $\frac{kA_J}{Q_B}C_1C_2$.

From equation (4.13), it can be inferred that collector current has a direct relationship with temperature, and then self-heating can affect large-signal behavior of BJT transistors.

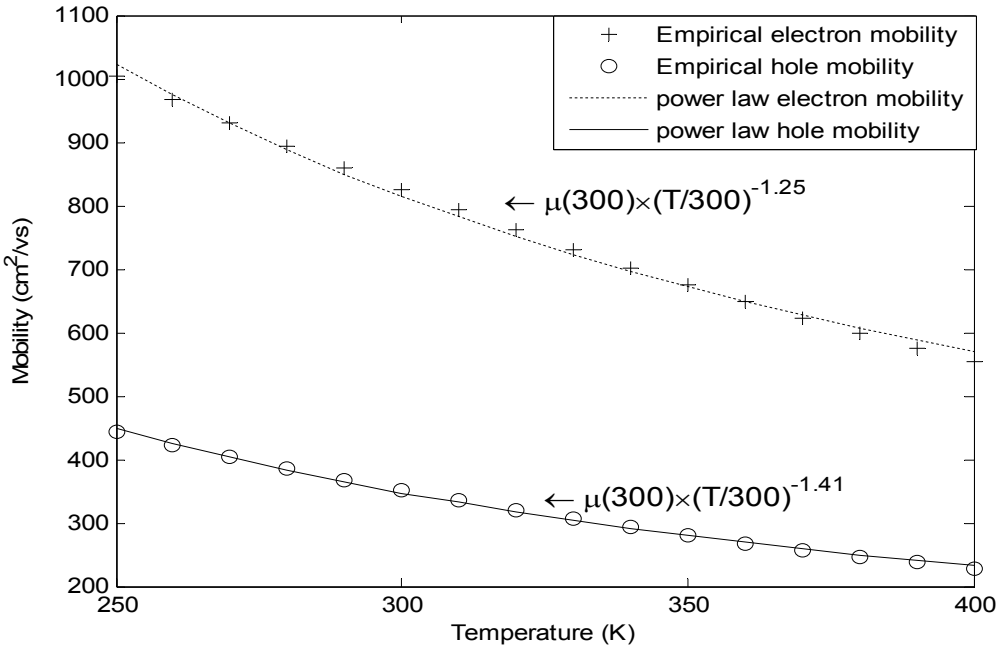

Figure 4.3 Electron mobility and hole mobility temperature dependence when $N=10^{17}$ cm^{-3}

4.2.2 Collector Current of a Current Driven Transistor

Equation (4.13) gives the collector current as a function of base-emitter voltage. The base current, I_B, is also an important parameter and at moderate current levels, consists of two major components. One of these (I_{Bp}) is due to injection of holes from the base into the emitter and usually represents the dominant one in a silicon BJT [32]-[33]. This current component depends on the gradient of the minority-carrier hole distribution in the emitter and is [33]

$$I_{Bp} = \frac{qA_E D_{pE}}{L_{pE}} \cdot \frac{n_{iE}^2}{N_E} \cdot \exp\left(\frac{qV_{BE}}{kT}\right), \tag{4.14}$$

where

A_E is emitter area,

N_E is the emitter doping level,

D_{pE} is the minority hole diffusion coefficient in the emitter,

L_{pE} is the diffusion length for holes in the emitter,

n_{iE} is the intrinsic carrier concentration in the emitter.

The second major component ($I_{B,\,bulk}$) of base current represents recombination of holes and electrons in the base and is proportional to the minority-carrier charge in the base [33]

$$I_{B,bulk} = \frac{1}{2} \cdot \frac{qA_E X_B}{\tau_B} \cdot \frac{n_{iB}^2}{N_B} \cdot \exp\left(\frac{qV_{BE}}{kT} \right), \tag{4.15}$$

where

A_E is emitter area,

N_B is the base doping level,

τ_B is the minority carrier lifetime in the base,

X_B is the base width,

n_{iB} is the intrinsic carrier concentration in the base.

Experimental values of electron lifetime in p-type silicon can be fitted to an empirical equation (4.16) [30]. For a given base doping concentration, e.g. N=1×10^{17} cm^{-3}, this will give the minority-carrier lifetime τ_{nB} approximately as 2.89×10^{-6} second. The full expression for τ_n is

$$\frac{1}{\tau_n} = 3.45\times10^{-12} N + 0.96\times10^{-31} N^2 \quad s^{-1} \tag{4.16}$$

Experiment values of hole lifetime in n-type silicon can be fitted to an empirical equation of the form (4.17) [31]. For a given emitter doping concentration, e.g. N=1×10^{19} cm^{-3}, this will give the minority-carrier lifetime in the emitter τ_{pE} as 3.87×10^{-8} second. The full expression for τ_p is

$$\frac{1}{\tau_p} = 7.8\times10^{-13} N + 1.8\times10^{-31} N^2 \quad s^{-1} \tag{4.17}$$

From equation (4.8) and (4.10), the diffusion coefficient, D_{pE} is obtained. Thus the diffusion length for holes in the emitter is obtained from the following equation and is 2.67×10^{-4} cm.

$$L_{pE} = \sqrt{D_{pE}\cdot\tau_{pE}}\ . \tag{4.18}$$

Combining equation (4.14) and (4.15) and put corresponding values in there gives

$$\frac{I_{Bp}}{I_{B,bulk}} = 2\cdot\frac{D_{pE}}{L_{pE}}\cdot\frac{\tau_{nB}}{X_B}\cdot\frac{N_B}{N_E} = 2\cdot\frac{1.85}{2.67\times10^{-4}}\cdot\frac{2.89\times10^{-6}}{5\times10^{-5}}\cdot\frac{1\times10^{17}}{1\times10^{19}} = 8\,.$$

Since I_{Bp} represents the dominant component in the base current in silicon BJT, so equation (4.15) can be written in another form assuming a moderately doped emitter,

$$V_{BE} \cong V_T\cdot\ln\left(\frac{I_B\cdot L_{pE}N_E}{qD_{pE}n_{iE}^2A_E}\right). \tag{4.19}$$

Substituting equation (4.5), (4.8) and (4.12) in equation (4.19) gives

$$V_{BE} \cong V_T\cdot\ln\left(\frac{I_B\cdot L_{pE}N_E}{kC_1C_3A_ET^{4-m}\cdot e^{\left(-E_g(T)/kT\right)}}\right). \tag{4.20}$$

Simplification of (4.20) gives

$$V_{BE} = V_T\cdot\ln(I_B\cdot C') + V_g(T) - V_T\cdot\ln(T^{4-m}) \tag{4.21}$$

where $C' = \dfrac{L_{pE}N_E}{kC_1C_3A_E}$, $V_g(T) = E_g(T)/q$ and $V_T = kT/q$.

Substituting equation (4.21) in equation (4.13) gives

$$I_C = CC'I_B\cdot T^{m-n}\cdot\left(1+\frac{V_{CB}}{V_A}\right) - CT^{4-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\cdot\left(1+\frac{V_{CB}}{V_A}\right) \tag{4.22}$$

where $C = \dfrac{kA_E}{Q_B}C_1C_2$, $\mu_n = C_2T^{-n}$ and $\mu_p = C_3T^{-m}$.

Now collector current is represented as a function of base current, temperature and collector-base voltage. Further analysis will reveal how self-heating affects large-signal behavior of current driven BJT transistors.

4.2.3 Large-Signal Behavior of a Current Driven Transistor

4.2.3.1 Output Conductance

The influence of the Early effect on the transistor large-signal characteristic in the forward-active region can be represented approximately as [33]

$$I_C = I_S \cdot \left(1 + \frac{V_{CE}}{V_A}\right) \cdot \exp\left(\frac{V_{BE}}{V_T}\right). \tag{4.23}$$

Small changes, dV_{CE}, in V_{CE} produce corresponding changes dI_C in I_C, where

$$dI_C = \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{I_B,T} \cdot \Delta V_{CE}\,. \tag{4.24}$$

Therefore a small-signal output conductance is,

$$g_o = \frac{dI_C}{dV_{CE}} = \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{I_B,T} = \frac{I_C}{V_A} \tag{4.25}$$

where V_A is the Early voltage. Figure 4.4 shows typical bipolar transistor output characteristic which can be used to extract V_A.

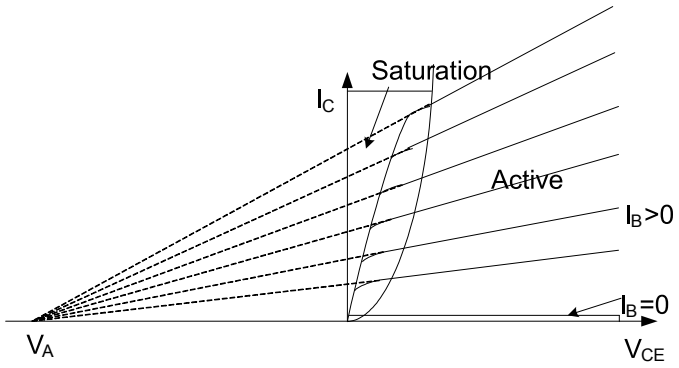

Figure 4.4 Bipolar transistor output characteristic showing the Early voltage, V_A.

4.2.3.2 Self-Heating Output Conductance of a Current Driven Transistor

Equation (4.22) describes a detailed relationship between collector current and temperature, collector-base voltage and base current. Since self-heating causes an increase in the device temperature, it will play a role in the output conductance of a BJT.

Since equation (4.22) is a function of temperature, collector-base voltage and base current, the total differential of I_C is

$$dI_C = \left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B,T} \cdot \Delta V_{CB} + \left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}} \cdot \Delta T + \left.\frac{\partial I_C}{\partial I_B}\right|_{T,V_{CB}} \cdot \Delta I_B . \tag{4.26}$$

By holding base current constant a self-heating output conductance is

$$g_{osh} = \left.\frac{dI_C}{dV_{CB}}\right|_{I_B} = \left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B,T} + \left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}} \cdot \frac{\partial T}{\partial V_{CB}} . \tag{4.27}$$

A derivative of equation (4.1) gives ignoring base current

$$\begin{aligned} \frac{\partial T_j}{\partial V_{CB}} &= \frac{\partial\left(T_A + P_{th} \cdot R_{th}\right)}{\partial V_{CB}} \\ &= \frac{\partial\left(T_A + V_{CE} \cdot I_C \cdot R_{th} + V_{BE} \cdot I_B \cdot R_{th}\right)}{\partial V_{CB}} . \\ &\cong I_C R_{th} + V_{CE} R_{th} \left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B} \end{aligned} \tag{4.28}$$

The derivative of the collector current with respect to the collector-base voltage $\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B,T}$ can be first solved as follows

$$\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B,T} = \left.\frac{\partial}{\partial V_{CB}}\left(C\cdot C'\cdot I_B\cdot T^{m-n}\cdot\left(1+\frac{V_{CB}}{V_A}\right)-CT^{4-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\cdot\left(1+\frac{V_{CB}}{V_A}\right)\right)\right|_{I_B,T}$$

$$= \frac{C\cdot C'\cdot I_B\cdot T^{m-n}}{V_A} - \frac{CT^{4-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)}{V_A}$$

$$+ \underbrace{\frac{CT^{4-n}\cdot\left(1+\frac{V_{CB}}{V_A}\right)\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)}{V_T}}_{Negligible}$$

$$\cong \frac{\left(C\cdot C'\cdot I_B\cdot T^{m-n}-CT^{4-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\right)\cdot(1+\frac{V_{CB}}{V_A})}{V_A+V_{CB}}$$

$$= \frac{I_C}{V_A+V_{CB}}$$

(4.29)

The derivative of the collector current with respect to temperature $\left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}}$ can be solved as follows

$$\left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}} = \left.\frac{\partial}{\partial T}\left(C\cdot C'\cdot I_B\cdot T^{m-n}\cdot\left(1+\frac{V_{CB}}{V_A}\right)-CT^{4-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\cdot\left(1+\frac{V_{CB}}{V_A}\right)\right)\right|_{I_B,V_{CB}}$$

$$= (m-n)\cdot C\cdot C'\cdot I_B\cdot T^{m-n-1}\cdot\left(1+\frac{V_{CB}}{V_A}\right)$$

$$+ \underbrace{CT^{3-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\cdot\left(1+\frac{V_{CB}}{V_A}\right)\cdot\left(\frac{V_{BC}-V_g(T)}{V_T}+n-4\right)}_{Negligible}$$

$$\cong (m-n)\cdot C\cdot C'\cdot I_B\cdot T^{m-n-1}\cdot\left(1+\frac{V_{CB}}{V_A}\right)$$

$$\cong (m-n)\cdot\frac{I_C}{T}$$

(4.30)

Substituting equation (4.28), (4.29) and (4.30) into equation (4.27) gives

$$\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B} = \frac{\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B,T} + \left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}} \cdot I_C R_{th}}{1 - V_{CE} R_{th} \left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}}}$$

$$= \frac{\frac{I_C}{V_A + V_{CB}} + (m-n)\cdot C \cdot C' \cdot I_B \cdot T^{m-n-1} \cdot \left(1 + \frac{V_{CB}}{V_A}\right) \cdot C \cdot C' \cdot I_B \cdot T^{m-n} \cdot \left(1 + \frac{V_{CB}}{V_A}\right) \cdot R_{th}}{1 + (n-m)\cdot C \cdot C' \cdot I_B \cdot T^{m-n-1} \cdot \left(1 + \frac{V_{CB}}{V_A}\right) \cdot V_{CE} \cdot R_{th}}$$

$$= \frac{\frac{I_C}{V_A + V_{CB}} - (n-m)\cdot \frac{I_C^2 \cdot R_{th}}{T}}{1 + (n-m)\cdot \frac{I_C}{T} \cdot V_{CE} \cdot R_{th}}$$

(4.31)

Equation (4.31) shows that self-heating effects could generate negative self-heating output conductance due to temperature increase if the emitter is moderately doped. The $(n-m)\cdot\frac{I_C}{T}\cdot V_{CE}\cdot R_{th}$ part in the denominator is negligible since it has a magnitude of approximately 10^{-3} at room temperature. So if n is greater than m, then at some point where the power dissipation is large enough that the value of $(n-m)\cdot\frac{I_C^2\cdot R_{th}}{T}$ is greater than $\frac{I_C}{V_A + V_{CB}}$, the self-heating output conductance will become negative. Table 4.1 shows at certain doping level the temperature dependence of electron mobility is more sensitive than that of hole mobility, i.e. n>m. In this case the self-heating output conductance with constant base current will be negative when the power dissipation is large enough.

In the case of the emitter being heavily doped, the preponderance of dislocations and lattice deformations introduced by heavy emitter doping lowers the silicon band-gap energy, E_g, by some value ΔE_g. This, in turn causes a change in the value and temperature dependence of the equilibrium carrier concentration n_i^2, where [34]

$$n_i^2(T) = C_1 T^3 \exp\left(\frac{-\left(E_g(T) - \Delta E_g\right)}{kT}\right). \tag{4.32}$$

The variable ΔE_g can be modeled as [31]

$$\Delta E_g = 18.7\times10^{-3}\ln\left(\frac{N_D}{7\times10^{17}}\right)\ \text{eV} \qquad \text{for } N_D \geq 7\times10^{7}\ \text{cm}^{-3}. \tag{4.33}$$

ΔE_g is equal to 49.72 eV when $N_D = 1\times10^{19}\ \text{cm}^{-3}$.

Hence equation (4.22) can be modified as follows

$$I_C = CC'I_B\cdot T^{m-n}\cdot\left(1+\frac{V_{CB}}{V_A}\right)\exp\left(\frac{-\Delta E_g}{kT}\right) - CT^{4-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\cdot\left(1+\frac{V_{CB}}{V_A}\right) \tag{4.34}$$

A derivate of I_C over temperature with constant I_B and V_{CB} now gives

$$\begin{aligned}
\left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}} &= \left.\frac{\partial}{\partial T}\left(C\cdot C'\cdot I_B\cdot T^{m-n}\cdot\left(1+\frac{V_{CB}}{V_A}\right)\cdot\exp\left(\frac{-\Delta E_g}{kT}\right)\right)\right|_{I_B,V_{CB}} \\
&\quad \left.-\frac{\partial}{\partial T}\left(CT^{4-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\cdot\left(1+\frac{V_{CB}}{V_A}\right)\right)\right|_{I_B,V_{CB}} \\
&= (m-n)\cdot C\cdot C'\cdot I_B\cdot T^{m-n-1}\cdot\left(1+\frac{V_{CB}}{V_A}\right)\cdot\exp\left(\frac{-\Delta E_g}{kT}\right) \\
&\quad + C\cdot C'\cdot I_B\cdot T^{m-n-1}\cdot\frac{\Delta E_g}{KT}\cdot\left(1+\frac{V_{CB}}{V_A}\right)\cdot\exp\left(\frac{-\Delta E_g}{kT}\right) \\
&\quad + \underbrace{CT^{3-n}\cdot\exp\left(\frac{qV_{BC}-E_g(T)}{kT}\right)\cdot\left(1+\frac{V_{CB}}{V_A}\right)\cdot\left(\frac{V_{BC}-V_g(T)}{V_T}+n-4\right)}_{Negligible} \\
&\cong \left(m-n+\frac{\Delta E_g}{KT}\right)\cdot C\cdot C'\cdot I_B\cdot T^{m-n-1}\cdot\left(1+\frac{V_{CB}}{V_A}\right)\cdot\exp\left(\frac{-\Delta E_g}{kT}\right) \\
&\cong \left(m-n+\frac{\Delta E_g}{KT}\right)\cdot\frac{I_C}{T}
\end{aligned} \tag{4.35}$$

Substituting equation (4.28), (4.29) and (4.35) into (4.27) gives $\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B}$ assuming heavy emitter doping as

$$\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B} = \frac{\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{I_B,T} + \left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}} \cdot I_C R_{th}}{1 - V_{CE} R_{th} \left.\frac{\partial I_C}{\partial T}\right|_{I_B,V_{CB}}}$$

$$= \frac{\frac{I_C}{V_A + V_{CB}} + \left(m - n + \frac{\Delta E_g}{KT}\right) \cdot C \cdot C' \cdot I_B \cdot T^{m-n-1} \cdot \left(1 + \frac{V_{CB}}{V_A}\right) \cdot \exp\left(\frac{-\Delta E_g}{kT}\right) \cdot I_C R_{th}}{1 + \left(n - m + \frac{\Delta E_g}{KT}\right) \cdot C \cdot C' \cdot I_B \cdot T^{m-n-1} \cdot \left(1 + \frac{V_{CB}}{V_A}\right) \cdot \exp\left(\frac{-\Delta E_g}{kT}\right) \cdot V_{CE} \cdot R_{th}}$$

$$= \frac{\frac{I_C}{V_A + V_{CB}} - \left(n - m - \frac{\Delta E_g}{KT}\right) \cdot \frac{I_C^2 \cdot R_{th}}{T}}{1 + (n - m - \frac{\Delta E_g}{KT}) \cdot \frac{I_C}{T} \cdot V_{CE} \cdot R_{th}} \cong \frac{I_C}{V_A + V_{CB}} - \left(n - m - \frac{\Delta E_g}{KT}\right) \cdot \frac{I_C^2 \cdot R_{th}}{T}$$

(4.36)

Equation (4.36) shows the self-heating output conductance with constant base current driven when emitter is heavily doped. The difference between equation (4.31) and equation (4.36) is $\Delta E_g/kT$ due to the reduction of band-gap energy when the emitter is heavily doped. When the emitter doping concentration is 10^{19} cm^{-3}, $\Delta E_g/kT$ is approximately 2. With n=1.25 (N_B=1*10^{17} cm^{-3}) and m=0.43 (N_E=1*10^{19} cm^{-3}) as shown in table 4.1. In this case $\left(n - m - \frac{\Delta E_g}{KT}\right)$ is roughly -1.2. Hence the self-heating output conductance with constant base current will be always positive when the emitter is heavily doped. This is because an emitter energy-gap reduction of ΔE_g causes a positive exponential temperature dependence of collector current while electron and hole mobility causes a negative power law temperature dependence of collector current. The exponential temperature dependence dominates.

4.2.4 Large-Signal Behavior of a Constant Base-emitter Voltage Driven BJT Transistor

Equation (4.13) lays the foundation for the analysis of large-signal behavior of a BJT driven by a constant base-emitter voltage. Since equation (4.13) is a function of temperature, collector-base voltage and base-emitter voltage, the total differential of I_C is

$$dI_C = \left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE},T} \cdot \Delta V_{CB} + \left.\frac{\partial I_C}{\partial T}\right|_{V_{BE},V_{CB}} \cdot \Delta T + \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{T,V_{CB}} \cdot \Delta V_{BE} \,. \tag{4.37}$$

By holding base-emitter voltage constant a self-heating output conductance is

$$g_{osh} = \left.\frac{dI_C}{dV_{CE}}\right|_{V_{BE}} = \left.\frac{dI_C}{dV_{CB}}\right|_{V_{BE}} = \left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE},T} + \left.\frac{\partial I_C}{\partial T}\right|_{V_{BE},V_{CB}} \cdot \frac{\partial T_j}{\partial V_{CB}} \,. \tag{4.38}$$

The derivative of the collector current with respect to the temperature $\left.\frac{\partial I_C}{\partial T}\right|_{V_{BE},V_{CB}}$ can be first solved as

$$\begin{aligned}
\left.\frac{\partial I_C}{\partial T}\right|_{V_{BE},V_{CB}} &= C(4-n)T^{3-n}\left[e^{qV_{BE}-E_g(0)\big/kT} - e^{qV_{BC}-E_g(0)\big/kT}\right]\cdot\left(1+\frac{V_{CB}}{V_A}\right) \\
&\quad + CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BE}-E_g(0)\big/kT}\right)\left(-\frac{(qV_{BE}-E_g(0))}{kT^2}\right) \\
&\quad - CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BC}-E_g(0)\big/kT}\right)\left(\frac{-(qV_{BC}-E_g(0))}{kT^2}\right) \\
&= C(4-n)T^{3-n}\left[e^{qV_{BE}-E_g(0)\big/kT} - e^{qV_{BC}-E_g(0)\big/kT}\right]\cdot\left(1+\frac{V_{CB}}{V_A}\right) \\
&\quad - CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BE}-E_g(0)\big/kT}\right)\left(\frac{(qV_{BE}-E_g(0))}{kT^2}\right) \\
&\quad + CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BC}-E_g(0)\big/kT}\right)\left(\frac{(qV_{BE}-E_g(0))}{kT^2}\right) \\
&\quad - CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BC}-E_g(0)\big/kT}\right)\left(\frac{(qV_{BE}-E_g(0))}{kT^2}\right) \\
&\quad - CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BC}-E_g(0)\big/kT}\right)\left(\frac{-(qV_{BC}-E_g(0))}{kT^2}\right) \\
&= (4-n)\frac{I_C}{T} - \frac{(V_{BE}-V_g(0))}{V_T\cdot T}\cdot I_C - \frac{V_{CE}}{V_T\cdot T}CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BC}-E_g(0)\big/kT}\right)
\end{aligned} \tag{4.39}$$

The derivative of the collector current with respect to the collector-base voltage $\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE},T}$ can be solved as follows

$$\begin{aligned}
\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE},T} &= \frac{CT^{4-n}}{V_T}\cdot e^{qV_{BC}-E_g(0)\big/kT}\cdot\left(1+\frac{V_{CB}}{V_A}\right)-\frac{CT^{4-n}}{V_A}\cdot e^{qV_{BC}-E_g(0)\big/kT} \\
&\quad+\frac{CT^{4-n}}{V_A}\cdot e^{qV_{BE}-E_g(0)\big/kT} \\
&= \frac{CT^{4-n}}{V_A}\cdot\left[e^{qV_{BE}-E_g(0)\big/kT}-e^{qV_{BC}-E_g(0)\big/kT}\right]+\frac{CT^{4-n}}{V_T}\cdot e^{qV_{BC}-E_g(0)\big/kT}\cdot\left(1+\frac{V_{CB}}{V_A}\right) \\
&= \frac{I_{CT}}{V_A+V_{CB}}+\underbrace{\frac{CT^{4-n}}{V_T}\cdot e^{qV_{BC}-E_g(0)\big/kT}\cdot\left(1+\frac{V_{CB}}{V_A}\right)}_{\text{Negligible}} \\
&\cong \frac{I_C}{V_A+V_{CB}}
\end{aligned} \tag{4.40}$$

A derivative of equation (4.1) under constant base-emitter voltage driven circumstance gives

$$\frac{\partial T_j}{\partial V_{CB}} = I_C R_{th} + V_{CE} R_{th}\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE}} . \tag{4.41}$$

Combining equation (4.39), (4.40) and (4.41) into equation (4.38) gives

$$\begin{aligned}
\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE}} &= \frac{\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE},T}+I_C R_{th}\cdot\left.\frac{\partial I_C}{\partial T}\right|_{V_{BE},V_{CB}}}{1-V_{CE}R_{th}\cdot\left.\frac{\partial I_C}{\partial T}\right|_{V_{BE},V_{CB}}} \\
&= \frac{\frac{I_C}{V_A+V_{CB}}+\frac{I_C^2 R_{th}}{T}\left(4-n-\frac{(V_{BE}-V_g(0))}{V_T}\right)-\frac{I_C R_{th}V_{CE}}{V_T\cdot T}CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BC}-E_g(0)\big/kT}\right)}{1-V_{CE}R_{th}\left[(4-n)\frac{I_C}{T}-\frac{(V_{BE}-V_g(0))}{V_T\cdot T}\cdot I_C-\frac{V_{CE}}{V_T\cdot T}CT^{4-n}\left(1+\frac{V_{CB}}{V_A}\right)\left(e^{qV_{BC}-E_g(0)\big/kT}\right)\right]}
\end{aligned} \tag{4.42}$$

Since $e^{qV_{BC}-E_g(0)\big/kT} << 0$, so equation (42) can be simplified as

$$\left.\frac{\partial I_C}{\partial V_{CB}}\right|_{V_{BE}} = \frac{\dfrac{I_C}{V_A + V_{CB}} + \dfrac{I_C^2 R_{th}}{T}\left[4 - n - \dfrac{(V_{BE} - V_g(0))}{V_T}\right]}{1 - V_{CE} R_{th}\dfrac{I_C}{T}\left[(4-n) - \dfrac{(V_{BE} - V_g(0))}{V_T}\right]} \cong \frac{I_C}{V_A + V_{CB}} + \frac{I_C^2 R_{th}}{T}\left[4 - n + \frac{(V_g(0) - V_{BE})}{V_T}\right] \tag{4.43}$$

where $V_g(0) = E_g(0)/q$, and $V_{CE} R_{th}\dfrac{I_C}{T}\left[(4-n) - \dfrac{(V_{BE} - V_g(0))}{V_T}\right] << 1$.

Equation (4.43) describes the self-heating output conductance of a BJT driven by constant base-emitter voltage. It consists of two parts. The first part, $\dfrac{I_C}{V_A + V_{CB}}$, represents the output conductance when V_{BE} and temperature are constant, which results from the Early effect. The second part results from the self-heating effect. Note that it is related to collector current, thermal resistance and a constant $\left[4 - n + \dfrac{(V_g(0) - V_{BE})}{V_T}\right]$ which has the value of approximately 14. Since the second part is always positive and much greater than the first part, the slope of the device output characteristic will be steeper than the results without self-heating effects considered.

4.3 A Method for Extraction of the Early Voltage and Thermal Resistance

4.3.1 Theory

An output conductance observed in I_C-V_{CE} characteristics originates from multiple sources including the Early effect and the self-heating effect. Since an accurate prediction of output conductance is desirable for high-power applications, identifying the early voltage and thermal resistance is important [35].

Equations (4.36) and (4.43) describe the output conductance when the device is driven by a constant base current or constant base-emitter voltage, respectively. Based on these two equations, a method for extraction of Early Voltage and thermal resistance is proposed.

Equation (4.36) and (4.43) can be rewritten in the following form,

$$\left.\frac{\Delta I_C}{\Delta V_{CB}}\right|_{IB} = \frac{I_C}{V_A + V_{CB}} - a \cdot I_C^2 \cdot \frac{R_{th}}{T}, \tag{4.44}$$

$$\left.\frac{\Delta I_C}{\Delta V_{CB}}\right|_{V_{BE}} = \frac{I_C}{V_A + V_{CB}} + b \cdot I_C^2 \cdot \frac{R_{th}}{T}. \tag{4.45}$$

The variable a, b, and T are defined as follows

$$a = \left(n - m - \frac{\Delta E_g}{KT} \right),$$

$$b = 4 - n + \frac{(V_g(0) - V_{BE})}{V_T},$$

$$T = T_A + P_{diss} \cdot R_{th}.$$

For extraction purposes, four measurement points are needed, two points with device driven by a constant base current and two by a constant base-emitter voltage respectively. The voltage-current pairs (I_{C1}, V_{CB1}) and (I_{C1}, V_{CB1}) are determined as the two measurement points with the device driven by a constant base current while (I_{C3}, V_{CB3}) and (I_{C4}, V_{CB4}) are denoted as the two measurement points with device driven by constant base-emitter voltage. P_{dissn} is denoted as power dissipation at measurement nth point.

Substituting measurement data into equation (4.44) and (4.45) gives

$$\frac{I_{C2} - I_{C1}}{V_{CB2} - V_{CB1}} + a \cdot I_{C1}^2 \cdot \frac{R_{th}}{T_A + P_{diss1} \cdot R_{th}} = \frac{I_{C1}}{V_A + V_{CB1}}, \tag{4.46}$$

$$\frac{I_{C4} - I_{C3}}{V_{CB4} - V_{CB3}} - b \cdot I_{C3}^2 \cdot \frac{R_{th}}{T_A + P_{diss3} \cdot R_{th}} = \frac{I_{C3}}{V_A + V_{CB3}}. \tag{4.47}$$

Letting $r = \frac{I_{C1}(V_A + V_{CB3})}{I_{C3}(V_A + V_{CB1})} \cong \frac{I_{C1}}{I_{C3}}, g' = \frac{I_{C2} - I_{C1}}{V_{CB2} - V_{CB1}} - r \cdot \frac{I_{C4} - I_{C3}}{V_{CB4} - V_{CB3}}, a' = a \cdot I_{C1}^2,$

$b' = b \cdot r \cdot I_{C1}^2$ and dividing equation (4.46) by equation (4.47) give

$$A \cdot R_{th}^2 + B \cdot R_{th} + C = 0 . \tag{4.48}$$

The variable A, B and C are defined as follows,

$$A = g' \cdot P_{diss1} \cdot P_{diss3} + a' \cdot P_{diss3} + b' \cdot P_{diss1} ,$$

$$B = g' \cdot T_A \cdot \left(P_{diss1} + P_{diss3} \right) + \left(a' + b' \right) \cdot T_A ,$$

$$C = g' \cdot T_A^2 .$$

The thermal resistance, Rth, can be obtained by solving the quadratic equation (4.48), and hence the Early voltage V_A can be obtained.

4.3.2 Parameters Mapping

For an unknown device, it is necessary to map the values of the variables, a and b, to the VBIC model parameters. The temperature dependence of the transport saturation current in the VBIC model is [5]

$$I_S(T) = I_S(T_{nom}) \left(\frac{T}{T_{nom}} \right)^{XIS} \exp\left[-\frac{q \cdot EA}{kT} \left(1 - \frac{T}{T_{nom}} \right) \right]^{1/N_F} . \tag{4.49}$$

Thus the temperature coefficient of collect current below knee current, I_{KF} with the reverse transport current neglected is

$$TC(I_C) = \frac{\partial I_C}{\partial T} = \frac{I_C}{T} \left(XIS + \frac{EA}{V_T} - \frac{V_{BE}}{N_F \cdot V_T} \right) . \tag{4.50}$$

Comparing this result to equation (4.45) gives

$$b = XIS + \frac{EA}{V_T} - \frac{V_{BE}}{N_F \cdot V_T} . \tag{4.51}$$

The intrinsic ideal base-emitter saturation current, I_{bei}, varies with temperature as [5]

$$I_{bei}(T) = I_{bei}(T_{nom}) \left(\frac{T}{T_{nom}} \right)^{XII} \exp\left[-\frac{q \cdot EAIE}{kT_2} \left(1 - \frac{T}{T_{nom}} \right) \right]^{1/N_{EI}} . \tag{4.52}$$

Thus the temperature coefficient of current gain over most of the mid current region with non-ideal base-emitter saturation current, I_{ben}, neglected is

$$TC(\beta_F) = \frac{\partial(I_C/I_B)}{\partial T} = \frac{\beta_F}{T}\left(XIS - XII + \frac{EA - EAIE}{V_T} + \frac{V_{BE}}{V_T}\left(\frac{1}{N_{EI}} - \frac{1}{N_F}\right)\right). \quad (4.53)$$

Comparing this result to equation (4.44) gives

$$a = -\left(XIS - XII + \frac{EA - EAIE}{V_T} + \frac{V_{BE}}{V_T}\left(\frac{1}{N_{EI}} - \frac{1}{N_F}\right)\right). \quad (4.54)$$

4.3.3 Procedure for Extraction

The procedure needed for extraction of the thermal resistance and the Early voltage is:

1. Obtain the value of I_S, I_{bei}, N_F, and N_{ei} through the forward Gummel plot. The transport saturation current, I_S, is the y-intercept value of the straight line I_C in figure 4.5, and the slope of that gives N_F. The ideal base-emitter saturation current, I_{bei}, is the y-intercept value of the straight line I_B in figure 4.5, and the slope of that gives N_{EI}. The base emitter voltage V_{BE} should be between 0.5 V and 0.8 V during the measurement [36].
2. Repeat step 1 to get data of I_S (T) and I_{bei} (T) at different temperatures [36].
3. Apply the data of I_S (T) and I_{bei} (T) obtained in step 2 to fit equation (4.49) and (4.52) with a least square approximation. The values of EA, EAIE, XIS and XII can be obtained through fitting [37].
4. Obtain the values of a and b by applying the extracted values of EA, EAIE, XIS and XII to equation (4.51) and (4.54) respectively.
5. Four measurement points are obtained, two points with a device driven by a constant base current and two by a constant base-emitter voltage. The measurement points should be selected in the mid current region.
6. Apply the data obtained in step 5 and the values of a and b in step 4 to equation (4.48) to get the thermal resistance, R_{th}, and the Early voltage, V_A.

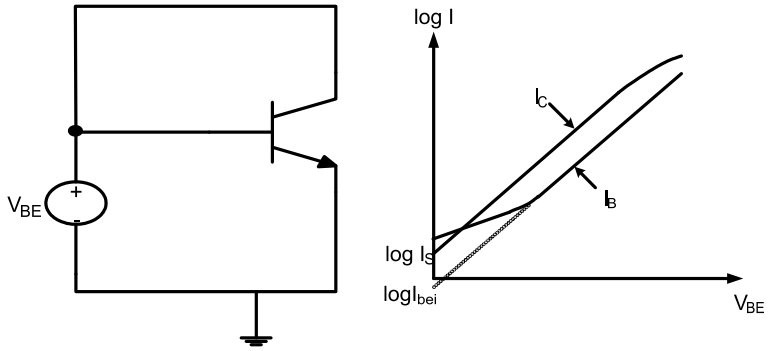

Figure 4.5 Forward Gummel plot

4.3.4 Simulation Results

Figure 4.6 shows the forward Gummel plot of the NPN transistor with the ambient temperature at 298 K. Figure 4.7 shows the variation of the transport saturation current with temperature. The circle represents the extracted I_S through the forward Gummel plot at different temperatures. The solid line represents fitting the data to equation (4.49) with the nominal temperature at 298 K. Figure 4.8 shows the variation of the ideal base-emitter saturation current with temperature. The circle represents the extracted I_{bei} data from the forward Gummel plot at different temperatures. The solid line represents fitting the data to equation (4.52) with the nominal temperature at 298K. Table 4.2 summarizes the values of a and b obtained through the extracted VBIC parameters and compares these to the values of a and b obtained via the VBIC model parameters attached in Appendix A.

Figure 4.9 shows the DC response with I_B=2 μA and T_A=298 K, and figure 4.10 shows the DC response with V_{BE}=819.1 mV and T_A=298 K. Four simulation points are obtained from figure 4.9 and figure 4.10. By applying the data of the four simulation points into equation (4.49), a thermal resistance value Rth=2908 is obtained compared to the thermal resistance value R_{th}=3000 in the model parameters. Thereby an Early voltage value, V_A=141, is obtained comparable to the Early voltage value V_A=156 in the model parameters.

Table 4.3 shows the variation of the thermal resistance, R_{th}, and the Early voltage, V_A, with the collector-emitter voltage, V_{CE}. It is seen that around V_{CE}=1.7 V, the extracted value of

R_{th} and V_A approach the real model value most. This is because the VBIC models the quasi-saturation effect and the Early voltage, V_A, models the critical point where the operating mode of transistor transfers from saturation to forward-active.

Table 4.2 Extracted parameters

	Extracted	Model
XIS	5.9973	5.75
XII	3.0001	3.77
EA (eV)	1.1127	1.3
EAIE (eV)	1.1257	1.2
NF	0.999	1
NEI	1.021	1
a	-2.49	-2.36
b	17.35	17.77

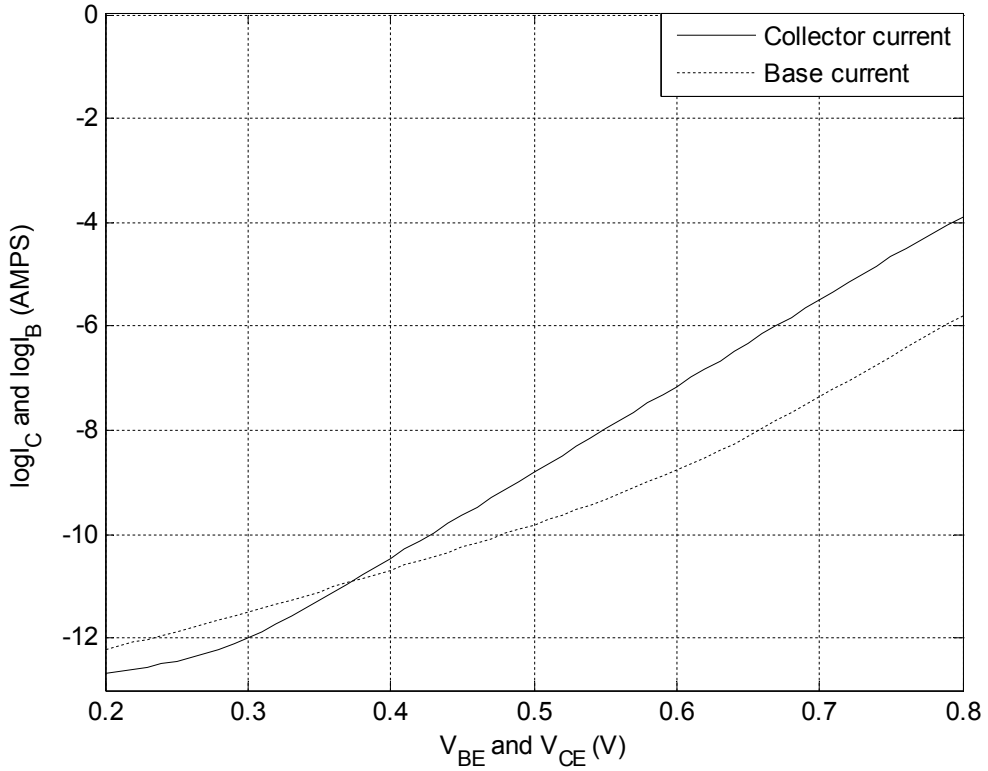

Figure 4.6 Forward Gummel plot with T_A=298 K

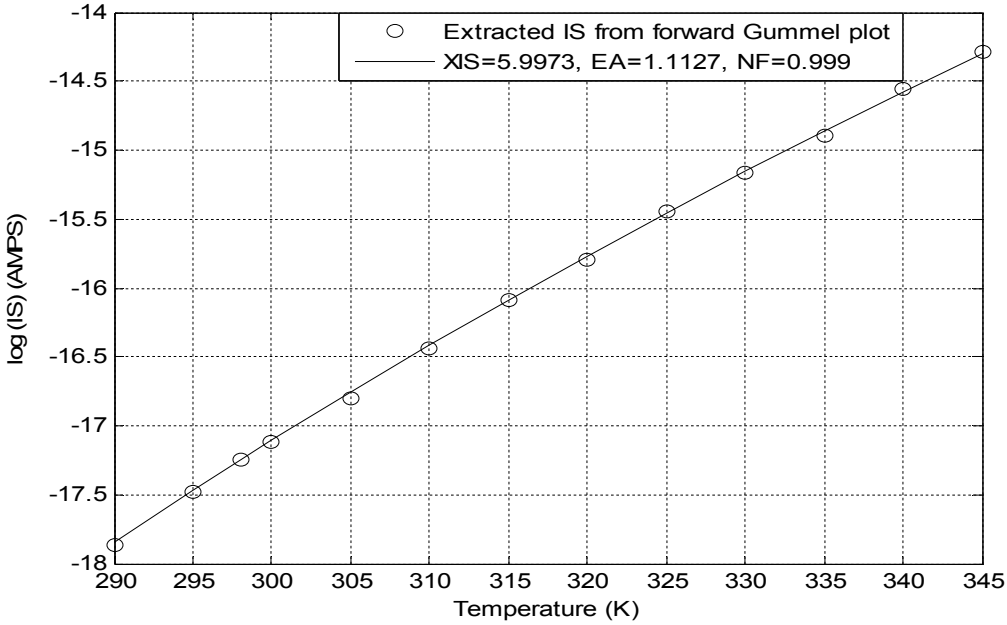

Figure 4.7 Transport saturation current versus temperature

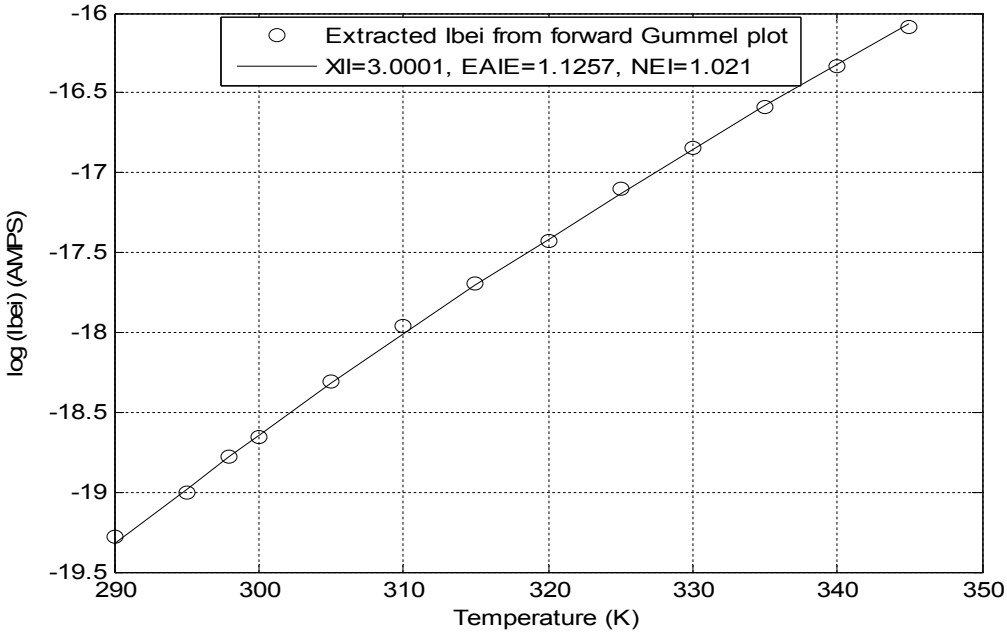

Figure 4.8 Ideal base-emitter saturation current versus temperature

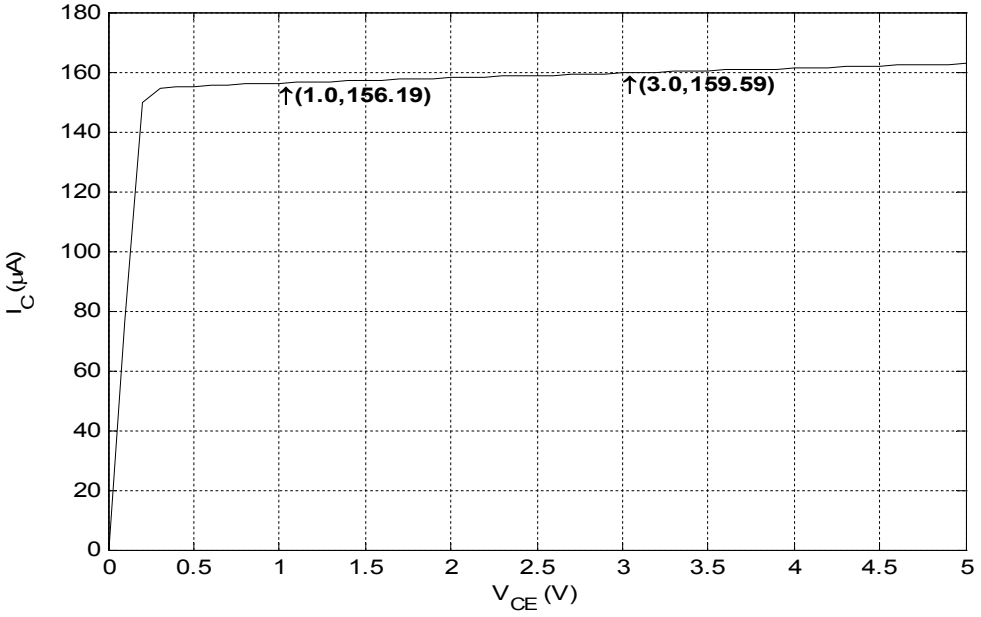

Figure 4.9 DC Response with constant I_B=2 μA, T_A=298K

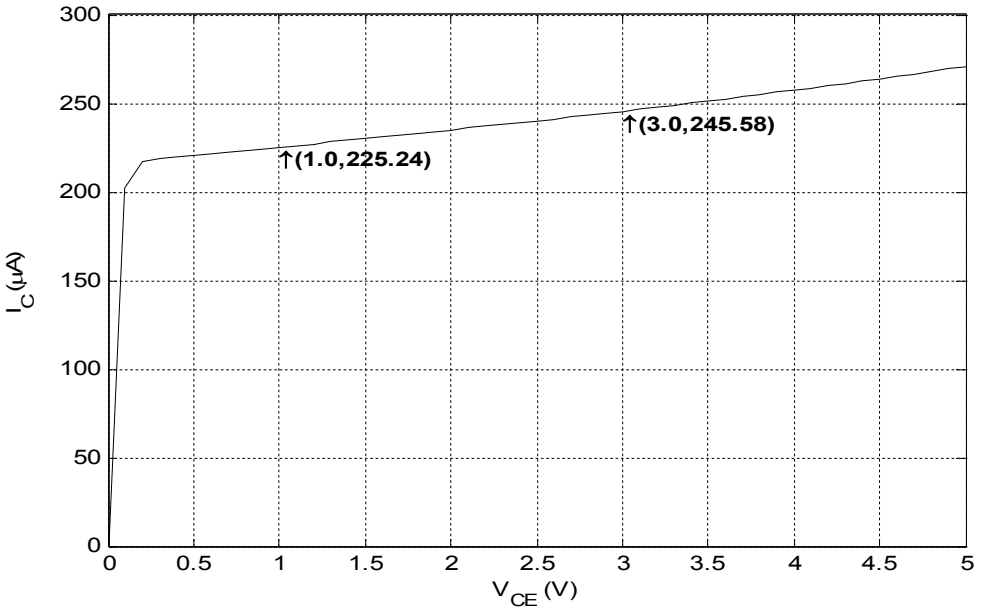

Figure 4.10 DC Response with constant V_{BE}=819.1 mV, T_A=298K

Table 4.3 R_{th} and V_A at different V_{CE}

VCE (V)	Rth (K/W)	VA (V)
1	2908	141
1.1	2924	144
1.2	2936	146
1.3	2950	148
1.4	2965	150
1.5	2980	152
1.6	2994	154
1.7	3008	155
1.8	3022	157
1.9	3037	159
2	3055	161
2.1	3069	163
2.2	3082	164
2.3	3099	166
2.4	3113	167
2.5	3132	169
2.6	3148	170
2.7	3165	172
2.8	3181	174
2.9	3197	175

4.4 Summary

The large-signal behaviors of a BJT transistor driven by a constant base-emitter voltage and a constant base current are investigated from both the physical and model point of view. Based on the derived formulation, a simple method of measuring the thermal resistance and the Early voltage is proposed.

CHAPTER 5

SELF-HEATING EFFECTS ON BJT SMALL-SIGNAL BEHAVIOR

This chapter investigates the BJT small-signal model with self-heating effects. Self-heating effects on BJT small-signal behavior are examined by investigating the two-port network parameters. The output impedance of current mirrors is also investigated. Techniques to reduce self-heating effects are also discussed.

5.1 Small-Signal Model with Self-Heating Effects

Figure 5.1 shows a simplified BJT small-signal equivalent circuit with self-heating effects included [38]. The variables, I_C, I_B, V_B, V_C, T_A, T_j and P_{th} are the DC collector current, base current, base voltage, collector voltage, ambient temperature, device operating temperature and thermal power dissipation respectively. R_{th} and C_{th} are the thermal resistance and thermal capacitance respectively. The DC device operating temperature, T_j, is equal to $T_A+P_{th}R_{th}$, and the DC thermal power dissipation, P_{th}, is equal to $I_BV_B+I_CV_C$ for the common emitter configuration.

In small-signal operation, i_b and i_c are the small-signal base and collector currents while v_b and v_c are the small-signal voltages driving the base and collector terminal, respectively, t_j is the induced small-signal device operating temperature variation, g_{bt} and g_{ct} are the base and collector thermal transconductance, respectively, g_m is the intrinsic transconductance, g_π is the intrinsic input conductance and g_o is the intrinsic output conductance.

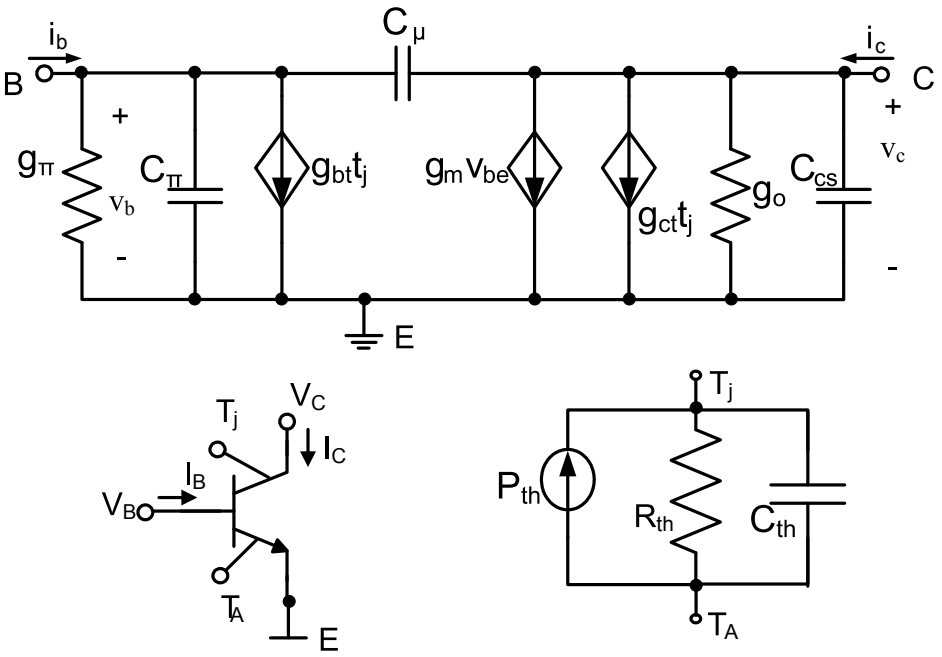

Figure 5.1 Simplified BJT small-signal equivalent circuit with self-heating effects included [38]

The Kirchhoff's Current Law (KCL) is applied to the at base and collector terminal,

$$i_b = \left(g_\pi + s\left(C_\pi + C_\mu\right)\right)\cdot v_b - sC_\mu \cdot v_c + g_{bt}\cdot t_j\,, \tag{5.1}$$

$$i_c = \left(g_m - sC_\mu\right)\cdot v_b + \left(g_o + s\left(C_\mu + C_{CS}\right)\right)\cdot v_c + g_{ct}\cdot t_j\,, \tag{5.2}$$

where $g_\pi = \dfrac{\partial I_B}{\partial V_B}$, $g_o = \dfrac{\partial I_C}{\partial V_C}$, $g_m = \dfrac{\partial I_C}{\partial V_B}$, $g_{bt} = \dfrac{\partial I_B}{\partial T_j}$ and $g_{ct} = \dfrac{\partial I_C}{\partial T_j}$.

The induced small-signal power dissipation variation, dP_{th}, is

$$dP_{th} = i_c \cdot V_C + I_C \cdot v_c + i_b \cdot V_B + I_B \cdot v_b\,. \tag{5.3}$$

Therefore the induced small-signal device operating temperature variation, t_j, can be expressed as

$$t_j = \left(i_c \cdot V_C + I_C \cdot v_c + i_b \cdot V_B + I_B \cdot v_b\right)\cdot Z_{th} \tag{5.4}$$

where the thermal impedance, Z_{th} (s), is equal to $R_{th}/\left(1 + sR_{th}C_{th}\right)$.

Substituting equation (5.1) and (5.2) into equation (5.4) gives

$$t_j Y_{th} = \left(I_C + g_o V_C\right)\cdot v_c + \left(I_B + g_\pi V_B + g_m V_C\right)\cdot v_b + \left(g_{ct} V_C + g_{bt} V_B\right)\cdot t_j \,. \tag{5.5}$$

Here the variable, Y_{th}, is the thermal admittance and is the reciprocal of the thermal impedance. Therefore the small-signal device operating temperature variation, t_j, is [38]

$$t_j = \frac{\left(I_C + g_o V_C\right)\cdot v_c + \left(I_B + g_\pi V_B + g_m V_C\right)\cdot v_b}{Y_{th} - \left(g_{ct} V_C + g_{bt} V_B\right)} \,. \tag{5.6}$$

The small-signal equivalent circuit with self-heating effects included in figure 5.1 can be simplified as a two-port equivalent circuit in figure 5.2 where $i_1=i_b$, $i_2=i_c$, $v_1=v_b$ and $v_2=v_c$. The parameters, y_{11}, y_{12}, y_{21} and y_{22}, can be found and interpreted as follows: $y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0}$ is the input admittance with the output short-circuited, $y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0}$ is the reverse transconductance with the input short-circuited, $y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0}$ is the forward transconductance with the output short circuited and $y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0}$ is the output admittance with the input short circuited [33].

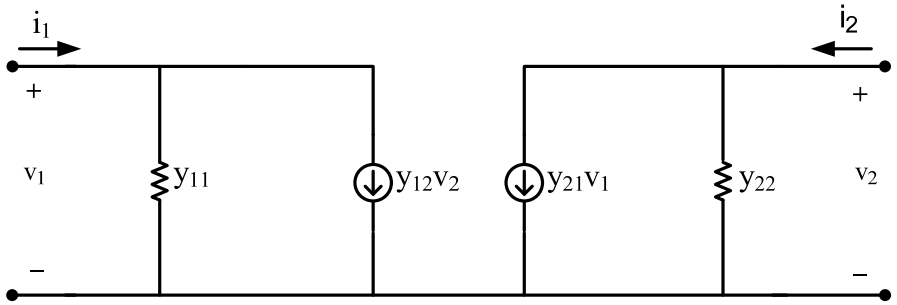

Figure 5.2 Admittance-parameter, two-port equivalent circuit [33].

By applying the above parameters definition and substituting equation (5.6) into equation (5.1) and (5.2), the small-admittance parameters with self-heating effects included are thus obtained as follows: [38]

$$y_{11}(s) = g_\pi + \frac{g_{bt}(I_B + g_\pi V_B + g_m V_C)}{Y_{th} - (g_{ct} V_C + g_{bt} V_B)} + s(C_\pi + C_\mu), \tag{5.7}$$

$$y_{12}(s) = \frac{g_{bt}(I_C + g_o V_C)}{Y_{th} - (g_{ct} V_C + g_{bt} V_B)} - sC_\mu, \tag{5.8}$$

$$y_{21}(s) = g_m + \frac{g_{ct}(I_B + g_\pi V_B + g_m V_C)}{Y_{th} - (g_{ct} V_C + g_{bt} V_B)} - sC_\mu \tag{5.9}$$

$$y_{22}(s) = g_o + \frac{g_{ct}(I_C + g_o V_C)}{Y_{th} - (g_{ct} V_C + g_{bt} V_B)} + s(C_\mu + C_{CS}) \tag{5.10}$$

Note that by neglecting $g_{bt}V_B$ and substituting equation (4.39) and equation (4.40) for g_{ct} and g_o respectively, the DC output admittance with self-heating in equation (5.10) agrees with the large-signal output conductance with self-heating in equation (4.43). It should be also noted from equation (5.10) that the output admittance is composed of two components. One is the intrinsic component, i.e. $g_o + s(C_\mu + C_{CS})$, the other is the thermal induced component, i.e. $\frac{g_{ct}(I_C + g_o V_C)}{Y_{th} - (g_{ct} V_C + g_{bt} V_B)}$. The output admittance tends to decrease with frequency until the effect of thermal capacitance dominates the thermal induced component. After that, the output admittance will be dominated by the intrinsic component. This behavior can be also explained by the following pole-zero analysis of the output impedance.

The output impedance with self-heating included when the input is short circuited can be obtained by using equation (5.10) as [39]

$$Z_o(s)\big|_{v_{in}=0} = \frac{1}{y_{22}(s)} = \frac{\dfrac{1}{g_o + X_g R_{th}/(1 - MR_{th})}\left(1 + \dfrac{s}{(1 - MR_{th})/R_{th}C_{th}}\right)}{\dfrac{R_{th}C_{th}C_{eq}}{g_o(1 - MR_{th}) + X_g R_{th}} s^2 + \dfrac{R_{th}C_{th}g_o + C_{eq}(1 - MR_{th})}{g_o(1 - MR_{th}) + X_g R_{th}} s + 1} \tag{5.11}$$

where $M = g_{ct}V_C + g_{bt}V_B$, $X_g = g_{ct}(I_C + g_o V_C)$, and $C_{eq} = C\mu + C_{CS}$. Assuming $MR_{th} << 1$ and $R_{th}C_{th}g_o >> C_{eq}$, a left half plane (LHP) zero and two LHP poles can be identified as [39]

$$z = (1 - MR_{th}) \cdot \frac{1}{R_{th}C_{th}} \ , \tag{5.12}$$

$$p_{1,2} = \frac{-g_o \pm \sqrt{g_o^2 - 4 \cdot \frac{\left(g_o + X_g R_{th}\right) \cdot C_{eq}}{R_{th}C_{th}}}}{2C_{eq}} . \tag{5.13}$$

By using Taylor series expansion of the square root function, i.e. $\sqrt{1+x} \cong 1 + x/2$ and assuming $(g_o+X_gR_{th})C_{eq} << g_o^2R_{th}C_{th}$, the two poles can be further simplified as

$$p_1 \cong \frac{\left(g_o + X_g R_{th}\right)}{g_o} \cdot \frac{1}{R_{th}C_{th}} , \tag{5.14}$$

$$p_2 \cong \frac{g_o}{C_{eq}} . \tag{5.15}$$

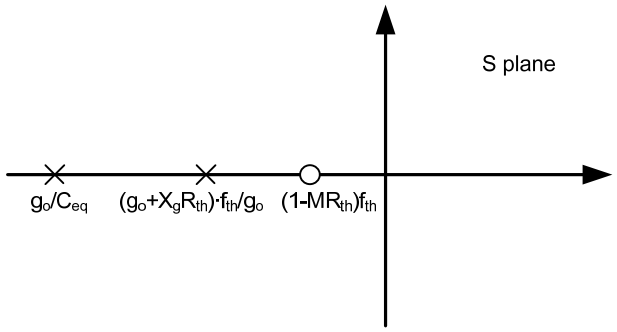

Figure 5.3 Poles and zero of the output impedance with self-heating included.

It can be inferred from equation (5.12) and (5.14) that the LHP thermal induced zero precedes the thermal induced LHP pole, and the intrinsic pole of the device positions leftmost as in figure 5.3. Thus the magnitude of the output impedance begins to increase at 20 dB/decade at $f=f_z$, becomes flat at $f=f_{p1}$, and then begins to drop at 20 dB/decade at $f=f_{p2}$.

The frequency response behavior of the output impedance can affect the gain of amplifier significantly. Figure 5.4 shows a common-emitter amplifier with a current source load driven by a voltage source. The output impedance response behavior dominates the gain

response of the amplifier as shown in figure 5.5. The gain magnitude starts to increase around $f_z \approx 31.6$ KHz at 20 dB/decade and begins to drop around $f_{p2} \approx 12.6$ MHz.

It is clear that techniques that raise the effective output impedance can reduce error due to self-heating. On the one hand, raising the effective output impedance can make the intrinsic component of the output impedance dominate in magnitude; on the other hand, it can also make the intrinsic pole closer to the thermal induced zero and pole pair that the frequency response will be more flat. These techniques include cascoding and negative feedback as with Wilson current mirrors or emitter degeneration [26].

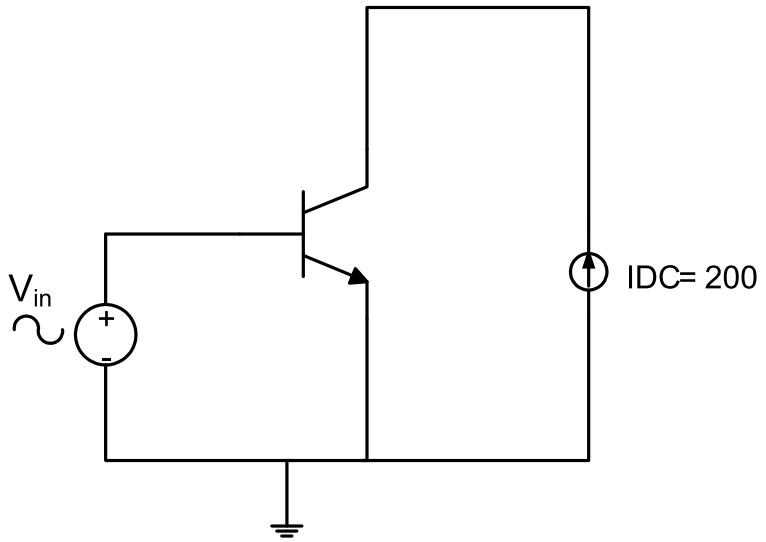

Figure 5.4 A common-emitter amplifier with a current source load driven by a voltage source.

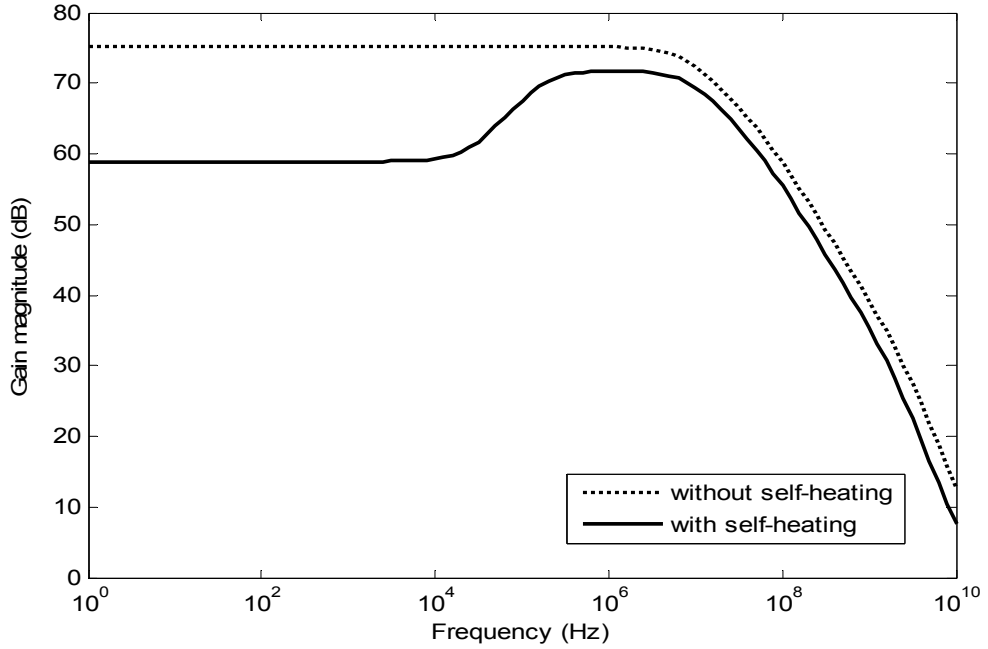

Figure 5.5 The gain magnitude of the amplifier shown in figure 5.4.

5.2 Self-heating Effects on the Output Impedance of a Current Mirror

Current mirrors are widely used in analog integrated circuits both as biasing elements and as loads for amplifier stages. When used as a load in amplifiers, the high output impedance of current mirrors results in high voltage gain at low-supply voltages. This section investigates self-heating effects on the output impedance of current mirrors.

The simplest form of a current mirror, which composed of two transistors, is shown in figure 5.6. The output resistance of the current mirror without self-heating in the forward-active region is $r_o = V_A / I_{bias}$ [33]. Neglecting the resistance looking into the base of Q_1, the output impedance of the current mirror can be approximated using equation (5.11). The location of the zero and the two poles can be obtained via equation (5.12), (5.14) and (5.15). Thus the magnitude of the output impedance begins to increase at 20 dB/decade at $f=f_z$, becomes flat at $f=f_{p1}$, and then begins to drop at 20 dB/decade at $f=f_{p2}$.

The frequency response of the output impedance of the simple current mirror of figure 5.6 using the VBIC model in appendix A is shown in figure 5.7. The area of the transistors used

in the simulation is 8x5 μm^2, I_{bias}=200 μA, V_{cc}=5V and V_o=5V. In the low frequency region, the thermal induced conductance is significant that the output resistance of the simple current mirror with self-heating is approximately 60% of the one without self-heating. As frequency increases up to the thermal induced zero, the thermal induced conductance begins to decrease, thus the output resistance of the simple current mirror continues to increase until the frequency reaches the thermal induced pole, f_{p1}. The output resistance becomes flat. As the frequency reaches the intrinsic pole, f_{p2}, the output resistance of the simple current mirror begins to drop.

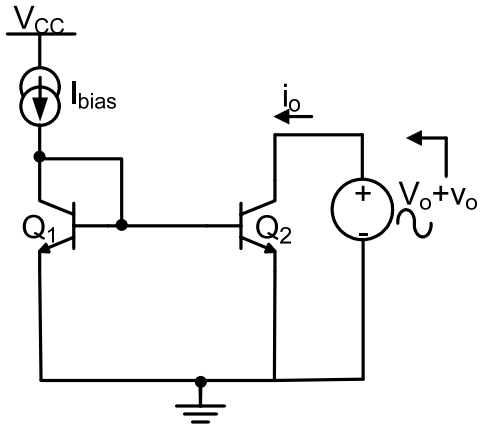

Figure 5.6 A simple current mirror and its output impedance simulation configuration.

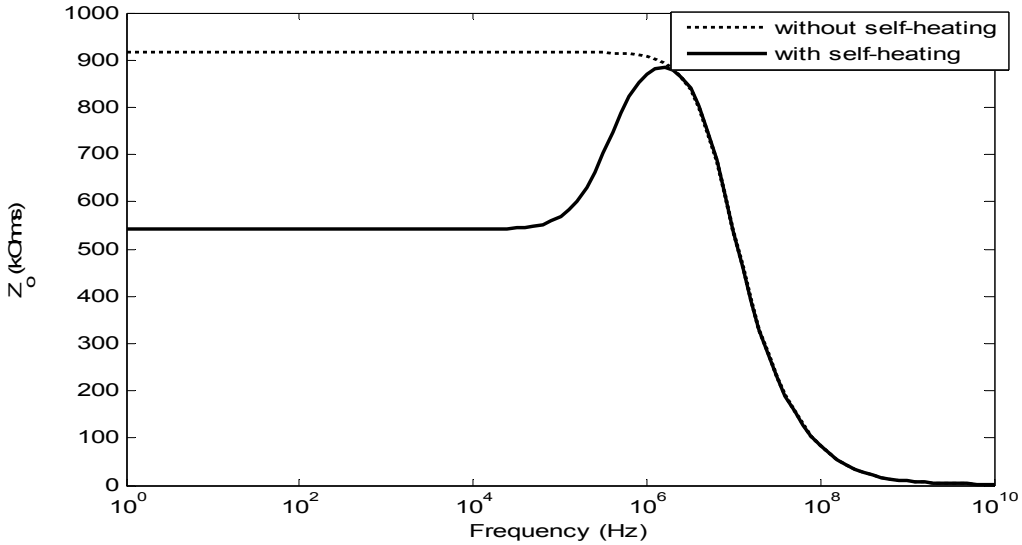

Figure 5.7 The magnitude of the output impedance of the simple current mirror in figure 5.6.

Raising the effective output impedance is an effective approach to reduce error in the current mirror. The cascode current mirror shown in figure 5.8 offers a very high output resistance. The output resistance of the cascode current mirror is approximately $\beta r_{o4}/2$ where β is the current gain [33].

The output admittance of the cascade current mirror can be approximated as [39]

$$y_{22} = \left[g_{o4} - \frac{(g_{m4} + g_{o4}) \cdot g_{o4}}{g_{m4} + g_{o4} + g_{o2} + g_{\pi 4}} + sC_{\mu} \right] + \left[\left(g_{ct} - \frac{(g_m + g_{o4}) \cdot (g_{bt} + g_{ct})}{g_m + g_{o4} + g_{o2} + g_{\pi 4}} \right) \cdot \left(\frac{(I_c + g_{o4} V_c) \cdot Z_{th}}{1 - (g_{ct} V_c + g_{bt} V_b) \cdot Z_{th}} \right) \right]. \tag{5.16}$$

Assuming $g_m + g_{o4} >> g_{o2} + g_{\pi 4}$, equation (5.16) can be simplified as

$$y_{22} = \left[g_{o4} - \frac{(g_{m4} + g_{o4}) \cdot g_{o4}}{g_{m4} + g_{o4} + g_{o2} + g_{\pi 4}} + sC_{\mu} \right] - \frac{g_{bt} (I_c + g_{o4} V_c) \cdot Z_{th}}{1 - (g_{ct} V_c + g_{bt} V_b) \cdot Z_{th}}. \tag{5.17}$$

Because g_{bt} is generally 1/20 of g_{ct}, it is cleared that the thermal induced admittance is greatly suppressed by comparing equation (5.17) to equation (5.10). At the same time, the intrinsic admittance is greatly reduced by cascoding transistors.

The frequency response of the output impedance of the cascode current mirror of figure 5.8 is shown in figure 5.9. The VBIC model in appendix A is used in this simulation. The area of the transistors is 8x5 μm^2, I_{bias}=200 μA, V_{cc}=5V and V_o=5V. As shown in figure 5.9, the low frequency error is suppressed in cascode current mirror at the expense of bandwidth and the output resistance of the cascode current mirror without self-heating is slightly higher than without self-heating.

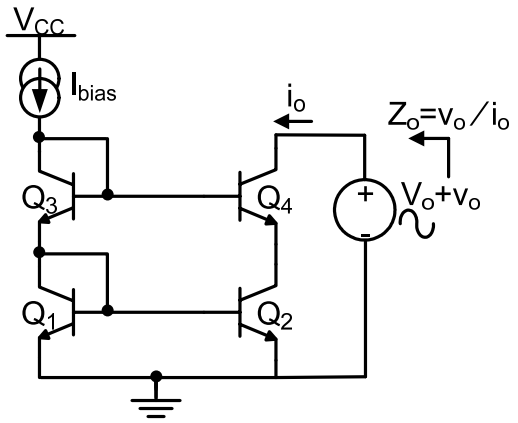

Figure 5.8 Cascode current mirror and its output impedance simulation configuration.

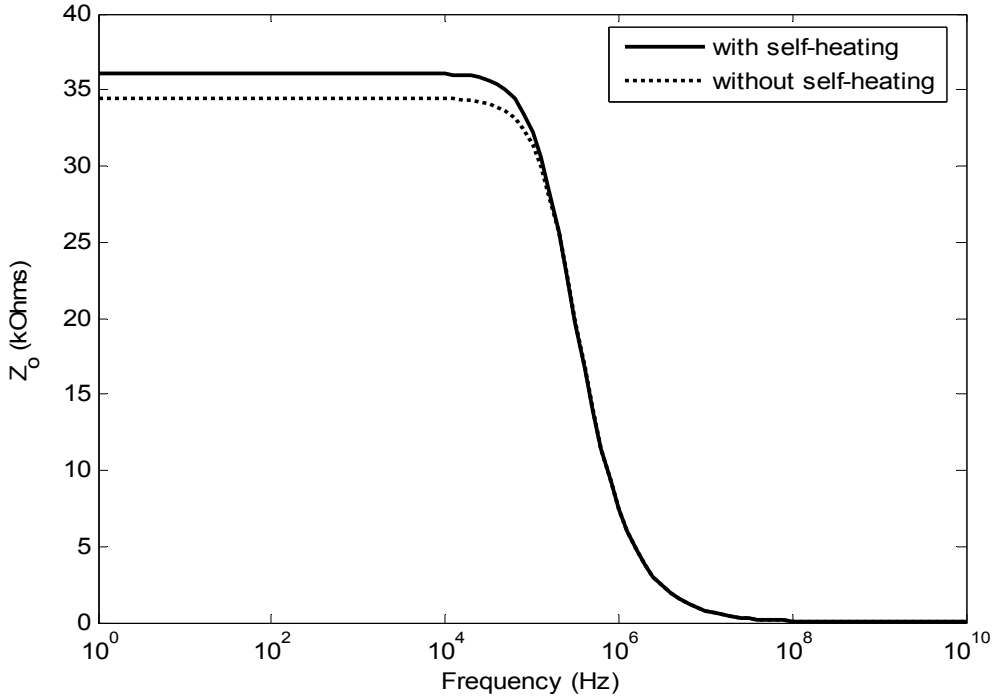

Figure 5.9 The magnitude of the output impedance of the cascode current mirror in figure 5.8.

Another technique to raising the effective output impedance is using negative feedback. The Wilson current mirror is shown in figure 5.10. The Wilson current mirror uses negative feedback through Q_2, activating Q_1 to reduce the base-current error and raising the output

resistance. The output resistance of the Wilson current mirror without self-heating can be approximated as $\beta r_{o3}/2$ which is the same as the cascode current mirror [33].

The frequency response of the output impedance of the Wilson current mirror of figure 5.10 is shown in figure 5.11. The VBIC model in appendix A is used in this simulation. The area of the transistors is 8x5 μm^2, I_{bias}=200 μA, V_{cc}=5V and V_o=5V. As shown in figure 5.11, the output resistance of the Wilson current mirror displays the same characteristic as the cascode current mirror.

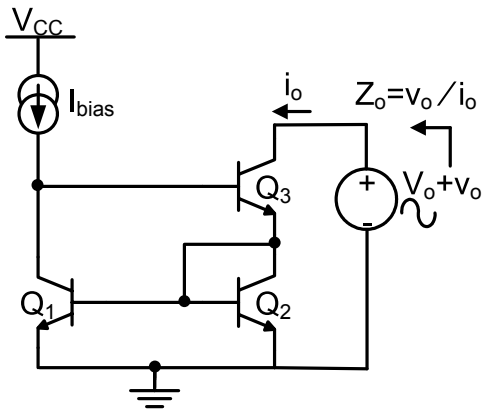

Figure 5.10 Wilson current mirror and its output impedance simulation configuration.

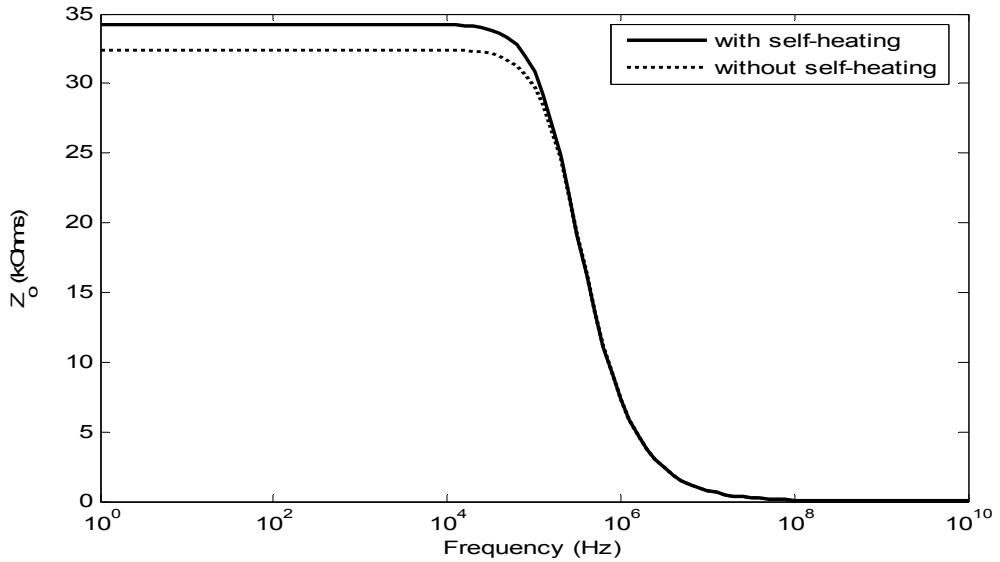

Figure 5.11 The magnitude of the output impedance of the Wilson current mirror in figure 5.10.

5.3 Summary

The self-heating effects on the small-signal behavior of a BJT are discussed. The output impedance of a BJT with self-heating displays serious reduction at low frequency due to thermal induced zero and poles. Gain of amplifiers is reduced at low frequency. Techniques that raise the output resistance can reduce such errors, i.e. cascoding, negative feedback as with the Wilson current mirrors, or emitter degeneration.

CHAPTER 6

THE EFFECT OF SELF-HEATING IN TRANSIENT OPERATION

Errors caused by self-heating effects in transient operation can be substantial, especially for some switching circuits. In switching circuits the change of device operating temperature causes a change in the the base-emitter voltage which consequently a thermal tail in the output of the transistor. The change of device operating temperature is an exponentially increasing function of time with a time constant equal to the product of the thermal resistance and the thermal capacitance. Therefore, the settling time of switching circuits can be significantly degraded by self-heating since thermal transients take a much longer time to settle. This chapter investigates the effect of self-heating on the transient operation and applies it to the operation analysis of a high speed voltage buffer.

6.1 Time Dependent Device Temperature

The change in device temperature, $\Delta T=T_j-T_A$, can be described in terms of the power dissipation in the device, P_{th}, thermal resistance, R_{th}, thermal capacitance, C_{th}, and ambient temperature, T_A, by the electro-thermal model in figure 6.1:

$$C_{th}\frac{d\Delta T}{dt}+\frac{\Delta T}{R_{th}}-P_{th}=0. \tag{6.1}$$

The solution for ΔT in equation (6.1) is an exponentially increasing function of time with a time constant, $\tau_{th}=R_{th}C_{th}$, and an asymptotic value of $P_{th}R_{th}$. It is in the following form [1]:

$$\Delta T=P_{th}R_{th}\left(1-\exp\left(-\frac{t}{\tau_{th}}\right)\right). \tag{6.2}$$

Equation (6.2) shows that the change in device temperature varies with time, and reaches the asymptotic value of $P_{th}R_{th}$ after a time delay of about five times the time constant τ_{th}. Figure 6.2 shows a typical curve of variation of the change in device temperature with time in a transient

operation. Because of the device temperature change with time, the collector current and the base-emitter voltage (V_{BE}) will also change with time. Figure 6.3 shows a typical curve of the variation of voltage with time in transient operation.

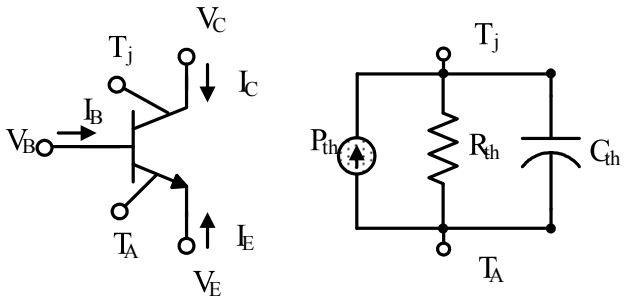

Figure 6.1 Electro-thermal model of BJT.

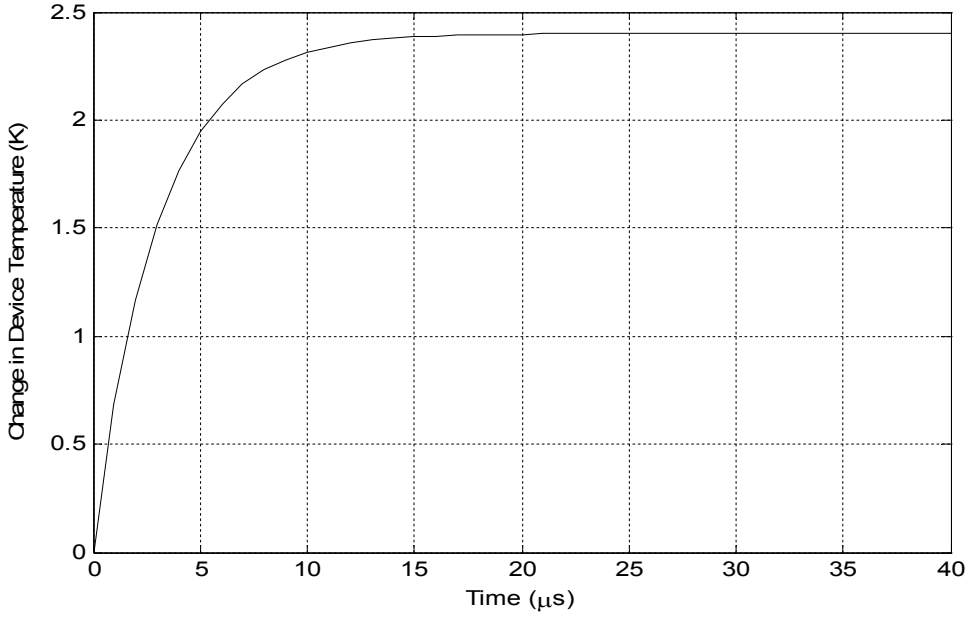

Figure 6.2 Typical curve of variation of the change in device temperature with time.

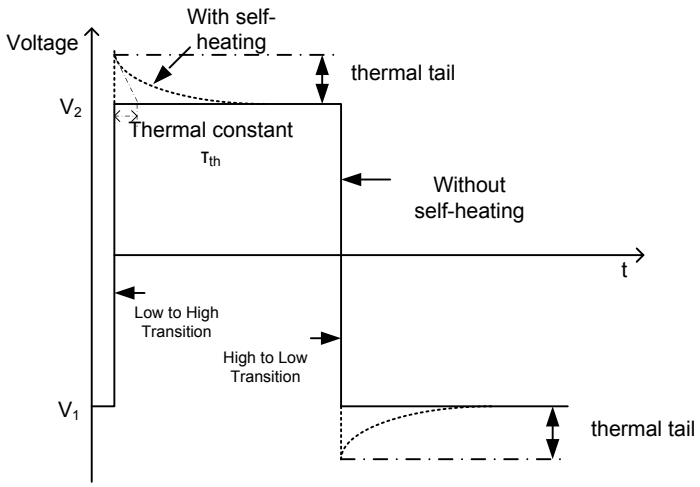

Figure 6.3 Typical curve of the variation of voltage with time.

6.2 Self-Heating on Collector Current

In bipolar devices, collector current is a function of V_{BE} (base-emitter voltage), V_{CE} (Collector-emitter voltage) and device operating temperature. For a constant base-emitter voltage driven BJT device, the collector current can be represented as a second order, two – dimensional Taylor series expansion:

$$I_C(T_A+\Delta T_j, V_{CE}+\Delta V_{CE}) = I_C(T_A, V_{CE}) + \left[\left.\frac{\partial I_C}{\partial T}\right|_{V_{CE}} \cdot \Delta T_j + \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{T_A} \cdot \Delta V_{CE}\right] + \frac{1}{2}\left[\left.\frac{\partial^2 I_C}{\partial T^2}\right|_{V_{CE}} \cdot \Delta T_j^{\,2} + \left.\frac{\partial^2 I_C}{\partial V_{CE}^2}\right|_{T_A} \cdot \Delta V_{CE}^2 + 2 \cdot \frac{\partial^2 I_C}{\partial T \partial V_{CE}} \cdot \Delta T_j \cdot \Delta V_{CE}\right] \quad (6.3)$$

where T_A is the ambient temperature, ΔT_j is the change of device operating temperature because of self-heating, $\frac{\partial I_C}{\partial T}$ and $\frac{\partial^2 I_C}{\partial T^2}$ are the first and second order temperature derivative of collector current respectively, $\frac{\partial I_C}{\partial V_{CE}}$ and $\frac{\partial^2 I_C}{\partial V_{CE}^2}$ are the first and second order collector-

emitter voltage derivative of collector current respectively and $\frac{\partial^2 I_C}{\partial T \partial V_{CE}}$ is the second order cross derivative of collector current.

Figure 6.4 shows a transistor biased with a constant base emitter voltage, V_{BE} and a collector-emitter voltage, V_{CE}. With collector-emitter voltage increasing from V_{CE} to $V_{CE}+\Delta V_{CE}$, the increasing power dissipation will increase the device operating temperature. Here the base-emitter voltage, V_{BE}, is 819.1 mV, the collector-emitter voltage, V_{CE}, is 4.15 V, the change in collector-emitter voltage, ΔV_{CE}, is 1 V, and the ambient temperature, T_A, is 27 °C. Figures 6.5 and 6.6 show the variations of the first and second order temperature derivative of collector current with temperature when V_{BE}=819.1 mV and V_{CE}=4.15 V, and the first and second order temperature derivative are 9.31 μA/K, 0.313 μA/K^2 respectively at 27 °C. Figures 6.7 and 6.8 show the variations of the first and second order collector-emitter voltage derivative of collector current with collector-emitter voltage when V_{BE}=819.1 mV and T_A=27 °C, and first and second order collector-emitter voltage derivative are 1.13 μA/V, -0.0491 μA/V^2 respectively when V_{CE}=4.15 V. The SPECTRE simulator is used here to get these curves.

The change of device operating temperature from the ambient temperature can be expressed as:

$$\Delta T_j = (V_{CE} + \Delta V_{CE}) \cdot I_C (T_A + \Delta T_j, V_{CE} + \Delta V_{CE}) \cdot R_{th} \tag{6.4}$$

Substituting equation (6.3) into equation (6.4) and solving a quadratic equation about ΔT_j gives ΔT_j =3.665 C. Thus collector current after a change in collector-emitter voltage change can be expressed as

$$I_C(T_A+\Delta T_j, V_{CE}+\Delta V_{CE}) = \underbrace{I_C(T_A, V_{CE})}_{199.7} + \left[\underbrace{\left.\frac{\partial I_C}{\partial T}\right|_{V_{CE}} \cdot \Delta T}_{34.14} + \underbrace{\left.\frac{\partial I_C}{\partial V_{CE}}\right|_{T_A} \cdot \Delta V_{CE}}_{1.125} \right] +$$

$$\frac{1}{2!}\left[\underbrace{\left.\frac{\partial^2 I_C}{\partial T^2}\right|_{V_{CE}} \cdot \Delta T_j^{\,2}}_{4.20} + \underbrace{2 \cdot \frac{\partial^2 I_C}{\partial T \partial V_{CE}} \cdot \Delta T_j \cdot \Delta V_{CE}}_{0.374} + \underbrace{\left.\frac{\partial^2 I_C}{\partial V_{CE}^2}\right|_{T_A} \cdot \Delta V_{CE}^2}_{-0.05} \right]$$

$$= 237.20\,\mu\text{A}$$

Figure 6.9 shows how collector current varies with collector-emitter voltage with and without self-heating effects. The simulation result agrees well with the analytical result. It can be seen that the second order dependence of collector current on the collector-emitter voltage and the cross term are negligible. By considering the first order dependence of collector current on temperature and the collector-emitter voltage, the collector current of a BJT driven by fixed base-emitter voltage with self-heating effect can be roughly estimated.

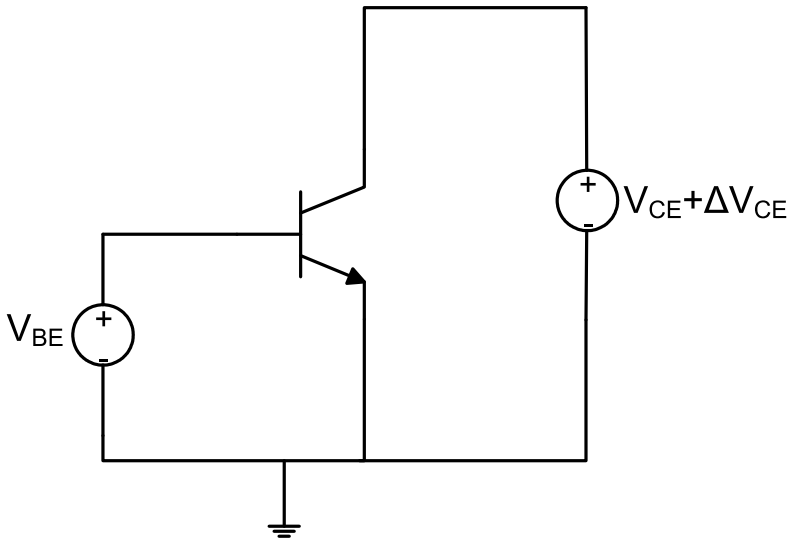

Figure 6.4 A biased BJT with collector-emitter voltage changing.

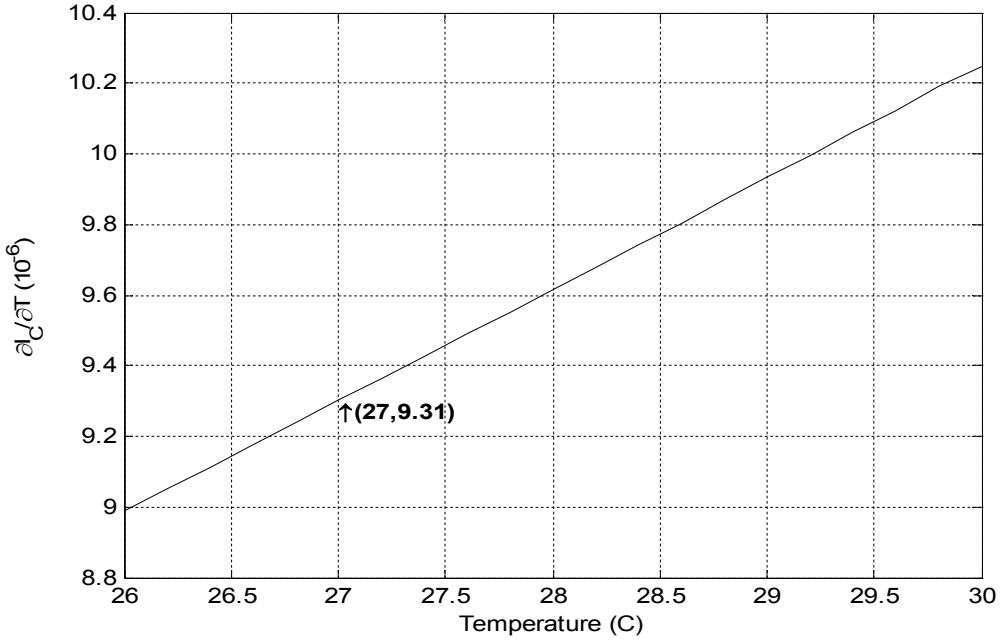

Figure 6.5 First order temperature derivative of collector current with V_{BE}=819.1 mV and V_{CE}=4.15 V.

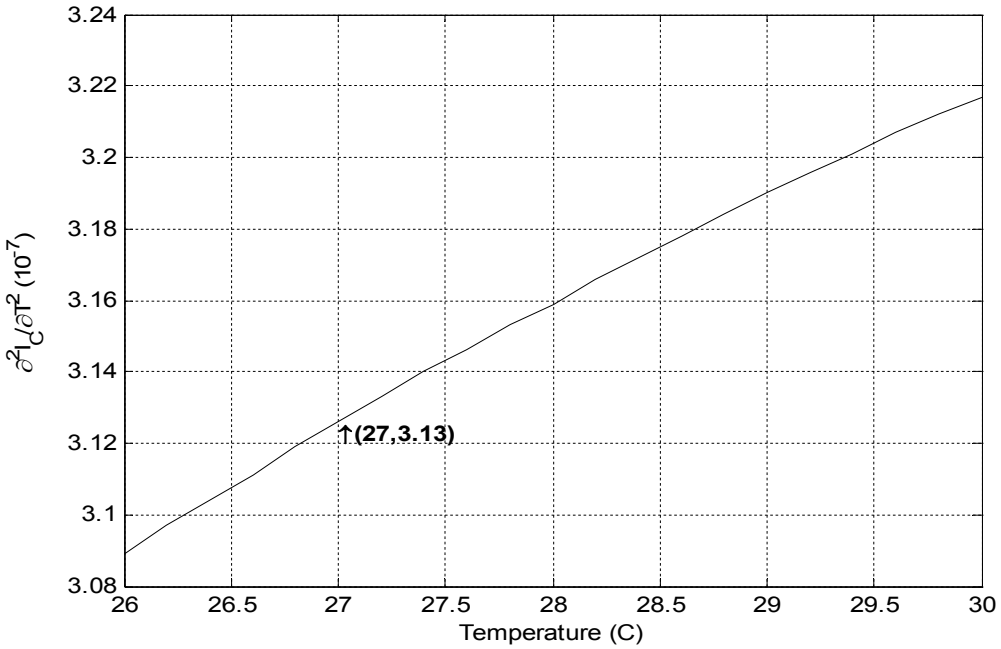

Figure 6.6 Second order temperature derivative of collector current with V_{BE}=819.1 mV and V_{CE}=4.15 V.

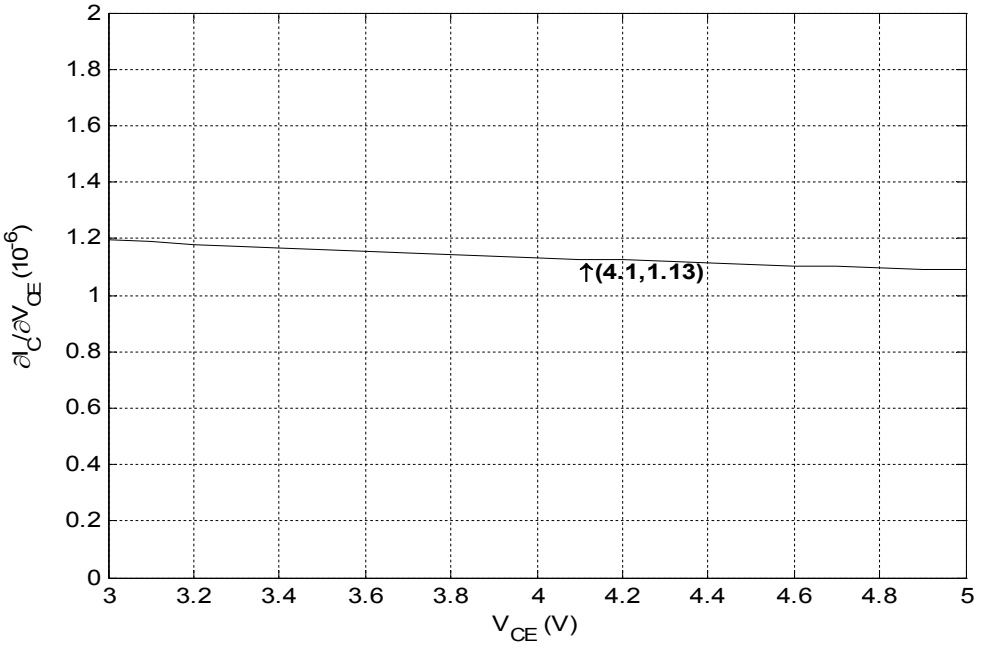

Figure 6.7 First order collector-emitter voltage derivative of collector current with V_{BE}=819.1 mV and T_A=27 C.

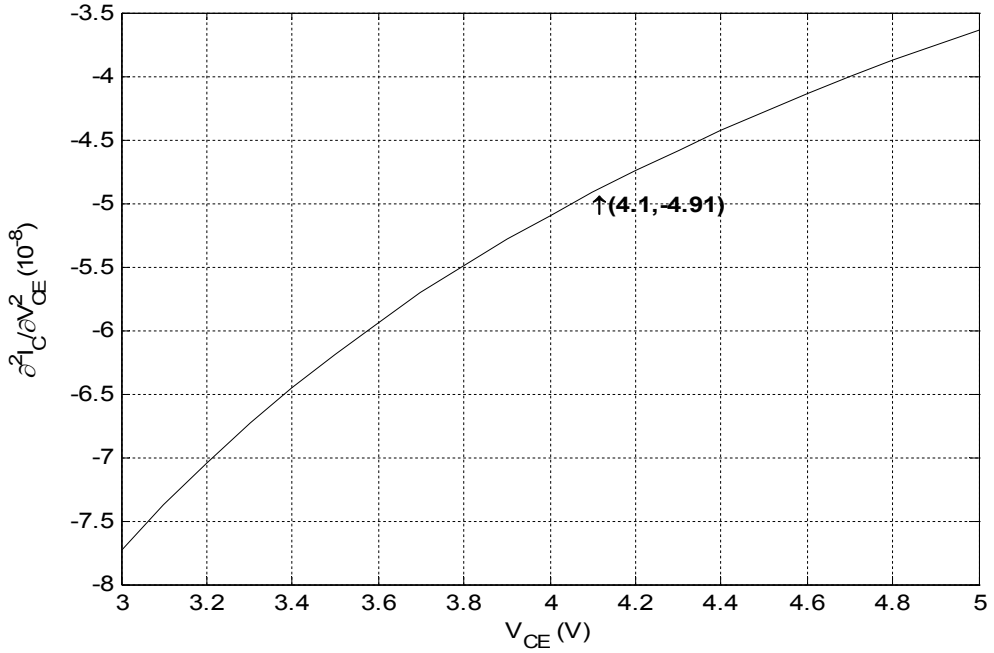

Figure 6.8 Second order collector-emitter voltage derivative of collector current with V_{BE}=819.1 mV and T_A=27 C.

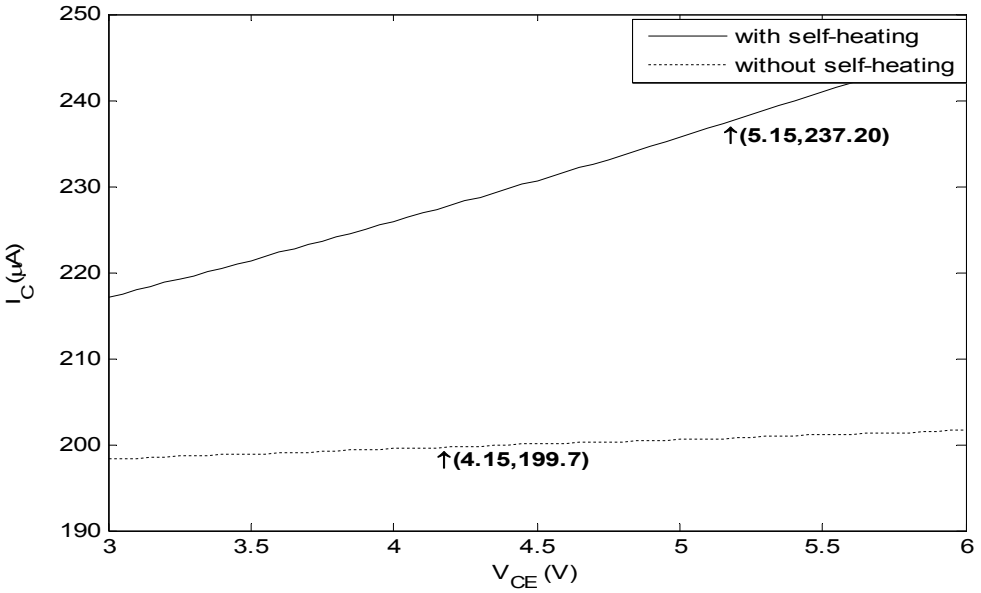

Figure 6.9 Variation of collector current with V_{CE} when with and without self-heating effects, V_{BE}=819.1 mV and T_A=27 C.

6.3 Temperature Effect on the Base-Emitter Voltage

The temperature coefficient of the base-emitter voltage is a function of collector current and temperature. The collector current can be expressed as [29]

$$I_C = C \cdot T^{4-n} \cdot \exp\left(\frac{V_{BE} - V_g(0)}{kT/q}\right) \tag{6.5}$$

where q is the electronic charge, k is Boltzmann's constant, C is an empirical constant, the band-gap voltage at 0 K, $V_g(0)$, is equal to $E_g(0)/q$ and n is the mobility exponent for $\mu = \mu_0 \left(T/T_0\right)^{-n}$. Solving for V_{BE} gives

$$V_{BE} = V_g(0) + V_T \cdot \ln\left(I_C / \left(C \cdot T^{4-n}\right)\right) \tag{6.6}$$

Therefore the temperature coefficient of the base-emitter voltage at a fixed collector current can be approximated as [29]

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{I_C} = -\frac{k}{q}(4-n) + \frac{k}{q} \cdot \ln\left(\frac{I_C}{C \cdot T^{4-n}}\right) \tag{6.7}$$

Figure 6.10 shows the variation of the base-emitter voltage with temperature for NPN and PNP transistors used in the dissertation at 200 μA. The temperature coefficients of the base-emitter voltages for NPN and PNP transistors are -1.45 mV/°C and -1.3 mV/°C respectively.

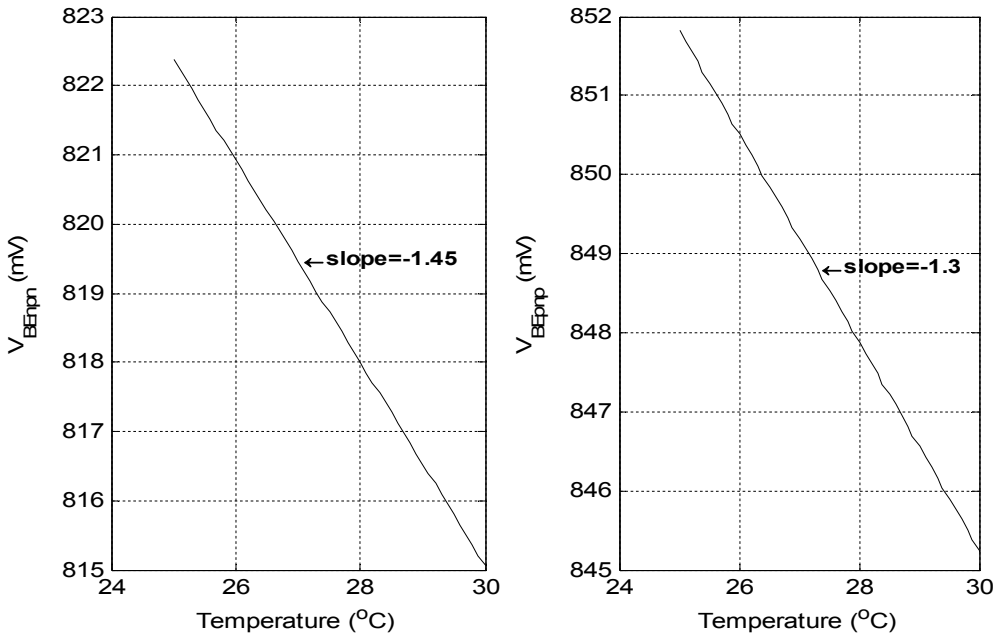

Figure 6.10 The variation of the base-emitter voltage with temperature for NPN and PNP transistors at 200 μA

6.4 Self-Heating on Transient Operation of Voltage Buffer

6.4.1 Voltage Buffer Biased with an Ideal Current Source

Figure 6.11 shows a voltage buffer biased with an ideal constant current source. Since the input voltage switches from low to high, the power dissipation of the transistor Q_2 decreases because of the decrease of the collector-emitter voltage of Q_2. Hence the device operating temperature of Q_2 decreases. Consequently, the base-emitter voltage of Q_2 increases with device operating temperature decreasing, and the collector current of Q_2 will also reflect the change of the base-emitter voltage and the device operating temperature.

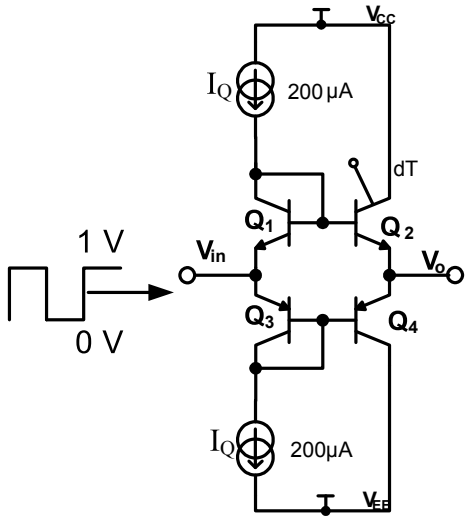

Figure 6.11 Voltage buffer biased with ideal constant current source.

There are three important times to be considered:

1. The time just before the input step occurs is t=0-, or t=0-δ. At this time, the static self-heating effect before the input step is applied. The notation $\underset{Rth}{\Delta} I_C$ denotes the change in collector current resulting from self-heating to the collector current when self-heating is ignored, i.e. $\underset{Rth}{\Delta} I_C = I_C(t = 0-, R_{th} = \text{finite}) - I_C(t = 0-, R_{th} = 0)$, where the symbol $\underset{Rth}{\Delta}$ is an abbreviation for “change in because of static self-heating effect”.
2. The time, t=0+, or t=0+δ. At this time, the Early effect caused by the change in the collector-emitter voltage is applied. The notation $\underset{E}{\Delta} I_C$ denotes the change in collector current due to the Early effect caused by the change in the collector-emitter voltage, where the symbol $\underset{E}{\Delta}$ is an abbreviation for “change in because of the Early effect”.
3. The circuit response reaches equilibrium at $t>>5\tau_{th}$. The dynamic self-heating effect, i.e. the change of power dissipation after the input step is applied at this time. The notation $\underset{Vin}{\Delta} I_C$ denotes the change in collector current due to the change of power dissipation caused by the input step, where the symbol $\underset{Vin}{\Delta}$ is an abbreviation for “change in because of the power

dissipation". For simplicity purpose, t=final is used to represent this time.

After the input voltage, V_{in}, steps from 0 to 1, the device operating temperature of transistor Q_2 varies with time ignoring the Early effect as,

$$T_{jQ2}(t>0+) = T_{jQ2}(t=0-) + \underset{Vin}{\Delta} T_{Q2}(t), \tag{6.8}$$

$$\underset{Vin}{\Delta} T_{Q2}(t) = -\Delta V_{in} \cdot I_{CQ2}(t=0-) \cdot R_{thQ2} \cdot (1 - e^{-\frac{t}{R_{thQ2}C_{thQ2}}}). \tag{6.9}$$

As a result the base-emitter voltage of Q_2 varies with time as:

$$\underset{Vin}{\Delta} V_{BEQ2}(t>0+) = \left.\frac{\partial V_{BE}}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_{Q2}(t) \tag{6.10}$$

where $\left.\frac{\partial V_{BE}}{\partial T}\right|_{I_{CQ2}(t=0-)}$ is the base-emitter voltage temperature coefficient at fixed collector current $I_{CQ2}(t=0-)$.

The collector current of Q_2 after the input step can be found using Kirchhoff's Voltage Law (KVL) around translinear loop composed of transistors Q1 through Q4 as:

$$\begin{aligned}
I_{CQ2}(t>0+) &= I_Q \cdot \exp\left[\frac{V_P(t>0+) - V_N(t>0+)}{V_T(t>0+)}\right] + \left.\frac{\partial I_C}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_{Q2}(t) \\
&= I_Q \cdot \exp\left[\frac{V_P(t=0-) - V_N(t=0-) + \underset{Vin}{\Delta} V_{BEQ2}(t)}{V_T(t>0+)}\right] + \left.\frac{\partial I_C}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_{Q2}(t) \\
&= \underbrace{I_Q \cdot \exp\left[\frac{V_P(t=0-) - V_N(t=0-)}{\frac{kT_{jQ2}(t>0+)}{q}}\right]}_{I_2(t=0-)} \cdot \exp\left[\frac{\left.\frac{\partial V_{BE}}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_{Q2}(t)}{\frac{kT_{jQ2}(t>0+)}{q}}\right] \\
&\quad + \left.\frac{\partial I_C}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_{Q2}(t) \\
&\cong I_{CQ2}(t=0-) \cdot \exp\left[\frac{\left.\frac{\partial V_{BE}}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_{Q2}(t)}{\frac{kT_{jQ2}(t>0+)}{q}}\right] + \left.\frac{\partial I_C}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_{Q2}(t)
\end{aligned} \tag{6.11}$$

If $\rho = \left.\frac{\partial V_{BE}}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \frac{q}{k}$, and the exponential function is expanded as a Taylor series to the second order, taking into account the Early effect, equation (6.11) becomes

$$I_{CQ2}(t>0+) \cong I_{CQ2}(t=0-) \cdot \left[1 + \frac{\rho \cdot \underset{Vin}{\Delta} T_{Q2}(t)}{T_{jQ2}(t>0+)} + \frac{1}{2} \cdot \left(\frac{\rho \cdot \underset{Vin}{\Delta} T_{Q2}(t)}{T_{jQ2}(t>0+)} \right)^2 \right] + \left.\frac{\partial I_C}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_2(t) + \left.\frac{\partial I}{\partial V_{CE}}\right|_{I_{CQ2}(t=0-)} \cdot \Delta V_{in} \quad (6.12)$$

Equation (6.12) describes the variation of collector current of Q_2 with time after the input step. The first term in equation (6.12) addresses the effect of the base-emitter change with device operating temperature on collector current, the second term describes the direct effect of device temperature change on collector current, and the third term deals with the Early effect.

The power transistors Q_2 and Q_4 have different temperature coefficients of the collector current and the base-emitter voltage because NPN and PNP transistors mismatch. Therefore the thermal tail magnitude of the collector current of Q_2's and Q_4's is different, as is the base-emitter voltage. The base-emitter voltages of Q_2's and Q_4's are then corrected to satisfy the KVL around the translinear loop and the Kirchhoff's Current Law (KCL) at the V_o node.

A few variables are to be defined here before further discussion. The magnitude of thermal tail of the corrected base-emitter voltage is

$$\underset{Vin}{\Delta} V_{BE,C} = V_{BE,C}(\mathrm{t = final}) - V_{BE,C}(\mathrm{t = 0+}) \quad (6.13)$$

where the subscript C stands for the corrected. The magnitude of thermal tail of the corrected collector current is

$$\underset{Vin}{\Delta} I_{C,C} = I_{C,C}(\mathrm{t = final}) - I_{C,C}(\mathrm{t = 0+}) . \quad (6.14)$$

Substituting equation (6.12) and (6.13) into equation (6.14) while ignoring the second order effect gives

$$\underset{Vin}{\Delta} I_{C,C} = g_{ct} \cdot \underset{Vin}{\Delta} T + g_m \cdot \underset{Vin}{\Delta} V_{BE,C} \tag{6.15}$$

where $g_{ct} = \left.\frac{\partial I_C}{\partial T}\right|_{I_2(t=0-)}$, $g_m = \left.\frac{I_C}{V_T}\right|_{t=0-}$ and $\underset{Vin}{\Delta} T = \Delta V_{in} \cdot I_C(t=0-) \cdot R_{th}$.

The KCL at node V_o requires that the thermal tail magnitude of the collector current of Q_2 and Q_4 be the same assuming $\beta_2=\beta 4$. This gives

$$g_{ct,Q2} \cdot \underset{Vin}{\Delta} T_{Q2} + g_{m,Q2} \cdot \underset{Vin}{\Delta} V_{BEQ2,C} = g_{ct,Q4} \cdot \underset{Vin}{\Delta} T_{Q4} + g_{m,Q4} \cdot \underset{Vin}{\Delta} V_{EBQ4,C}. \tag{6.16}$$

The KVL around the translinear loop requires that

$$\underset{Vin}{\Delta} V_{BEQ2,C} + \underset{Vin}{\Delta} V_{EBQ4,C} = \underset{Vin}{\Delta} V_{BEQ1,C} + \underset{Vin}{\Delta} V_{EBQ3,C}. \tag{6.17}$$

Since Q_1 and Q_3 are biased with ideal constant current sources in figure 6.11 and the change of power dissipation is small because of the diode connection, the base-emitter voltage of Q_1 and Q_3 barely change. If the base-emitter voltage change in Q_1 and Q_3 is ignored, equations (6.16) and (6.17) are combined to give

$$\begin{aligned} \underset{Vin}{\Delta} V_{BEQ2,C} &= \frac{g_{ct,Q4} \cdot \underset{Vin}{\Delta} T_{Q4} - g_{ct,Q2} \cdot \underset{Vin}{\Delta} T_{Q2}}{g_{m,Q2} + g_{m,Q4}} \\ \underset{Vin}{\Delta} V_{BEQ2,C} &= -\underset{Vin}{\Delta} V_{EBQ4,C} \\ \underset{Vin}{\Delta} V_{BEQ2,C}(t>0+) &= \underset{Vin}{\Delta} V_{BEQ2,C} \cdot (1 - e^{-\frac{t}{R_{thQ2}C_{thQ2}}}) \end{aligned} \tag{6.18}$$

Substituting $\underset{Vin}{\Delta} V_{BEQ2,C}(t)$ for $\underset{Vin}{\Delta} V_{BEQ2}(t)$ in equation (6.11) gives

$$\begin{aligned} I_{CQ2}(t>0+) \cong I_{CQ2}(t=0-) \cdot \left[1 + \frac{\underset{Vin}{\Delta} V_{BEQ2,C}(t)}{V_{TQ2}(t>0+)} + \frac{1}{2} \cdot \left(\frac{\underset{Vin}{\Delta} V_{BEQ2,C}(t)}{V_{TQ2}(t>0+)} \right)^2 \right]. \\ + \left.\frac{\partial I_C}{\partial T}\right|_{I_{CQ2}(t=0-)} \cdot \underset{Vin}{\Delta} T_2(t) + \left.\frac{\partial I}{\partial V_{CE}}\right|_{I_{CQ2}(t=0-)} \cdot \Delta V_{in} \end{aligned} \tag{6.19}$$

Figure 6.12 shows the variations of collector current and base-emitter voltage of Q_2 with time after t=0+ based on equation (6.19) while figure 6.13 shows simulation results. The input

switches from 0 V to 1 V, time period is 4 ms, and the rise time is 1 ns. The thermal resistance of Q_1 through Q_4 is 3000 K/W, and the thermal capacitance is 1.69 nF. Therefore the thermal time constant, τ_{th}, is about 5 μs. The response reached 99.3% of the steady state after about $5\tau_{th}$. The corrected base-emitter voltage increases from 818.8 mV to 819.8 mV. Figure 6.14 shows the variations of collector current and base-emitter voltage of Q_4 with time after t=0+. This is based on equation (6.19) while figure 6.15 shows the corresponding simulation results. The collector current of Q_4 displays the same characteristic as Q_2 while the corrected base-emitter voltage of Q_4 decreases from 848.3 mV to 847.3 mV. The difference between the corrected base-emitter voltage thermal tail magnitude and the uncorrected voltage based on equation (6.10) is about 0.1 mV.

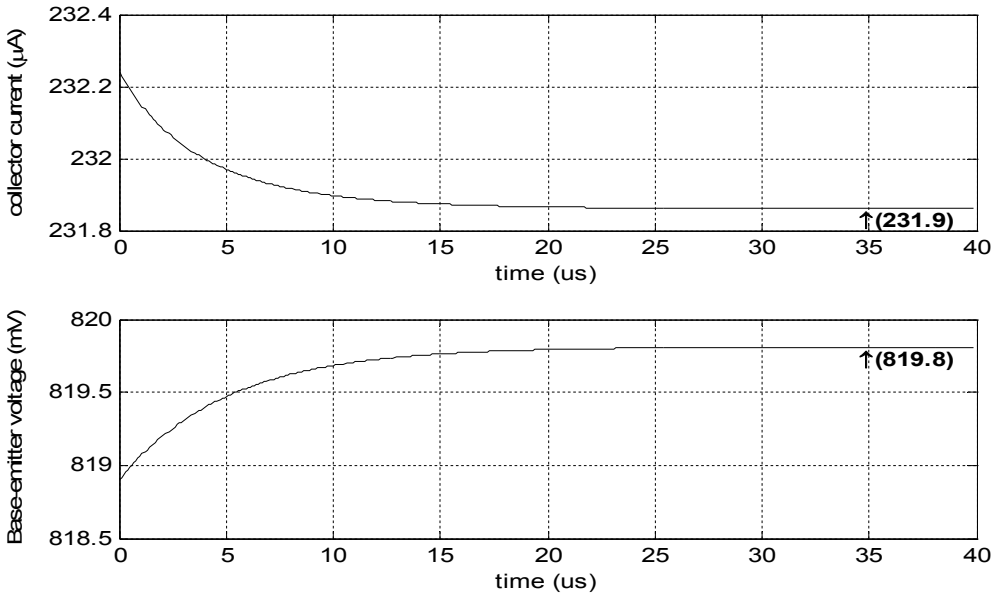

Figure 6.12 The variations of collector current and base-emitter voltage of Q_2 with time after initial input step based on equation (6.19).

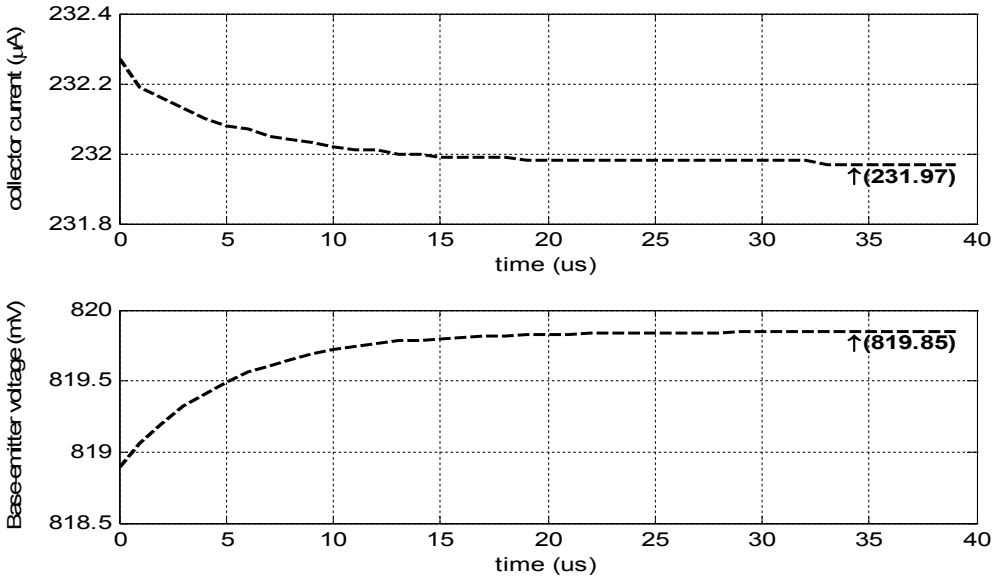

Figure 6.13 The simulated variations of collector current and base-emitter voltage of Q_2 with time after initial input step.

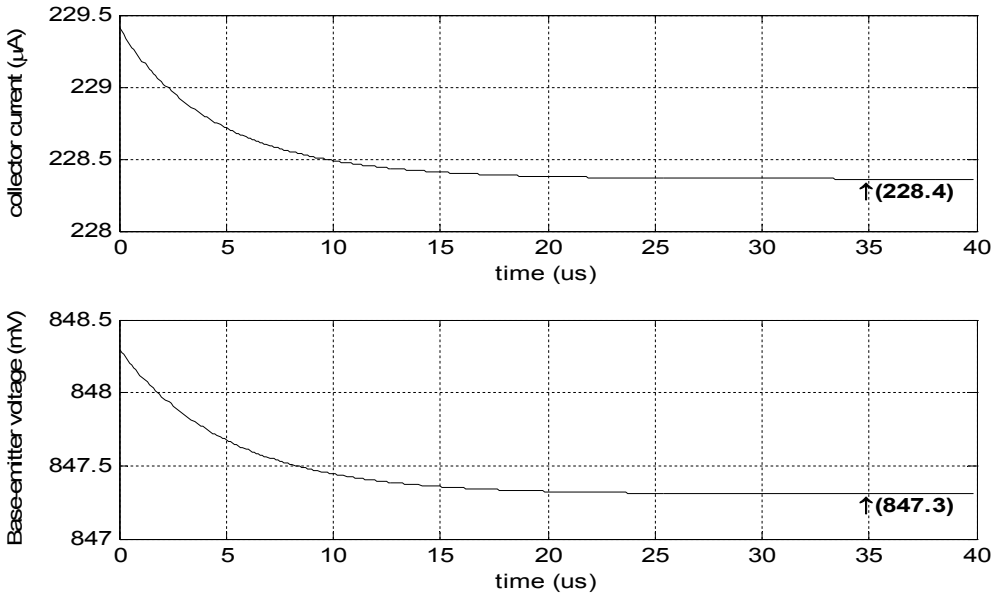

Figure 6.14 The variations of collector current and base-emitter voltage of Q_4 with time after initial input step based on equation (6.19).

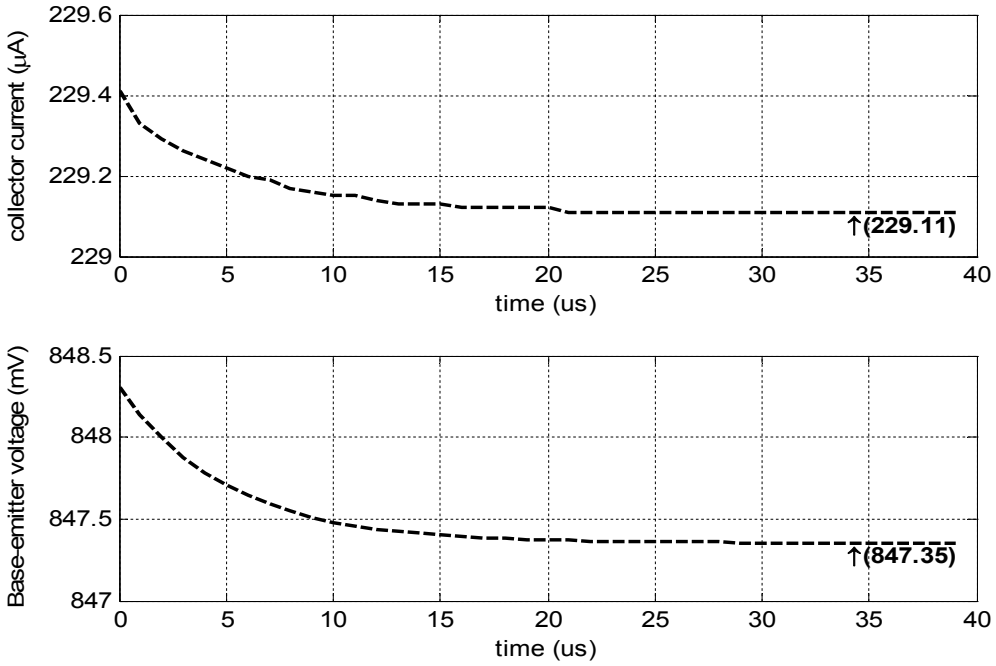

Figure 6.15 The simulated variations of collector current and base-emitter voltage of Q_4 with time after initial input step.

6.4.2 Voltage Buffer Biased with a Current Mirror

Figure 6.16 shows a simple voltage buffer biased with a current mirror. If the input voltage switches from low to high, the collector current of transistor Q_5 decreases because of the decrease of device operating temperature while the collector current of Q_7 increases. The thermal tail of bias currents are reflected to the base-emitter voltage change of transistors Q_1 and Q_3, and then reflected to the thermal tail of the output voltage. The mechanism of transient operation in the current mirror is first investigated.

Below this branch notations are defined for simplicity: $I_C = I_C(t < 0-, R_{th} = 0)$,

$I_{C,0-} = I_C(t = 0-, R_{th} = \text{finite})$, $I_{C,0+} = I_C(t = 0+, R_{th} = \text{finite})$,

$I_{C,f} = I_C(t = \text{final}, R_{th} = \text{finite})$, and so on.

Since the topology in figure 6.16 is symmetrical, only the lower half of the transient operation is examined here. The upper half is similar. Since the base-emitter voltage change of Q_6 and Q_8 due to the static self-heating effect are much less than the supply voltage, i.e. $\underset{Rth}{\Delta} V_{BE8} + \underset{Rth}{\Delta} V_{BE6} << V_{CC} - V_{EE}$, the collector current of Q_8 is assumed to be constant. Hence the base-emitter voltage of Q_8 decreases to cancel the increase in the collector current of Q_8 resulting from device temperature increase, i.e.

$$\underset{Rth}{\Delta} V_{BEQ8} = -\frac{g_{ct,Q8} \cdot \underset{Rth}{\Delta} T_{Q8}}{g_{m,Q8}} = -\frac{g_{ct,Q8} \cdot V_{BEQ8} \cdot I_Q \cdot R_{thQ8}}{g_{m,Q8}}. \tag{6.20}$$

Therefore the collector currents of Q_7 at different times are

$$I_{CQ7,0-} = I_Q + g_{ct,Q7} \cdot V_{CEQ7} \cdot I_Q \cdot R_{thQ7} + g_{m,Q7} \cdot \underset{Rth}{\Delta} V_{BEQ8}, \tag{6.21}$$

$$I_{CQ7,0+} = I_{CQ7,0-}\left(1 + \Delta V_{in} / V_A\right), \tag{6.22}$$

$$I_{CQ7,f} = I_{CQ7,0+} + g_{ct,Q7} \cdot \Delta V_{in} \cdot I_{CQ7,0-} \cdot R_{thQ7}. \tag{6.23}$$

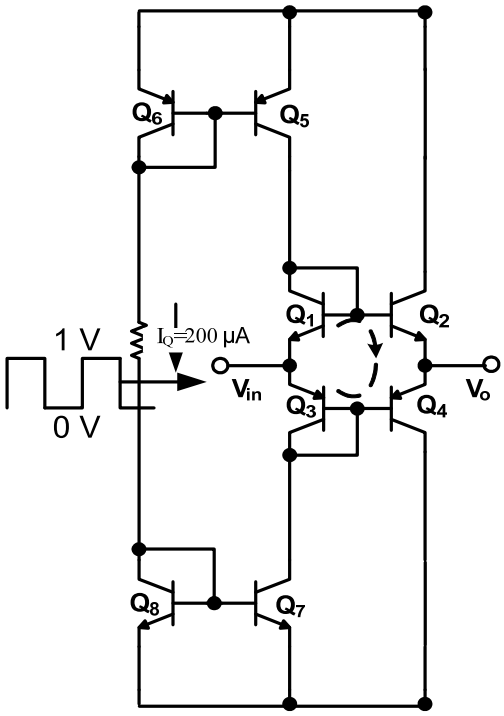

Figure 6.16 Voltage buffer biased with current mirror.

The thermal tail of the collector current of Q_7 is then reflected to the base-emitter voltage of Q_3. The collector current of Q_3 at t=0- is

$$I_{CQ3,0-} = (I_{CQ7,0-} - \frac{I_{CQ4,0-}}{\beta_4}) \cdot \frac{\beta_3}{\beta_3 + 1}, \tag{6.24}$$

where

$$\begin{aligned} I_{CQ4,0-} &= I_{CQ4} + g_{ct,Q4} \cdot \underset{Rth}{\Delta} T_{Q4} + g_{m,Q4} \cdot \underset{Rth}{\Delta} V_{EBQ4,C} \\ \underset{Rth}{\Delta} T_{Q4} &= -V_{EE} \cdot I_{CQ4} \cdot R_{thQ4} \\ \underset{Rth}{\Delta} V_{EBQ4,C} &\cong -\frac{g_{ct,Q4} \cdot \underset{Rth}{\Delta} T_{Q4} - g_{ct,Q2} \cdot \underset{Rth}{\Delta} T_{Q2}}{g_{m,Q2} + g_{m,Q4}} \\ I_{CQ4} &\cong \sqrt{I_{CQ5,0-} \cdot I_{CQ7,0-}} \end{aligned} \tag{6.25}$$

The collector currents of Q_2 and Q_4 have different variations because of the Early effect. Thus similar to the procedure in section 6.4.1, the base-emitter voltage correction of Q_2 and Q_4 occurs to satisfy the KVL around the translinear loop and the KCL at node V_o. The base-emitter voltage of Q_4 at t=0+ tends to decrease from t=0- and the base-emitter voltage of Q_3 will increase. The collector current of Q_4 at t=0+ is

$$I_{CQ4,0+} = I_{CQ4,0-}\left(1 + \Delta V_{in} / V_{AQ4}\right) + g_{m,Q4} \cdot \underset{E}{\Delta} V_{EBQ4,C}, \tag{6.26}$$

where

$$\begin{aligned} \underset{E}{\Delta} V_{EBQ4,C} &= -\frac{I_{CQ4,0-} \cdot \Delta V_{in} / V_{AQ4} + I_{CQ2,0-} \cdot \Delta V_{in} / V_{AQ2} - g_{m,Q2}\left(\underset{Vin}{\Delta} V_{BEQ1} + \underset{Vin}{\Delta} V_{EBQ3}\right)}{g_{m,Q2} + g_{m,Q4}} \\ \underset{E}{\Delta} V_{BEQ3} &= \frac{I_{CQ3,0+} - I_{CQ3,0-}}{g_{m,Q3}} \\ I_{CQ3,0+} &\cong (I_{CQ7,0+} - \frac{I_{CQ4,0-}}{\beta_4}) \cdot \frac{\beta_3}{\beta_3 + 1} \end{aligned} \tag{6.27}$$

Similarly the collector currents of Q_2 and Q_4 have different variations because of the change of power dissipation after the initial input step. Following the procedure mentioned before, the collector current of Q_4 at t=final is

$$I_{CQ4,f} = I_{CQ4,0+} + g_{ct,Q4} \cdot \Delta V_{in} \cdot I_{CQ4,0-} \cdot R_{thQ4} + g_{m,Q4} \cdot \underset{Vin}{\Delta} V_{EBQ4,C}, \tag{6.28}$$

$$\underset{Vin}{\Delta} V_{EBQ4,C} = -\frac{g_{ct,Q4}\cdot\Delta V_{in}\cdot I_{CQ4,0-}\cdot R_{thQ4} + g_{ct,Q2}\cdot\Delta V_{in}\cdot I_{CQ2,0-}\cdot R_{thQ2}}{g_{m,Q2}+g_{m,Q4}} + \frac{g_{m,Q2}\left(\underset{Vin}{\Delta} V_{BEQ1} + \underset{Vin}{\Delta} V_{EBQ3}\right)}{g_{m,Q2}+g_{m,Q4}} \quad , \tag{6.29}$$

where

$$\underset{Vin}{\Delta} V_{BEQ3} = \frac{I_{CQ3,f} - I_{CQ3,0+}}{g_{m,Q3}} \quad . \tag{6.30}$$

$$I_{CQ3,f} \cong (I_{CQ7,f} - \frac{I_{CQ4,0+}}{\beta_4})\cdot\frac{\beta_3}{\beta_3+1}$$

Table 6.1 shows the collector currents and base-emitter voltages of transistors Q_1 through Q_8 at different time based on previous analysis, and table 6.2 shows the corresponding simulation results. The input switch from 0 V to 1 V, time period is 4 ms, and the rise time is 1 ns. The thermal resistance of Q_1 through Q_8 is 3000 K/W, and the thermal capacitance is 1.69 nF as shown in the VBIC model attached in Appendix A. The thermal tail of V_o is

$$TT_{V_o} = V_{o,f} - V_{o,0+} = \underset{Vin}{\Delta} V_{BE1} - \underset{Vin}{\Delta} V_{BE2}\,. \tag{6.31}$$

The theoretical value of TT_{V_o} is -2107 μV comparable to -2009 μV of the simulated value.

Table 6.1 Theoretical V_{BE} and I_C of Q_1 through Q_8 at different time

	non self-heating VBE mV	non self-heating IC uA	self-heating VBE 0-	self-heating IC 0-	self-heating VBE 0+	self-heating IC 0+	Δ VBE (0+-0-) uV	Δ IC (0+-0-) uA	self-heating VBE f	self-heating IC f	Δ VBE (f-0+) uV	Δ IC (f-0+) uA
Q8	819.1	195.5	818.4	195.5	818.4	195.5	0.0	0.00	818.4	195.5	0.0	0.00
Q7	819.1	199.7	818.4	218.6	818.4	220.0	0.0	1.40	818.4	228.4	0.0	8.41
Q6	848.3	190.1	847.7	190.1	847.7	190.1	0.0	0.00	847.7	190.1	0.0	0.00
Q5	848.3	199.1	847.7	213.8	847.7	210.9	0.0	-2.85	847.7	206.4	0.0	-4.46
Q1	821.1	208.3	820.4	208.3	820.0	205.5	-440.8	-2.82	819.3	201.1	-689.8	-4.41
Q3	851.5	207.3	852.1	207.3	852.4	208.7	251.3	1.37	853.9	216.9	1507.8	8.20
Q2	821.1	219.0	820.4	247.9	820.8	248.4	324.1	0.48	822.2	250.5	1417.2	2.04
Q4	851.5	216.2	852.1	244.8	851.6	245.2	-513.6	0.47	851.0	247.3	-599.2	2.04

Table 6.2 Simulated V_{BE} and I_C of Q_1 through Q_8 at different time

	non self-heating VBE mV	non self-heating IC uA	self-heating VBE 0-	self-heating IC 0-	self-heating VBE 0+	self-heating IC 0+	Δ VBE (0+-0-) uV	Δ IC (0+-0-) uA	self-heating VBE f	self-heating IC f	Δ VBE (f-0+) uV	Δ IC (f-0+) uA
Q8	819.1	195.5	818.4	195.2	818.4	195.2	-40.4	0.00	818.3	195.1	-17.6	-0.10
Q7	819.1	199.7	818.4	221.4	818.4	222.7	-40.4	1.32	818.3	230.7	-17.6	7.96
Q6	848.3	190.1	847.6	189.7	847.6	189.7	-28.4	0.00	847.6	189.8	26.7	0.10
Q5	848.3	199.1	847.6	214.9	847.6	212.2	-28.4	-2.68	847.6	207.1	26.7	-5.09
Q1			820.5	209.4	820.1	206.8	-394.7	-2.62	819.4	201.8	-732.8	-5.02
Q3			851.1	209.6	851.4	211.1	302.1	1.48	852.7	218.7	1290.6	7.63
Q2			820.6	248.8	820.8	249.1	210.0	0.34	822.1	250.9	1276.5	1.80
Q4			851.1	245.5	850.7	246.0	-400.1	0.51	850.0	247.8	-721.0	1.78

6.5 Summary

The change of device temperature is an exponentially increasing function of time with a time constant, $\tau_{th}=R_{th}C_{th}$, and an asymptotic value of $P_{th}R_{th}$. The change of the base-emitter voltage is also a function of time as V_{BE} generally decreases with device temperature linearly. The transient collector current of a BJT device can be estimated by considering the first order dependence of collector current on the change of device temperature, the collector-emitter voltage and the base-emitter voltage. The effect of self-heating on transient operation in the high speed voltage buffer is analyzed and compared to the simulation results.

CHAPTER 7

DESIGN OF A SELF-HEATING TOLERANT CURRENT FEEDBACK OPERATIONAL AMPLIFIER

This chapter examines the contribution of each transistor in a operational amplifier to the overall thermal tail of current feedback amplifiers. A cascode bootstrapped CFOA is proposed that minimizes the self-heating effect. The SPECTRE simulator verifies the design.

7.1 Superposition of the Overall Thermal Tail in CFOA

To design current feedback amplifiers free of a thermal tail, it is worthwhile to first look at each transistor's contribution in the total thermal tail. The overall thermal tail of a CFOA is a linear addition of thermal tails caused by each transistor. Figure 7.1 shows the complete circuit of the classical CFOA in figure 3.1 with emitter degeneration [24]. The complete circuit is divided into six "sticks" from left to right as shown in figure 7.1. Every stick consists of vertically connected transistors. According to the type and functionality of the transistors, each transistor in a stick is named using the format, stkn-npn/pnp-bf or stkn-npn/pnp-cm for buffers or current mirrors respectively. For example, Q_8 belongs to stick3, and it is a part of the input buffer, so it is called stk3-pnp-bf. While Q_4 belongs to stick 2 and is a part of the current mirror, so it is called stk2-pnp-cm. By enabling the self-heating effect in the transistor of interest and disabling self-heating for the rest of the transistors, the contribution of each transistor to the total thermal tail can be obtained [41]. Figure 7.2 shows the overall large-signal transient response of the CFOA in figure 7.1 with input driven by a 2 V peak to peak square wave, in unity-gain non-inverting configuration with a feedback resistor of 800 Ω. Table 7.1 shows the thermal tail obtained at the output terminal, V_O, of the CFOA in figure 7.1 caused by self-heating of each individual transistor.

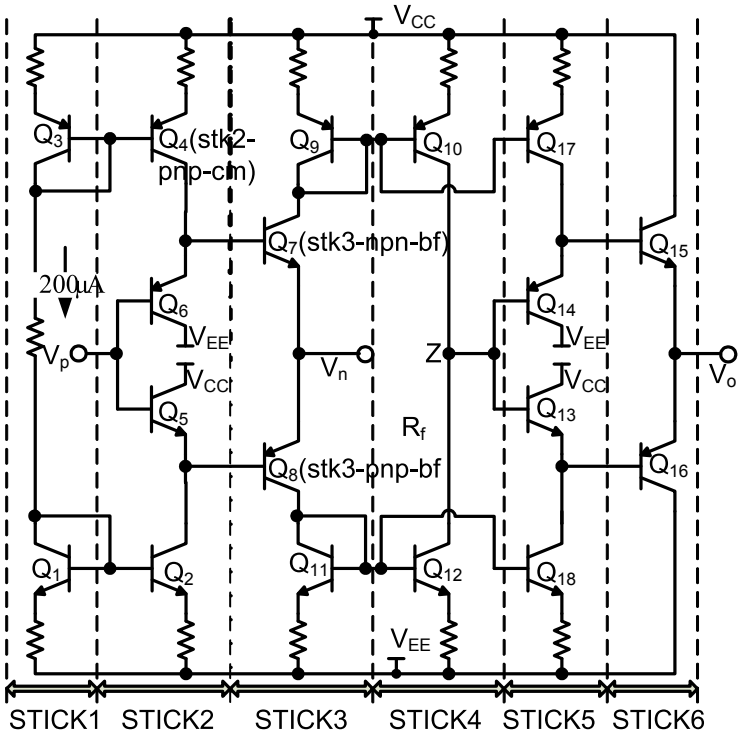

Figure 7.1 Complete circuit of the classical CFOA in figure 3.1 with emitter degeneration resistors of 1kΩ.

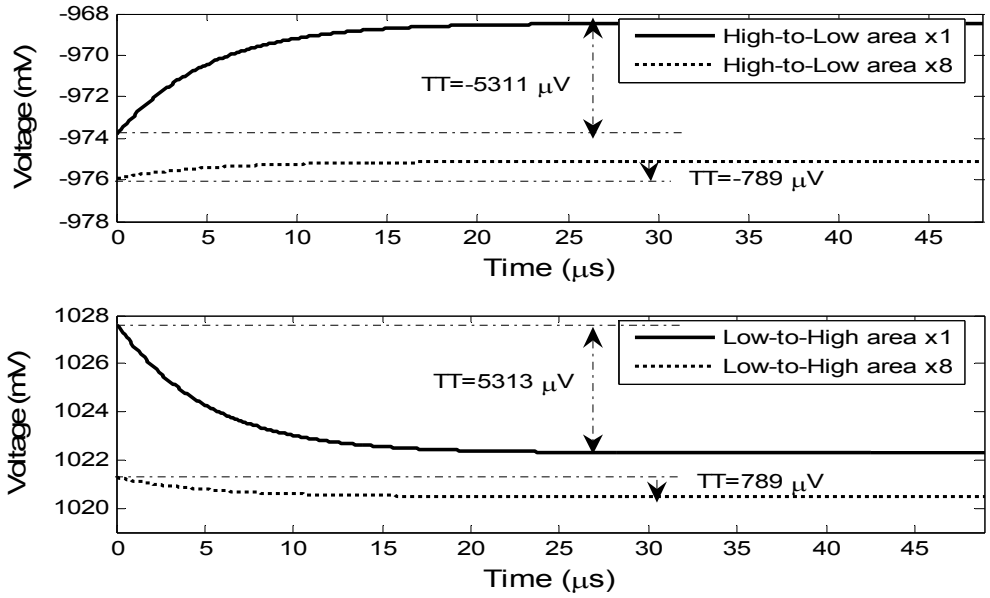

Figure 7.2 Overall large-signal transient response of the CFOA in figure 7.1 with input driven by a 2 V peak to peak square wave, in unity-gain non-inverting configuration with feedback resistor of 800 Ω.

Table 7.1 Thermal tail obtained at terminal V_O of the CFOA in figure 7.1 caused by self-heating of each individual transistor, in unity-gain non-inverting configuration with feedback resistor of 800 Ω [41]

	Area 1x5 μm^2		Area 8x5 μm^2	
Thermal Tail (uV/V)	High-to-Low	Low-to-High	High-to-Low	Low-to-High
stk2-npn-bf (Q_5)	822	-842	124	-128
stk2-pnp-bf (Q_6)	727	-712	101	-98
stk2-npn-cm (Q_2)	89	-91	11	-12
stk2-pnp-cm (Q_4)	91	-89	10	-9
stk3-npn-bf (Q_7)	877	-850	111	-106
stk3-pnp-bf (Q_8)	783	-808	111	-115
stk4-npn-cm (Q_{12})	1213	-1217	172	-173
stk4-pnp-cm (Q_{10})	1075	-1073	159	-158
stk5-npn-bf(Q_{13})	-13	13	-2	2
stk5-pnp-bf(Q_{14})	4	-4	1	-1
stk5-npn-cm(Q_{18})	-16	15	-2	2
stk5-pnp-cm(Q_{17})	5	-2	0	0
stk6-npn-bf(Q_{15})	0	-1	0	0
stk6-pnp-bf(Q_{16})	1	0	0	0
Sum of the thermal tails above	5658	-5661	796	-796
Overall simulated thermal tail	5311	-5313	789	-789

As shown in Table 7.1, the overall thermal tail mainly comes from the input power transistors, Q_5 (stk2-npn-bf), Q_6 (stk2-pnp-bf), Q_7 (stk3-npn-bf) and Q_8 (stk3-pnp-bf), and from the current mirrors of the trans-impedance stage, Q_{10} (stk4-pnp-cm) and Q_{12} (stk4-npn-cm). The overall thermal tail is a linear addition of the thermal tails contributed by each transistor of the CFOA. Note that the current mirror transistors to bias the output stage, Q_{17} (stk5-npn-cm) and Q_{18} (stk5-pnp-cm), contribute negligible amount to the overall thermal tail because of the double voltage buffer configuration at the output stage. Also the power transistors in the output stage, Q_{13} (stk5-npn-bf) and Q_{16} (stk5-pnp-bf), Q_{15} (stk6-npn-bf) and Q_{16} (stk6-pnp-bf) contribute negligible thermal tail to the overall thermal tail because of the large magnitude of transimpedance and negative feedback. This can be verified by the following analysis.

Figure 7.3 shows a CFOA in the non-inverting amplifier configuration. The overall thermal tail at the output can be classified into three categories. The first is the thermal tail generated in the input stage which mainly comes from the base-emitter voltage correction of the input power transistors, and is denoted $v_{n,tt}$. The second is the thermal tail generated by the current mirrors in the transimpedance stage and is denoted as $i_{z,tt}$. The third is the thermal tail generated in the output stage which is denoted as $v_{os,\,tt}$.

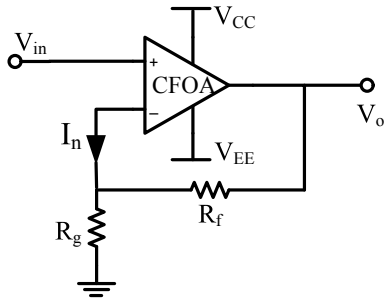

Figure 7.3 A CFOA in the non-inverting amplifier configuration.

The Kirkchhoff's current law at the inverting input terminal gives [24]

$$I_n = \left(V_{in} + v_{n,tt}\right)\cdot\left(\frac{1}{R_g} + \frac{1}{R_f}\right) - \frac{V_o}{R_f}\,. \tag{7.1}$$

The output voltage can be expressed as follows because of amplification is provided by the impedance stage which senses the current I_n delivered by the voltage buffer at the output stage to the external feedback network

$$V_o = \left(I_n + i_{z,tt}\right)\cdot Z_T + v_{os,tt}\,, \tag{7.2}$$

where Z_T is the transimpedance of the CFOA.

Combining equation (7.1) and (7.2) gives

$$V_o = \left(\left(V_{in} + v_{n,tt}\right)\cdot\left(\frac{1}{R_g} + \frac{1}{R_f}\right) - \frac{V_o}{R_f} + i_{z,tt}\right)\cdot Z_T + v_{os,tt}\,. \tag{7.3}$$

Equation (7.3) can be expressed in another form as

$$V_o \cdot \left(1+\frac{Z_T}{R_f}\right) = \left(V_{in} + v_{n,tt}\right)\cdot\left(1+\frac{R_f}{R_g}\right)\cdot\frac{Z_T}{R_f} + i_{z,tt}\cdot Z_T + v_{os,tt} \tag{7.4}$$

Assuming $R_g=\infty$ in unity gain configuration and $Z_T>>R_f$ and, equation (7.4) becomes

$$V_o \cong V_{in} + v_{n,tt} + i_{z,tt}\cdot R_f + \frac{v_{os,tt}}{1+Z_T/R_f}, \tag{7.5}$$

where $\frac{v_{os,tt}}{1+Z_T/R_f}$ is negligible. This explains why the thermal tail contributed from the power transistors in the output stage is negligible.

7.2 Cascode Bootstrapped CFOA

Table 7.1 shows that the overall thermal tail is reduced about 8 times when the size of each transistor in the CFOA of figure 7.1 is increased 8 times. The thermal resistance decreases with increasing area of a transistor. But this is not an attractive technique because of the large area requirement. As discussed in chapter 5, techniques that raise the effective output resistance can reduce effects of self-heating. These techniques include cascoding, negative feedback as with the Wilson current mirror, or emitter degeneration.

Figure 7.4 shows four possible cascode half-circuits of the input stage that can raise the effective output resistance [40]. Here a single buffer is used rather than a double buffer because of the double buffer's offset voltage. In the circuit shown in figure 7.4.(a), the base of Q_3 is bootstrapped to the inverting input, V_n, by two diode connected transistors. This is called reverse bootstrapping [40]. The effective output resistance at the collector of Q_3 is approximately equal to βr_o. In the circuit shown in figure 7.4.(b), a beta helper, Q_8, is used to increase the slew rate by making more current available at the base of Q_2. In figure 7.4.(c) the base of Q_3 is bootstrapped to the non-inverting input, V_p, rather than the inverting input by two diode connected transistors. This is called forward bootstrapping [40]. The circuit in figure 7.4.(d) improves offset voltage by keeping the collector-base voltage of Q_1 and Q_2 same (≈0).

Besides using cascode configuration in the input stage, a Wilson or a Cascode current mirror can be used for the bias circuit in the input stage as well as in the transimpedance stage. This will also reduce the thermal tail.

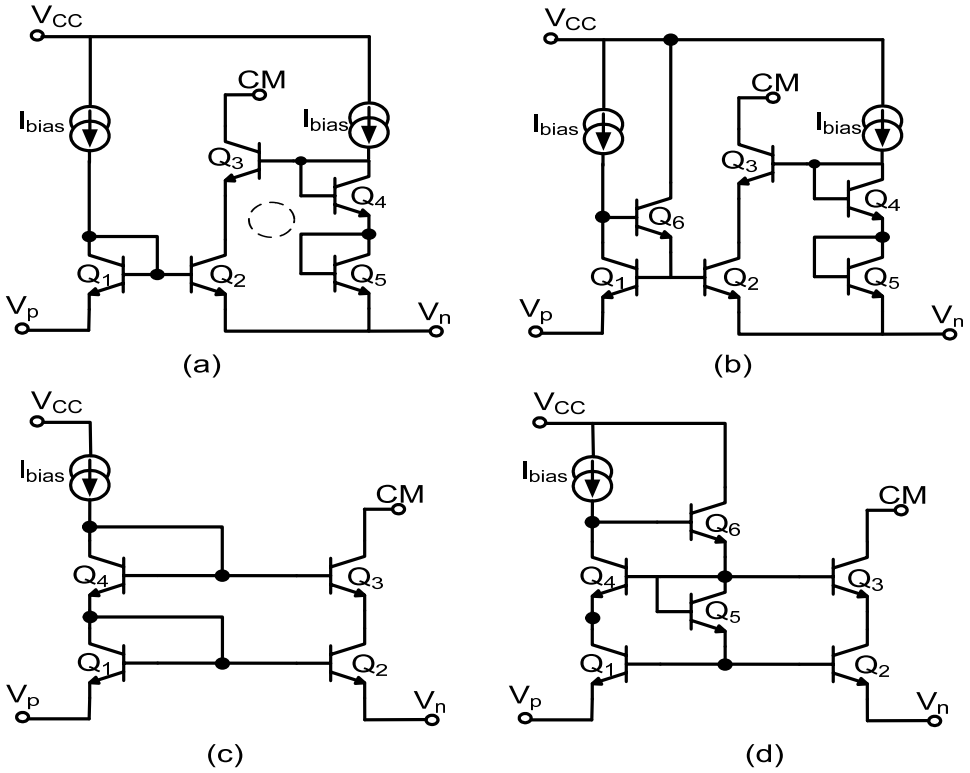

Figure 7.4 Four possible cascode half-circuits of the input stage [40].

Figure 7.5 shows the complete circuit of the CFOA in which the Wilson current mirror is used in the bias circuit as well as in the transimpedance stage, single buffer is used in the input stage and double buffer is used in the output stage. All transistors are 1x5 μm^2 device and the emitter degeneration resistors are 1 kΩ. Figure 7.6 shows the overall large-signal transient response of the CFOA in figure 7.5 with input driven by a 2 V peak to peak square wave, in a unity-gain non-inverting configuration with feedback resistor of 800 Ω. The overall thermal tail is 1736 μV in the low-high transition and -1738 μV in the high-low transition. Compared to 5311 μV of the overall thermal tail of the CFOA in figure 7.1 in which simple current mirror is used in the bias circuit and in the transimpedance stage, it can be inferred that the use of the Wilson current

mirror in the bias circuit as well as in the transimpedance stage greatly suppress the self-heating effects.

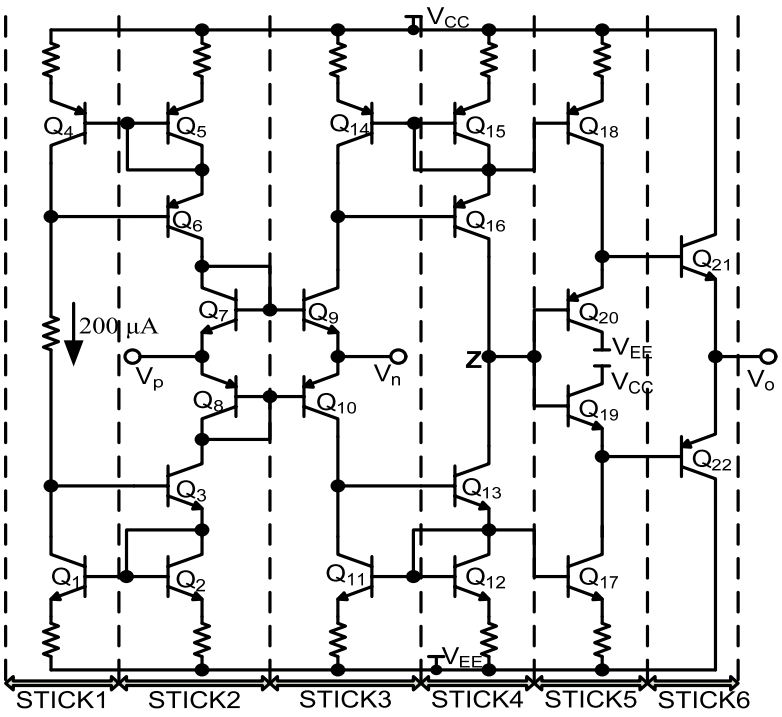

Figure 7.5 Complete circuit of the CFOA with Wilson current mirror at the input and transimpedance stage. All transistors are 1x5 μm^2 device. Emitter degeneration resistors are 1kΩ.

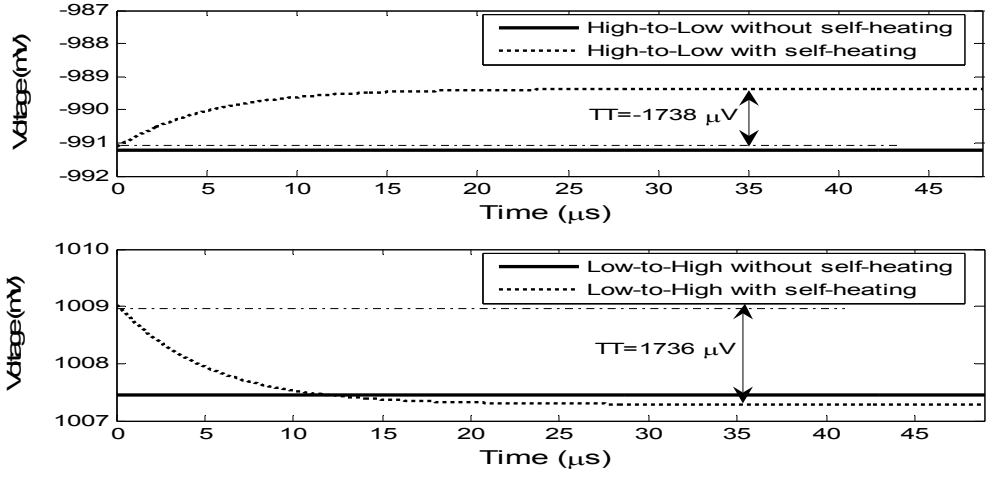

Figure 7.6 Overall large-signal transient response of the CFOA in figure 7.5 with input driven by a 2 V peak to peak square wave, in unity-gain non-inverting configuration with feedback resistor of 800 Ω.

Figure 7.7 shows the complete cascode reverse bootstrapped CFOA [40]. Transistors Q_{23} and Q_{24} are cascode devices to improve the output resistance of Q_9 and Q_{10}, respectively; Q_{26} and Q_{27} are used to bootstrap the base of Q_{23} to the inverting input; Q_{28} and Q_{29} are used to bootstrap the base of Q_{24} to the inverting input. Wilson current mirrors are used in the biasing circuit of the input stage and the transimpedance stage. Single voltage buffer is used at both the input stage and the output stage. Q_{25} and Q_{30} are used to bias Q_{26} through Q_{29}. With the technique of cascoding, the power transistors in the input stage, Q_9 and Q_{10}, hardly contribute any to the overall thermal tail as shown in Table 7.2.

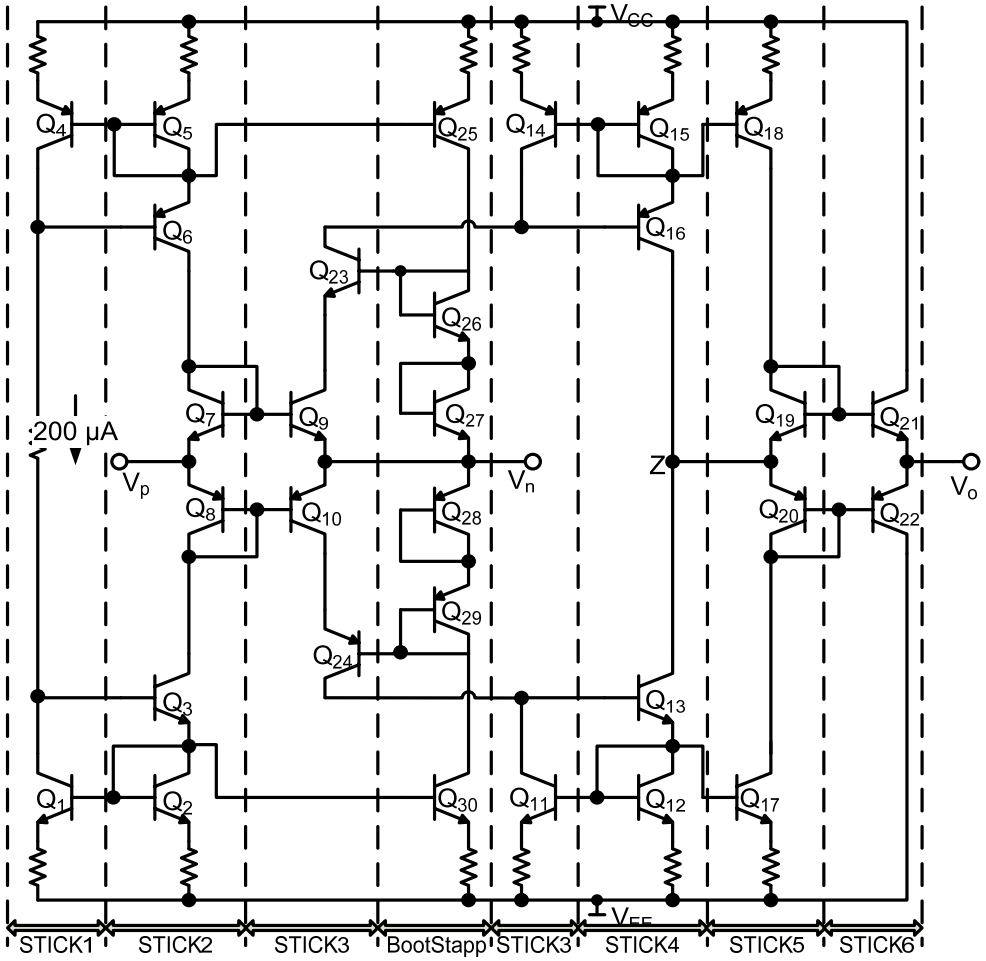

Figure 7.7 Complete circuit of the cascode reverse bootstrapped CFOA. Q_{23} and Q_{24} are cascode devices to improve the output resistance of Q_9 and Q_{10}, respectively [40].

It can be inferred that the thermal tail, introduced by Q_{25} and Q_{30} is opposite to that introduced by Q_{18} (stk5-pnp-cm) and Q_{17} (stk5-npn-cm) in figure 7.7. Therefore, the overall thermal tail can be minimized by making the thermal tail caused by Q_{25} and Q_{30} to be equal and opposite to the thermal tail caused by stk5-cm (Q_{17} and Q_{18}). This can be done by optimizing the areas of transistors in a specific stick selectively. It is found that by setting the areas of transistor from stick1 to stick 4 to 8x5 μm^2, and from stick5 and stick6 to 64x5 μm^2, the overall thermal tail is minimized to around 19 μV as shown in figure 7.8 and Table 7.2 for the CFOA in figure 7.7.

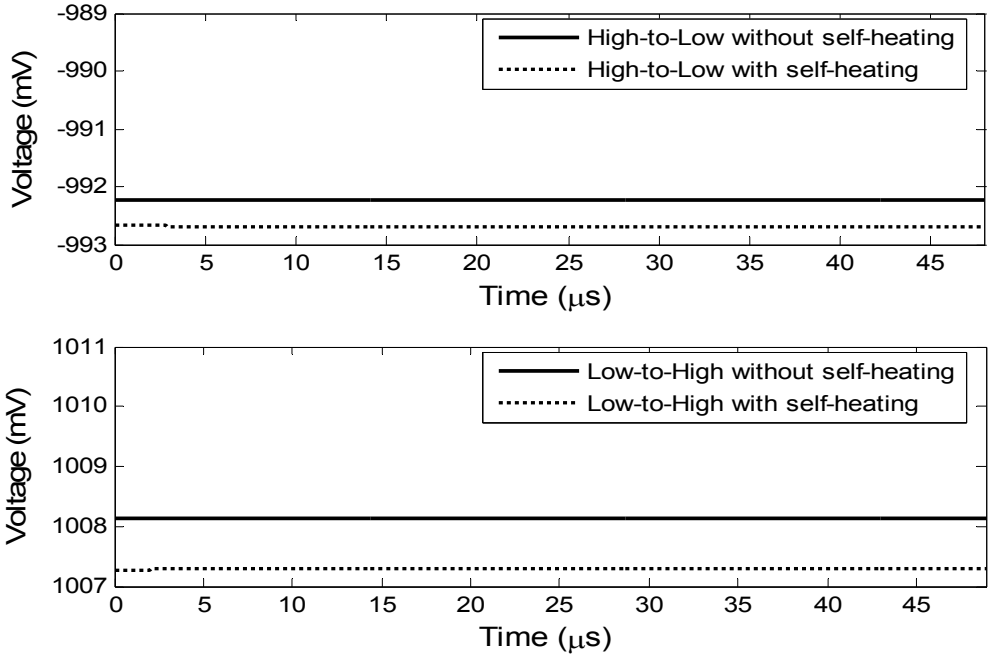

Figure 7.8 Overall large-signal transient response of the cascode reverse bootstrapped CFOA in figure 7.7 with input driven by a 2 V peak to peak square wave, in unity-gain non-inverting configuration with feedback resistor of 800 Ω.

Table 7.2 Thermal tail obtained at terminal V_O of the CFOA in figure 7.5 and 7.7 caused by self-heating of each individual transistor, in unity-gain non-inverting configuration with feedback resistor of 800 Ω [41]

	CFOA in Fig.7.5		CFOA in Fig.7.7	
Thermal Tail (uV)	High-to-Low	Low-to-High	High-to-Low	Low-to-High
stk2-npn-cm (Q_3)	5	-5	-1	1
stk2-pnp-cm (Q_6)	-3	3	1	-1
stk3-npn-bf (Q_9)	-1179	1158	N/A	N/A
stk3-pnp-bf (Q_{10})	-523	538	N/A	N/A
Bootstrapped-npn-cm (Q_{25})	N/A	N/A	173	-173
Bootstrapped-pnp-cm (Q_{30})	N/A	N/A	158	-157
stk3-npn-cm (Q_{11})	9	-8	-1	1
stk3-pnp-cm (Q_{14})	-9	8	-1	1
stk4-npn-cm (Q_{13})	34	-34	3	-3
stk4-pnp-cm (Q_{16})	-10	10	-1	1
stk5-npn-bf (Q_{19})	14	-14	N/A	N/A
stk5-pnp-bf (Q_{20})	-4	3	N/A	N/A
stk5-npn-cm (Q_{17})	-48	48	-165	164
stk5-pnp-cm (Q_{18})	-53	53	-149	148
stk6-npn-bf (Q_{21})	0	0	-4	5
stk6-pnp-bf (Q_{22})	0	0	5	-4
added total	-1767	1760	18	-17
simulated total	-1738	1736	19	-18

Figure 7.9 shows the overall thermal tails when the classic CFOA in figure 7.5 and the cascode bootstrapped CFOA in figure 7.7 drive a load of 2 kΩ and 2 pF. The input is a 1 V peak to peak square wave. The area of the transistors Q_{19} and Q_{20}, Q_{21} and Q_{22} is set to 64x5 μm^2, 2048x5 μm^2, respectively in order to drive the load of 2 kΩ and 2 pF. The overall thermal tail of the classic CFOA in figure 7.5 is 1032 μV while the overall thermal tail of the cascode bootstrapped CFOA in figure 7.7 is 9 μV. For all loads, a similar reduction should be expected.

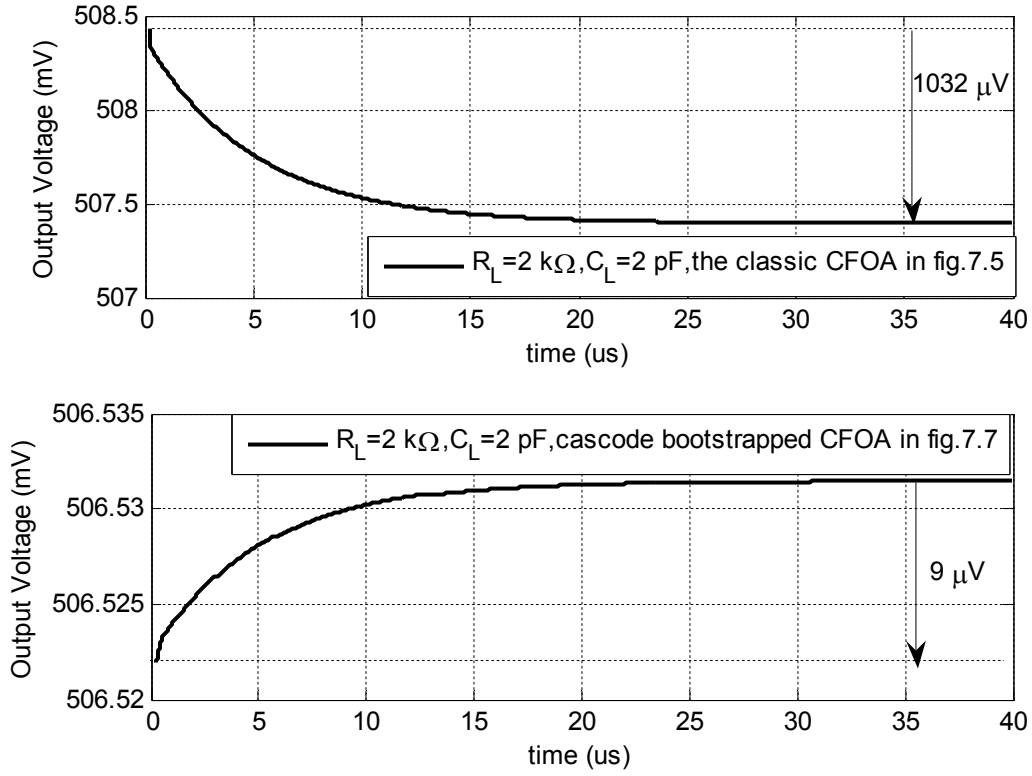

Figure 7.9 The overall thermal tails of the classic CFOA in figure 7.5 and the cascode bootstrapped CFOA in figure 7.7 when driving a load of 2 kΩ and 2 pF

7.3 Other CFOA Parameters

For all the simulation in this section, the SPECTRE simulator is used. The model used is attached in Appendix A. The power supply voltages are set to V_{CC}=+5V, and V_{EE}=-5 V.

Figure 7.10 shows the inverting input DC current transfer curve of the cascode reverse bootstrapped CFOA in figure 7.7. As shown in figure 7.10, the DC input offset current, I_{offset}, is equal to -5.898 μA. By applying I_{offset} to the inverting input terminal, the transimpedance frequency response is obtained as in figure 7.11. The low frequency transimpedance is around 1.8 MOhms. Since a Wilson current mirror is used in the transimpedance stage, the effect of self-heating is minimized at low frequencies.

Figures 7.12 and 7.13 show the positive and negative power rejection ratio of the cascode reverse bootstrapped CFOA in figure 7.7. The positive PSRR is about 63.26 dB and the negative PSRR is about 60.1 dB.

Figure 7.14 shows the DC voltage transfer curve of the cascode reverse bootstrapped CFOA in figure 7.7. The input offset voltage is about -0.652 mV. By applying the input offset voltage at the input, the common mode rejection ratio frequency response is obtained in figure 7.15. The CMRR is around 95.6 dB. Due to the use of cascode topology in the input stage, the CMRR is greatly improved.

Figure 7.16 shows the simulation result of the common mode input range via the configuration in figure 3.11. Resistors of 2 kΩ are used here. As shown in figure 7.16, the positive CMIR is 2.96 V, and the negative CMIR is -2.98 V.

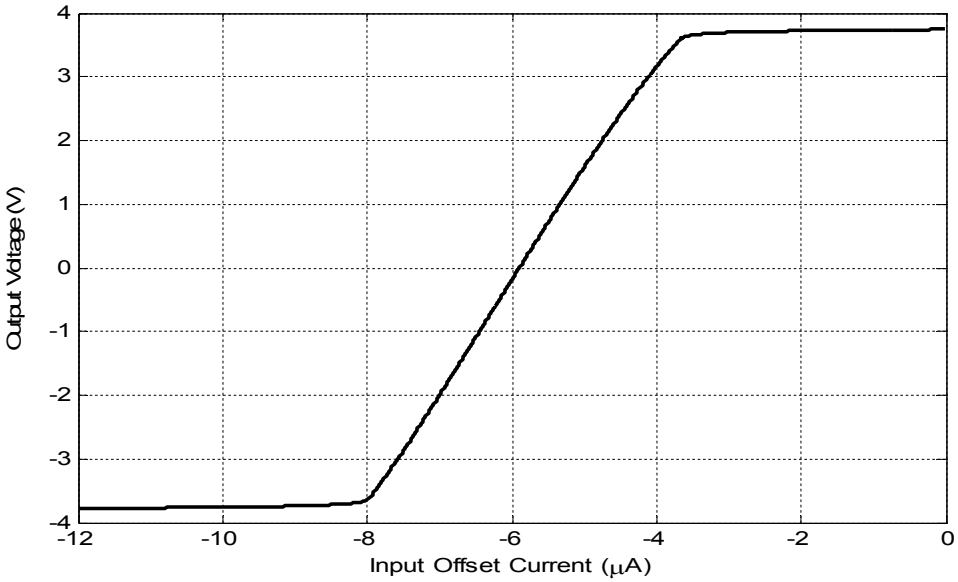

Figure 7.10 DC Current transfer curve of the cascode reverse bootstrapped CFOA in figure 7.7.

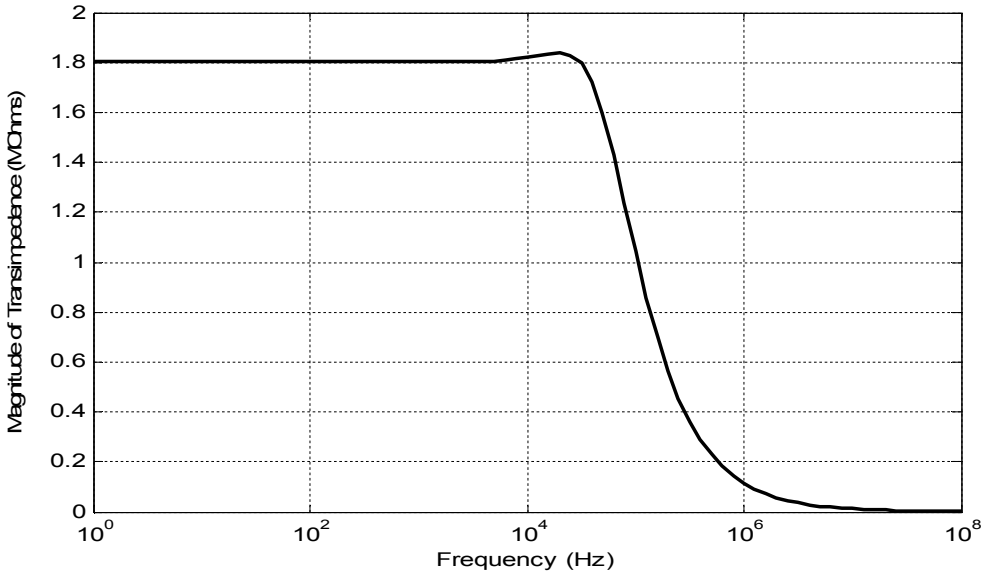

Figure 7.11 Transimpedance of the cascode reverse bootstrapped CFOA in figure 7.7.

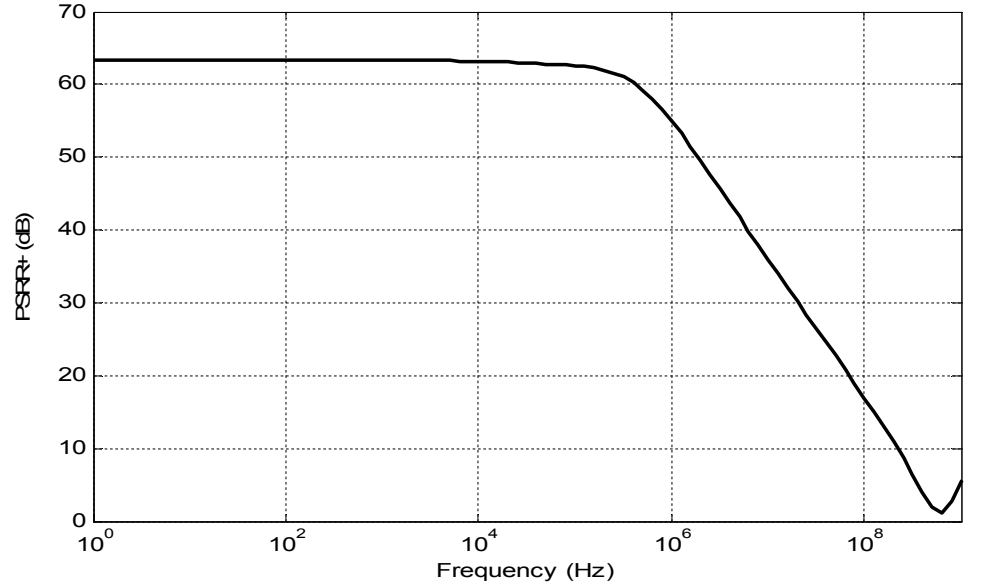

Figure 7.12 Positive PSRR of the cascode reverse bootstrapped CFOA in figure 7.7.

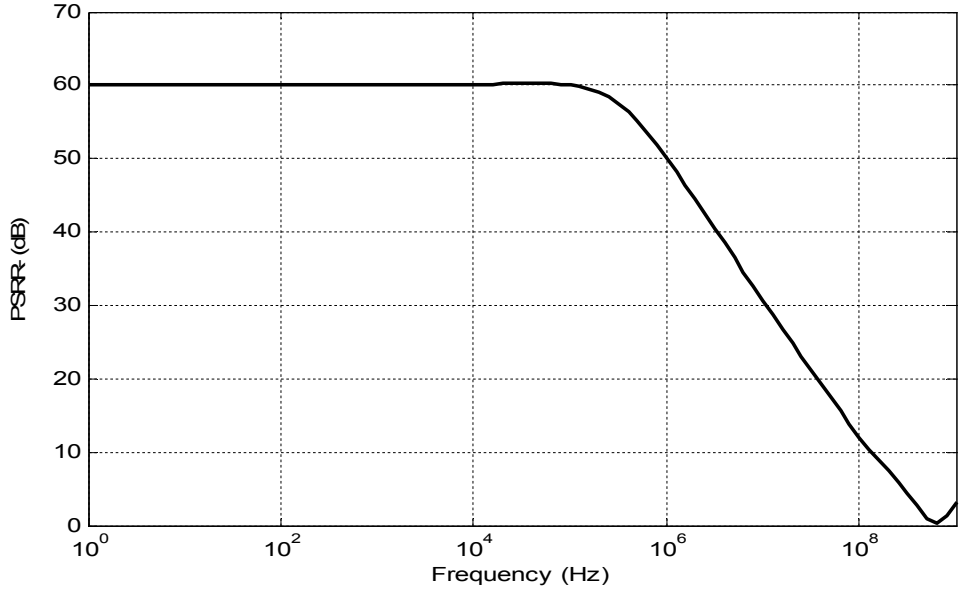

Figure 7.13 Negative PSRR of the cascode reverse bootstrapped CFOA in figure 7.7

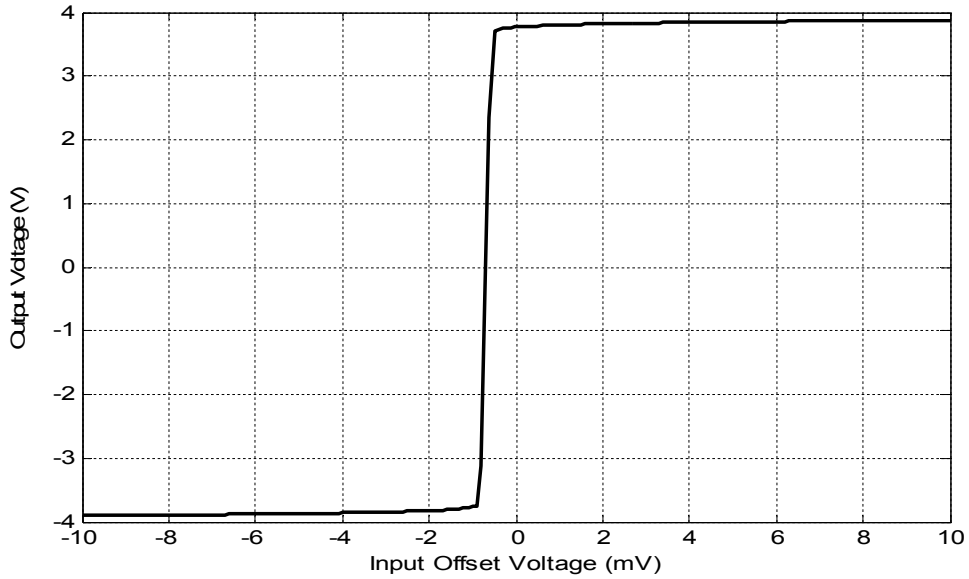

Figure 7.14 DC voltage transfer curve of the cascode reverse bootstrapped CFOA in figure 7.7

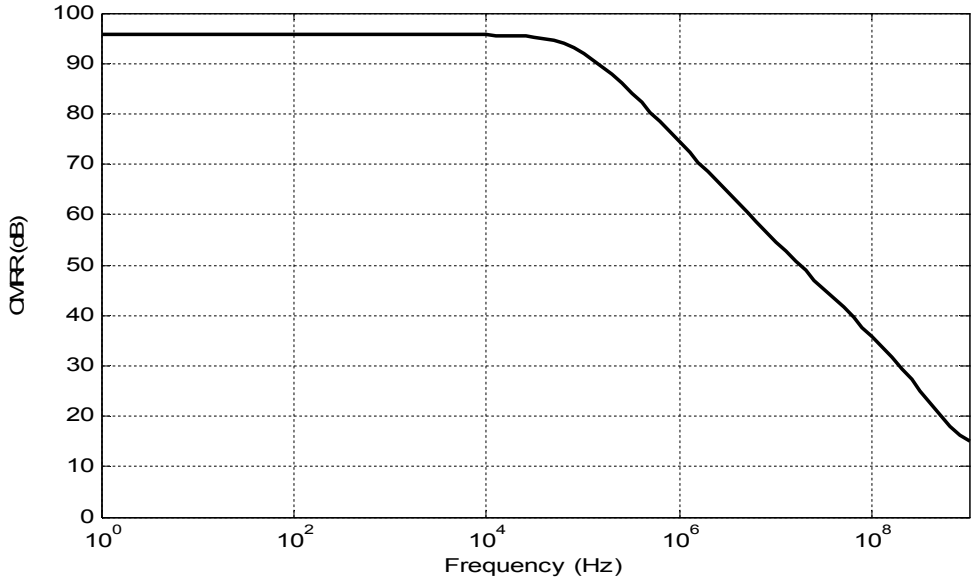

Figure 7.15 CMRR of the cascode reverse bootstrapped CFOA in figure 7.7

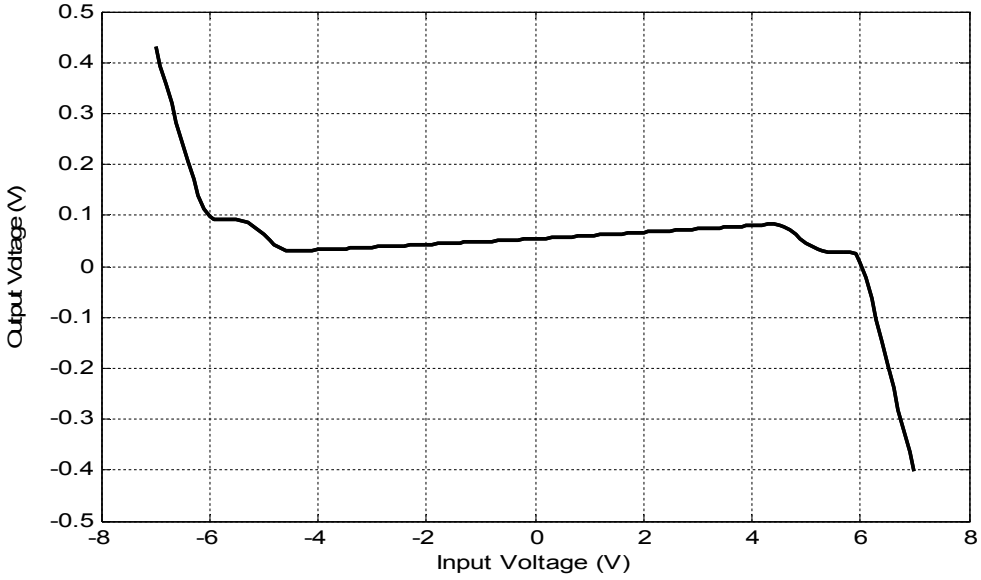

Figure 7.16 CMIR of the cascode reverse bootstrapped CFOA in figure 7.7

7.4 Summary

An approach to analyze the contribution of each transistor to the overall thermal tail of a current feedback operational amplifier is presented. It is shown that the overall thermal tail of a CFOA is a linear superposition of each individual transistor. Techniques to minimize the thermal tail are proposed. A cascode bootstrapped CFOA is designed and optimized to minimize the thermal tail. The overall thermal tail is reduced to 9 μV/V compared with 1032 μV/V of a classical CFOA when driving a 2 kΩ load in unity gain feedback configuration. For all loads, a similar reduction of the thermal tail should be expected. Also the common mode rejection ratio (CMRR) is greatly improved to 92 dB compared with 60 dB of the classical CFOA. Note that the common mode input range (CMIR) is sacrificed in order to get reduced thermal tail.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

Self-heating effects have been studied extensively in large-signal behavior, small-signal behavior and transient behavior for silicon-on-insulator (SOI) bipolar junction transistors. For a bipolar junction transistor (BJT) driven by a constant base-emitter voltage, self-heating can significantly increase the collector current. If the base is driven by a constant current source, self-heating increases collector current very slowly. By knowing the thermal resistance, the power dissipated and the mobility exponent factor, DC errors caused by self-heating effects can be roughly estimated. A simple method of extracting the thermal resistance and the Early voltage is proposed avoiding precise junction temperature control. It is shown that self-heating effects can strongly affect the output impedance of a BJT, and hence the gain of an amplifier by inducing a thermal zero-pole pair at lower frequencies than the intrinsic pole. Techniques raising the effective output impedance can reduce such error due to self-heating. These techniques include cascoding and negative feedback as done with Wilson current mirrors or emitter degeneration. In the transient operation, the change of device operating temperature is an exponentially increasing function of time with a time constant of the product of the thermal resistance and the thermal capacitance. Therefore, the settling time of switching circuits can be significantly degraded by self-heating since thermal transients take a much longer time to settle. Also the change of device operating temperature due to the change of power dissipation can cause the base-emitter voltage correction, current correction and consequently the thermal tail in the output. By knowing the thermal resistance, the power dissipated and the typical temperature coefficient, an approach to estimate thermal tails is presented. The thermal tail of a high speed voltage buffer biased with a current mirror is analyzed via this approach.

An analysis of the contribution of each transistor in a current feedback operational amplifier to the overall thermal tail is presented. It is shown that the overall thermal tail of a current feedback operational amplifier is a linear superposition of each individual transistor. By balancing the positive and negative thermal tail together via a cascode bootstrapped circuit topology, and using a Wilson current mirror in the biasing stage and transimpedance stage, the overall thermal tail is reduced to 9 μV/V compared with 1032 μV/V of a classical CFOA when driving a 2kΩ load in a unity gain feedback configuration. For all loads, a similar reduction of the thermal tail should be expected. Also the common mode rejection ratio (CMRR) is greatly improved from 60 dB of the classical CFOA to 92 dB.

The design of a low-voltage, rail to rail BJT current feedback operational amplifier would be an interesting topic. Self-heating effects on distortion of bipolar junction transistor would be another topic to look into. Also the analysis of self-heating effects on voltage feedback operational amplifier would be worthwhile.

APPENDIX A

BIPOLAR JUCNTION TRANSISTOR MODEL FILE [10]

A summary of the VBIC and SGP model parameters in SPECTRE format for the NPN and PNP transistors is provided in this appendix. These parameters are not meant to characterize any true proprietary specific SOI process technology. The emitter area of the NPN and PNP transistors listed in this appendix is 1x5 μm^2.

.model qinn vbic type=NPN
+IS=5.45E-18 NF=1.0 NR=1.0 RBX=30.0 RCX=10.0
+RCI=100.0 VO=5.0 GAMM=1.0E-10 HRCF=1.1E03 QCO=1.0E-15
+RBI=3.70E02 RE=15.0 RS=1.0E07 FC=9.0E-01 CJC=1.0E-14
+CJEP=2.1E-15 PC=0.73 MC=2.50E-01 AJC=-0.5 CJCP=5.0E-15
+CJE=4.70E-15 PE=0.93 ME=3.33E-01 AJE=-0.5 AJS=-0.5
+IBEI=4.66E-20 NEI=1.0 IBEN=7.50E-15 NEN=2.0 IBCI=2.02E-18
+NCI=1.0 NCN=2.0 IBCN=5.97E-16 AVC1=2.0 AVC2=50.0
+NCNP=2.0 VEF=78.0 VER=2.5 IKP=2.0E-04 IKF=2.73E-03
+IKR=1.52E-02 XTF=10.0 TF=4.42E-12 QTF=0.3 VTF=2.5
+ITF=3.04E-03 AFN=2.0 TR=1.77E-09 TD=7.72E-12 KFN=1.0E-09
+BFN=1.0 EA=1.13 EAIE=1.12 EAIC=1.12 EAIS=1.12
+EANE=1.12 EANC=1.12 EANS=1.12 XIS=3.50 XII=1.70
+XIN=1.7 TNF=0.0 IMELT=1.0E3 RBP=1.0 CBEO=1.01E-16
+CBCO=2.02E-16 XVO=0 PS=1.0 MS=0 WBE=1
+ISP=0.0 WSP=1.0 NFP=1.0 IBEIP=0.0 IBENP=0
+IBCIP=0 NCIP=1 IBCNP=0 XRE=0 XRB=0
+XRC=0 XRS=0 TAVC=0 SELFT=1
+CTH=1.67E-09 RTH=3000.0 TNOM=25.0

.model qinp vbic type=PNP
+IS=2.42E-18 NF=1.0 NR=1.0 RBX=13.33 RCX=22.50
+RCI=225.0 VO=2.22 GAMM=4.44E-11 HRCF=1.0E03 QCO=2.25E-15
+RBI=164.44 RE=33.75 RS=1.0E07 FC=9.0E-01 CJC=1.0E-14
+CJEP=2.1E-15 PC=0.73 MC=2.50E-01 AJC=-0.5 CJCP=5.0E-15
+CJE=4.70E-15 PE=0.93 ME=3.3E-01 AJE=-0.5 AJS=-0.5
+IBEI=3.76E-20 NEI=1.0 IBEN=7.50E-15 NEN=2.0 IBCI=8.97E-19
+NCI=1.0 NCN=2.0 IBCN=5.97E-16 AVC1=3.0 AVC2=55.0
+NCNP=2.0 VEF=26.0 VER=1.5 IKP=2.0E-04 IKF=1.2E-03
+IKR=6.75E-03 XTF=22.50 TF=4.98E-12 QTF=0.3 VTF=2.5
+ITF=1.35E-03 AFN=2.0 TR=1.99E-09 TD=8.68E-12 KFN=6.26E-10
+BFN=1.0 EA=1.13 EAIE=1.12 EAIC=1.12 EAIS=1.12
+EANE=1.12 EANC=1.12 EANS=1.12 XIS=3.15 XII=0.76
+XIN=0.76 TNF=0.0 IMELT=1.0E3 RBP=1.0 CBEO=1.01E-16
+CBCO=2.02E-16 XVO=0 PS=1.0 MS=0 WBE=1
+ISP=0.0 WSP=1.0 NFP=1.0 IBEIP=0.0 IBENP=0
+IBCIP=0 NCIP=1 IBCNP=0 XRE=0 XRB=0
+XRC=0 XRS=0 TAVC=0 SELFT=1
+CTH=1.67E-09 RTH=3000.0 TNOM=25.0

.model npn NPN struct=vertical
+IS=6.06E-18 BF=130.00 NF=1.00
+VAF=156.00 IKF=3.04E-03 ISE=1.26E-15
+NE=2.00 BR=3.00 NR=1.00
+VAR=5.00 IKR=3.04E-02 ISC=6.06E-17
+NC=1.00 RB=400.00 RBM=30.00
+IRB=1.00E-03 RE=15.00 RC=10.00
+CJC=1.03E-14 VJC=7.32E-01 MJC=2.50E-01
+CJE=4.70E-15 VJE=9.28E-01 MJE=3.33E-01
+XCJC=1.00E+00 CJS=5.00E-15 VJS=6.55E-01
+MJS=0.00E+00 TR=1.77E-09 KF=1.00E-09
+AF=2.00 EG=1.13 XTB=0.00E+00
+XTI=4.00 FC=0.50 TF=1.77E-11
+XTF=10.00 VTF=2.50 ITF=1.00E-03
+PTF=25.00 TNOM=25.00

.model pnp PNP struct=vertical
+IS=2.69E-18 BF=71.50 NF=1.00
+VAF=52.00 IKF=1.35E-03 ISE=1.26E-15
+NE=2.50 BR=4.00 NR=1.00
+VAR=3.00 IKR=1.35E-02 ISC=2.69E-17
+NC=1.00 RB=177.78 RBM=13.33
+IRB=4.44E-04 RE=33.75 RC=22.50
+CJC=1.03E-14 VJC=7.32E-01 MJC=2.50E-01
+CJE=4.70E-15 VJE=9.28E-01 MJE=3.33E-01
+XCJC=1.00E+00 CJS=5.00E-15 VJS=6.55E-01
+MJS=0.00E+00 TR=1.99E-09 KF=3.43E-10
+AF=2.00 EG=1.13 XTB=0.00E+00
+XTI=4.00 FC=0.50 TF=1.99E-11
+XTF=100.00 VTF=2.50 ITF=1.35E-03
+PTF=30.00 TNOM=25.00

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BIOGRAPHICAL INFORMATION

Xuesong Xie was born in Guizhou, China in 1975. He received his Bachelor of Engineering degree in Electrical Engineering from Huazhong University of Science & Technology, Wuhan, China in May 1997. He received his Master of Science degree in Electrical Engineering from Huazhong University of Science & Technology, Wuhan, China in May 2000. He began working towards his Ph.D. degree in Electrical Engineering from fall 2000 at the University of Texas at Arlington. From January 2002, he began working in the Analog Integrated Circuits Design Laboratory under the guidance of Dr. Ronald L. Carter and Dr. W. Alan Davis. His research interest focuses on Current Feedback Amplifier design and functionality analysis. He acquired his Ph.D. degree in May 2010.