CHARGE PUMP CIRCUIT

by

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ABSTRACT

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The sole aim of this work is to show how to generate higher voltages greater than the power supply voltage. This idea is implemented using transistors and capacitors on silicon and is called a charge pump circuit. A charge pump circuit is implemented as a voltage doubler circuit in this work using 0.25um gate length technology. A 6-stage Dickson charge pump circuit was designed to produce a 15 V output from a 5 V supply using two phase non-overlapping clock signals that drive the charge pump. It also describes the advanced architectures with complex circuit design and dynamic techniques for improving efficiency in low voltage operations.

EEPROMs, flash memories, power management blocks, audio and video codec, image sensor circuits and displays require voltages greater than the supply voltage and it needs to be generated on a chip. An on chip charge pump circuit provides an excellent solution in comparison with a power hungry switch capacitor or inductor based linear regulators in these systems. The charge pump circuit is a basic block of a phase lock loop (PLL) and a delay lock loop (DLL)

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CHAPTER 1

INTRODUCTION

The generation of higher voltage from the lower supply has been a quest since the discovery of electricity. Initially, engineers came up with idea of transformers which can up and down convert the supply voltage. During this time, Cockcroft and Walton invented a method using discrete capacitors and diodes for generating very high voltages[2]. Later, John Dickson adopted their method for implementation on integrated circuits[3].

1.1 Generating High Voltages Using Transformer

A transformer is a device that converts AC power at a given voltage level to AC power at a different voltage level. It transfers electrical energy through inductively coupled conductors. The maximum power of the circuit remains constant. If the voltage is increased at the secondary side the current is reduced to make V·I constant. The transformer is shown in figure 1.1

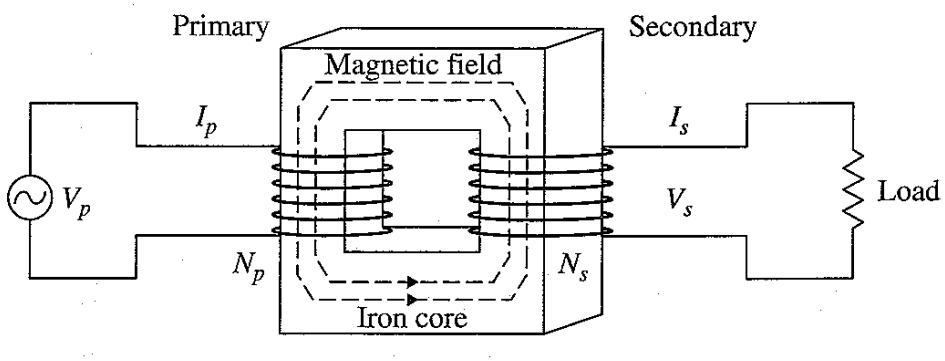


Figure 1.1 Transformer for generating high voltages [4]

For an ideal transformer,

$$\frac{V_S}{V_P} = \frac{N_S}{N_P} \qquad 1.1$$

where V_s and V_p are the voltages at the secondary and primary nodes respectively, N_s and N_p are the number of turns of the secondary and primary coils respectively.

A transformer is used with only alternating voltages and currents. But electronic circuits require DC voltages that are obtained using a rectifier circuit which is a cumbersome process. Also, high voltage generation using transformers make the circuits large, heavy, and inefficient and unsuitable for micro miniaturized implementation[4].

1.2 High Voltage Charge Pump By Cockcroft-Watson

The increase in voltage can be achieved by voltage multiplication of supply by cascading more than one diode capacitor voltage stage in series. Cockcroft and Walton, at Cavendish Laboratory in Cambridge, England needed higher particle energies to accelerate sub-atomic particles along a straight discharge tube. They built a voltage multiplier circuit using stack of capacitors connected to diodes acting as switches. By asserting and de-asserting the switches in proper sequence, they built up a potential of 800 kilovolts[2]. This voltage multiplier circuit was far lighter and cheaper than transformers. The Cockcroft-Walton multiplier circuit is shown in figure 1.2. The circuit has 3 capacitors of capacity C connected in series and capacitor C_A is connected to the supply voltage, V_{DD}. During phase, ϕ, capacitor C_1 is connected to C_A and charged to voltage V_{DD}. When the switches change position during the next cycle ϕ_b, capacitor C_1 will share its charge with capacitor C_B and both will be charged to $V_{DD}/2$ if they have equal capacity. In the next cycle, V_{DD} and V_{DD} will be connected and share a potential of $V_{DD}/4$ while V_{DD} is once again charged to V_{DD}. It is thus obvious that if this process continues for a few cycles, charge will be transferred to all the capacitors until a potential of $3V_{DD}$ is developed across the output V_{out}[1].

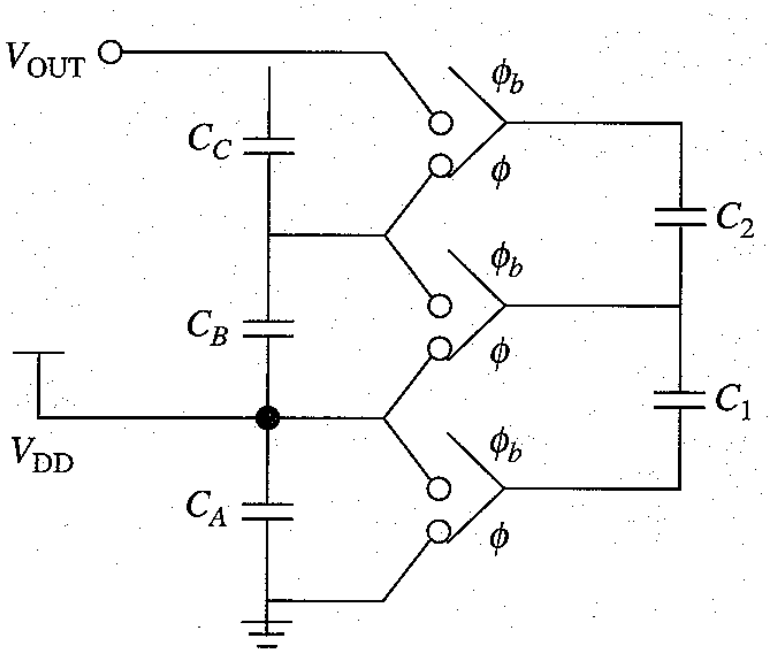


Figure 1.2 Cockcroft-Walton voltage multiplier[1]

The multiplier circuit of Cockcroft and Walton becomes very inefficient when implemented in integrated circuits due to very large on chip stray capacitance. Also, the output impedance increases rapidly with increase in the number of multiplying stages[1].

1.3 Dickson Charge Pump

Dickson used the same concept of the Cockcroft-Walton voltage multiplication circuit and implemented it in integrated circuits[3]. The Dickson charge pump circuit is shown in figure 1.3. As seen in the figure, it is very similar to Cockcroft-Walton circuit but the nodes of the diode chain are coupled to the inputs via capacitor in parallel, instead of in series, so that capacitors have to withstand the full voltages developed along the chain. The advantages of this configuration are that efficient multiplication can be achieved with relatively high value of stray capacitance and the current drive capability is independent of the number of stages[4].

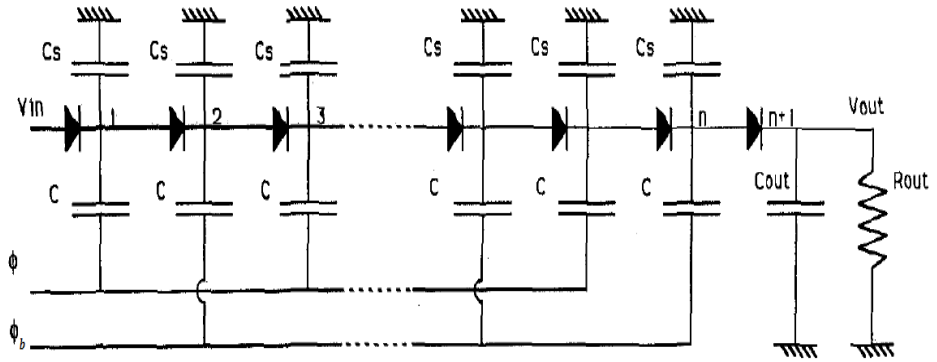


Figure 1.3 Dickson charge pump with diode-capacitor [9]

The basic Dickson charge pump circuit was very robust with all different high voltage generation issues until the advent of sub-micron design technology. The scaling down of supply voltages below 1.8V for better performance has highlighted a new issue, the body effect[4]. The body effect varies the threshold voltage in MOSFETs and results in smaller charge storage in the capacitors which reduces the voltage multiplication to a lower value.

CHAPTER 2

MOS DEVICE PHYSICS

To understand the operation and design of a charge pump circuit, it is necessary to have a basic knowledge of semiconductor physics and MOSFETs (Metal Oxide Semiconductor Field Effect Transistor). The switches in the Dickson charge pump are implemented by MOS transistors[1]. The concept of a p-n junction, forward bias, reverse bias, MOS capacitance and operating regions of MOS are useful to understand the behavior of MOSFETs. The second order effects of MOSFETs are important since they can change the expected behavior of the device. Lastly, the velocity saturation region of a short channel device will be discussed since this is important in understanding the operation of MOSFETs in sub-micron technology at low supply voltages[5].

2.1 The P-N Junction

There exist free electrons in N-type silicon and free holes in P-type silicon. At the junction of these two types of semiconductors, holes from the P-type material migrate towards the N-type leaving behind donors and electrons from N-type move towards P-type leaving behind uncompensated acceptors. This results in a depletion region which creates an electric field whose direction opposes the diffusion of majority carriers. The electric field will sweep minority carriers across the junction resulting in a drift current which opposes the direction of diffusion current. The junction field builds up until these two current flows are equal and equilibrium is achieved[4]. The Cockcroft-Walton voltage multiplier circuit uses a P-N junction diode[2]. The P-N junction diode is shown in figure below. The expression for the zero bias built in potential is given by equation (2.1)

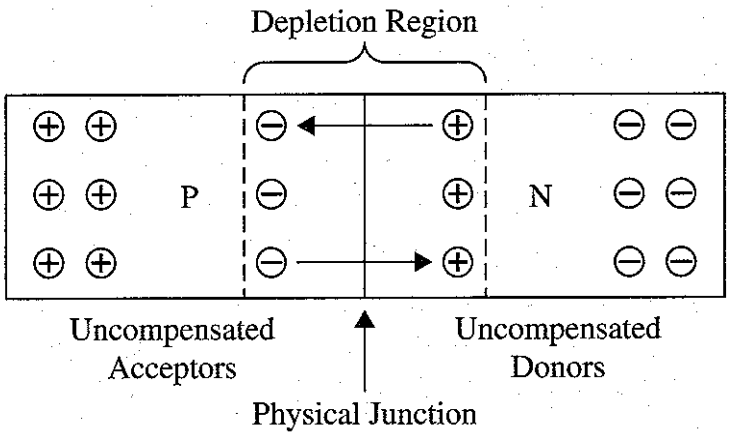


Figure 2.1 P-N Junction [4]

$$\phi_0 = V_t \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) \tag{2.1}$$

where $V_t = k \cdot T/q$ is thermal equivalent voltage with a value close to 26mV at room temperature, N_D and N_A are the doping concentrations of the P-type and N-type materials respectively and n_i is the intrinsic carrier concentration of silicon with the value of $1.45*10^{10}$ atoms/cm^3.

The expression of depletion capacitance C_j of the P-N junction diode is

$$C_j = \frac{C_{j0}}{\left[1-\left(\frac{V_d}{\phi_0}\right)\right]^m} \tag{2.2}$$

where V_d is the forward bias voltage applied across the junction, C_{j0} is the zero bias capacitance i.e. the effective capacitance when V_d = 0V and *m* is the grading profile whose value is 0.33 for a linear graded junction and 0.5 for an abrupt junction[7].

2.1.1. Reverse Bias

When applying, $V_d < 0$, the positive terminal of source connected to n-type material and negative terminal connected to p-type material, the process causes holes from the P-type material to become attracted towards the negative terminal and the same for electrons from the N-type material. This increases the width of the depletion region resulting in higher potential barrier. Figure 2.2 shows the energy band diagram under reverse bias.

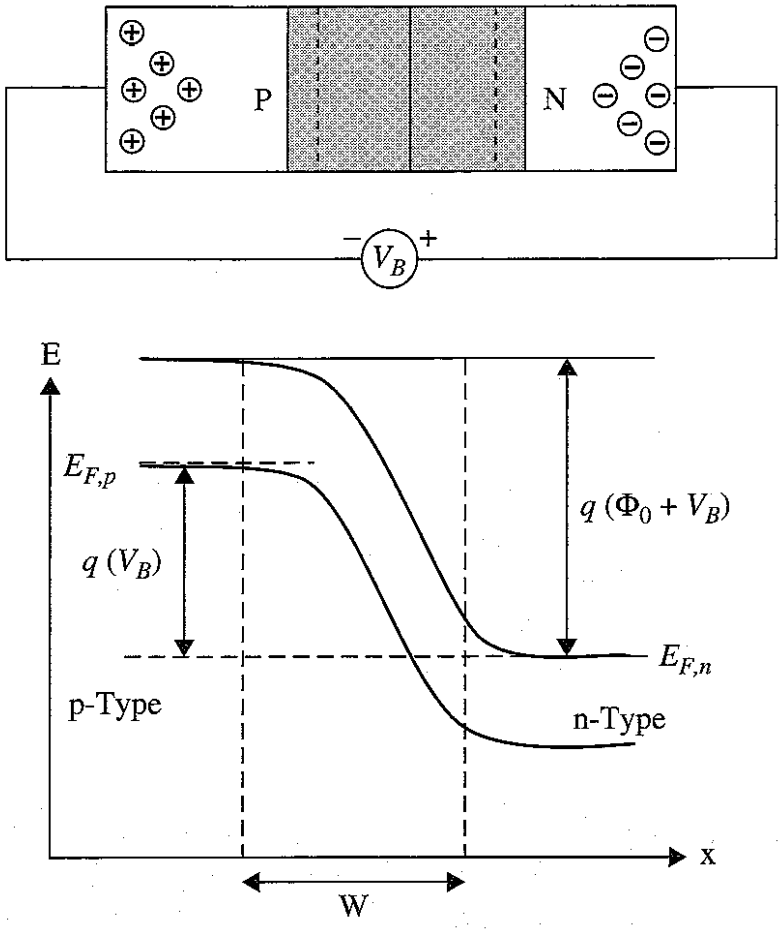


Figure 2.2 Reverse Bias [4]

The application of reverse bias voltage results in a higher potential barrier of ϕ_0+V_d. This high potential barrier near the junction reduces diffusion current to almost zero. The electron/hole

pair drift current is very small and insensitive to the height of the potential barrier. The drift current is a result of minority carrier crossing the junction.

2.1.2. Forward Bias

When applying $V_d > 0$, the positive terminal of the voltage source is connected to the P-type material and the negative terminal to the N-type material, the width of the depletion region decreases and the height of the potential barrier reduces to ϕ_0-V_d. Figure 2.3 shows the energy band diagram under forward bias. The majority carriers will easily cross the junction so that the diffusion current will be much larger than the drift current. In this case, excess electrons from the N-type material will easily cross the junction and recombine with holes in the P-type material and same is true for holes.

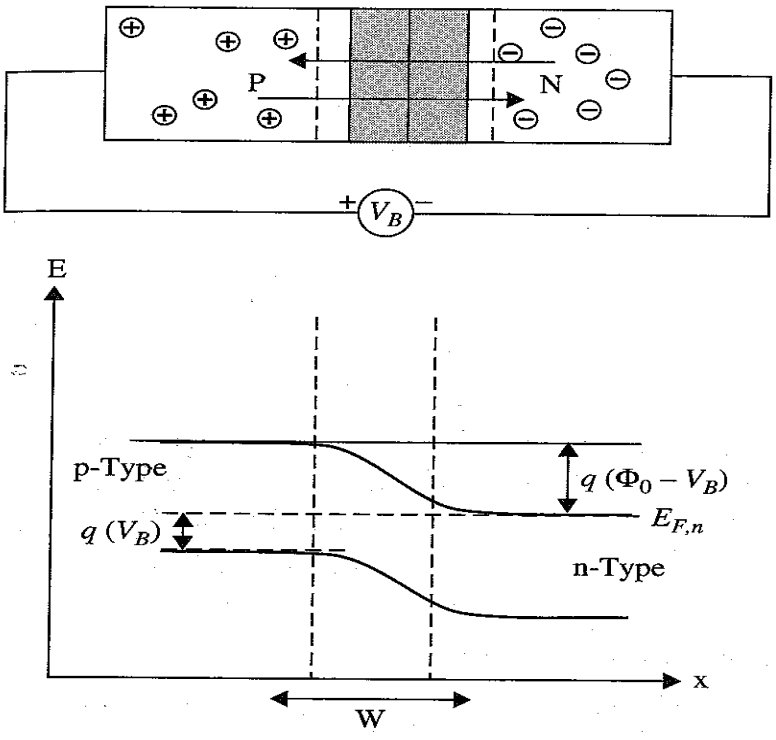


Figure 2.3 Forward Bias [4]

The expression for current density due to electron injection in the P-type material is:

$$J_n = q \cdot \frac{D_n}{L_n} . n_{p0} \left(e^{V/V_T} - 1 \right) \quad 2.3$$

The expression for current density due to hole injection in the N-type material is:

$$J_p = q \cdot \frac{D_p}{L_p} . p_{n0} \left(e^{V/V_T} - 1 \right) \quad 2.4$$

The total net current can be expressed as sum of the above two equations:

$$I = A \cdot \left(J_p + J_n \right) \quad 2.5$$

$$I = qA \left(\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0} \right) \left(e^{V/V_T} - 1 \right) \quad 2.6$$

or

$$I = I_S \left(e^{V/V_T} - 1 \right) \quad 2.7$$

where I_S is known as the reverse leakage current

$$I_S = qA \left(\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0} \right) \quad 2.8$$

From equation (2.8), the value of current depends on doping concentration of the material. Also, in the forward bias region the current increases exponentially with increase in the forward voltage whereas under reverse bias, the current is almost constant with value of $-I_S$[7].

2.1.3. P-N Junction Diode Characteristics

Figure 2.4 shows the I-V characteristics of a diode.

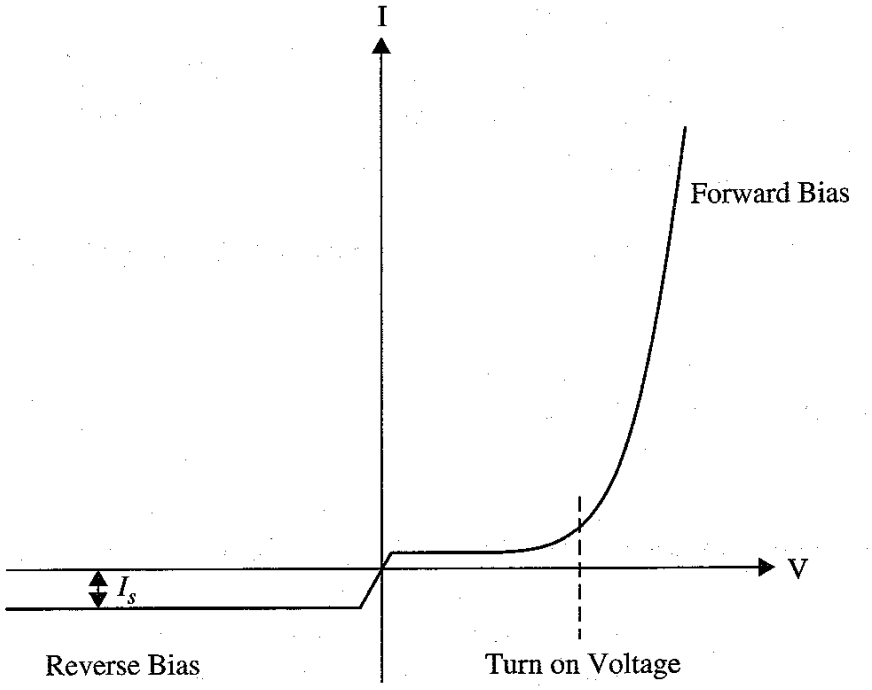


Figure 2.4 I-V characteristics of a diode [4]

In the third quadrant when the applied voltage is less than zero, i.e. reverse bias, the depletion region has significant width and diode can be thought of as an open switch with ideally no current flowing. In the first quadrant, with the increase in the applied voltage, at certain condition diode will conduct and act as a closed switch with almost zero impedance. Since, the transfer function is exponential, a little increase in the forward voltage results in the large current. The voltage at which the diode starts conducting is called the turn on potential and it has value close to 0.7V.

The reverse current through the diode is very small, but in some special diodes, like avalanche and zener diodes, high current is generated at some large reverse bias[7].

2.2 The MOS Capacitor

The MOSFET structure is shown in figure 2.5 where the gate is connected to the variable voltage source called V_{gs}. Also, the substrate, drain and source are connected to ground. A capacitor works on the principle of storing charge between two conducting plates. When V_{gs}=0, there is no potential difference between gate and substrate and hence no charge is stored.

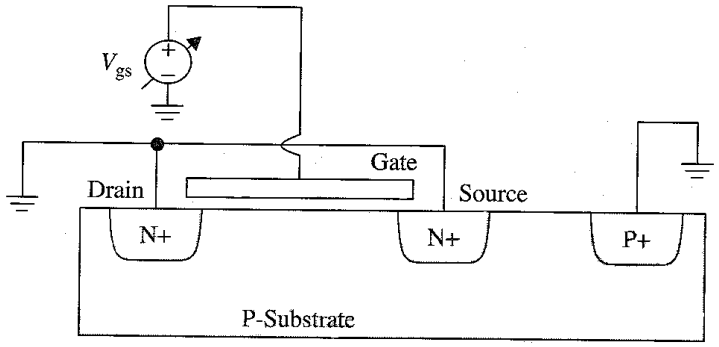


Figure 2.5 MOS Transistor structure [4]

Figure 2.6 shows the energy flat band diagram of a MOSFET in a steady state. The Fermi level of the gate, E_{FG}, is the same as the Fermi level of semiconductor, E_{FS}, since the metal work function, ϕ_m, is equal to the semiconductor work function, ϕ_s. There is no band bending in the MOSFET which indicates the gate dielectric does not have charge stored.

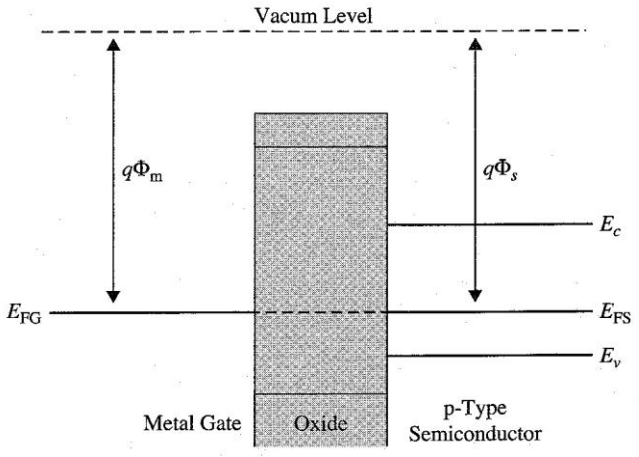


Figure 2.6 Flat band diagram at steady state [4]

2.2.1 Accumulation

When the gate bias is negative, $V_{gs} < 0$, the supply source provides negative charge on the gate. A net positive charge is gathered at the surface of the silicon substrate to maintain charge neutrality. Hence majority charge carriers are accumulated under the gate, and this is known as the accumulation phase. Figure 2.7 shows the MOSFET in accumulation.

During accumulation the Fermi level of the gate increases with respect to the Fermi level of the semiconductor due to negative bias at the gate. Figure 2.8 shows the Fermi level at accumulation. The energy band in the silicon substrate bends upward, bringing the valence band closer to the Fermi level due to accumulation of holes.

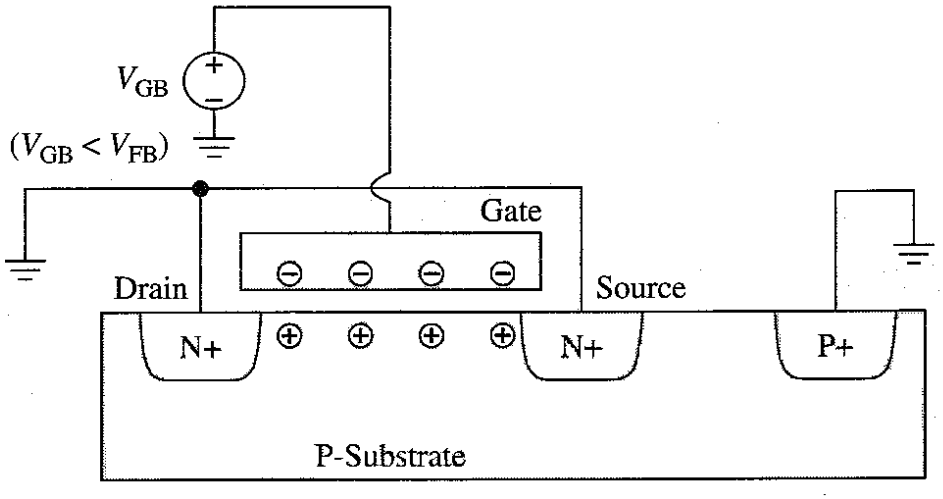


Figure 2.7 MOS transistor in accumulation [4]

2.2.2 Depletion

When gate bias, V_{gs} increases from a negative to a slightly positive value, the region under the gate is depleted of the holes that were gathered in accumulation. The holes are pushed away leaving behind ionized, negatively charged acceptor atoms, creating a depletion region, Figure 2.9 shows the MOSFET in depletion. During the depletion phase the Fermi level in the substrate is higher than the Fermi level of the gate by $q \cdot V_{gs}$. A positive surface potential

on the gate results from the downward bending of the energy bands. The valence band moves away from the Fermi level in the depletion region. Figure 2.10 shows the Fermi level at depletion

2.2.3. Weak Inversion

The surface under the gate oxide attracts more electrons when the gate bias exceeds a certain threshold. As more electrons start gathering under the oxide, the semiconductor surface is changed to act like N-type material and is termed *inverted*. In weak inversion, the surface contains

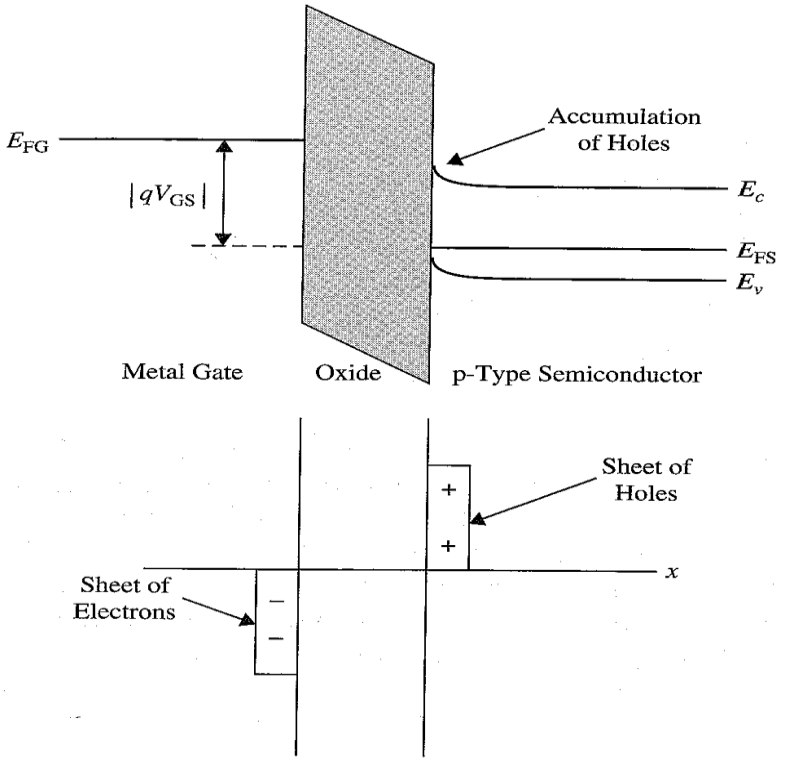


Figure 2.8 Fermi level at accumulation [4]

less electrons than the hole concentration and hence known as weak inversion. Figure 2.11 shows the Fermi level in weak inversion.

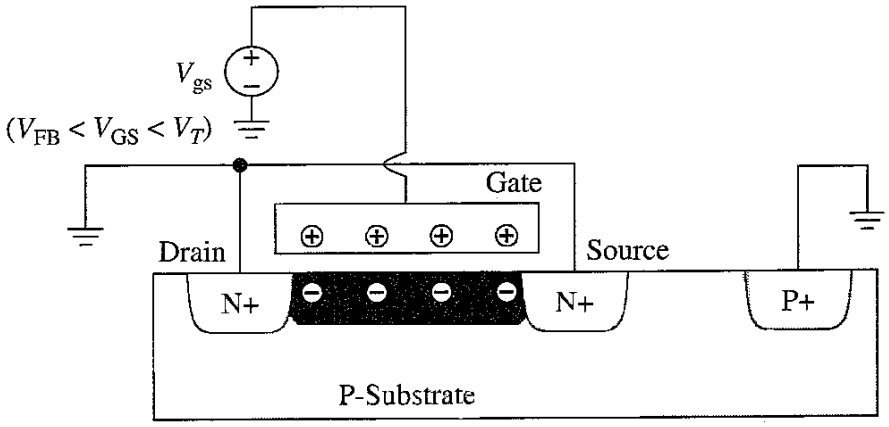


Figure 2.9 MOS transistor in depletion [4]

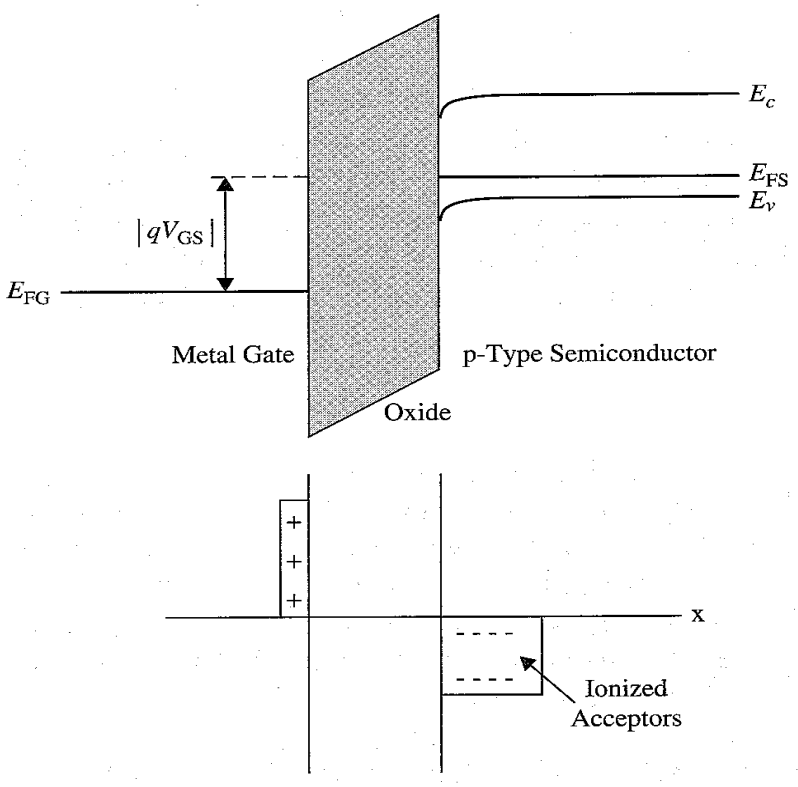


Figure 2.10 Fermi level at accumulation [4]

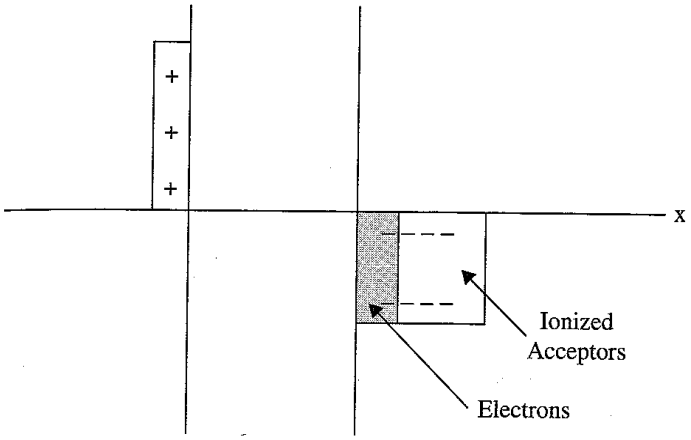


Figure 2.11 Fermi level at weak inversion [4]

2.2.4. Strong Inversion

When gate bias is sufficiently large, more electrons are attracted under the gate oxide, the region no longer remains P-type and hence it becomes *strongly inverted*. Figure 2.12 shows the MOSFET in strong inversion. The potential at which strong inversion is achieved is known as the *threshold voltage*. With increase in gate bias, bending in energy band increases as shown in figure 2.13

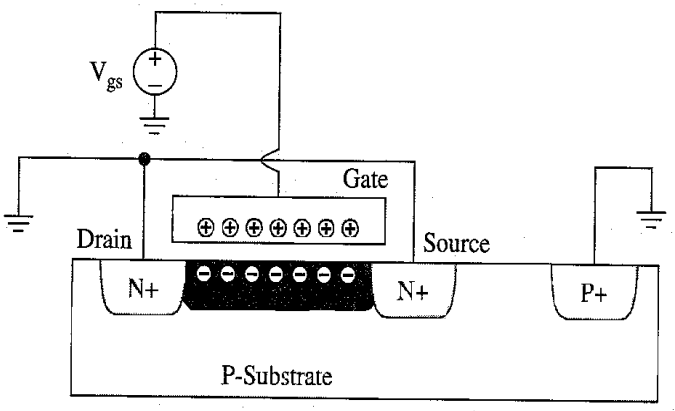


Figure 2.12 MOS transistor in strong inversion [4]

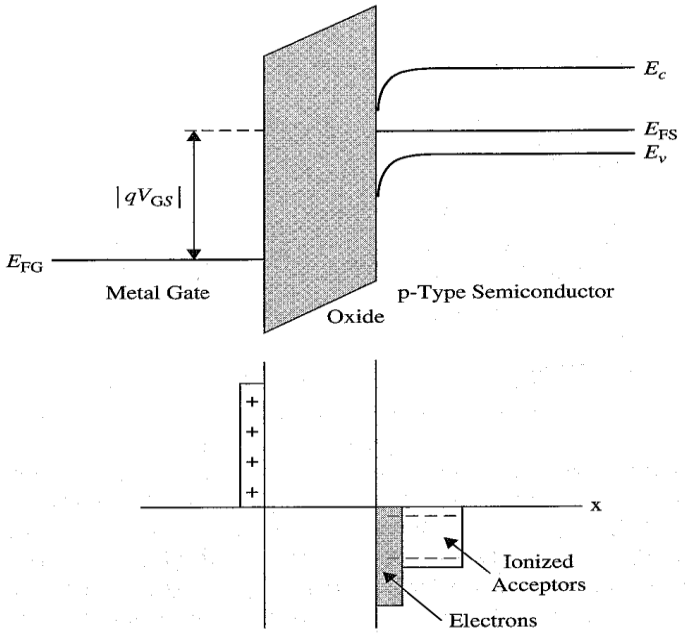


Figure 2.13 Fermi level at strong inversion [4]

2.3 Capacitance Variation of a MOS

The C-V curve of a N-type MOSFET can be better understood from the figure 2.14

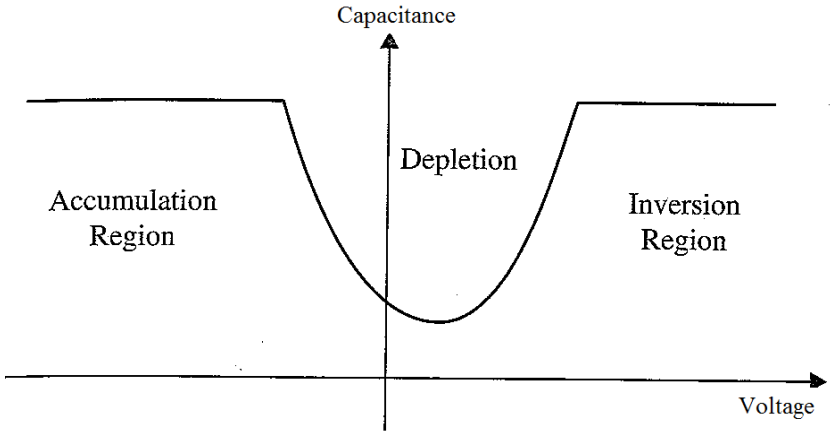


Figure 2.14 C-V curve of n-type MOSFET transistor [4]

With negative gate bias, the holes will be attracted under the oxide and MOSFET will be operating in the strong accumulation region with capacitance of C_{OX}. The gate is considered as

the upper plate and the substrate as the lower plate of a capacitor with the gate oxide as a dielectric material. Next, as the gate bias increases, the MOSFET enters the depletion region, the holes are pushed away from the surface and eventually the MOSFET enters the weak inversion region. The MOSFET capacitance is equal to the series capacitance of the gate oxide and the capacitance from the depletion layer. The series capacitance reduces the equivalent capacitance in the depletion region. Finally, with increase in gate bias above the threshold voltage, the MOSFET enters the strong inversion region. The channel is formed between the source and the drain which can be considered as the bottom plate of a capacitor, and the equivalent capacitance increases to C_{OX}. This is the best region to use the MOSFET as a capacitor with value close to C_{OX}.

2.4 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The two types of MOSFETs are the N-channel MOSFET and the P-channel MOSFET; these are called NMOS and PMOS respectively. The static model of the MOSFET will be derived using the NMOS device. All the arguments are valid for the PMOS devices also. The concept of the velocity saturation region in the sub-micron technology will be discussed at the end of chapter. There are two modes of NMOS:

1. Enhancement mode with no conducting channel at $V_G=0$
2. Depletion mode with a conducting channel at $V_G=0$

The operating region of the NMOS will be limited to the enhancement mode MOSFET. The MOSFET operates on the principle of controlling the current between the source and the drain using the electric field generated by the gate voltage as a control variable[6].

2.4.1 Device Operating Region

The threshold voltage of the MOSFET is the gate voltage where current starts flowing between the source and the drain. It is given by equation (2.9)

$$V_t = V_{t0} + \gamma\left[\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right] \quad 2.9$$

where ϕ_F is the Fermi potential of the substrate, V_{SB} is the voltage between the source and the bulk and γ = the body effect coefficient and is given by

$$\gamma = \frac{\sqrt{2qE_{SI}N_A}}{C_{OX}} \quad 2.10$$

When gate bias is less than V_t, $V_{GS} < V_t$, there is no channel between the source and the drain. Current through the device is almost zero so the MOSFET can be viewed as an open switch. This is called the cut-off region of the MOSFET. Figure 2.15 shows the MOSFET in the cut-off region

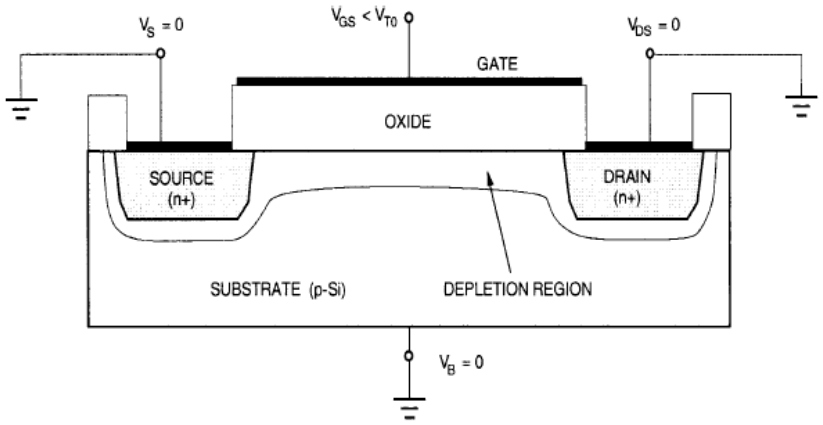


Figure 2.15 MOS in cut-off region [6]

When gate bias is above V_t, $V_{GS} > V_t$, the channel forms between the source and the drain. The electrons flow from the source to the drain resulting in the drain current. In this region, voltage at the drain is small compared to V_{GS} - V_t and the MOSFET is operating in the ohmic or triode region behaving like a resistor. Figure 2.16 shows the MOS in the triode region.

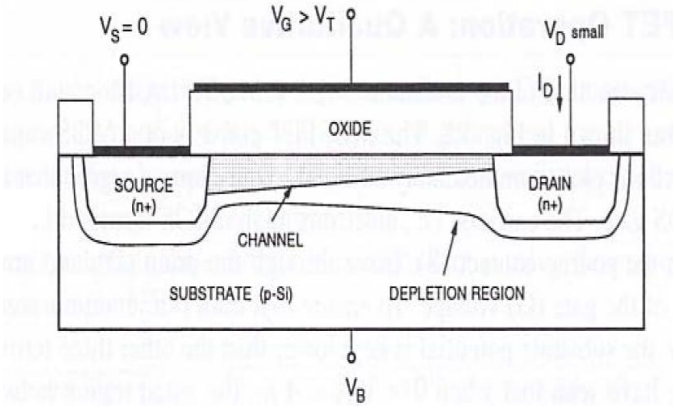


Figure 2.16 MOS in triode region [6]

The drain current in the triode region is given by the following equation

$$I_{DS,lin} = \frac{W}{L}\mu \cdot C_{OX}^{'}\left[\left(V_{GS} - V_t\right)\cdot V_{DS} - \frac{1}{2}V_{DS}^2\right] \qquad 2.11$$

where W/L is the ratio of width to length ratio of the MOSFET gate, μ is the mobility of electrons in NMOS and holes in PMOS, and C_{OX} is the capacitance of gate oxide.

Next, when V_{DS} is increased to $V_{DS} \geq V_{GS} - V_t$, the channel between the source and the drain is pinched off due to the drain end of channel being at higher potential than the source[4]. This is called the saturation region of the MOSFET where it behaves like a constant current source with a fixed value of drain current. Figure 2.17 shows the MOSFET in the saturation region.

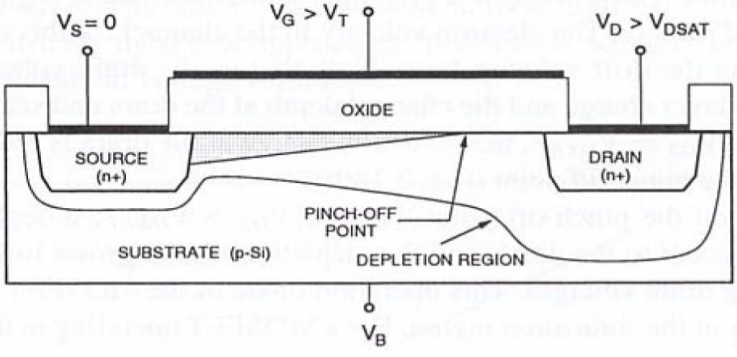


Figure 2.17 MOS in saturation region [6]

The drain current no longer follows the equation same as the triode region, but it is given by the equation (2.12)

$$I_{DS,sat} = \frac{W}{L_{eff}} \mu \cdot C_{OX}^{'} \left(V_{GS} - V_{DS}\right)^2 \qquad 2.12$$

where L_{eff} is the effective length of the device. Figure 2.18 shows the basic I-V characteristics of a long channel NMOS device. As shown in the figure, in the linear region current increases linearly with the applied voltage, and in the saturation region the drain current is almost constant. It also shows quadratic dependence of I_{DS} on V_{GS} in saturation region which is not the case with short channel devices that use sub-micron technology[5].

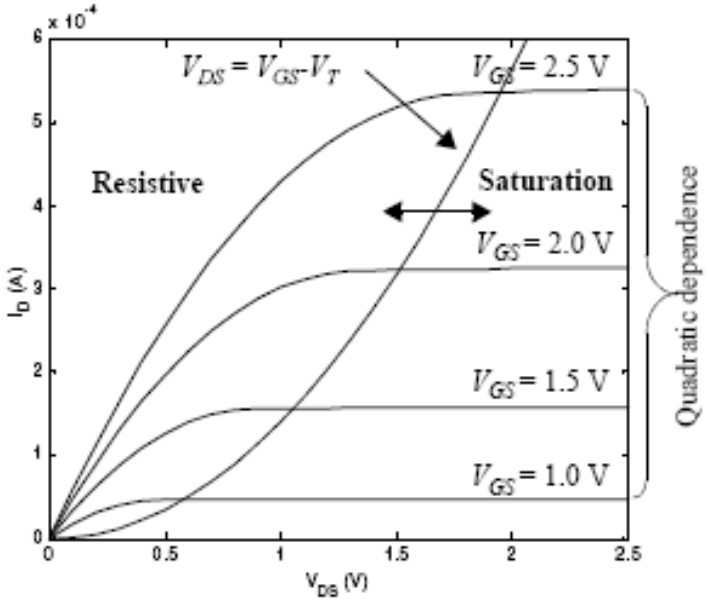


Figure 2.18 I-V characteristics of NMOS [5]

2.4.2 Second order effects in MOS Devices

Second order effects of MOSFETs, which are used as switches become important for some charge pump applications.

2.4.2.1 Substrate Bias Effect (Body Bias Effect)

The value of the threshold voltage, V_t, is strongly dependent on the source to the bulk voltage. The value of V_t is calculated from the equation (2.9), and $V_t = V_{t0}$ for $V_{SB} = 0$. But sometimes the value of V_{SB} is not zero and V_t varies according to the value of V_{SB} in a charge pump circuit. This effect is known as body bias effect which plays a major role in designing a charge pump circuit using sub-micron technology.

2.4.2.2 Channel Length Modulation

In the saturation region, the current between the source and the drain is constant or estimated to be a current source independent of the applied terminal voltage, V_{DS}. The effective channel length is modulated by the applied V_{DS}. Increasing the V_{DS} causes depletion region to grow reducing the effective length of channel[6]. A more realistic description of the current can be given by

$$I_D = I_D^{'}\left(1+\lambda \cdot V_{DS}\right) \qquad 2.13$$

where $I_D^{'}$ is the current in the saturation region and λ is called the channel length modulation parameter.

2.4.2.3 Punch Through Effect

When the drain of the MOSFET is biased at higher voltage than the source, there might be a case where the depletion region of the drain could overlap the depletion region of the source. It will cause current to flow irrespective of the gate voltage. This phenomenon is known as punch through effect[4].

2.4.2.4 Impact Ionization

In sub-micron technology, the gate length decreases which results in stronger electric field near the drain region of the transistor and imparts electrons with enough energy to become

hot. These hot electrons impact the drain, dislodging the holes that are swept towards the substrate and appear as current. This effect is known as impact ionization[4].

2.4.3 Velocity Saturation[5]

The behavior of short channel devices, transistors with a short channel length, varies considerably from the resistive and saturation mode discussed in earlier sections. The difference in behavior of the MOSFET is due to the effect of velocity saturation. In long channel devices, carriers have a constant mobility and the velocity of the carriers is directly proportional to electric field. But in short channel devices, the velocity of carriers tend to saturate after reaching a critical electric field due to the scattering effect. Figure 2.19 shows the velocity saturation effect.

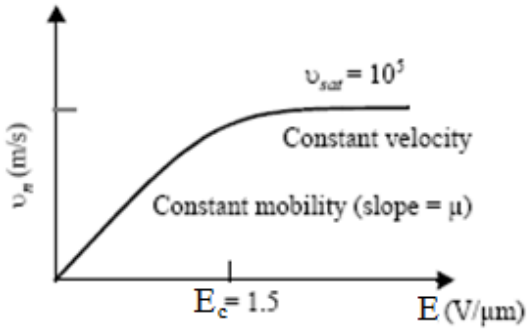


Figure 2.19 Velocity Saturation Effect[5]

Due to the velocity saturation effect, short channel devices have an extended saturation region compared to long channel devices. Figure 2.20 shows the extended saturation region in short channel devices.

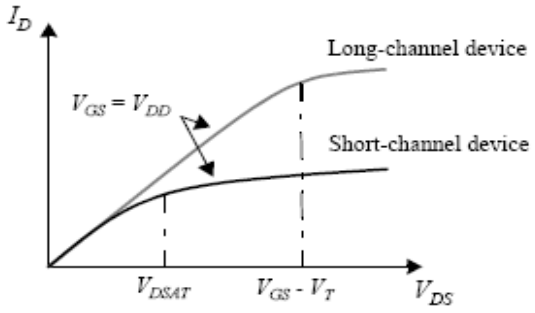


Figure 2.20 Saturation regions in long channel and short channel devices [5]

Figure 2.21 shows the basic I-V characteristics of a short channel device. Also, the quadratic behavior of I_{DS} with respect to applied voltage V_{GS} in long channel devices no longer exists in short channel devices. The behavior in short channel devices between I_{DS} and V_{GS} is linear as shown in figure 2.21. So the increase in drain current is not quadratic in sub-micron technology.

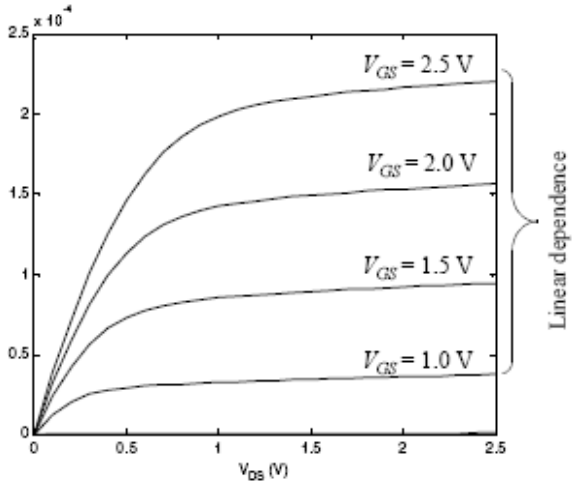


Figure 2.21 I-V characteristics of short channel device [5]

CHAPTER 3

OPERATION OF A CHARGE PUMP

The charge pump circuit is used to generate a voltage larger than the supply voltage in EEPROMs, flash memories, power management blocks, image sensor circuits and displays etc. Multiplication of voltage is done by using the concept of the bucket brigade delay line by Dickson[3]. The bucket brigade delay line stores the value of voltage along the line of capacitors with each step of clock cycle.

3.1 Voltage Doubler Circuit

3.1.1 Voltage doubler with no load:

Consider the simple circuit shown in figure 3.1 consisting of three switches and a capacitor.

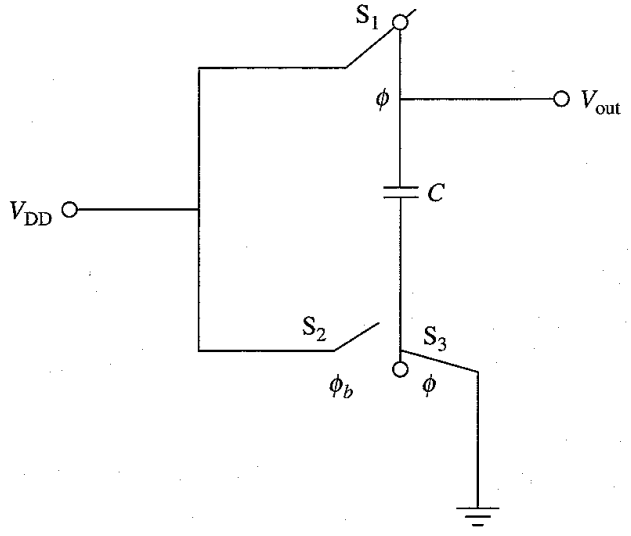


Figure 3.1 Voltage doubler circuit with no load [1]

During clock phase, ϕ, switches S_1 and S_3 are closed and the capacitor is charged to the value of the supply voltage, V_{DD}. In the clock phase, ϕ_b, switches S_1 and S_3 are opened and switch S_2 is closed. The bottom plate of the capacitor assumes a potential of V_{DD}, while the capacitor maintains its charge of $Q = C \cdot V_{DD}$ from the previous phase. This means that during phase ϕ_b,

$$Q = C(V_{out} - V_{DD}) = C \times V_{DD} \quad 3.1$$

$$V_{out} = 2 \times V_{DD} \quad 3.2$$

Thus, in the absence of a load, an output voltage has been generated that is twice the supply voltage[1,3].

3.1.2 Voltage doubler with a load:

Figure 3.2 shows the circuit with the load resistor R_L and the capacitor C_{out} in parallel at the output.

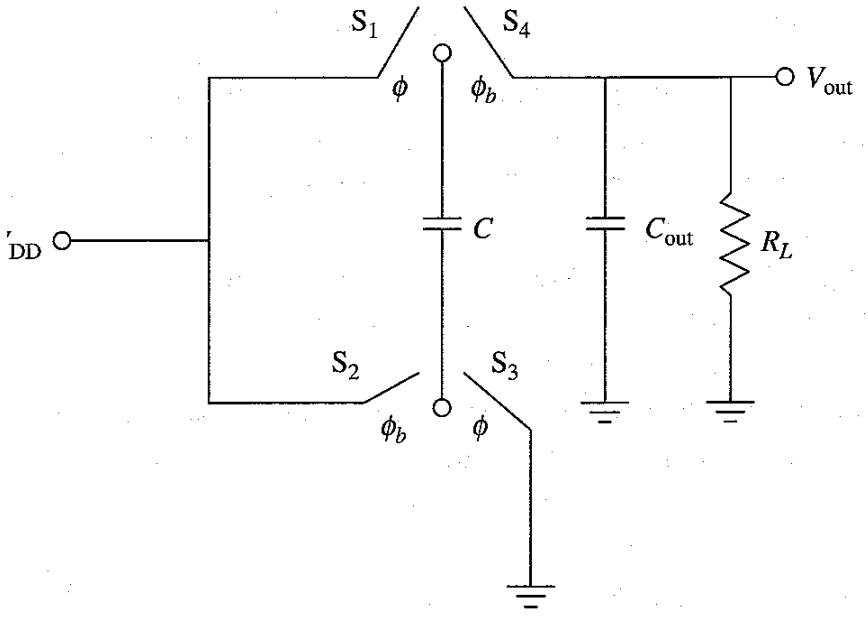


Figure 3.2 Voltage doubler circuit with a load [1]

During clock phase, ϕ, switches S_1 and S_3 are closed and the capacitor *C* is charged to the supply voltage V_{DD}. In the next phase, ϕ_b, switches S_2 and S_4 are closed, switches S_1 and S_3 are opened and the bottom plate of the capacitor is charged to V_{DD} with the top plate charging to $2 \cdot V_{DD}$. The ideal V_{out} is given by the following equation,

$$V_{out} = \frac{C}{C + C_{out}} \bullet 2V_{DD} \qquad 3.3$$

The presence of the capacitor C_{out} reduces the value of the output voltage, V_{out}. Due to R_L at the load, a ripple voltage, V_R each be reduced by making the value of C_{out} larger resulting in the reduction of the output voltage, V_{out}.

3.2 Dickson Charge Pump

The charge pump by Dickson uses the principle of the voltage multiplication circuit by Cockcroft-Walton[2]. Figure 3.3 shows the Dickson charge pump circuit using diodes for the switches.

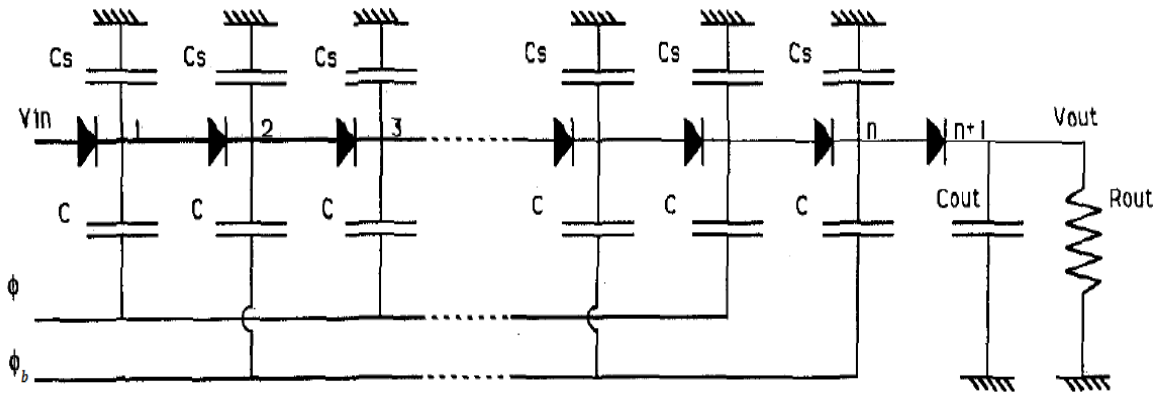


Figure 3.3 Dickson charge pump using diode switches[9]

For implementation on monolithic integrated circuits, Dickson used diode connected N-type MOSFETs. The forward bias voltage of diode V_d, is replaced with the threshold voltage V_t of an

N-channel MOSFET. Figure 3.4 shows the charge pump implementation with N-type MOSFETs.

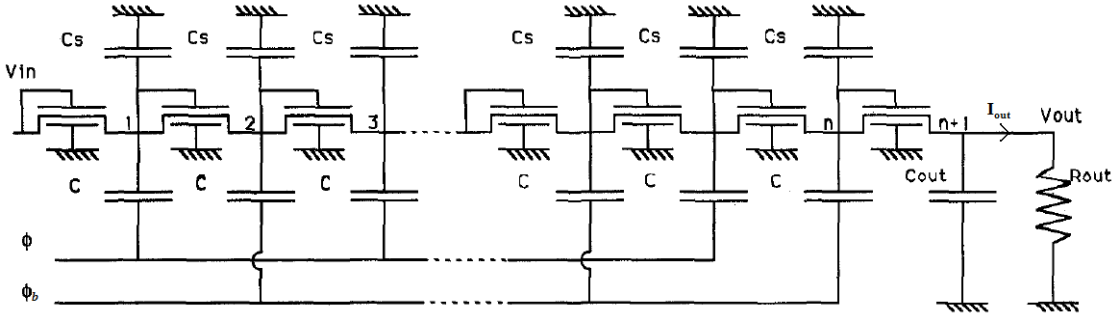


Figure 3.4 Dickson charge pump using N-type MOSFET switches[9]

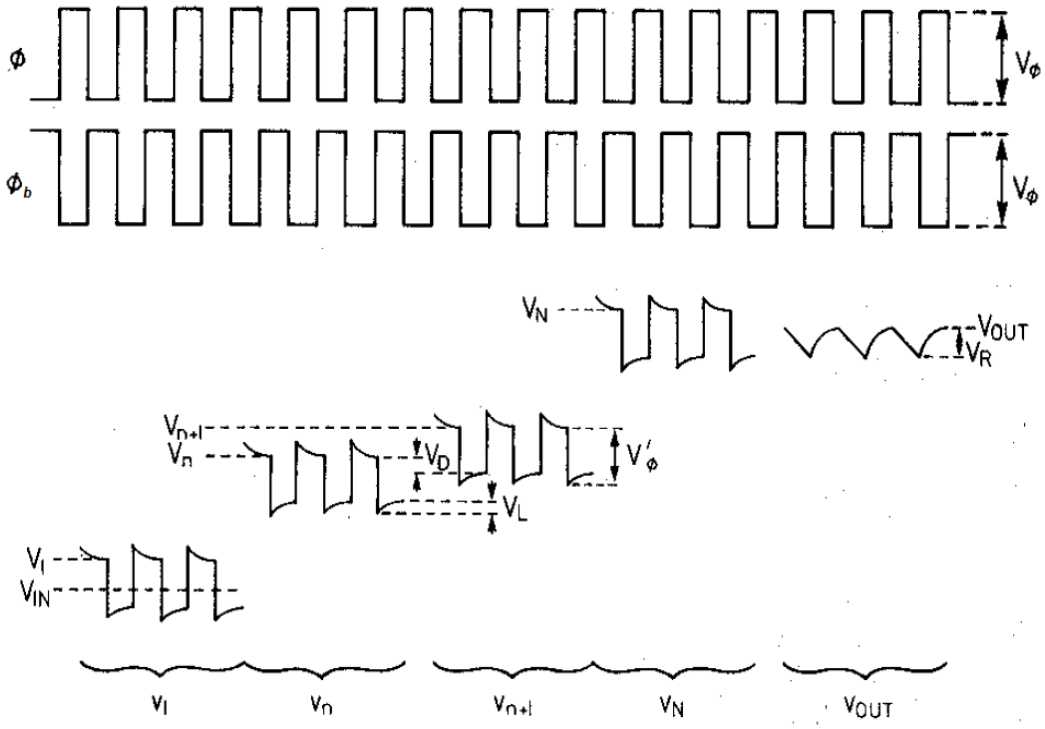


Figure 3.5 Voltage waveforms in N-stage multiplier [3]

Figure 3.5 shows the typical voltage waveforms in an N-stage multiplier. The two out-of-phase clocks ϕ and ϕ_b with amplitude V_ϕ are capacitively coupled to alternate nodes. During each half of the clock cycle, the two clocks alternatively increase the potential voltage at subsequent

nodes by pumping the packets of charge along the diode chain. As shown in figure 3.5, the voltage difference between the n^{th} and $(n+1)^{th}$ node is given by

$$V_{n+1} - V_n = V_\phi^{'} - V_t - V_L \quad 3.4$$

where $V_\phi^{'}$ is the voltage swing at each node due to capacitive coupling from the clock, V_t is the threshold voltage of the MOSFET and V_L is the voltage to charge and discharge output capacitance when multiplier is supplying an output current I_{out}. Due to parallel connection between stray capacitance, C_s and a clock coupling capacitance, C, the value of V_ϕ is reduced to $V_\phi^{'}$.

$$V_\phi^{'} = \left(\frac{C}{C + C_S} \right) \bullet V_\phi \quad 3.5$$

A higher value of C_S results with a lower value of $V_\phi^{'}$ which reduces the value of V_{out}. Also, the current supplied at the clock frequency, f, by the multiplier is

$$I_{out} = f(C + C_S) \cdot V_L \quad 3.6$$

Substituting equations (3.5) and (3.6) in (3.4) gives,

$$V_{n+1} - V_n = \left(\frac{C}{C + C_S} \right) \bullet V_\phi - V_t - \frac{I_{out}}{f(C + C_S)} \quad 3.7$$

above equation gives the value for single stage. Hence, for N stages it is given by the following equation

$$V_N - V_{in} = N\left[\left(\frac{C}{C + C_S} \right) \bullet V_\phi - V_t - \frac{I_{out}}{f(C + C_S)} \right]$$

where $V_N = V_{out}$ and $V_{in} = V_{DD}$. An additional isolating diode with the threshold voltage V_t is required at the output to prevent clock breakthrough, thus V_{out} is given by,

$$V_{OUT} = V_{DD} + N\left[\left(\frac{C}{C+C_S}\right)\bullet V_\phi - V_t - \frac{I_{out}}{f(C+C_S)}\right] - V_t \qquad 3.8$$

Rearranging equation (3.8) gives

$$V_{OUT} = V_{DD} + N\left[\left(\frac{C}{C+C_S}\right)\bullet V_\phi - V_t\right] - V_t - \frac{N\cdot I_{out}}{f(C+C_S)} \qquad 3.9$$

At the multiplier output, there is also a ripple voltage, V_R, discharging the output capacitance C_{OUT} which is given by

$$V_R = \frac{I_{OUT}}{f\cdot C_{OUT}} = \frac{V_{OUT}}{f\cdot R_L\cdot C_{OUT}} \qquad 3.10$$

Large ripple voltage can affect the operations of EEPROMs, flash memories, PLLs etc. From equation (3.10), the value of the ripple voltage can be decreased by increasing the values of clock frequency or the load capacitance. Frequency is related to the charge pump's efficiency and hence cannot be increased beyond a certain limit. Also, increasing the load capacitance C_{OUT} can affect output ramp up time[1,3,4]. As seen from equation (3.8), a charge pump will only work if

$$N\left[\left(\frac{C}{C+C_S}\right)\bullet V_\phi - V_t - \frac{I_{out}}{f(C+C_S)}\right] > 0$$

which can be simplified as

$$\left[\left(\frac{C}{C+C_S}\right)\bullet V_\phi - V_t - \frac{I_{out}}{f(C+C_S)}\right] > 0$$

Equation (3.8) can be written as,

$$V_{OUT} = V_O - I_{OUT}\cdot R_S \qquad 3.11$$

where

$$V_O = V_{DD} + N\left[\left(\frac{C}{C+C_S}\right)\bullet V_\phi - V_t\right] - V_t \qquad 3.12$$

and

$$R_S = \frac{N}{f(C+C_S)} \qquad 3.13$$

V_O and R_S are the open-circuit output voltage and output series resistance of the charge pump circuit respectively. Figure 3.6 shows the equivalent circuit of a charge pump represented by equation (3.11)

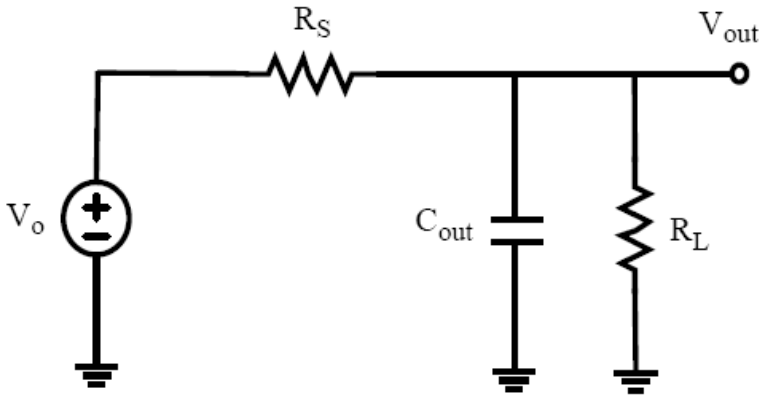


Figure 3.6 Charge pump equivalent circuit [1]

where the values of V_o and R_S are given by the equations (3.12) and (3.13) respectively.

3.3 Charge Pump System

A charge pump system is a closed loop system where the output of the charge pump is maintained at the pre-determined voltage. The charge pump should be on whenever the output voltage is less than the regulation voltage. Also, if the output voltage reaches or exceeds the regulation voltage level, the charge pump should be turned off. Figure 3.6 shows the block diagram of the charge pump system.

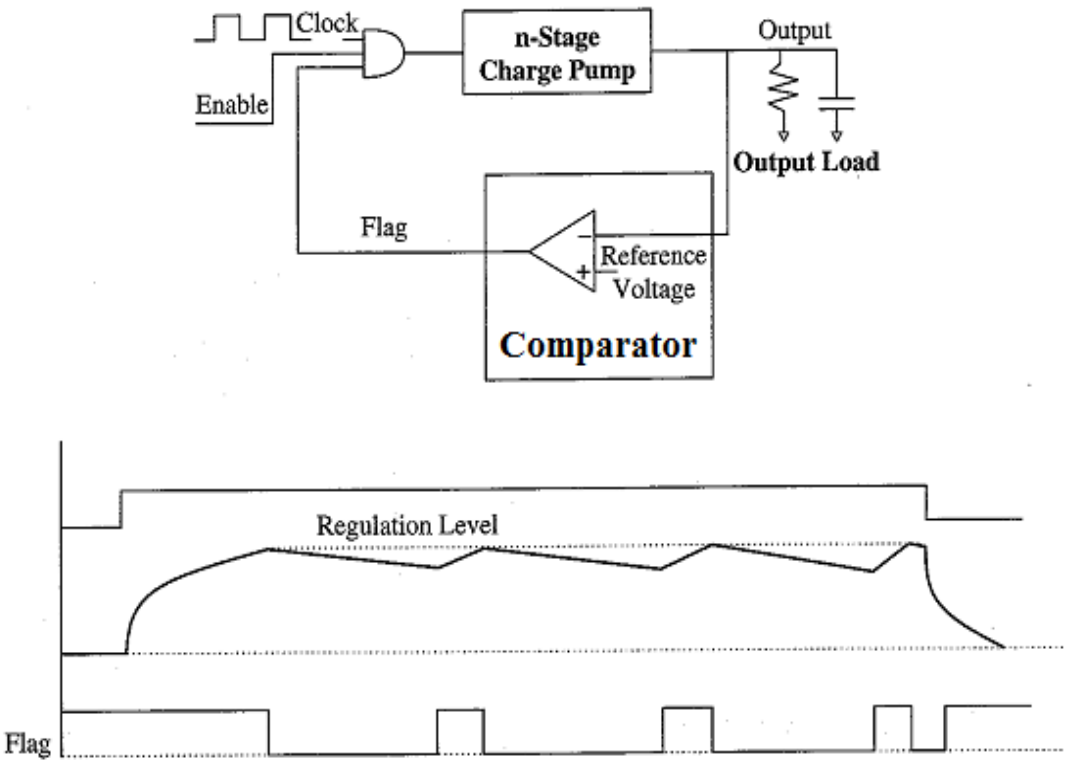


Figure 3.7 Charge pump system [4]

Initially, the output voltage of the pump is zero which enables the charge pump using the feedback voltage regulator. The voltage regulator uses the comparator to enable or disable the charge pump. It compares the value of the output voltage with the reference voltage to turn on or off the charge pump. With the enabling of charge pump, the output voltage will start rising and finally will reach the regulated voltage level. As soon as the output voltage reaches the regulated voltage, the voltage regulator turns off the charge pump. If the load consists of only capacitance, the charge pump output should remain in this state for a longer period of time and ideally the charge pump should not be turned on again once the regulation voltage level is reached. But leaking of output DC current, capacitive coupling from nearby signals and current dissipation in the voltage regulator will cause the output of the charge pump to discharge with

time[4]. This causes the output voltage to go below the regulated voltage which results in enabling of the charge pump by the voltage regulator and the process keeps on repeating.

CHAPTER 4

DESIGN OF THE CHARGE PUMP

The factors that need to be considered while designing the charge pump are gate length of the device, voltage increase, loading, pump power consumption and die size. For optimization of the charge pump design, there is a trade-off between the number of charge pump stages and the output current drivability, that is, how much current a charge pump can deliver at a prescribed voltage. The increase in the number of charge pump stages results in the increase of internal impedance of the charge pump which reduces the current drivability. For a particular number of stages, the output current can be increased by increasing the width of diode connected MOSFETs and the size of capacitors, which increases the parasitic resistance and the parasitic capacitance in each stage. This increase in the R·C delay plays a significant role in determining the output voltage and the charge pump efficiency.

4.1 MOSFET Parameters

The design of the charge pump depends on IC manufacturing technology. Reduction in device size reduces the value of the required supply voltage resulting in a lower value of output voltage of the charge pump after each stage. Small device size increases the number of transistors on a die which results in the decrease of the area of the die and hence reduction in the cost of a chip.

The architecture and circuit design of the charge pump is a function of the technology. The supply voltage, gate oxide, threshold voltage, channel length modulation coefficient, minimum gate length are important parameters that play a role in charge pump design. This project uses 0.25 μm Taiwan Semiconductor Manufacturing Company (TSMC) technology for

the design of the charge pump. The technology files used in cadence software for N-channel MOSFETs and P-channel MOSFETs are included in the Appendix A.

4.2 Charge Pump Specifications

The important parameters for a charge pump are the steady state output voltage, output voltage ramp-up, recovery time, output drive current and power supply voltage.

4.2.1 Output Voltage

The number of stages in the charge pump is directly related to the output voltage by the following equation (Figure 4.1)

$$V_{out} = N \cdot V_{\phi} + V_{in} - (N+1) \cdot V_t \qquad 4.1$$

For example, if the clock amplitude, V_{ϕ}, is 2.5 V, the input voltage, V_{in}, is 2.5 V and the threshold voltage, V_t, is 0.2 V, then to generate the output voltage V_{out} of 16 V, there should be at least N=6 stages.

However, due to the body bias effect at higher pump stages the performance of the charge pump degrades. The value of the threshold voltage, V_t, increases to more than 2 due to the higher source to bulk voltage V_{SB} which results in less increase in the output voltage. There are other factors such as the parasitic capacitance which stores charge and increase the internal impedance of the charge pump. Hence, it is advised to use 8 to 9 stages for generating 16V output voltage from 2.5 V input voltage.

4.2.2 Current Drivability

The output current is a very critical specification since with the increase in the output voltage of the charge pump the internal impedance of the charge pump increases. This results in the decrease of the output drive current. The power efficiency of the charge pump decreases

as the pump output voltage increases[4]. The relation between the number of charge pump stages and the internal impedance can be given by following equation

$$R_S = \left[\frac{N}{C + C_S} \right] \times \frac{1}{F_{clk}} \qquad 4.2$$

To achieve a higher output voltage, the number of pump stages, N, needs to be increased, but from the equation (4.2), this increases the internal impedance, R_S, resulting in lower output current. To achieve higher output current at the higher output voltage, the pump clock frequency needs to be increased or the size of the capacitor C needs to be boosted. Also, an increase in the threshold voltage, V_t, increases the internal impedance of the charge pump circuit. The higher value of the output drive current results in faster output ramp-up time and quicker recovery time. The output drive current I_{out} can be calculated using the following equation (Figure 4.1)

$$I_{out} = C_{Load} \cdot \frac{V_{out}}{T_{ramp-up}} \qquad 4.3$$

where C_{Load} is the load capacitance, V_{out} is the output voltage of the charge pump and $T_{ramp-up}$ is the time required by the charge pump to reach the output voltage.

Next, the value of the boost capacitors, C, is calculated. In the last stage of the charge pump, the value of the output voltage increases by ΔV from stage 5 to stage 6 as shown in figure 4.1. The output drive current is I_{out} and the charge pump clock frequency is F_{clk}. Therefore, the value of capacitor, C, is calculated by the following equations

$$I_{out} = C \cdot \Delta V \cdot F_{clk}$$

$$C = \frac{I_{out}}{\Delta V \cdot F_{clk}} \qquad 4.4$$

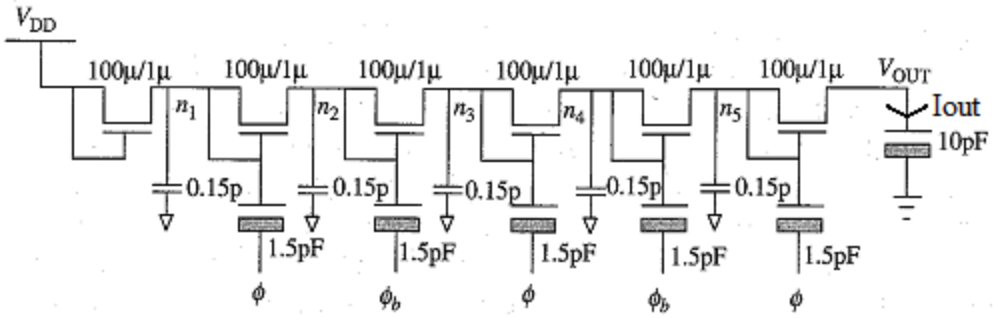


Figure 4.1 Charge pump circuit with N=6 stages [4]

4.2.3 Output Ramp-up time and Recovery time

The output ramp-up time and the voltage recovery time are the benchmarks of the charge pump performance. The charge pump needs to ramp up the output fast enough to complete the operation in the shortest possible time to meet the speed requirements[4]. The important measure of the charge pump's capability is the output voltage recovery time. The charge pump's output voltage is inversely proportional to the output drive current. When a sudden change in the load occurs a current spike may drain the charge pump output stage resulting in a decrease in the output voltage. The time needed to restore the output voltage is the recovery time.

The output ramp-up time and the voltage recovery time can be controlled by the clock frequency and the size of the capacitors. An increase in the frequency of operation will expedite the process of charge transfer in each stage. A larger capacitor will allow more charges to be transferred and decrease the time needed to recover the output voltage. The charge pump should be designed at 70%-80% of its maximum voltage step up to meet the specifications of the ramp-up time and the output voltage recovery time.

4.2.4 Power Consumption

The rising demand in handheld devices and low power applications has made power consumption in charge pump devices a very important factor. Whenever the voltage step value is increased, the efficiency decreases. This can be a substantial part to the power consuming circuits on a chip. The power consumption in the charge pump circuit is given by the following equation,

$$P_D = C \cdot V_{DD}^2 \cdot F_{clk} \qquad 4.5$$

Increasing the size of capacitor, C, and frequency of operation will improve the performance, but it will also increase the overall power consumption of the circuit. There is a major trade-off between the performance and the power of the charge pump circuit. There are many design techniques that can reduce the power dissipation in equation (4.5). One such method uses a multistep frequency control, where the charge pump is operated at a high frequency till the regulated output voltage is achieved, and then switched to a lower frequency to maintain that regulated output voltage[4].

4.3 Charge Pump Clock Source

The generation of a clock source for the charge pump operation is a very important aspect in the circuit design of the charge pump. Figure 4.2 shows the clock source built using a ring oscillator. The ring oscillator consists of an odd number of inverting gates connected in a ring pattern. The oscillation in the circuit is enabled using the NAND gate. The frequency of oscillation can be given by the following equation

$$f = \frac{1}{N \cdot \left(t_{phl} + t_{plh}\right)} \qquad 4.6$$

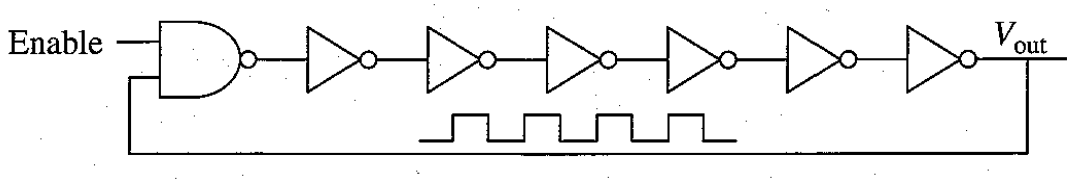


Figure 4.2 Clock source using ring oscillator

where N is the number of stages in the oscillator, t_{phl} is the propagation delay from high to low or the falling edge and t_{plh} is the propagation delay from low to high or the rising edge. But, for 50% duty cycle $t_{plh}=t_{phl}$ and the frequency of oscillation is given by the following equation,

$$f = \frac{1}{2N \cdot T_D} \tag{4.7}$$

where T_D is the propagation delay. However, the ring oscillator frequency varies with supply voltage and temperature. The oscillation frequency can vary as much as 30% over the typical operating conditions, which will cause a change in the output voltage noise, power consumption, output voltage recovery time etc.

A better technique is to use the current controlled ring oscillator. Figure 4.3 shows the current controlled ring oscillator. The voltage source derived from the band gap reference voltage generator adds stability to the oscillator over temperature and process variations. The frequency of operation can be given by the following equation

$$f = \frac{I_{ref}}{N \cdot C_{stage} \cdot V_{DD}} \tag{4.8}$$

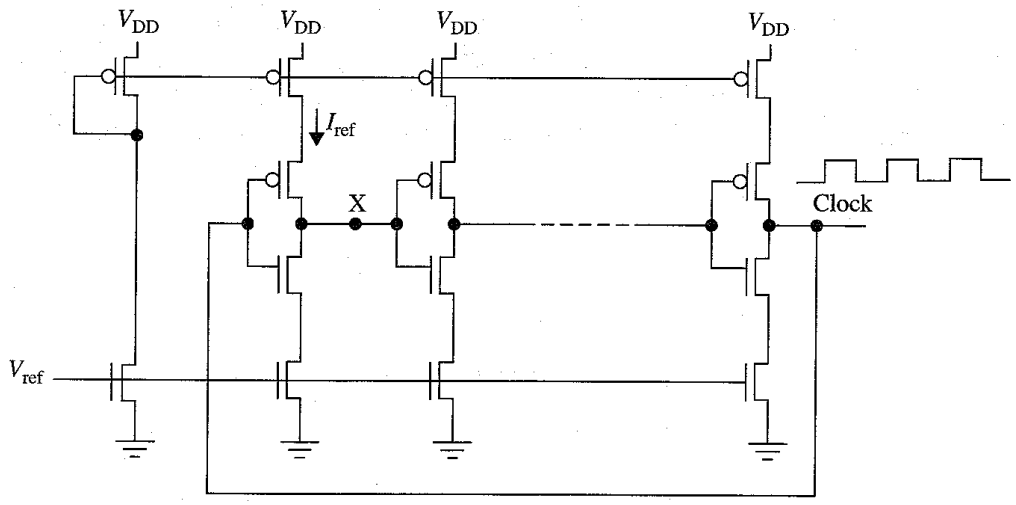


Figure 4.3 Current controlled ring oscillator

The design of the charge pump circuit always requires the amplitude of the clock source voltage to be higher than the power supply voltage of V_{DD}. The higher amplitude of clock source voltage results in a smaller number of stages connected serially. Thus the internal impedance of the charge pump is reduced. The use of higher amplitude clocks makes the charge pump design more efficient. When the power supply is scaled down and the frequency of operation is high, the threshold voltage of the MOSFET increases resulting in the reduced pump gain.

4.4 Cross Coupled Voltage Doubler

A cross coupled voltage doubler circuit is shown in figure 4.4. The two non-overlapping clocks with voltage V_O and V_{Ob} are the inputs of the voltage doubler circuit, while Out and Out_b are the outputs of the circuit. When V_O of the clock input goes high, it causes MOSFET P_{1b} to turn off and MOSFET N_{1b} turns on pulling down the output node Out_b to ground, while MOSFET N_{2b} turns on, which precharges the node X_{1b} to the value $V_{DD} – V_t$. In the next clock phase, V_O goes low, which causes MOSFET N_{1b} and N_{2b} to turn off, while MOSFET P_{1b} turns on.

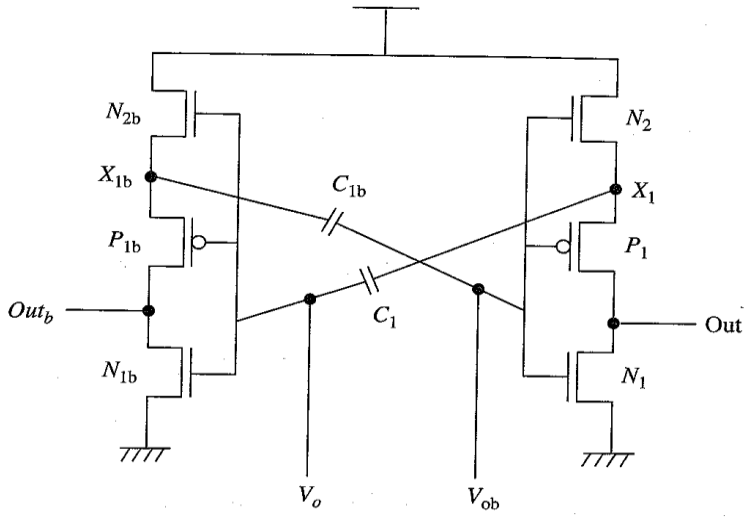


Figure 4.4 Cross coupled voltage doubler circuit

Also, the clock V_{Ob} goes high, pushing node X_{1b} to $2V_{DD} – V_t$, which is passed through P_{1b} to the output. A similar operation is performed on the right side of the voltage doubler circuit. The negative V_t term results in the lower efficiency of the charge pump circuit. With an increase in the number of stages, the negative V_t term keeps on increasing resulting in a lower increase in the output voltage. Figure 4.5 shows the voltage waveform of the cross coupled voltage doubler circuit. The 2 stages of cross coupled voltage doubler circuit can be cascaded to generate a voltage of $3V_{DD} – 2V_t$. The 3 stages of cross coupled voltage doubler circuit can be cascaded to produce $4V_{DD} – 3V_t$. Figure 4.6 shows the cascaded voltage doubler circuit with 2 stages. The capacitance at nodes $X_1(X_{1b})$ is to be kept minimum, since the charge of this capacitance is shared between the capacitor $C_1(C_{1b})$ and the parasitic capacitances.

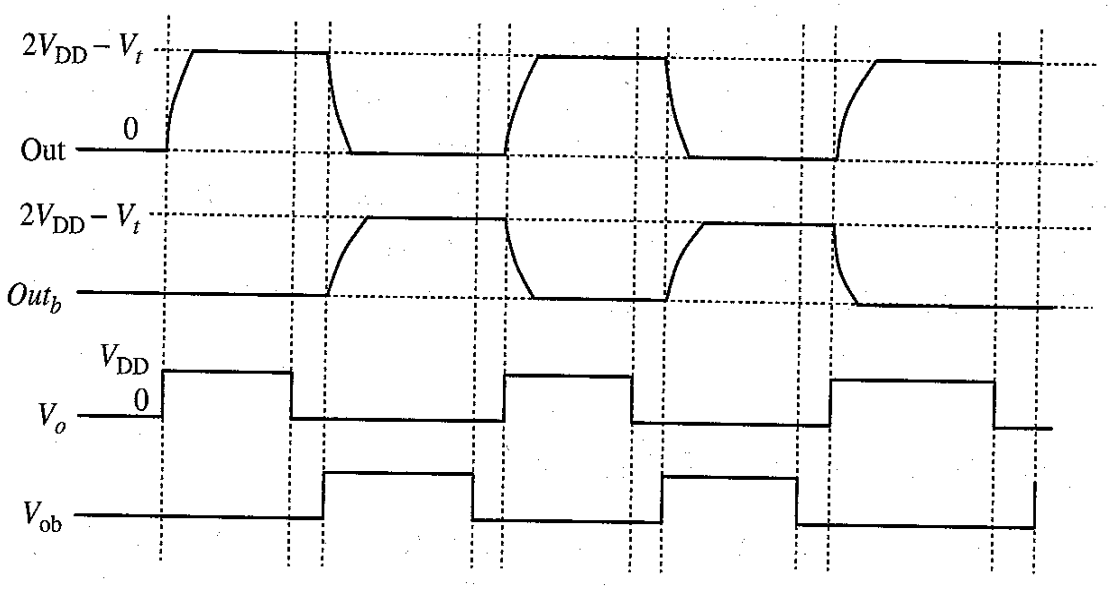


Figure 4.5 Voltage waveform of a cross coupled voltage doubler circuit

As two or more stages are cascaded to generate higher voltages, the charge sharing problem will result in inefficiency of the charge pump.

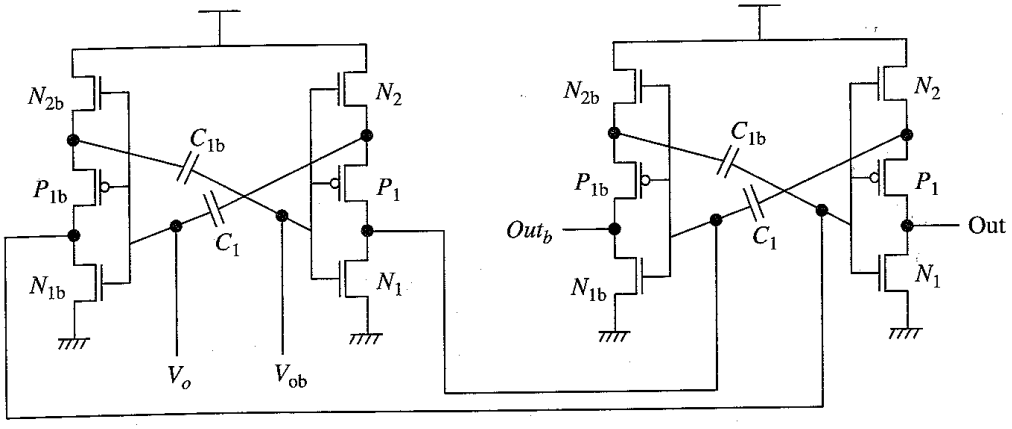


Figure 4.6 Cascaded cross coupled voltage doubler circuit

CHAPTER 5

ADVANCED CHARGE PUMP ARCHITECTURE

The Dickson two phase charge pump has a voltage drop of V_t in each stage. With an increase in the number of stages the value of V_t increases due to the body effect. Also, as the supply voltage, V_{DD}, decreases the pumping gain of the charge pump decreases since the output voltage is directly proportional to the supply voltage. Thus, it is obvious that Dickson charge pump is not suitable for low voltage operation. If the threshold voltage drop could be eliminated at each stage, the Dickson charge pump would be usable at low voltages, offering a better pumping gain and higher output voltage. The V_t cancellation circuit is added to the Dickson charge pump circuit and is called the static Charge Transfer Switch(CTS) charge pump[1,4,14].

5.1 Static CTS Charge Pump

The static CTS charge pump is also called the New Charge Pump-1(NCP-1). The static CTS charge pump is a charge pump that uses dynamic feedback to improve the charge-transfer efficiency. This architecture uses a V_t cancellation technique to improve the performance at low voltages. Figure 5.1 shows the schematic of static a CTS charge pump circuit with a V_t cancellation scheme. The circuit is divided into 2 parts by the dividing line. The bottom portion of the static CTS charge pump circuit is similar to the two phase Dickson charge pump circuit. The top portion is the new circuit added to cancel the V_t of N-channel MOSFET using dynamic feedback technique. Figure 5.2 shows the output voltage at each stage. For better understanding of the charge pump operation, consider the first charge pump stage of the circuit. Assuming parasitic capacitance is smaller than the boost capacitance of the charge pump

circuit, the threshold voltage V_t of MOSFET M_5 get cancelled by the high phase voltage of Clk_b.

The following equations are to be satisfied for operation of a static CTS charge pump circuit

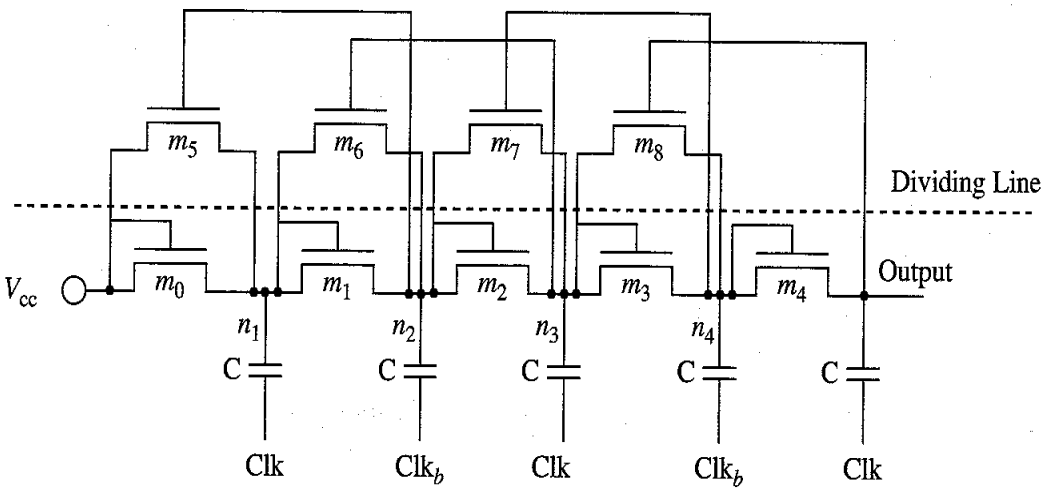


Figure 5.1 Static CTS charge pump (NCP-1) [4]

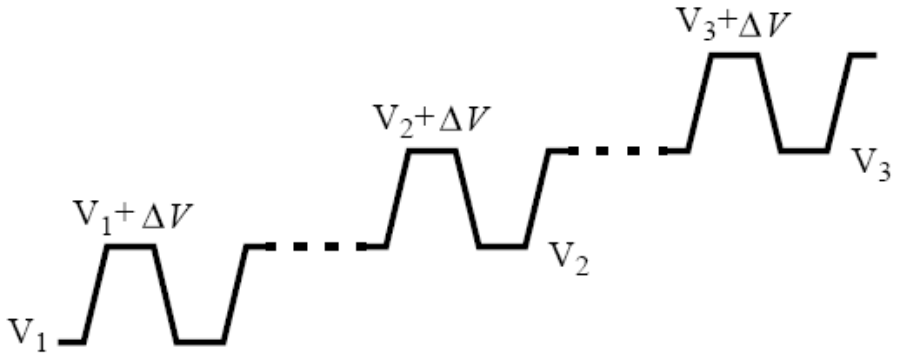


Figure 5.2 CTS based charge pump voltage fluctuation

When Clk_b goes high, following equations are satisfied

$$V_{n1} = V_{cc} - V_t \qquad 5.1$$

Now, calculating the voltage at node n_2, when Clk_b is high,

$$V_{n2} = V_{n1} + V_{cc} - V_t + V_{cc} = 3V_{cc} - 2V_t \quad (5.2)$$

$$V_{n2} - V_t \geq 0 \quad \Rightarrow \quad 3V_{cc} - 3V_t \geq 0 \quad (5.3)$$

At the low phase voltage of Clk_b, M_5 is in the cut-off state and hence V_{gs} of M_5 is less than V_t. The following equations are to be satisfied for operation of a static CTS charge pump circuit.

$$V_{n2} - V_t \leq 0 \quad (5.4)$$

$$V_{cc} - V_t + V_{cc} - V_t \leq 0 \quad (5.5)$$

$$2V_{cc} - 2V_t \leq 0 \quad (5.6)$$

Equations (5.1 – 5.3) are satisfied as long as the chip supply voltage is higher than the V_t of N-channel MOSFET. If equations (5.1 – 5.3) are satisfied, equations (5.4 – 5.6) cannot be satisfied since reverse leakage current occurs. This is one of the problems with the static CTS charge pump circuit. In order to fix this problem, there are some modifications made to the circuit. The modified circuit is called the New Charge Pump-2 (NCP-2).

5.2 New Charge Pump-2 (NCP-2)

The problem of NCP-1 can be resolved by adding N-channel MOSFET M_1 and P-channel MOSFET M_2 to control the gate voltage of M_5. The P-channel MOSFET, M_2, allows the higher voltage potential from the next stage to the gate of M_5 during the charge transferring process. The N-channel MOSFET, M_1, will lower the V_{gs} of M_5 taking the gate to source voltage below the threshold voltage. The equations (5.4 – 5.6) are not satisfied with the modified circuit when Clk_b goes low. This modified circuit is called the New Charge Pump-2 (NCP-2). Figure 5.3 shows the modification in the NCP-1 circuit. The difference between the gate and the source voltage of static charge switches in each clock phase is $2 \cdot \Delta V$. The necessary conditions for the NCP-2 charge pump to operate properly are

$$2 \cdot \Delta V > V_{tp} \tag{5.7}$$

$$2 \cdot \Delta V > V_{tn} \tag{5.8}$$

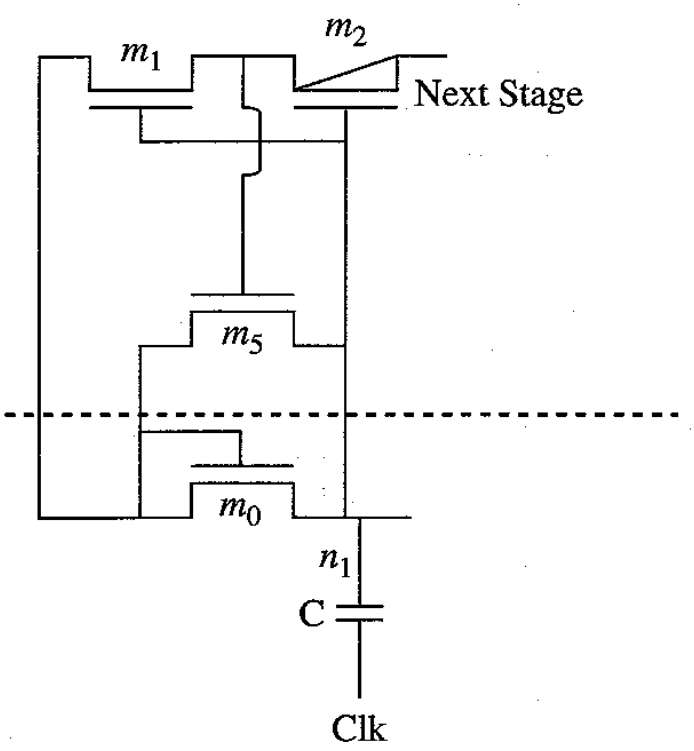


Figure 5.3 Modification in NCP-1 [4]

The NCP-2 circuit has improved performance over the Dickson charge pump at low voltage operations. The NCP-2 circuit has added 3 extra transistors compared to the original Dickson charge pump circuit. This results in an increase of area and parasitic capacitance of the charge pump. There is an additional N-well required in the process for P-channel MOSFETs in the NCP-2 circuit. Also, the P-channel MOSFET device is added to the high voltage path. The technology should be available to process the high voltage P-channel MOSFET. It is inferred from figure 5.2 that dynamic feedback can be used to improve the efficiency of the charge pump circuit.

CHAPTER 6

SIMULATION RESULTS

This chapter shows the simulation results of the voltage doubler circuit with ideal switches and diode connected N-channel MOSFET switches. Also, simulation results of the Dickson charge circuit with N=6 stages and output voltage, V_{out} = 15 V is shown

6.1 Voltage Doubler Circuit using Ideal Switches

Figure 6.1 shows the schematic of the voltage doubler circuit used for simulation with ideal switches S_1 and S_3 closed and switch S_2 open. The power supply voltage V_{DD} used for simulation is 2.5 V.

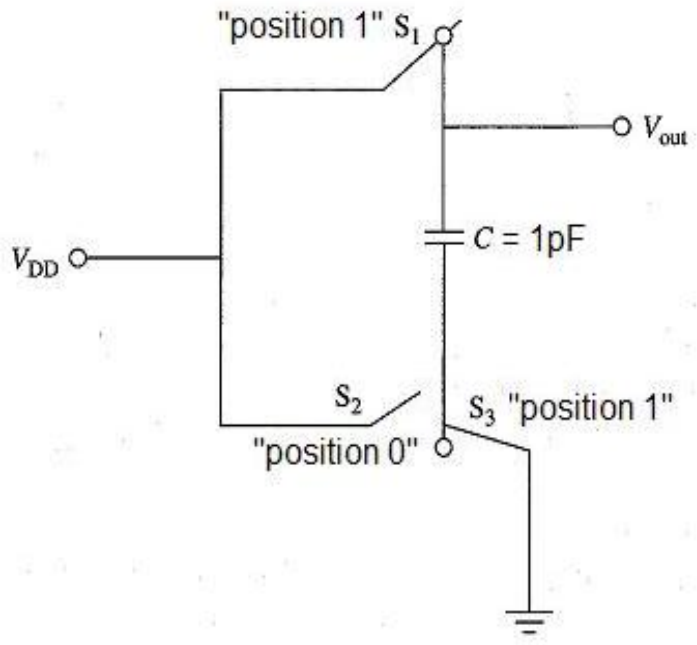


Figure 6.1 Schematic with switches S_1 and S_3 ON

Figure 6.2 shows the schematic with ideal switches S_1 and S_3 open and switch S_2 close.

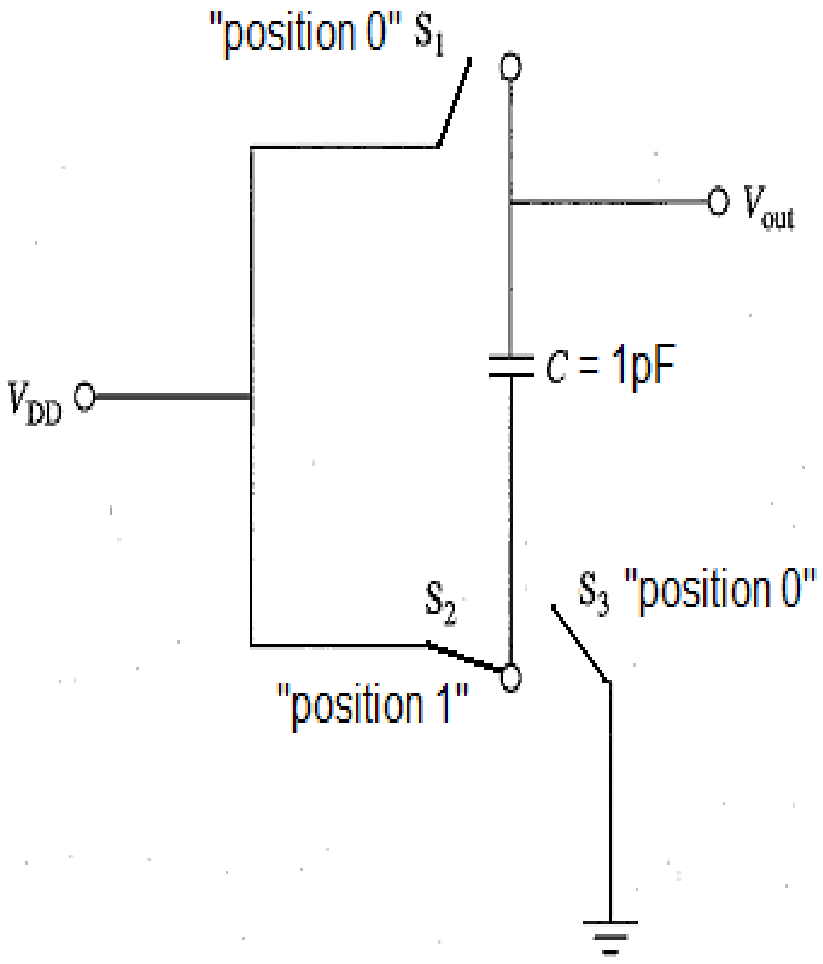
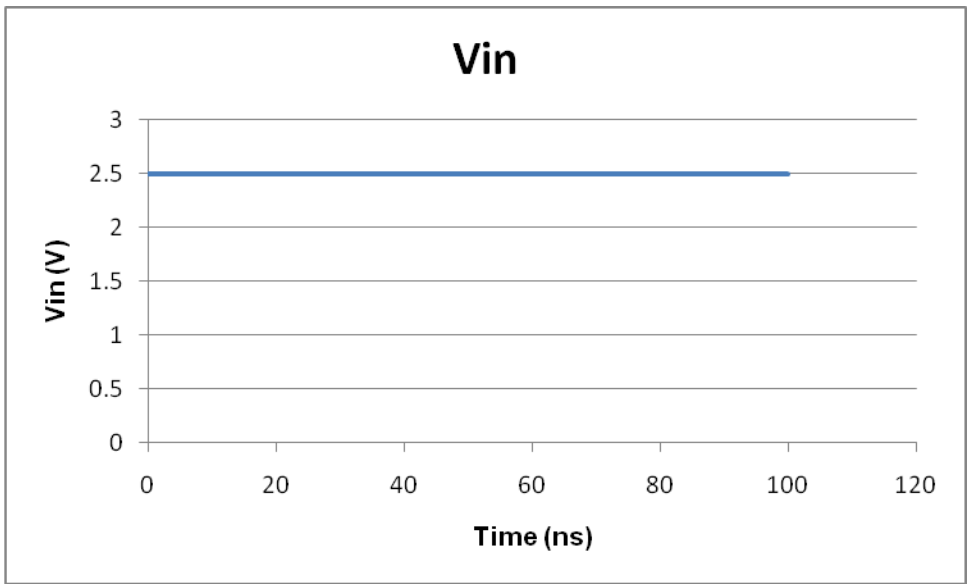


Figure 6.2 Schematic with switch S_2 ON

Figure 6.3 shows the simulation results of the voltage doubler circuit with ideal switches.



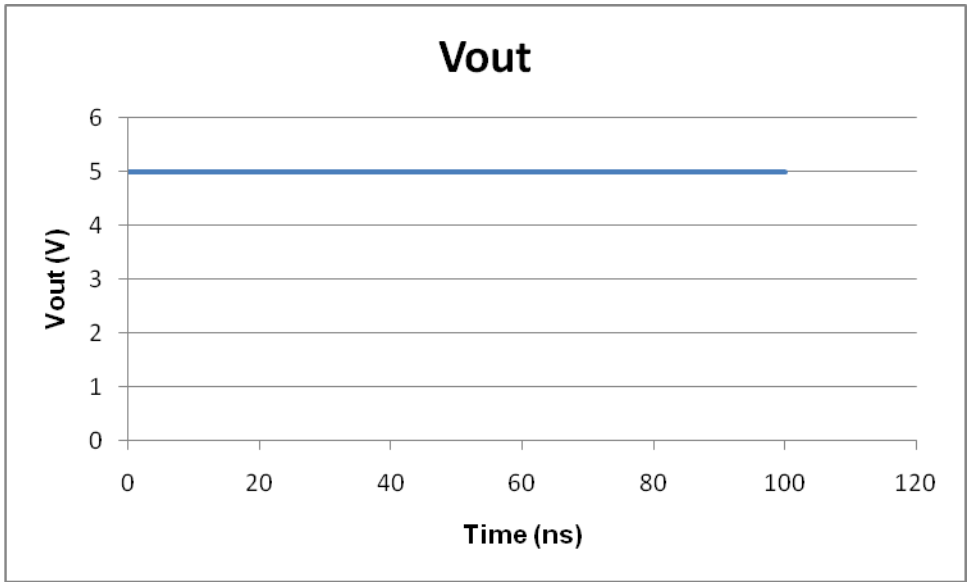


Figure 6.3 Voltage doubler output waveform

6.2 Voltage Doubler using N-channel MOSFET Switches

Figure 6.4 shows the schematic of voltage doubler circuit with diode connected N-channel MOSFET switches used for simulation. The circuit uses two non-overlapping clocks with the same amplitude of 2.5 V. Figure 6.5 shows the output voltage waveform for the voltage doubler circuit with diode connected MOSFETs

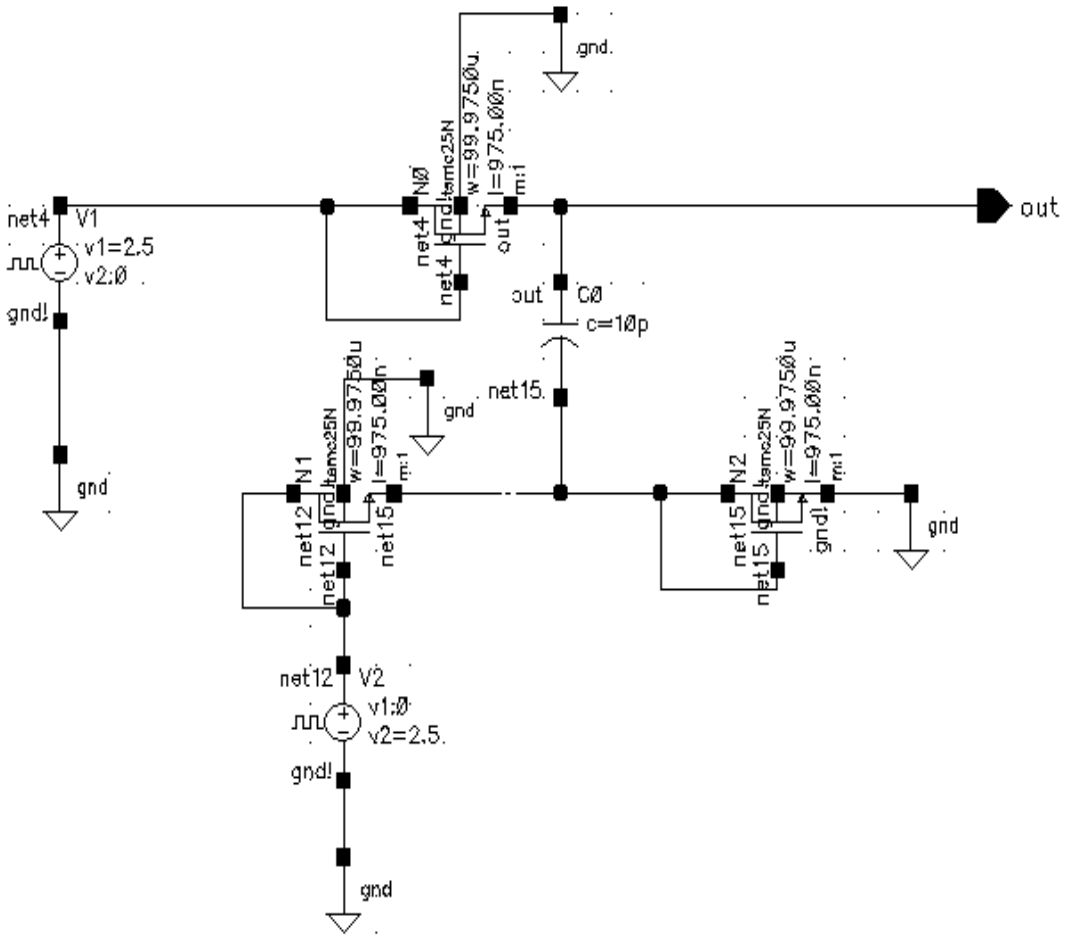


Figure 6.4 Voltage doubler with NMOS switches

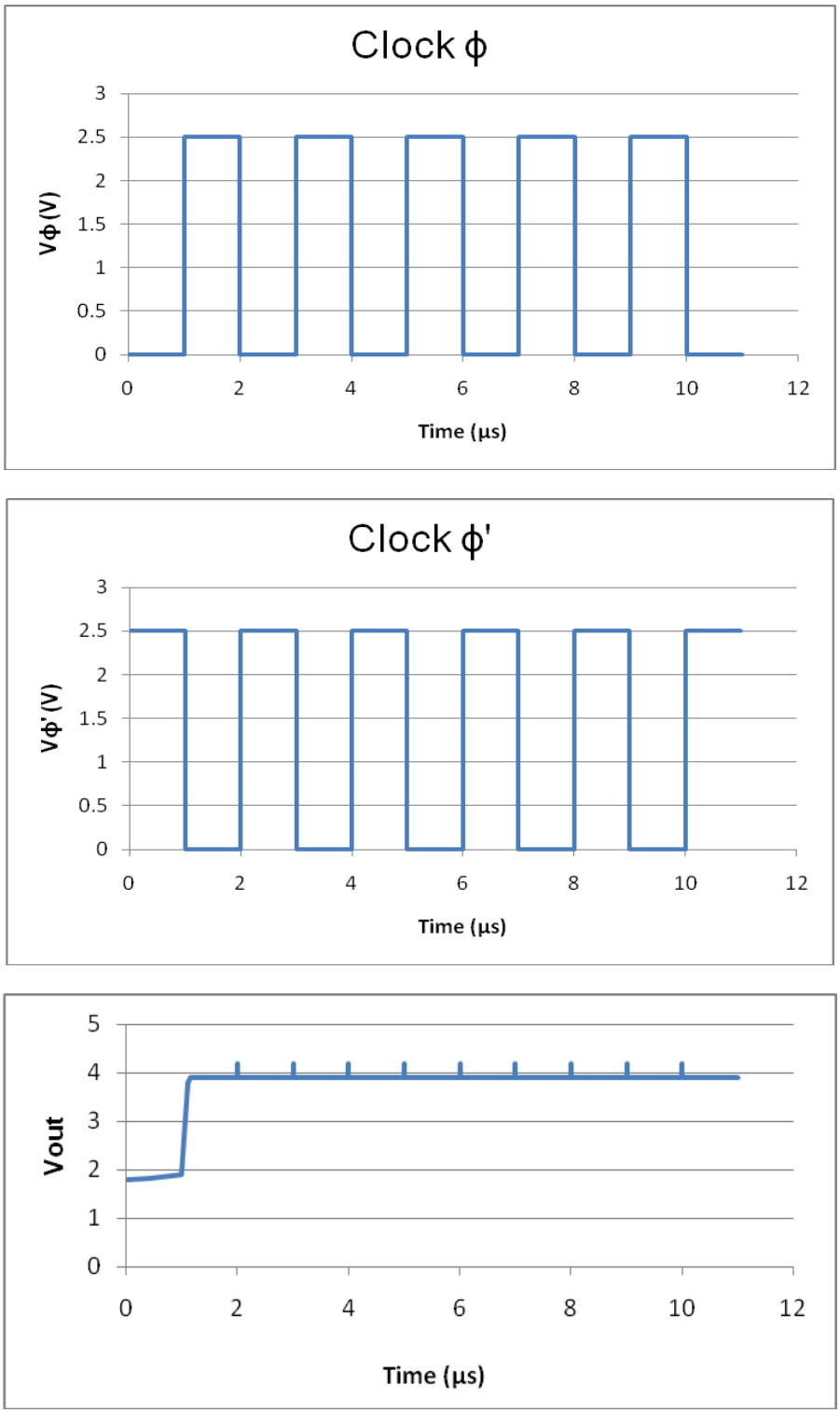


Figure 6.5 Voltage doubler output waveform

6.3 Dickson Charge Pump Circuit

The Dickson charge pump circuit is designed and simulated for output voltage of 15 V with N=6 stages. Figure 6.6 shows the schematic used for simulation of the Dickson charge pump circuit. Figure 6.7 shows the output voltage of the Dickson charge pump circuit with respect to time.

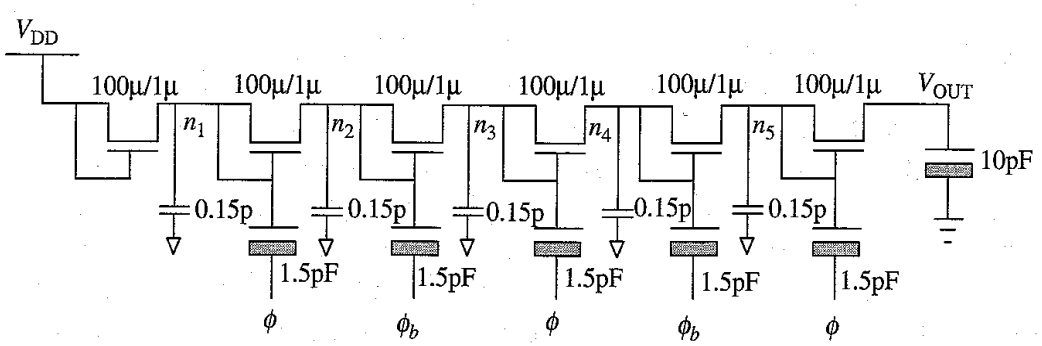


Figure 6.6 Schematic of Dickson Charge Pump Circuit with N=6

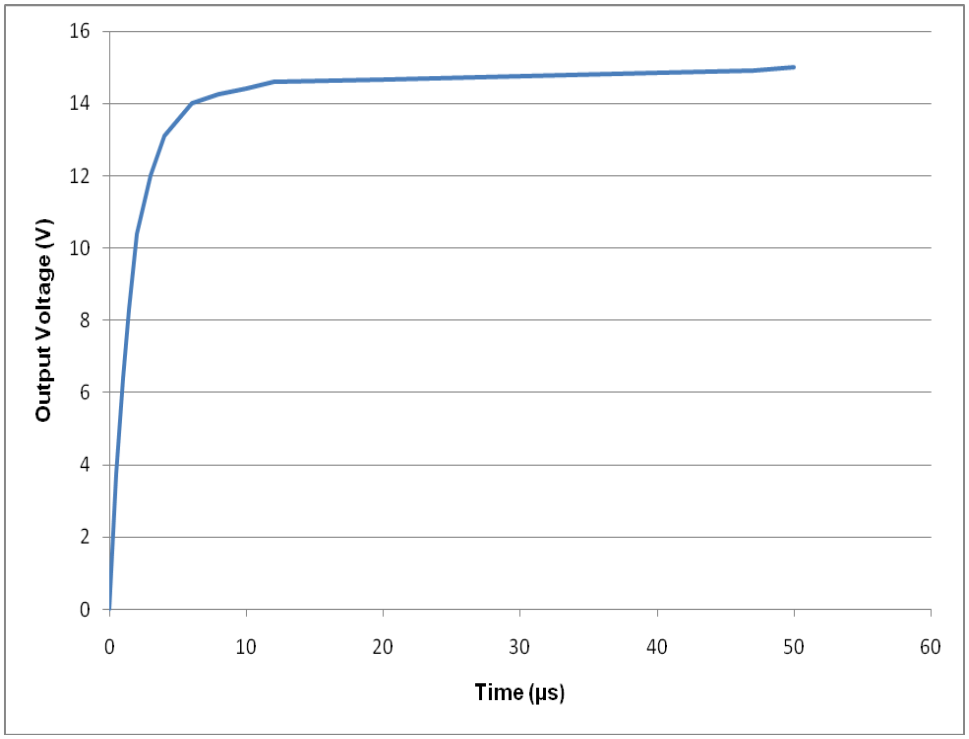


Figure 6.7 Output voltage of Dickson charge pump with N=6 stages

CHAPTER 7

CONCLUSION

The charge pump circuit is designed for 0.25 µm TSMC technology with the supply voltage of 5 V and the output voltage of 15 V. The Dickson charge pump with N=6 stages is designed to meet the specification. The difficulty is realized in designing the charge pump circuit for the sub-micron technology due to the low threshold voltage of the MOSFET. The charge stored in boost capacitors leaks away easily so proper measures need to be taken to avoid leakage. Also, the N-channel MOSFETs used as switches in the charge pump circuits are not ideal switches and have some value of resistance in the closed condition. Architectures with robust design and low supply voltages are discussed in this thesis to solve the problems of the charge pump circuit in sub-micron technology.

The design of a charge pump circuit is simulated using Cadence software. The schematic of the charge pump circuit is created in the capture tool of Cadence and waveform analysis is done in the Analog Design Environment (ADE) using SPECTRE. The charge pump circuit plays a very important role in memory chips and hence is used extensively in this technology era.

APPENDIX A

MOSFET TECHNOLOGY FILES

Tsmc_25N_Spectre

The MOSFET technology file for N-channel MOSFET contains important parameters such as threshold voltage, body effect coefficient, channel length modulation coefficient, nominal temperature, thickness of silicon dioxide and the values of parasitic capacitance at zero bias.

```
* LOT: n94s                WAF: 08
* Temperature_parameters=Default
.MODEL tsmc25N NMOS (                          LEVEL = 11
+VERSION = 3.1          TNOM    = 27           TOX     = 5.8E-9
+XJ      = 1E-7         NCH     = 2.3549E17    VTH0    = 0.4308936
+K1      = 0.3519429    K2      = 0.0298493    K3      = 1E-3
+K3B     = 0.0592323    W0      = 1E-5         NLX     = 1.465901E-7
+DVT0W   = 0            DVT1W   = 0            DVT2W   = 0
+DVT0    = 0.0183405    DVT1    = 4.897584E-3  DVT2    = -0.0252658
+U0      = 455.3033362  UA      = 5.223592E-10 UB      = 1.104713E-18
+UC      = 3.287888E-11 VSAT    = 1.050993E5   A0      = 1.2318623
+AGS     = 0.3043334    B0      = 6.67749E-8   B1      = 5E-6
+KETA    = 8.518046E-4  A1      = 0            A2      = 1
+RDSW    = 509.5675851  PRWG    = 0.0227558    PRWB    = -1E-3
+WR      = 1            WINT    = 2.126497E-9  LINT    = 4.393474E-9
+XL      = -3E-8        XW      = 0            DWG     = -3.409033E-9
+DWB     = 2.794842E-9  VOFF    = -0.1026054   NFACTOR = 0.1344887
+CIT     = 0            CDSC    = 1.527511E-3  CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.48737E-3   ETAB    = 4.557986E-4
+DSUB    = 3.045473E-3  PCLM    = 1.0446257    PDIBLC1 = 0.1441952
```

+PDIBLC2 = 4.513382E-4 PDIBLCB = -2.816756E-5 DROUT = 0.4698725

+PSCBE1 = 1.761109E10 PSCBE2 = 3.772916E-9 PVAG = 0.0361824

+DELTA = 0.01 MOBMOD = 1 PRT = 0

+UTE = -1.5 KT1 = -0.11 KT1L = 0

+KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18

+UC1 = -5.6E-11 AT = 3.3E4 WL = 0

+WLN = 1 WW = 0 WWN = 1

+WWL = 0 LL = 0 LLN = 1

+LW = 0 LWN = 1 LWL = 0

+CAPMOD = 2 XPART = 0.4 CGDO = 6.27E-10

+CGSO = 6.27E-10 CGBO = 0 CJ = 1.918655E-3

+PB = 0.9784049 MJ = 0.4721729 CJSW = 4.441595E-10

+PBSW = 0.9419636 MJSW = 0.2871118 PVTH0 = 1.342985E-3

+PRDSW = -61.8357222 PK2 = -3.140724E-3 WKETA = 7.512693E-4

+LKETA = -6.144062E-3)

Tsmc25P_Spectre

The MOSFET technology file for P-channel MOSFET contains important parameters such as threshold voltage, body effect coefficient, channel length modulation coefficient, nominal temperature, thickness of silicon dioxide and the values of parasitic capacitance at zero bias.

* LOT: n94s WAF: 08

* Temperature_parameters=Default

.MODEL tsmc25P PMOS (LEVEL = 11

+VERSION = 3.1 TNOM = 27 TOX = 5.8E-9

+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.6158735

+K1 = 0.4598379 K2 = 0.0399415 K3 = 0

+K3B = 8.7410723 W0 = 1E-6 NLX = 1E-9

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.6249485 DVT1 = 0.203296 DVT2 = -0.0513763

+U0 = 158.67524 UA = 2.200024E-10 UB = 4.457415E-18

+UC = 1.02138E-10 VSAT = 1.85064E5 A0 = 1.3826397

+AGS = 0.4192977 B0 = 2.844099E-6 B1 = 5E-6

+KETA = 0.0208695 A1 = 0 A2 = 1

+RDSW = 968.5463 PRWG = -0.1026483 PRWB = -0.325

+WR = 1 WINT = 2.748811E-8 LINT = 8.71907E-9

+XL = -3E-8 XW = 0 DWG = -4.087585E-8

+DWB = 2.032008E-8 VOFF = -0.15 NFACTOR = 1.5460516

+CIT = 0 CDSC = 1.413317E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.3241245 ETAB = -0.1842

+DSUB = 1.0287138 PCLM = 5.2654567 PDIBLC1 = 4.228338E-3

+PDIBLC2 = 1.204519E-3 PDIBLCB = 2.37525E-3 DROUT = 0

+PSCBE1 = 3.011456E10 PSCBE2 = 3.037042E-7 PVAG = 8.9564294

+DELTA = 0.01 MOBMOD = 1 PRT = 0

+UTE = -1.5 KT1 = -0.11 KT1L = 0

+KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18

+UC1 = -5.6E-11 AT = 3.3E4 WL = 0

+WLN = 1 WW = 0 WWN = 1

+WWL = 0 LL = 0 LLN = 1

+LW = 0 LWN = 1 LWL = 0

+CAPMOD = 2 XPART = 0.4 CGDO = 5.59E-10

+CGSO = 5.59E-10 CGBO = 0 CJ = 1.882857E-3

+PB = 0.9891317 MJ = 0.4679789 CJSW = 3.67186E-10

+PBSW = 0.9884654 MJSW = 0.3562128 PVTH0 = 3.923756E-3

+PRDSW = 15.3953053 PK2 = 2.061759E-3 WKETA = 4.10049E-3

+LKETA = -0.0232426 LVSAT = 1.257E5)

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BIOGRAPHICAL INFORMATION

Paras Shah was born in the state of Gujarat, India in December 1983. He received his Bachelor of Engineering in Electronics & Communication from Sarvajanik College of Engineering & Technology, South Gujarat University, Surat in 2006. He worked in Defense Research Development & Organization(DRDO) and Sardar Vallabhbhai National Institute of Technology(SVNIT) in India and for Advanced Micro Devices in Texas, USA. The author commenced his graduate studies in Electrical Engineering Department at the University of Texas at Arlington in Fall 2007 to achieve expertise in the field of Solid State Devices and Analog/Digital/Mixed-Signal/RF Circuit Design. During his graduate studies, he was a teaching assistant for graduate and undergraduate courses for Dr. Alan Davis, Dr. Ronald Carter, Dr. Kambiz Alavi and Dr. William Dillon. His interests include Analog/Digital/Mixed-Signal/RF Circuit Design, Digital & Wireless Communication and Embedded Systems.