AN ULTRA WIDE BAND CMOS LOW NOISE AMPLIFIER DESIGN

by

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ABSTRACT

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An RF ultra wide band low noise amplifier designed for the frequency range of 12-18 GHz of operation is presented in this paper. The low noise amplifier is designed using the state-of-the-art complementary metal oxide semiconductor 45 nm technology. Berkeley's Predictive Technology Model (PTM) is used to generate a fairly accurate mathematical model and the SPICE data is implemented into the BSIM 4 version of the Advanced Design Systems (ADS) program. The low noise design strategy is mainly based on the analysis of high frequency CMOS operation. This LNA has two stages: the first stage is a RL feedback amplifier with an inductive load, and the second stage is a RC feedback amplifier with an inductive load. High frequency small signal MOSFET models with shunt-shunt feedback are used to determine the input impedance, output impedance and gain equations governing this circuit.

Simulation results of this two stage feedback amplifier demonstrate a gain of 19 dB over a 6 GHz bandwidth, high linearity, and a low noise figure – less than 2.4 dB. This is a low voltage high current amplifier which requires a supply voltage of simply 0.5 V and has low power consumption (~13.5 mW).

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER 1

INTRODUCTION

CMOS ultra wide band systems have gained importance and great research interests in recent years. With many System on Chip (SOC) designs developing rapidly in RF broadband applications, low noise amplifier (LNA) designs have become much more challenging, especially with miniaturized sub 100 nanometer gate length CMOS technologies. This is because at these gate lengths, it is extremely difficult to accurately predict the behavior, the physics behind the characteristics of operation of these infinitesimal MOSFETs. Yet, this is of high interest because of the low cost, smaller size and low noise capability. Also, small gate lengths are capable of easily driving ultra high frequency amplifiers in the GHz range, if designed accurately. MOSFETs with a gate length of 90 nm or less have been known to have a transition frequency up to 300 GHz or more [5].

Nevertheless, analog circuit design has always been a compromise between many design factors. Not only is it difficult to model the transistors, but the behavior of passive electronic components like resistors, inductors and capacitors built on monolithic integrated circuits suffer massive stability problems when operated at these extremely high frequencies. Monolithic transmission line designs come into picture as a solution, if not completely, to these problems.

The mathematical equations used in this work to determine the fundamental device physics quantities such as the surface potential and a few other device voltage/current relationships are used directly from the BSIM v4 Manual [1]. This is because BSIM 4 is known to have one of the most accurate mathematical predictions to the behavior of short channel CMOS transistors. This is evident from the depth of mathematics involved in the set of equations they have invented to define short channel MOSFETs, and the large number of parameters involved in these calculations that define a short channel MOSFET. Also, most of

their parameters directly relate to the SPICE file parameters from the Berkeley's Predictive Technology Model which is the main simulation model on which this 45 nm CMOS design is based upon. So, an attempt was made to predict the device characteristics based on those equations from BSIM to obtain fundamental quantities that define the 45 nm transistor, so that upon verification of accuracy of these equations from simulation results, it would make these equations valid to be later used in the actual circuit design. This procedure was required since none of the conventional equations that define a MOSFET could be used here because of all the dominant short channel effects that come into the picture.

The SPICE parameters used for the simulation model in this work; originally developed at Arizona State University, is available at http://ptm.asu.edu. This model is known as the predictive technology model (PTM). The specific model used in this work is a 45 nm PTM model for a metal gate, high-k process. The direct link to the specific parameter list is http://ptm.asu.edu/modelcard/45nm_MGK.pm. This file is also printed in Appendix B. The defining values of various SPICE parameters are thus available for mathematical calculations through this SPICE file. Each and every parameter used in the mathematical calculations is explained here for convenience. This information is available from reference [1] and the Agilent ADS website.

CHAPTER 2

MODELING OF FUNDAMENTAL PARAMETERS THAT DEFINE THE 45NM CMOS PROCESS

2.1 Surface Potential

The electrostatic potential at the dielectric-substrate interface of a MOSFET is defined as the surface potential. The inversion phenomenon in MOSFETs occurs when this potential becomes equal to twice the Fermi level. For a short channel MOSFET, the surface potential is given by [1],

$$\Phi_s = 0.4 + \frac{k_B T}{q} \ln\left(\frac{NDEP}{n_i}\right) + PHIN \tag{2.1}$$

where,

PHIN = 0 is the non uniform vertical doping effect on surface potential [Appendix B].

NDEP = 6.5 x10^{18} cm^{-3} is the channel doping concentration at the depletion edge for zero body bias [Appendix B].

k_B –Boltzmann's constant. At nominal room temperature of 300 K, KT/q = 25.85 mV, a well known constant. The charge of an electron is q.

n_i = 1.5 x10^{10} cm^{-3} is the intrinsic carrier concentration of silicon.

Substituting these values in equation (2.1) gives,

$$\Phi_s = 0.4 + 25.85 \times 10^{-3} \ln\left(\frac{6.5 \times e^{18}}{1.5 \times e^{10}}\right) + 0$$

Φ_s = 0.914 V.

2.2 Threshold Voltage

The complete threshold voltage V_{th} equation that accounts for all the short channel and doping effects is given by [1],

$$V_{th} = VTH0 + \left[\left(K_{1ox} \cdot \sqrt{\Phi_s - V_{bseff}} - K1 \cdot \sqrt{\Phi_s} \right) \sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox} V_{bseff} \right]$$
$$+ \left[K_{1ox} \left(\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + (K3 + K3B \cdot V_{bseff}) \frac{TOXE}{W_{eff}' + W0} (\Phi_s) \right]$$
$$- \left[0.5 \cdot \left[\frac{DVT0W}{\cosh\left(DVT1W \frac{L_{eff} W_{eff}'}{l_{tw}} \right) - 1} + \frac{DVT0}{\cosh\left(DVT1 \frac{L_{eff}}{l_t} \right) - 1} \right] (V_{bi} - \Phi_s) \right]$$
$$- \left[\frac{0.5}{\cosh\left(DSUB \frac{L_{eff}}{l_{t0}} \right) - 1} (ETA0 + ETAB \cdot V_{bseff}) \cdot V_{ds} \right] \qquad (2.21)$$

From Appendix B,

VTH0 = 0.3423 V, where VTH0 is the threshold voltage with substrate bias V_{SB} = 0.

K1 = 0.2 V^0.5 is the first order body bias coefficient.

K2 = K3 = K3B = 0

K2 is the second order body bias coefficient.

K3 is the narrow width coefficient.

In short channel devices, when the channel width is decreased to a small value, the depletion region below the fringing fields become comparable to the depletion region formed by the vertical field. The result is an increase in the threshold voltage. This is known as the narrow width effect.

K3B is the body effect coefficient of K3.

LPEB = 0 m is the equivalent length of pocket implant accounting for the body bias.

Non-uniform lateral doping or pocket implant means that the doping concentration near the source/drain regions is higher than that in the middle of the region, and the parameter LPEB models this characteristic, if present.

TOXE = 0.9 x10^{-9} m is the electrical gate equivalent oxide thickness.

TOXM = 0.9 x10^{-9} m is the oxide thickness at which parameters are extracted.

W0 = 2.5 x10^{-6} m is the narrow width effect parameter.

DVT0W, DVT1W = 0 are the first and second coefficients that define the narrow width effect on the threshold voltage for small channel lengths.

DVT0 =1, DVT1 = 2, are the first and second coefficients that model short channel effects on the threshold voltage.

ETA0 = 0.0055, models the drain induced barrier lowering (DIBL) effect, the DIBL co-efficient in the sub-threshold region.

DSUB = 0.078 is the exponent of the DIBL co-efficient ETA0, in the sub-threshold region.

ETAB = 0 V^{-1} is the body bias co-efficient for the sub-threshold DIBL effect.

DVTP0 = 1 x 10^{-10} is the first co-efficient of drain induced V_{th} shift due to long channel pocket devices.

Now,

$$K_{1ox} = K1 \cdot \frac{TOXE}{TOXM} = 0.2 \qquad \text{and} \qquad K_{2ox} = K2 \cdot \frac{TOXE}{TOXM} = 0$$

V_{bs} = 0 V substrate body bias since no body voltage is supplied to any transistor in the LNA.

The effective V_{bs} voltage is given by [1],

$$V_{bseff} = V_{bc} + 0.5 \cdot \left[(V_{bs} - V_{bc} - \delta_1) + \sqrt{((V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 \cdot V_{bc})} \right]$$

This relation has no effect because the substrate voltage itself is zero.

2.2.1. Built In Potential

The built in potential of a MOSFET is given by [1],

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{NDEP \cdot NSD}{n_i^2}\right) \tag{2.22}$$

NSD = 2.0×10^{-20} cm^{-3} is the source/drain doping concentration.

NDEP = 6.5×10^{-18} cm^{-3} is the channel doping concentration at the depletion edge for zero body bias.

$$V_{bi} = 25.85\,mV \times \ln\left(\frac{6.5 \times 10^{18} \cdot 2.0 \times 10^{20}}{\left(1.5 \times 10^{10}\ cm^{-3}\right)^2}\right)$$

V_{bi}= 1.1167 V.

2.2.2. Characteristic Length

The characteristic length l_t is modeled separately for each of the short channel effects and included in the final equation for the threshold voltage.

2.2.2.1 Change In l_t Due To Narrow Width Effect

The characteristic length due to the narrow width effect is given by [1],

$$l_{tw} = \sqrt{\frac{\varepsilon_{si} \cdot TOXE \cdot X_{dep}}{EPSROX}} \cdot \left(1 + DVT2W \cdot V_{bs}\right)$$

This parameter may be neglected because the term that corresponds to the narrow width effect in the equation for the threshold voltage (2.21), the DVT0W = 0 from Appendix B.

2.2.2.2 Change In l_t Due To Short Channel Effects (SCE)

The characteristic length modeled due to short channel effects is given by [1],

$$l_t = \sqrt{\frac{\varepsilon_{si} \cdot TOXE \cdot X_{dep}}{EPSROX}} \cdot \left(1 + DVT2 \cdot V_{bs}\right) \tag{2.23}$$

DVT2 = 0 is the body bias coefficient of the short channel effect on V_{th} [Appendix B].

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}\left(\Phi_s - V_{bs}\right)}{qNDEP}} \tag{2.24}$$

$$X_{dep} = \sqrt{\frac{2 \times 11.68 \times (0.914 - 0)}{1.6 \times 10^{-19} \times 6.5 \times e^{18}}}$$

The permittivity of silicon ε_{si} = 11.68 ε_0 = 103.47x10^{-14} F/cm

X_{dep} = 13.48 nm.

$$l_t = \sqrt{\frac{11.68 \cdot 0.9 \times 10^{-9}\ \text{m} \cdot 13.48\text{nm}}{3.9}} \cdot (1 + 0 \cdot 0)$$

l_t = 6.025 nm.

2.2.2.3 Change In l_t Due To Drain Induced Barrier Lowering Effect (DIBL)

The characteristic length due to the DIBL effect is given by [1],

$$l_{t0} = \sqrt{\frac{\varepsilon_{si} \cdot \text{TOXE} \cdot X_{dep0}}{\text{EPSROX}}} \tag{2.25}$$

where,

$$X_{dep0} = \sqrt{\frac{2\varepsilon_{si}\Phi_s}{qNDEP}} \tag{2.26}$$

Since the body voltage is zero in SCE modeling, these equations are now similar to (2.23) and (2.24). Therefore,

$X_{dep\,0}$ = 13.48 nm.

l_{t0} = 6.025 nm.

2.2.2.4 Effective Gate Length

The transistor effective gate length modeled to account for various effects is explained below [1]

$$L_{eff} = L_{drawn} + XL - 2dL \tag{2.27}$$

where,

XL = -20 e-9 m is the channel length offset due to the mask/etch effect.

$$dL = \text{LINT} + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN} W^{LWN}} \quad [1] \tag{2.28}$$

From Appendix B,

LINT = $2.7\text{x}10^{-9}$ m is the channel length offset parameter.

LL = 0 is the co-efficient of length dependence for length offset.

LW = 0 is the co-efficient of width dependence for length offset.

LWL = 0 is the co-efficient of length and width cross term dependence for length offset.

LLN = 1 is the power of length dependence for length offset.

LWN = 1 is the power of width dependence for length offset.

Therefore, dL = $2.7\text{x}10^{-9}$ +0 +0 = 0 = $2.7\text{x}10^{-9}$

L_{eff} = $45\text{x}10^{-9}$ – $20\text{x}10^{-9}$ –($2.7\text{x}10^{-9}$)2, L_{eff} = 19.6 nm.

Substituting all these values into equation (2.21),

$$V_{th} = \left[0.3423 + \left(0.2\cdot\sqrt{0.914-0} - 0.2\cdot\sqrt{0.914}\right)\sqrt{1+\frac{0}{19.6\text{n}}} - 0\right]$$

$$+\left[0.2\cdot\left(\sqrt{1+\frac{\text{LPEO}}{19.6\text{n}}}-1\right)\sqrt{0.914\text{V}} + (0+0)\frac{0.9\text{x}10^{-9}}{W_{eff}+2.6\times10^{-6}}\times 0.914\right]$$

$$-\left[0.5\cdot\left[\frac{0}{\cosh\left(0\times\frac{19.6\text{n}\times W_{eff}}{l_{tw}}\right)-1}+\frac{1}{\cosh\left(2\times\frac{19.6\text{n}}{l_t}\right)-1}\right](1.1167-0.914)\right]$$

$$-\left[\frac{0.5}{\cosh\left(0.078\times\frac{19.6\text{n}}{6.025\text{n}}\right)-1}(0.0055+0)\times 0.6\right]$$

V_{th} = 0.28 V at V_{DS} = 0.6 V (2.28a)

2.3 The Drain Current

The drain current equation for the 45 nm CMOS in the linear/saturation region is given by [1],

$$I_{ds} = \frac{I_{ds0}\cdot NF}{1+\frac{R_{ds}I_{ds0}}{V_{dseff}}}\left[1+\frac{1}{C_{clm}}\ln\left(\frac{V_A}{V_{Asat}}\right)\right]\cdot\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADIBL}}\right)\cdot\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADITS}}\right)\cdot\left(1+\frac{V_{ds}-V_{dseff}}{V_{ASCBE}}\right)\cdot$$

(2.29)

where, R_{ds} is the bias dependent source/drain resistance model. To invoke the internal model, rdsmod = 0, which assumes that the drain and the source regions are symmetrical in terms of their doping profiles [Appendix B]. R_{ds} (V) is defined as [1],

$$R_{ds}(V) = \frac{\left\{RDSWMIN + RDSW \cdot \left[PRWB \cdot \left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right) + \frac{1}{1 + PRWG \cdot V_{gsteff}}\right]\right\}}{\left(1 \times 10^6 \cdot W_{effcj}\right)^{WR}} \quad (2.30)$$

From Appendix B,

RDSW = 105 Ω $(\mu m)^{WR}$ is the zero bias LDD (lightly doped drain) resistance per unit width for rdsmod = 0.

WR = 1 is the channel width dependence parameter of LDD resistance.

RDSWMIN = 0 is the lightly doped source resistance per unit width.

PRWB = 0 is the body bias dependence of LDD resistance.

W_{effcj} is the effective drain/source diffusion width given by [1],

$$W_{effcj} = \frac{W_{drawn}}{NF} - 2 \cdot \left(DWJ + \frac{WLC}{L^{WLN}} + \frac{WWC}{W^{WWN}} + \frac{WWLC}{L^{WLN} W^{WWN}}\right) \quad (2.30a)$$

From Appendix B,

DWJ = 0 is the offset of the source/drain junction width.

WLC = WL =0

WLC is the coefficient of length dependence for the CV (calculated coefficients of variation) channel width offset; WL is the coefficient of length dependence for width offset.

WWC = WW = 0

WWC is the coefficient of width dependence for CV channel width offset; WW is the coefficient of width dependence for width offset.

WWLC = WWL =0

WWLC is the coefficient of length and width cross term dependence for CV channel width offset; WWL is the of length and width cross term dependence for width offset.

NF = 10 is the number of fingers.

W_{drawn} = 2250 nm is the drawn channel width.

Substituting above values in the equation (2.30a),

$$W_{effcj} = \frac{2250n}{10} - 2\cdot\left(0 + \frac{0}{L^{WLN}} + \frac{0}{W^{WWN}} + \frac{0}{L^{WLN}W^{WWN}}\right)$$

W_{effcj} = 225 nm.

Substituting the above values into equation (2.30) gives,

$$R_{ds}(V) = \frac{\left\{0 + 105\cdot\left[0\cdot\left(\sqrt{0.914 - 0} - \sqrt{0.914}\right) + \frac{1}{1 + 0\cdot V_{gsteff}}\right]\right\}}{\left(1\times 10^{6}\cdot 225\times 10^{-9}\right)^{1}}$$

$R_{ds}(V)$ = 0.4666 mΩ.

2.3.1 Unified Mobility Model

The mathematical relation for the effective mobility of electrons that incorporates the short channel effects is given by [1],

$$\mu_{eff} = \frac{U0}{1 + \left(UA + UCV_{bseff}\right)\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^{2}} \qquad (2.31)$$

From Appendix B,

mobmod = 0.

U0 = 0.02947 m^2/V-s, is the low field mobility.

UA = -5x10^{-10} m/V, is the coefficient of the first order mobility degradation due to the vertical field.

UB = 1.7x10^{-18} m^2/V^2, is the coefficient of the second order mobility degradation due to the vertical field.

UC = 0, is the coefficient of mobility degradation due to body bias effect.

V_{gse} is the effective gate voltage. V_{gsteff} is the effective value of (V_{gse}-V_{th}) given by [1],

$$V_{gsteff} = \frac{nv_t \ln\left\{1+\exp\left[\frac{m^*\left(V_{gse}-V_{th}\right)}{nv_t}\right]\right\}}{m^*+nC_{oxe}\cdot\sqrt{\frac{2\Phi_s}{qNDEP\varepsilon_{si}}}\exp\left[-\frac{(1-m^*)\left(V_{gse}-V_{th}\right)-Voff'}{nv_t}\right]} \quad (2.32)$$

V_{gse} is given by [1],

$$V_{gse} = VFB+\Phi_s+\frac{q\varepsilon_{si}NGATE\cdot TOXE^2}{EPSROX^2}\left(\sqrt{1+\frac{2EPSROX^2\left(V_{gs}-VFB-\Phi_s\right)}{q\varepsilon_{si}NGATE\cdot TOXE^2}}-1\right) \quad (2.32a)$$

VFB = -1.058 V is the flat band voltage.

NGATE = 1 x10^{23} cm^{-3} is the poly silicon gate doping concentration.

Assuming Vgs = 0.5 V, and substituting above values into equation (2.32a),

$$V_{gse} = -1.058+0.914+\frac{1.6\times10^{-16}\times11.68\times e^{23}\cdot\left(0.9\times e^{-9}\right)^2}{3.9^2}\left(\sqrt{1+\frac{2\times3.9^2(0.5+1.058-0.914)}{1.6\times10^{-16}\times11.68\times e^{23}\cdot\left(0.9\times e^{-9}\right)^2}}-1\right)$$

V_{gse} = 0.499 V.

Voff is given by [1],

$$Voff' = VOFF+\frac{VOFFL}{L_{eff}} \quad (2.32b)$$

VOFF = -0.13 V is the offset voltage in sub-threshold region for large W and L.

VOFFL = 0 V is the channel-length dependence of VOFF.

Substituting above values in equation (2.32b),

$$Voff' = -0.13+\frac{0}{L_{eff}} = -0.13 \text{ V}.$$

m* is given by [1],

$$m^* = 0.5+\frac{\arctan(MINV)}{\pi}$$

MINV = 0.05 is the V_{gsteff} fitting parameter for moderate inversion condition.

Substituting for MINV in the above equation,

$$m^* = 0.5 + \frac{\arctan(0.05)}{\pi}$$

$m^* = 0.515$

$C_{oxe} = \frac{EPSROX \cdot \varepsilon_0}{TOXE}$, C_{oxe} is the effective gate oxide capacitance [1].

EPSROX = 3.9 is the gate dielectric constant relative to vacuum for silicon dioxide [Appendix B].

Substituting this value in the above equation,

$$C_{oxe} = \frac{3.9 \times 103.414 \cdot 10^{-14}}{0.9 \times 10^{-9}}$$

$C_{oxe} = 38.36 \times 10^{-15}$ F/μm^2

n is the sub threshold swing parameter given by [1],

$$n = 1 + NFACTOR \cdot \frac{C_{dep}}{C_{oxe}} + \frac{Cdsc\_Term + CIT}{C_{oxe}} \qquad (2.33)$$

where,

$$Cdsc\_Term = (CDSC + CDSCD \cdot V_{ds} + CDSCB \cdot V_{bseff}) \cdot \frac{0.5}{\cosh\left(DVT1 \frac{L_{eff}}{l_t}\right) - 1} \qquad [1]$$

This term represents the coupling capacitance between drain/source to channel.

From Appendix B,

CDSC = 0 is the coupling capacitance between source/drain and channel.

CDSCD = 0 is the body bias sensitivity of CDSC.

CDSCB = 0 is the drain bias sensitivity of CDSC.

Hence the term, $Cdsc\_Term = 0$.

CIT = 0 is the interface trap capacitance.

NFACTOR = 1.9

From [Appendix B of [1],

$K1 = \gamma_2 - 2K2\sqrt{\Phi_s - VBM}$

$\therefore \gamma_2 = K1$

$\gamma_2 = 0.2\ V^{0.5}$.

$$\gamma_2 = \frac{\sqrt{2q\varepsilon_{si}NSUB}}{C_{oxe}}$$

$$NSUB = \frac{(\gamma_2 C_{oxe})^2}{2q\varepsilon_{si}}$$

$$NSUB = \frac{\left(0.2 \times 38.36 \times 10^{-15}\right)^2}{2 \times 1.6 \times 10^{-19} \times 11.68}$$

NSUB = 1.77 x 10^{18} cm^{-3}.

$$C_{dep} = \frac{\varepsilon_{si}}{W_{dep}}$$

$$W_{dep} = \sqrt{\left(\frac{2\varepsilon_{si}}{qNSUB}\right)}$$

$$W_{dep} = \sqrt{\left(\frac{2 \times 11.68}{1.6 \times 10^{-19} \times 1.77 \times 10^{18}}\right)}$$

$$W_{dep} = 25.83nm$$

$$C_{dep} = \frac{11.68}{25.83n}$$

C_{dep} = 4 $fF/\mu m^2$

Substituting these values in (2.33),

$$n = 1 + 1.9 \cdot \frac{4 \times 10^{-15}}{38.36 \times 10^{-15}} + \frac{0 + 0}{38.36 \times 10^{-15}}$$

n = 1.198.

Replacing terms for their values in equation (2.32),

$$V_{gsteff} = \frac{1.198 \times 25.85m \times \ln\left\{1 + \exp\left[\frac{0.515(0.499 - 0.2922)}{1.198 \times 25.85m}\right]\right\}}{0.515 + 1.198 \times 38.36 \times 10^{-15} \cdot \sqrt{\frac{2 \times 0.914}{1.6 \times 10^{-19} \times 6.5 \times 10^{18} \times 11.68}} \exp\left[-\frac{(1 - 0.515)(0.499 - 0.2922) - (-0.13)}{1.198 \times 25.85m}\right]}$$

V_{gsteff} = 0.2577 V.

Substituting for V_{gsteff} and other terms in equation (2.31)

$$\mu_{eff} = \frac{0.02947}{1+\left(-5\times10^{-10}+0\cdot V_{bseff}\right)\left(\frac{0.2577+2\times0.2922}{0.9\times10^{-9}}\right)+1.7\times10^{-18}\left(\frac{0.2577+2\times0.2922}{0.9\times10^{-9}}\right)^2}$$

Effective mobility μ_{eff} = 0.0149 m^2/V-s.

Now E_{sat} is defined as the electric field at which carrier velocity becomes saturated. This is given by [1],

$$E_{sat} = \frac{2VSAT}{\mu_{eff}}$$

where, VSAT = 159550 m/s is the saturation velocity. Substituting these into above equation,

$$E_{sat} = \frac{2\times159550}{0.0149}$$

E_{sat} = 21416107.38 V/m.

2.3.2 Determination of $I_{ds\,0}$

I_{ds0} is the drain current excluding some of the short channel effects expressed in equation (2.29). This is given by [1],

$$I_{ds\,0} = \frac{W\mu_{eff}Q_{ch\,0}V_{ds}\left(1-\frac{V_{ds}}{2V_b}\right)}{L\left(1+\frac{V_{ds}}{E_{sat}L}\right)} \qquad (2.34)$$

where,

W = W_{eff} given by [1],

$$W_{eff} = \frac{W_{drawn}}{NF} + XW - 2\,dW$$

From Appendix B,

XW =0 is the channel width offset due to the mask/etch effect.

DWG = 0 is the coefficient of gate bias dependence of W_{eff}.

DWB = 0 is the coefficient of body bias dependence of W_{eff}.

WINT = 5 nm.

WW = WL = WWL = 0 are the coefficients of width/length and their cross dependencies on width offset.

Substituting above values, W_{eff} = 215 nm.

L = L_{eff} as defined earlier.

$$Q_{ch0} = C_{oxeff} \cdot V_{gsteff} \quad [1]$$

Q_{ch0} = 9.8853 x10^{-3} F/m^2.

$$V_b = \frac{V_{gsteff} + 2v_t}{A_{bulk}} \quad [1] \qquad (2.35)$$

where

$$A_{bulk} = \left\{1 + F\_doping \cdot \left[\frac{A0 \cdot L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}} \cdot \left(1 - AGS \cdot V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}}\right)^2\right) + \frac{B0}{W_{eff}' + B1}\right]\right\} \frac{1}{1 + KETA \cdot V_{bseff}}$$

[1]

$$F - doping = \frac{\sqrt{1 + \frac{LPEB}{L_{eff}}}K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} + K_{2ox} - K3B\frac{TOXE}{W_{eff}' + W0}(\Phi_s) \quad [1]$$

From Appendix B,

LPEB = 0 is the lateral non uniform doping effect on K1.

Substituting for LPEB and rest of the previously defined values in this equation,

$$F\_doping = \frac{\sqrt{1 + \frac{0}{19.6\,n}} \cdot 0.2}{2\sqrt{0.914 - 0}} + 0 - 0 \cdot \frac{0.9 \times 10^{-19}}{W_{eff}' + W0} \times 0.914$$

F_doping = 0.5229.

From Appendix B,

AGS = 0 is the coefficient of V_{gs} dependence of bulk charge effect.

A0 = 1 is the coefficient of channel length dependence of bulk charge effect.

B0 = 0 is the bulk charge effect coefficient for channel width.

XJ = 14 nm is the source/drain junction depth.

Substituting all values for A_{bulk},

$$A_{bulk} = \left\{1 + 0.5229 \cdot \left[\frac{1 \cdot 19.6n}{19.6n + 2\sqrt{14n \cdot 13.48\,n}} \cdot \left(1 - 0 \cdot V_{gsteff}\left(\frac{19.6n}{19.6n + 2\sqrt{14n \cdot 13.48\,n}}\right)^2\right) + \frac{0}{W_{eff}' + B1}\right]\right\} \frac{1}{1 + KETA \cdot 0}$$

A_{bulk} = 1.2177.

Now, substituting this in the equation (2.35),

$$V_b = \frac{0.2577 + 2 \times 25.85m}{1.2177}$$

V_b = 0.2540 V.

Substituting all these values in equation (2.34),

$$I_{ds0} = \frac{215n \times 0.0149 \times 9.8853 \times 10^{-3} \times 0.6\left(1 - \frac{0.6}{2 \times 0.2540}\right)}{19.6n\left(1 + \frac{0.6}{21416107.38 \times 45n}\right)}$$

I_{ds0} = -108.198 uA. (2.35a)

The saturation Voltage V_{dsat} is given by [1],

$$V_{dsat} = \frac{E_{sat}L\left(V_{gsteff} + 2v_t\right)}{A_{bulk}E_{sat}L + V_{gsteff} + 2v_t}$$

here, L = L_{drawn} = 45 nm. Substituting for other known terms,

$$V_{dsat} = \frac{21416107.38 \times 45 \times 10^{-9}\left(0.2577 + 2 \times 25.85 \times 10^{-3}\right)}{1.2177 \times 21416107.38 \times 45 \times 10^{-9} + 0.2577 + 2 \times 25.85 \times 10^{-3}}$$

V_{dsat} = 0.201 V.

Now, the effective V_{dsat} is given by [1],

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left[\left(V_{dsat} - V_{ds} - \delta\right) + \sqrt{\left(V_{dsat} - V_{ds} - \delta\right)^2 + 4\delta \cdot V_{dsat}}\right]$$

$$V_{dseff} = 0.201 - \frac{1}{2}\left[(0.201 - 0.6 - 0.01) + \sqrt{(0.201 - 0.6 - 0.01)^2 + 4 \times 0.01 \times 0.201} \right]$$

V_{ds} = 0.6 V, and δ = 0.01 V is a model parameter.

V_{dseff} = 0.1961 V.

The effect of channel length modulation on drain current is modeled in the relation [1],

$$C_{clm} = \frac{1}{PCLM} \cdot F \cdot \left(1 + PVAG \frac{V_{gsteff}}{E_{sat} L_{eff}} \right) \left(1 + \frac{R_{ds} \cdot I_{dso}}{V_{dseff}} \right) \left(L_{eff} + \frac{V_{dsat}}{E_{sat}} \right) \cdot \frac{1}{litl} \qquad (2.36)$$

where,

$$litl = \sqrt{\frac{\varepsilon_{si} TOXE \cdot XJ}{EPSROX}} \quad [1]$$

$$litl = \sqrt{\frac{11.68 \times 0.9 \times 10^{-9} \cdot XJ}{3.9}} = 6.1429 \text{ nm}$$

$$F = \frac{1}{1 + FPROUT \cdot \frac{\sqrt{L_{eff}}}{V_{gsteff} + 2v_t}} \qquad [1]$$

FPROUT = 0.2 V/(m)$^{0.5}$ is the effect of pocket implant on ROUT degradation [Appendix B].

Substituting this value in the above equation,

$$F = \frac{1}{1 + 0.2 \times \frac{\sqrt{19.6n}}{0.2577 + 2 \times 25.85m}}$$

F = 1.

From Appendix B,

PCLM = 0.06 is a channel length modulation parameter.

PVAG = 1 x10^{-20} is the gate bias dependence of early voltage.

Substituting all these values in equation (2.36),

$$C_{clm} = \frac{1}{0.06} \cdot 1 \cdot \left(1 + 10^{-20} \cdot \frac{0.2577}{21416107.38 \times 19.6n} \right) \left(1 + \frac{0.4666m \times -108.198u}{0.9161} \right) \left(19.6n + \frac{0.201}{21416107.38} \right) \cdot \frac{1}{6.1429n}$$

C_{clm} = 78.639.

Now from [1],

$V_{ACLM} = C_{clm} \cdot (V_{ds} - V_{dsat})$ is the equation for early voltage when only the CLM is the physical phenomenon taken into account.

$V_{ACLM} = 78.639 \cdot (0.6 - 0.201)$, V_{ACLM} = 31.376 V.

V_{Asat} is the early voltage at $V_{ds} = V_{dsat}$ given by [1],

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{ds}vsatC_{oxe}W_{eff}V_{gsteff} \cdot \left[1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff} + 2v_t)}\right]}{R_{ds}vsatC_{oxe}w_{eff}A_{bulk} - 1 + \frac{2}{\lambda}}$$

λ = 1 is the non saturation effects modeling parameter for a pMOS transistor.

Substituting for all parameters in the above equation,

$$V_{Asat} = \frac{21416107.38 \times 19.6n + 0.201 + 2 \cdot 0.4666m \cdot 159550 \cdot 38.36 \cdot 10^{-15} \cdot 215n \cdot 0.2577 \cdot \left[1 - \frac{1.2177 \cdot 0.201}{2(0.2577 + 2 \cdot 25.85m)}\right]}{0.4666m \times 159550 \times 38.36 \times 10^{-15} \times 215n \times 1.2177 - 1 + \frac{2}{1}}$$

V_{Asat} = 0.6207 V.

In equation (2.29) V_A is given by [1],

$V_A = V_{Asat} + V_{ACLM}$ = 31.9961 V.

Now V_{ADITS} is the early voltage due to the drain induced threshold shift (DITS) effects given by [1],

$$V_{ADITS} = \frac{1}{PDITS} \cdot F \cdot [1 + (1 + PDITSL \cdot L_{eff})\exp(PDITSD \cdot V_{ds})]$$

From Appendix B,

PDITS = 0.1 V^{-1} is the impact of drain-induced V_{th} shift on ROUT.

PDITSL = 2300000 m^{-1} is the channel length dependence of drain-induced V_{th} shift for ROUT.

PDITSD = 0.23 V^{-1} is the V_{ds} dependence of drain-induced V_{th} shift for ROUT.

Substituting these values in the above equation,

$$V_{ADITS} = \frac{1}{0.1} \cdot 1 \cdot \left[1 + \left(1 + 2300000 \cdot 19.6n\right) \exp\left(0.23 \times 0.6\right)\right]$$

V_{ADITS} = 21.99 V.

V_{ASBE} is the early voltage due to the substrate current effect given by [1],

$$\frac{1}{V_{ASCBE}} = \frac{PSCBE2}{L_{eff}} \exp\left(-\frac{PSCBE1 \cdot litl}{V_{ds} - V_{dsat}}\right)$$

From Appendix B,

PSCBE1 = 2 x10^{9} V/m is the first substrate current induced body effect parameter.

PSCBE2 = 1 x 10^{-7} m/V is the second substrate current induced body effect parameter.

Substituting these values in the above equation,

$$\frac{1}{V_{ASCBE}} = \frac{2 \times 10^{9}}{19.6n} \exp\left(-\frac{1 \cdot 10^{-7} \cdot 6.1429\,n}{0.6 - 0.201}\right)$$

V_{ASCBE} = 9.8 V.

V_{ADIBL} is the early voltage due to DIBL effects given by [1],

$$V_{ADIBL} = \frac{V_{gsteff} + 2v_t}{\theta_{rout}\left(1 + PDIBLCB \cdot V_{bseff}\right)}\left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t}\right) \cdot \left(1 + PVAG \frac{V_{gsteff}}{E_{sat} L_{eff}}\right) \qquad (2.37)$$

where, $$\theta_{rout} = \frac{PDIBLC1}{2\cosh\left(\frac{DROUT \cdot L_{eff}}{lt_0}\right) - 2} + PDIBLC2$$

From Appendix B,

DROUT = 0.5 is the channel length dependence of DIBL effect on ROUT.

PDIBLC1 = PDIBLC2 = 0.001 are the parameters for DIBL effects on ROUT.

PDIBLCB = -0.005 V^{-1} is the body bias coefficient of DIBL effect on ROUT.

Substituting these values in the above equation,

$$\theta_{rout} = \frac{0.001}{2\cosh\left(\frac{0.5 \times 19.6n}{6.025\,n}\right) - 2} + 0.001 = 0.001346$$

PVAG = 10^{-20} is the gate-bias dependence of early voltage [Appendix B].

Substituting the above values into equation (2.36) gives,

$$V_{ADIBL} = \frac{0.2577 + 2 \times 25.85m}{0.001346\left(1 - 0.005 \times 0\right)}\left(1 - \frac{1.2177 \times 0.201}{1.2177 \times 0.201 + 0.2577 + 2 \times 25.85m}\right) \cdot \left(1 + 10^{-20}\frac{0.2577}{21416107.3 \times 19.6n}\right)$$

V_{ADIBL} = 132.582 V

Finally, substituting all of the above deduced parameter values into the main drain current equation (2.29),

The drain current at V_{ds} = 0.6 V and V_{gs} = 0.5 V is

$$I_{ds} = \frac{-108.198u \times 10}{1 + \frac{0.4666m \times -108.198u}{0.1961}}\left[1 + \frac{1}{78.639}\ln\left(\frac{31.9961}{0.6207}\right)\right] \cdot \left(1 + \frac{0.6 - 0.1961}{132.582}\right) \cdot \left(1 + \frac{0.6 - 0.1961}{21.99}\right) \cdot \left(1 + \frac{0.6 - 0.1961}{9.8}\right) \cdot \quad (2.38)$$

I_{ds} = 1.224 mA.

and the current to channel width ratio I_{ds}/W_{drawn} = 0.54 mA/um.

CHAPTER 3

VERIFICATION OF THE MODEL

To test the accuracy of the model equations used in chapter 2 that define 45 nm CMOS transistors, the SPICE model file is uploaded to BSIM 4 version of the ADS (Advanced Design Systems), and simulation results are observed to verify the theory. Following sections show the simulation results and provide a comparison.

3.1 The Threshold Voltage

Simulation results for the threshold voltage with V_{ds} = 0.6 V and V_{gs} = 0.5 V is shown below. These test conditions are similar to the ones used in the mathematical model.

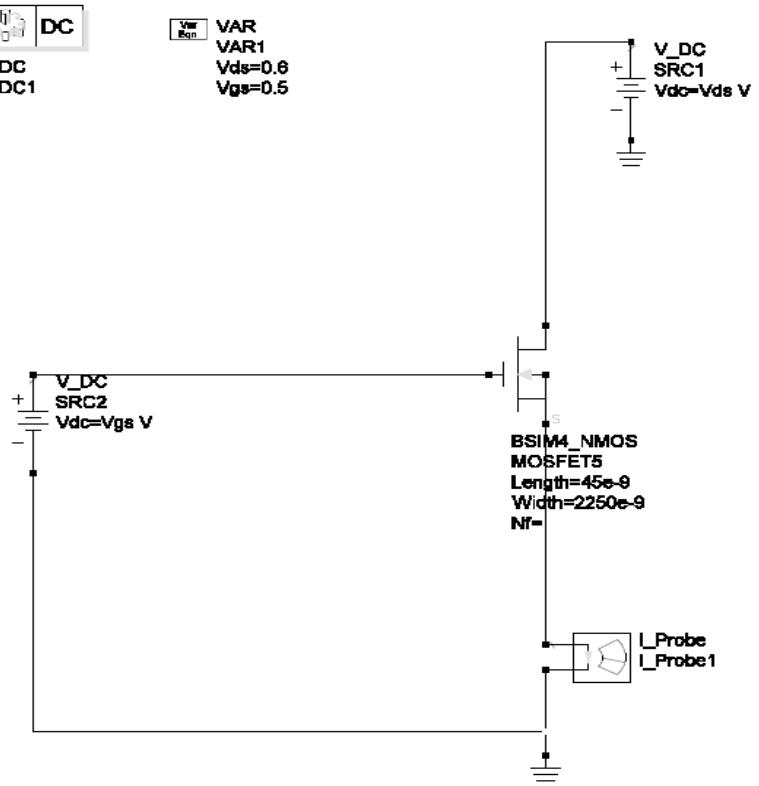


Figure 3.1 Circuit model set up in ADS with V_{ds} = 0.6 V and V_{gs} = 0.5 V

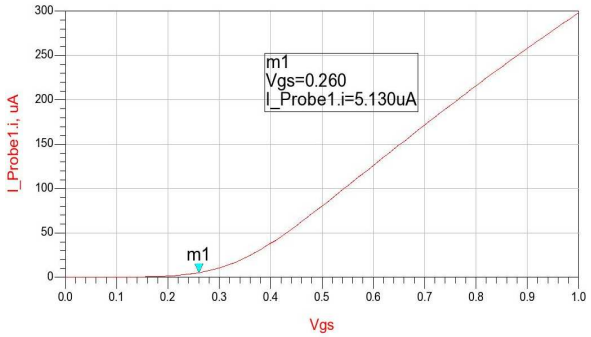


Figure 3.2 Threshold voltage is around 0.26 V as seen from the graph.

From equation (2.28a), the calculated value of the threshold voltage V_{th} = 0.28 V, which is consistent with the simulation data.

3.2 The Drain Current

Simulation results for the drain current with V_{ds} = 0.6 V and V_{gs} = 0.5 V is shown below.

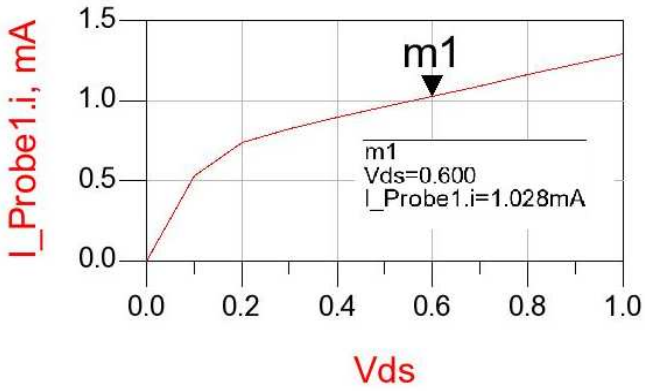


Figure 3.3 Drain Current Simulation result, I_D = 1.02 mA

From equation (2.38), the calculated value of the drain current is I_D = 1.22 mA, which is consistent with the simulation (Figure 3.2). These results show that this mathematical model is sufficiently accurate to be used in the LNA circuit design.

CHAPTER 4

LOW NOISE CMOS DESIGN CONSIDERATIONS

For MOSFETs in the saturation regime, the dominant noise sources are thermal noise and flicker noise. However, flicker noise becomes negligible when MOSFETs are operated in the GHz frequency range. This is explained in detail in section 4.2. The following sections define the factors that affect the noise performance of a short channel MOSFET.

4.1 Thermal Noise

Thermal noise in electronic circuits exists because of the resistive nature of the devices. In MOSFETs, the channel resistance is the main cause of the thermal noise. Fortunately, the short channel transistors have a very low drain to source output resistance (less than 1kΩ). This is one of the reasons short channel CMOS technologies tend to have the lowest noise figures [2] which is explained by the following equation,

$$F_{min} \approx 1 + \frac{\omega}{\omega_T}\sqrt{\gamma\delta\zeta\left(1-|C|^2\right)} \tag{4.1}$$

ω_T is the transition frequency, γ and δ are bias dependent factors. As seen, the minimum noise is inversely proportional to ω_T, which in turn is inversely related to L_{eff}. Hence, short channel CMOS transistors have the lowest noise figures.

Thermal noise in a MOSFET consists of drain current noise and induced gate current noise as defined by [3].

4.1.1 Drain Current Noise

The drain current noise is defined as [3]

$$\overline{i_d^2} = 4kT\Delta f\gamma g_{d0}$$

where g_{do} is the drain output conductance under zero drain bias. The parameter γ is a bias dependent factor.

4.1.2 Induced Gate Current Noise

The induced gate current noise is defined as [3]

$$\overline{i_g^2} = 4kT\Delta f\delta g_g \text{ , where } g_g = \zeta\frac{\omega^2 C_{gs}^2}{g_{d0}} \tag{4.2}$$

Hence, induced gate current noise is proportional to the square of ωC and dominates MOSFET noise at high frequencies. The parameters δ, ζ are bias dependent factors. This noise appears due to local fluctuations created by capacitive coupling through the gate oxide layer [2].

4.2 Flicker Noise

Flicker noise in MOSFETs is given by the relation [8],

$$\overline{i_n^2} = K\frac{I^a}{f^b}\Delta f$$

where K is a device specific constant, a and b are constants. Flicker noise is inversely proportional to the frequency of operation which makes its contribution significant only at low frequencies.

4.3 Noise Reduction in Parallel MOSFETs

When a number of transistors are connected in parallel as shown in Figure 4.1, the circuit tends to reduce the overall voltage noise of the amplifier.

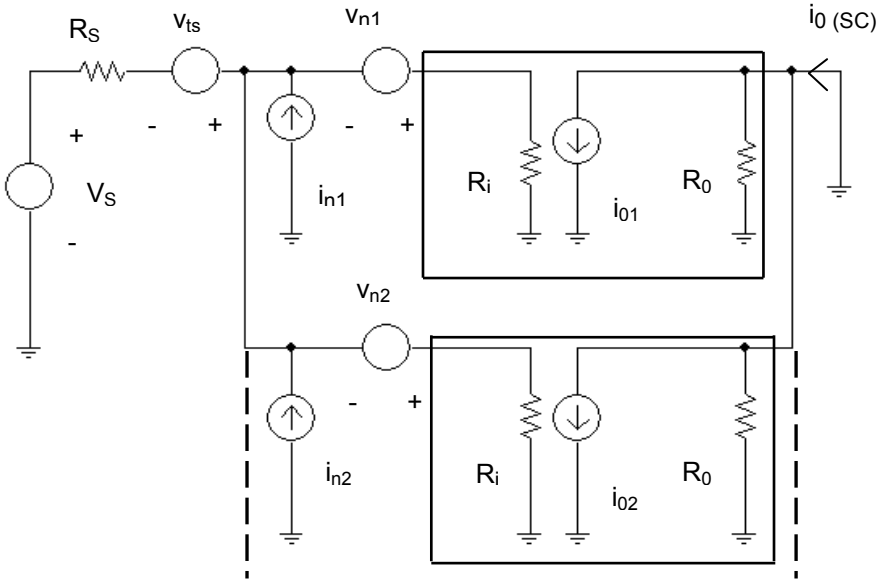


Figure 4.1 Small signal equivalent of two transistors connected in parallel

The instantaneous short circuit output current and the input referred noise voltage for such a parallel combination of 2 circuits is given by [6]

$$i_{o(sc)} = g_m \left[\begin{array}{l} N\dfrac{\dfrac{R_i}{N}}{R_S + \dfrac{R_i}{N}}(v_s + v_{ts}) + N\left(R_S \| \dfrac{R_i}{N}\right)\sum_{j=1}^{N} i_{nj} \\ + \sum_{j=1}^{N}\left(\dfrac{R_i}{R_i + R_S \| \left(\dfrac{R_i}{N-1}\right)} v_{nj} - \dfrac{R_S \| \left(\dfrac{R_i}{N-1}\right)}{R_i + R_S \| \left(\dfrac{R_i}{N-1}\right)} \sum_{\substack{k=1 \\ k\neq j}}^{N} v_{nk} \right) \end{array} \right]$$

$$V_{ni} = \sqrt{4kTR_S\Delta f + \frac{1}{N}V_n^2 + 2\rho V_n I_n R_S + N I_n^2 R_S^2}$$

In this equation, N is the total number of parallel devices. V_{ni} is the total voltage noise referred to the amplifier input. If R_s is 0 in the voltage noise equation, then [6]

$$V_{ni} = \frac{V_n}{\sqrt{N}} \tag{4.3}$$

Therefore, the larger the number of parallel devices, the lower is the noise voltage at the input of the amplifier.

For an amplifier with two stages, the overall amplifier noise figure is given by [7],

$$F = F_1 + \frac{(F_2 - 1)}{G_1} \tag{4.4}$$

It is evident from the above equation that the first stage contributes the major portion of the amplifier output noise figure, so paralleling multiple MOSFETs in the first stage results in a lower overall output noise figure.

Based on the analysis of the above noise sources in high frequency short channel CMOS circuits, it can be concluded that the MOSFETs in an LNA should have the minimum channel width that still gives the desired gain. This is because higher channel widths increase C_{gs} which is proportional to the induced gate current noise, a dominant source of noise in short channel CMOS at GHz frequencies [equation (4.2)]. Also, a high quiescent current can be split between many devices biased in parallel which further results in better noise figures (equation 4.3). Another important design technique is to reduce the number of resistors in the circuit as much as possible to minimize direct thermal noise contribution from resistors.

CHAPTER 5

LNA CIRCUIT ARCHITECTURE AND DESIGN

A new LNA architecture is proposed that includes all the low noise design factors discussed in the previous chapter. Due to the low output impedance of short channel devices, it is difficult to achieve high gain in a single stage. Therefore, two stages are designed where the first stage is a series RL shunt-shunt feedback network (Figure 5.1 (a)) and the second stage is a parallel RC shunt-shunt feedback network (Figure 5.3 (a)). Both stages have inductive loads. Inductor loads require more chip area, but provide better noise figures by avoiding resistive thermal noise in the circuit. The two stages are AC coupled through a capacitor.

The following sections show the schematic diagrams for each stage. High frequency small signal MOSFET models with shunt-shunt feedback are used to determine the input impedance, output impedance and gain equations governing these circuits (Figure 5.1 (b) and (5.3 (b)). This is followed by estimation of values for all the circuit components. The amplifier is then impedance matched to 50 ohms at both the input and output terminals over the desired pass band using LC filter impedance matching technique. This amplifier circuit is simulated in ADS and the feedback circuit components are then optimized from their calculated values to stabilize the circuit for the bandwidth of interest. During simulation, parasitic RLC networks are connected to both the supply voltage and the ground to include the parasitic effects of IC layout design.

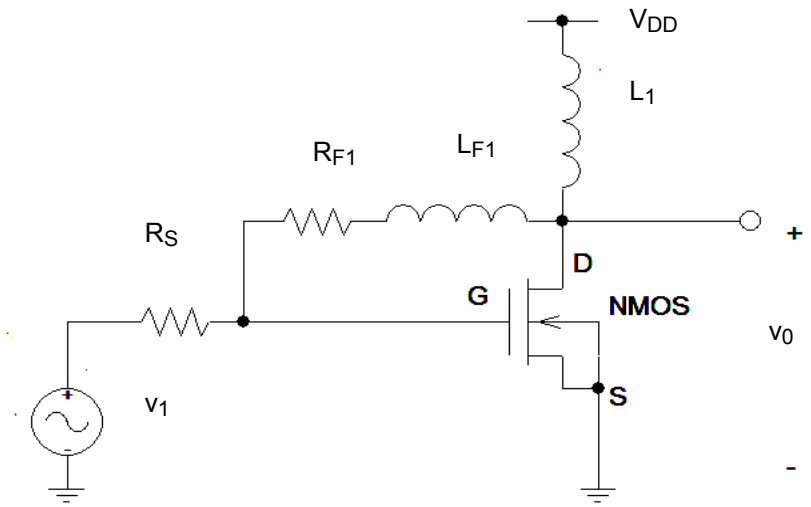
The aim is to achieve a voltage gain 20 log (S_{21}) of 20 dB (50 ohm impedance matched at the input and output ports) a Noise Figure less than 4 dB, a bandwidth (BW) of 6 GHz between 12 – 18 GHz, complete stable operation in this bandwidth, S_{11} and S_{22} less than -10 dB in this bandwidth to reduce return loss, a power consumption of less than 15 mW with a power supply of 0.5 V.

5.1 Biasing The Circuit

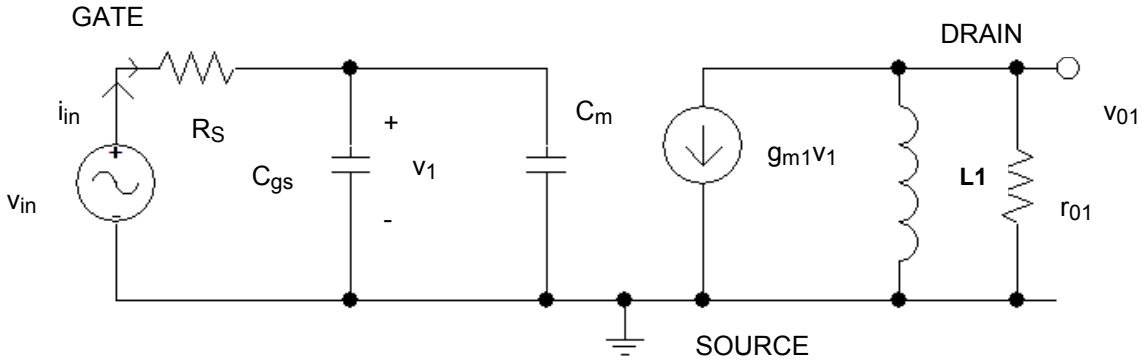
To bias this circuit, a resistive voltage divider is not implemented to avoid more resistors in the circuit in order to minimize the thermal noise. A second choice is to bias the circuit with a current mirror. Using a current mirror certainly stabilizes the bias point but increases the power consumption of the amplifier. To overcome these drawbacks, a DC blocking capacitor is used in the front end and the feedback network is used to provide the DC bias for the amplifier. This is possible in the case of MOSFETs, because the MOSFET gate acts as a capacitor and blocks DC.

5.2 LNA Design: Stage I

The first stage series RL shunt-shunt feedback amplifier with inductive load is shown in Figure 5.1(a). R_s is the source resistance, R_{F1} and L_{F1} are feedback elements, L_1 is the load inductor. Body is connected to source, so body bias is zero. Figure 5.1(b) is the high frequency small signal model for a NMOS. The equivalent miller capacitance C_m is given by $(1- A_{v1})\ C_{gd}$, where C_{gd} is the gate to drain capacitance.



(a)

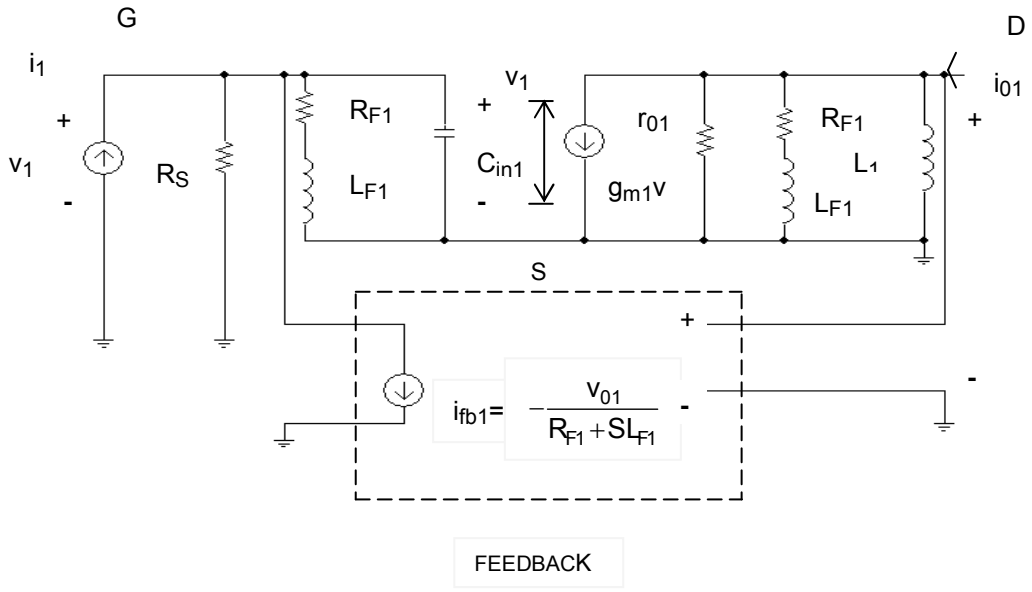


(b)

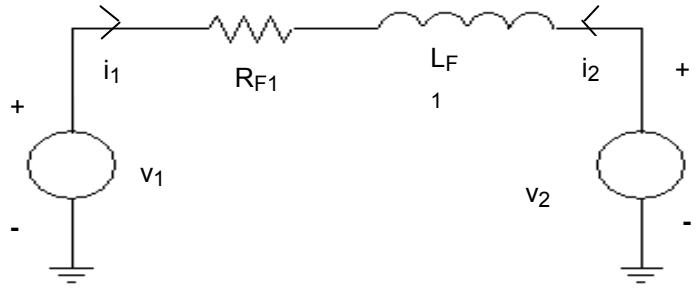
Figure 5.1 (a) Circuit architecture for input stage (b) High frequency small signal NMOS model

5.2.1Shunt-Shunt RL Feedback

The feedback in Figure 5.1 (a) is clearly a shunt-shunt feedback connection. Therefore this amplifier is modeled as a trans-resistance amplifier to simplify the analysis. From the fundamental feedback theory as explained in [8], this circuit is modeled by determining the feedback transfer function through admittance parameters.



(a)



(b)

Figure 5.2 (a) Shunt-Shunt small signal feedback circuit (b) feedback network

A shunt- shunt network is a current feedback amplifier. Therefore the transfer function of the feedback network is positive. But since the basic amplifier is an NMOS inverting amplifier, this becomes a negative feedback amplifier. Also, $C_{in1} = C_{gs} + C_m$,. The complete small signal model including feedback is given in Figure 5.2 (a).

The admittance parameters for the feedback circuit of Figure 5.2 (b) are,

$$y_{11f} = \frac{i_1}{v_1} = \frac{1}{R_{F1} + sL_{F1}} \qquad \text{when } V_2 = 0$$

$$y_{22f} = \frac{i_2}{v_2} = \frac{1}{R_{F1} + sL_{F1}} \qquad \text{when } V_1 = 0$$

$$y_{12f} = \frac{i_1}{v_2} = -\frac{1}{R_{F1} + sL_{F1}} = f_1 \qquad \text{when } V_1 = 0 \tag{5.1}$$

where f_1 is the feedback transfer function. When Kirchhoff's voltage law (KVL) is applied to the input and output loops of Figure 5.2(a),

$$v_1 = i_1\left(R_s \text{II}\left\{\frac{1}{sC_{in1}} \text{II}(R_{F1} + sL_{F1})\right\}\right)$$

$$v_1 = i_1\left[\frac{R_S(R_{F1} + sL_{F1})}{s^2L_{F1}C_{in1}R_S + s(C_{in1}R_{F1}R_S + L_{F1}) + R_S + R_{F1}}\right] \tag{5.2}$$

$$v_{01} = -g_{m1}v_1\{r_{01} \text{II}(R_{F1} + sL_{F1}) \text{II} sL_1\}$$

$$v_{01} = -g_{m1}v_1\left[\frac{r_{01}SL_1(R_{F1} + sL_{F1})}{r_{01}(sL_1 + R_{F1} + sL_{F1}) + (R_{F1} + sL_{F1})sL_1}\right] \tag{5.3}$$

The trans-resistance amplifier gain a_1 is the open loop gain derived from equations (5.2) and (5.3) given by,

$$a_1 = \frac{v_{01}}{i_1} = -g_{m1}\{(R_{F1} + sL_{F1}) \text{II} sL_1\}\left\{R_s \text{II}\left\{\frac{1}{sC_{in1}} \text{II}(R_{F1} + sL_{F1})\right\}\right\}$$

$$a_1 = -g_{m1}\left[\frac{sL_1R_s(R_{F1} + sL_{F1})^2}{(sL_1 + R_{F1} + sL_{F1})[R_S sC_{in1}(R_{F1} + sL_{F1}) + R_S + (R_{F1} + sL_{F1})]}\right] \tag{5.4}$$

The loop gain is

$$T_1 = a_1f_1$$

Substituting for f_1 from equation (5.1) and a_1 from equation (5.4),

$$T_1 = g_{m1}\left[\frac{sL_1R_s(R_{F1} + sL_{F1})}{(sL_1 + R_{F1} + sL_{F1})[R_S sC_{in1}(R_{F1} + sL_{F1}) + R_S + (R_{F1} + sL_{F1})]}\right] \tag{5.5}$$

The overall feedback amplifier gain A_1 is given by,

$$A_1 = \frac{a_1}{1+T_1} = \frac{a_1}{1+a_1 f_1}$$

Substituting for T_1 from equation (5.5) and a_1 from equation (5.4) and rearranging the terms gives,

$$A_1 = -\frac{g_{m1}\left[\dfrac{sL_1R_s(R_{F1}+sL_{F1})^2}{(sL_1+R_{F1}+sL_{F1})\left[R_S sC_{in1}(R_{F1}+sL_{F1})+R_S+(R_{F1}+sL_{F1})\right]}\right]}{1+g_{m1}\left[\dfrac{sL_1R_s(R_{F1}+sL_{F1})}{(sL_1+R_{F1}+sL_{F1})\left[R_S sC_{in1}(R_{F1}+sL_{F1})+R_S+(R_{F1}+sL_{F1})\right]}\right]}$$

$$A_1 = -\frac{g_{m1}sL_1R_s(R_{F1}+sL_{F1})^2}{(sL_1+R_{F1}+sL_{F1})\left[R_S sC_{in1}(R_{F1}+sL_{F1})+R_S+(R_{F1}+sL_{F1})\right]+g_{m1}sL_1R_s(R_{F1}+sL_{F1})}$$

$$A_1 = -\frac{g_{m1}sL_1R_s\left({R_{F1}}^2+2R_{F1}sL_{F1}+s^2{L_{F1}}^2\right)}{\begin{aligned}&s^2\cdot 2R_S C_{in1}L_{F1}R_{F1}+R_S C_{in1}{L_{F1}}^2 s^3+R_S C_{in1}{R_{F1}}^2 s+2L_{F1}R_{F1}s+sL_{F1}R_S+sL_1R_S\\&+sL_1R_{F1}+sg_{m1}L_1R_SR_{F1}+{L_{F1}}^2s^2+R_SL_1C_{in1}R_{F1}s^2+L_1L_{F1}s^2+g_{m1}L_1L_{F1}R_Ss^2\\&+R_SL_1C_{in1}L_{F1}s^3+R_{F1}(R_{F1}+R_S)\end{aligned}}$$

$$A_1 = -\frac{\dfrac{R_S g_{m1}}{R_{F1}(R_{F1}+R_S)}\left(sL_1{R_{F1}}^2+s^2(2L_{F1}L_1R_{F1})+s^3\left({L_{F1}}^2L_1\right)\right)}{\begin{aligned}&1+s\left[\frac{R_S C_{in1}{R_{F1}}^2+2L_{F1}R_{F1}+L_{F1}R_S+L_1R_S+L_1R_{F1}+g_{m1}L_1R_SR_{F1}}{R_{F1}(R_{F1}+R_S)}\right]\\&+s^2\left[\frac{2R_S C_{in1}L_{F1}R_{F1}+{L_{F1}}^2+R_SL_1C_{in1}R_{F1}+L_1L_{F1}+g_{m1}L_1L_{F1}R_S}{R_{F1}(R_{F1}+R_S)}\right]\\&+s^3\left[\frac{R_S C_{in1}{L_{F1}}^2+R_SL_1C_{in1}L_{F1}}{R_{F1}(R_{F1}+R_S)}\right]\end{aligned}} \qquad (5.6)$$

This is the overall trans-resistance gain of the amplifier. Hence the voltage gain for stage 1 is given by,

$$\frac{v_{01}}{v_0} = \frac{v_{01}}{i_1}\times\frac{i_1}{v_1}$$

Since $\dfrac{i_1}{v_1} = \dfrac{1}{R_s}$ from the small signal model,

Voltage gain $A_{V_1} = \dfrac{v_{01}}{v_1} = \dfrac{A_1}{R_S} = \dfrac{\dfrac{a_1}{R_S}}{1 + a_1 f_1}$

Substituting equation (5.6) for A_1 in the above equation, the voltage gain for stage I is given by,

$$A_{V_1} = -\frac{\dfrac{g_{m1}}{R_{F1}(R_{F1}+R_S)}\left(sL_1R_{F1}{}^2 + s^2(2L_{F1}L_1R_{F1}) + s^3\left(L_{F1}{}^2L_1\right)\right)}{1 + s\left[\dfrac{R_SC_{in1}R_{F1}{}^2 + 2L_{F1}R_{F1} + L_{F1}R_S + L_1R_S + L_1R_{F1} + g_{m1}L_1R_SR_{F1}}{R_{F1}(R_{F1}+R_S)}\right] + s^2\left[\dfrac{2R_SC_{in1}L_{F1}R_{F1} + L_{F1}{}^2 + R_SL_1C_{in1}R_{F1} + L_1L_{F1} + g_{m1}L_1L_{F1}R_S}{R_{F1}(R_{F1}+R_S)}\right] + s^3\left[\dfrac{R_SC_{in1}L_{F1}{}^2 + R_SL_1C_{in1}L_{F1}}{R_{F1}(R_{F1}+R_S)}\right]} \tag{5.7}$$

The shunt connection always reduces the impedance. The input impedance is given by,

$$Z_{inx} = \frac{Z_{ina}}{1 + T_1} \tag{5.8}$$

where Z_{ina} is the basic amplifier input impedance. From Figure 5.2(a),

$$Z_{ina} = R_S \,||\, (R_{F1} + sL_{F1}) \,||\, \frac{1}{sC_{in1}}$$

$$\therefore Z_{ina} = \left[\frac{R_S(R_{F1} + sL_{F1})}{s^2L_{F1}C_{in1}R_S + s(C_{in1}R_{F1}R_S + L_{F1}) + R_S + R_{F1}}\right] \tag{5.9}$$

Substituting equation (5.9) in the equation (5.8) gives,

$$Z_{inx} = \frac{\left[\dfrac{R_S(R_{F1} + sL_{F1})}{s^2L_{F1}C_{in1}R_S + s(C_{in1}R_{F1}R_S + L_{F1}) + R_S + R_{F1}}\right]}{1 + g_{m1}\left[\dfrac{sL_1R_s(R_{F1} + sL_{F1})}{(sL_1 + R_{F1} + sL_{F1})\left[R_SsC_{in1}(R_{F1} + sL_{F1}) + R_S + (R_{F1} + sL_{F1})\right]}\right]}$$

The input impedance of the feedback amplifier Z_{In1} excludes R_s, therefore

$$Z_{in1} = \left(\frac{1}{Z_{inx}} - \frac{1}{R_S}\right)^{-1}$$

The input impedance of the circuit Figure 5.1(a) is given by,

$$Z_{in} = R_s + Z_{in1} \tag{5.10}$$

In a similar way, the shunt connection at the output decreases the impedance as given by,

$$Z_{01} = \frac{Z_{01a}}{1 + T_1}$$

where Z_{01a} is the basic amplifier output impedance. From Figure 5.2 (a),

$$Z_{01a} = r_{01} \| (R_{F1} + sL_{F1}) \| sL_1$$

$$Z_{01a} = \frac{r_{01} sL_1 (R_{F1} + sL_{F1})}{r_{01}(sL_1 + R_{F1} + sL_{F1}) + (R_{F1} + sL_{F1}) sL_1} \tag{5.11}$$

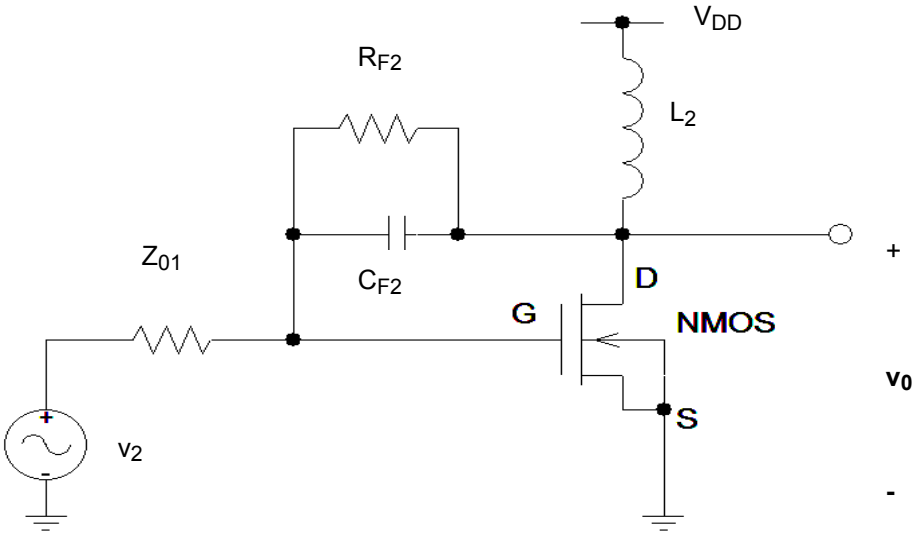
Substituting for Z_{01} in equation (5.11),

$$Z_{01} = \frac{\dfrac{r_{01} sL_1 (R_{F1} + sL_{F1})}{r_{01}(sL_1 + R_{F1} + sL_{F1}) + (R_{F1} + sL_{F1}) sL_1}}{1 + g_{m1}\left[\dfrac{sL_1 R_s (R_{F1} + sL_{F1})}{(sL_1 + R_{F1} + sL_{F1})[R_S sC_{in1}(R_{F1} + sL_{F1}) + R_S + (R_{F1} + sL_{F1})]}\right]} \tag{5.12}$$

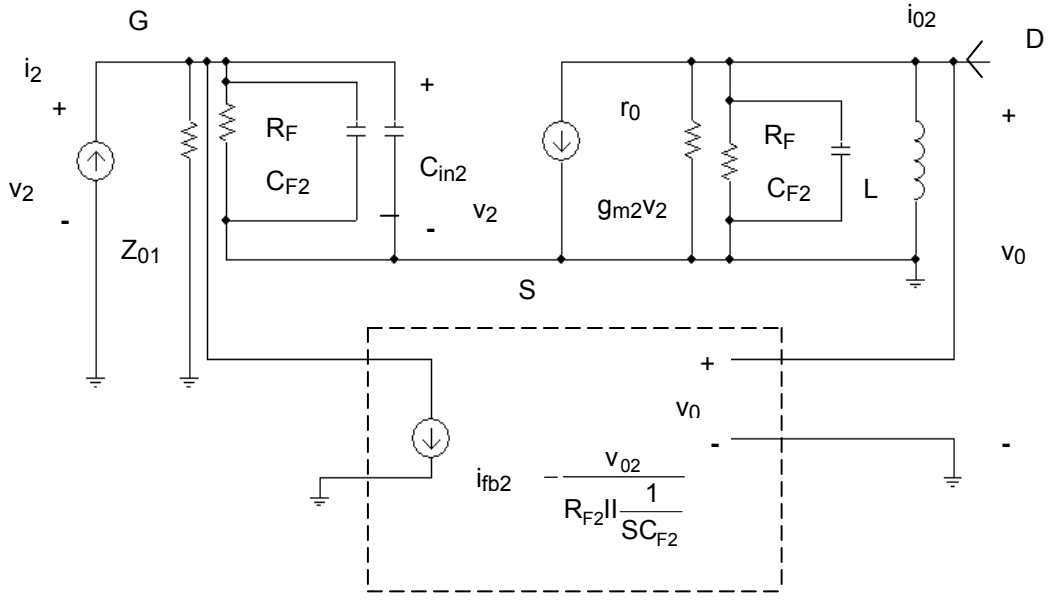
This is the output impedance for first stage of the amplifier, which is also the source impedance for stage II.

5.3 LNA Design: Stage II

The second stage is a parallel RC shunt-shunt feedback amplifier with inductive load [Figure 5.3(a)]. The source impedance is Z_{01} which is the output impedance of stage I, R_{F2} and C_{F2} are feedback elements and L_2 is the load inductor. The body is connected to the source, so body bias is zero. Similar shunt-shunt feedback theory is applied to this stage as in stage I. It is modeled as a trans-resistance amplifier. Figure 5.3(b) and (c) shows the small signal high frequency model with feedback for stage II.



(a)



FEEDBACK

(b)

Figure 5.3 (a) Circuit architecture for output stage (b) shunt-shunt small signal feedback circuit

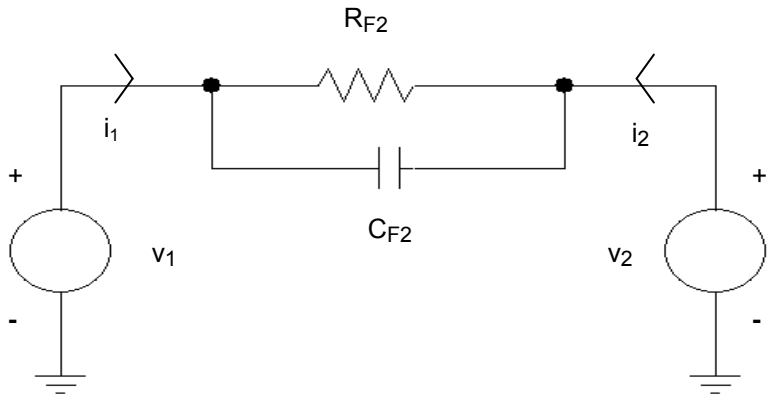


Figure 5.4 Feedback network

5.3.1Shunt-Shunt RC Feedback

The admittance parameters for the feedback circuit of Figure 5.4 are,

$$y_{11f} = \frac{i_1}{v_1} = \frac{1}{R_{F2} \| \left(\frac{1}{sC_{F2}} \right)} \qquad \text{when } V_2 = 0$$

$$y_{22f} = \frac{i_2}{v_2} = \frac{1}{R_{F2} \| \left(\frac{1}{sC_{F2}} \right)} \qquad \text{when } V_1 = 0$$

$$y_{12f} = \frac{i_1}{v_2} = -\frac{1}{R_{F2} \| \left(\frac{1}{sC_{F2}} \right)} = f_2 \qquad \text{when } V_1 = 0 \qquad (5.13)$$

where f_2 is the feedback transfer function. Application of the KVL at the input and output loops in Figure 5.3(b) gives,

$$v_2 = i_2 \left(Z_{01} \| \left\{ \frac{1}{sC_{in2}} \| R_{F2} \| \left(\frac{1}{sC_{F2}} \right) \right\} \right)$$

$$v_2 = i_2 \left[\frac{Z_{01} R_{F2}}{Z_{01} R_{F2} sC_{F2} + Z_{01} R_{F2} sC_{in2} + Z_{01} + R_{F2}} \right] \qquad (5.14)$$

$$v_{02} = -g_{m2} v_2 \left\{ r_{02} \| R_{F2} \| \left(\frac{1}{sC_{F2}} \right) \| sL_2 \right\}$$

$$v_{02} = -g_{m2} v_2 \left[\frac{R_{F2} sL_2 r_{02}}{r_{02} R_{F2} + r_{02} sL_2 + R_{F2} sL_2 r_{02} sC_{F2} + R_{F2} sL_2} \right] \qquad (5.15)$$

The basic amplifier open loop gain, a_2, derived from equations (5.14) and (5.15) is given by,

$$a_2 = \frac{v_{02}}{i_2} = -g_{m2}\left\{\left(R_{F2} \| \left(\frac{1}{sC_{F2}}\right)\right) \| sL_2\right\}\left\{Z_{01} \| \left\{\frac{1}{sC_{in2}} \| R_{F2} \| \left(\frac{1}{sC_{F2}}\right)\right\}\right\}$$

$$a_2 = -g_{m2}\left[\frac{R_{F2}{}^2 sL_2 Z_{01}}{(R_{F2} + sL_2 + R_{F2}sL_2sC_{F2})(Z_{01}R_{F2}sC_{F2} + Z_{01}R_{F2}sC_{in2} + Z_{01} + R_{F2})}\right] \tag{5.16}$$

The loop gain

$$T_2 = a_2 f_2$$

$$T_2 = \frac{g_{m2}R_{F2}sL_2Z_{01}(R_{F2}sC_{F2} + 1)}{(R_{F2} + sL_2 + R_{F2}sL_2sC_{F2})(Z_{01}R_{F2}sC_{F2} + Z_{01}R_{F2}sC_{in2} + Z_{01} + R_{F2})} \tag{5.17}$$

The overall trans-resistance amplifier gain A_2 is given by,

$$A_2 = \frac{a_2}{1 + T_2} = \frac{a_2}{1 + a_2 f_2}$$

Substituting (5.16) and (5.17) in the above equation and rearranging the terms gives,

$$A_2 = -\frac{g_{m2}\left[\frac{R_{F2}{}^2 sL_2 Z_{01}}{(R_{F2} + sL_2 + R_{F2}sL_2sC_{F2})(Z_{01}R_{F2}sC_{F2} + Z_{01}R_{F2}sC_{in2} + Z_{01} + R_{F2})}\right]}{1 + \frac{g_{m2}R_{F2}sL_2Z_{01}(R_{F2}sC_{F2} + 1)}{(R_{F2} + sL_2 + R_{F2}sL_2sC_{F2})(Z_{01}R_{F2}sC_{F2} + Z_{01}R_{F2}sC_{in2} + Z_{01} + R_{F2})}}$$

$$A_2 = -\frac{g_{m2}R_{F2}{}^2 sL_2 Z_{01}}{(R_{F2} + sL_2 + R_{F2}sL_2sC_{F2})(Z_{01}R_{F2}sC_{F2} + Z_{01}R_{F2}sC_{in2} + Z_{01} + R_{F2}) + g_{m2}R_{F2}sL_2Z_{01}(R_{F2}sC_{F2} + 1)}$$

$$\begin{aligned} A_2 = -\frac{sg_{m2}R_{F2}{}^2 L_2 Z_{01}}{} & \\ sR_{F2}{}^2 Z_{01}C_{F2} + sR_{F2}L_2 + sg_{m2}R_{F2}L_2Z_{01} + Z_{01}R_{F2} + R_{F2}{}^2 + R_{F2}Z_{01}C_{F2}L_2s^2 & \\ + sR_{F2}{}^2 Z_{01}C_{in2} + R_{F2}{}^2 C_{F2}L_2s^2 + sZ_{01}L_2 + s^2R_{F2}L_2Z_{01}C_{F2} + s^3Z_{01}C_{in2}L_2C_{F2}R_{F2}{}^2 & \\ + s^2R_{F2}Z_{01}C_{in2}L_2 + s^2g_{m2}R_{F2}{}^2 L_2 Z_{01}C_{F2} + s^3R_{F2}{}^2 L_2 Z_{01}C_{F2}{}^2 & \end{aligned}$$

$$A_2 = -\frac{s\left(\frac{g_{m2}R_{F2}L_2Z_{01}}{(Z_{01}+R_{F2})}\right)}{1+s\left[\frac{R_{F2}^2Z_{01}C_{F2}+R_{F2}^2Z_{01}C_{in2}+Z_{01}L_2+R_{F2}L_2+g_{m2}R_{F2}L_2Z_{01}}{(Z_{01}+R_{F2})R_{F2}}\right]+s^2\left[\frac{R_{F2}Z_{01}C_{F2}L_2+R_{F2}^2C_{F2}L_2+R_{F2}L_2Z_{01}C_{F2}+R_{F2}Z_{01}C_{in2}L_2+g_{m2}R_{F2}^2L_2Z_{01}C_{F2}}{(Z_{01}+R_{F2})R_{F2}}\right]+s^3\left[\frac{R_{F2}^2L_2Z_{01}C_{F2}^2+Z_{01}C_{in2}L_2C_{F2}R_{F2}^2}{(Z_{01}+R_{F2})R_{F2}}\right]} \quad (5.18)$$

The equation (5.18) is the trans-resistance gain of the amplifier. Therefore the voltage gain for stage 2 is given by,

$$\frac{v_{02}}{v_0} = \frac{v_{02}}{i_2} \times \frac{i_2}{v_2}$$

But, $\frac{i_2}{v_2} = \frac{1}{Z_{01}}$

Hence, $A_{V_2} = \frac{v_{02}}{v_2} = \frac{A_2}{Z_{01}} = \frac{\frac{a_2}{Z_{01}}}{1+a_2f_2}$

Substituting equation (5.18) for A_2 in the above equation, the voltage gain for stage II is given by,

$$A_{V2} = -\frac{s\left(\frac{g_{m2}R_{F2}L_2}{(Z_{01}+R_{F2})}\right)}{1+s\left[\frac{R_{F2}^2Z_{01}C_{F2}+R_{F2}^2Z_{01}C_{in2}+Z_{01}L_2+R_{F2}L_2+g_{m2}R_{F2}L_2Z_{01}}{(Z_{01}+R_{F2})R_{F2}}\right]+s^2\left[\frac{R_{F2}Z_{01}C_{F2}L_2+R_{F2}^2C_{F2}L_2+R_{F2}L_2Z_{01}C_{F2}+R_{F2}Z_{01}C_{in2}L_2+g_{m2}R_{F2}^2L_2Z_{01}C_{F2}}{(Z_{01}+R_{F2})R_{F2}}\right]+s^3\left[\frac{R_{F2}^2L_2Z_{01}C_{F2}^2+Z_{01}C_{in2}L_2C_{F2}R_{F2}^2}{(Z_{01}+R_{F2})R_{F2}}\right]} \quad (5.19)$$

Total gain of the amplifier is $A_v = (A_{v1})\,(A_{v2})$.

The shunt connection at the output decreases the impedance as given by,

$$Z_{02} = \frac{Z_{02a}}{1+T_2}$$

where Z_{02a} is the basic amplifier output impedance. From Figure 5.3 (b),

$$Z_{02a} = r_{02} \| \left(R_{F2} \| \left(\frac{1}{sC_{F2}} \right) \right) \| sL_2$$

Substituting equation (5.19) for Z_{02} in the above equation,

$$Z_{02} = \frac{\dfrac{R_{F2}sL_2r_{02}}{r_{02}R_{F2} + r_{02}sL_2 + R_{F2}sL_2r_{02}sC_{F2} + R_{F2}sL_2}}{1 + \dfrac{g_{m2}R_{F2}sL_2Z_{01}(R_{F2}sC_{F2}+1)}{(R_{F2}+sL_2+R_{F2}sL_2sC_{F2})(Z_{01}R_{F2}sC_{F2}+Z_{01}R_{F2}sC_{in2}+Z_{01}+R_{F2})}} \qquad (5.20)$$

This is the output impedance of the amplifier.

5.4 Design of Amplifier Circuit Components

Given the complexity of the circuit gain equations (5.7 and 5.19) and the impedance equations (5.4 and 5.20), simplification of the feedback theory is used in the design of an LNA for the desired specifications. The voltage gain equation for each stage of the amplifier as defined earlier can be approximated using feedback theory as shown below:

$$A_{V_1} = \frac{v_{01}}{v_1} = \frac{A_1}{R_S} = \frac{\dfrac{a_1}{R_S}}{1+a_1f_1}$$

If $T_1 = af_1 >> 1$,

then $$\frac{a_1}{1+a_1f_1} \cong \frac{1}{f_1} = -(R_{F1} + sL_{F1})$$

Therefore, $$A_{V_1} = -\frac{(R_{F1}+sL_{F1})}{R_S} \qquad (5.21)$$

The gain is negative for an inverting amplifier. Similarly for stage 2,

$$A_{V_2} = \frac{v_{02}}{v_2} = \frac{A_2}{Z_{01}} = \frac{\dfrac{a_2}{Z_{01}}}{1+a_2f_2}$$

If $T_2 >> 1$,

Then $\frac{a_2}{1+a_2 f_2} \cong \frac{1}{f_2} = -\left(R_{F2} \| \left(\frac{1}{sC_{F2}}\right)\right)$

$$A_{V_2} = -\frac{\left(R_{F2} \| \left(\frac{1}{sC_{F2}}\right)\right)}{Z_{01}}$$

Therefore, $A_{V_2} = \frac{-R_{F2}}{(R_{F2} sC_{F2} + 1) Z_{01}}$ (5.22)

The desired power consumption is to be less than 15 mW using a 0.5 V power supply. Therefore, the maximum current for the amplifier is given by,

Maximum Current = Total maximum Power Consumption / Supply Voltage

Therefore, the maximum current in the circuit has to be less than 30 mA. To achieve a voltage gain of 20 dB, let the maximum total current in the amplifier be limited to 25 mA. Let the desired voltage gain of the first stage be 13 dB and that of the second stage be 7 dB. Therefore,

A_{V_1} in dB= $\text{anti}\log\left(\frac{13}{20}\right) = 4.46$

A_{V2} in dB= $\text{anti}\log\left(\frac{7}{20}\right) = 2.23$

Taking the magnitude of equation (5.21),

$$\left|A_{V_1}\right| = 4.46 = -\frac{\sqrt{(R_{F1})^2 + (\omega L_{F1})^2}}{R_S}$$

$$L_{F1} = \frac{\sqrt{A_{V1}{}^2 R_S{}^2 - R_{F1}{}^2}}{\omega}$$

Resistance R_{F1} is a feedback element which determines the stability of circuit operation along with L_{F1}. Assuming R_{F1} to be 220 Ohms for now, and the center frequency f_c = 15 GHz,

$$L_{F1} = \frac{\sqrt{4.46^2 \times 50^2 - 220^2}}{2\pi \times 15 \times 10^9}$$

$L_{F1} = 0.38\text{nH}$

If say 10 NMOSFETs are connected in parallel with a total current in stage I being limited to 16 mA, and 5 NMOSFETs are connected in parallel for stage II with a total current of 9

mA leading up to a total of 25 mA in the amplifier, each NMOS in the LNA has to be biased with a quiescent current of 1.6 mA.

To operate in saturation, V_{DS} should be > (V_{GS} – V_{th}). Because both stages have inductor loads, the DC drop across these inductors are approximately zero. Because the MOS input gate current is zero, the gate voltage is approximately the same as the drain voltage which is approximately equal to 0.5 V. This ensures that the NMOS is always in the saturation region. Using the mathematical model equations from chapter 2, the required channel width to bias each NMOS to I_D = 1.6 mA is determined below.

All equations in chapter 2 use V_{gs} = 0.5 V and V_{ds} = 0.6 V. Therefore, all the equations that are affected when V_{ds} = 0.5 V, are recalculated below:

$$V_{th} = 0.3423\text{V} + \left(0.2\cdot\sqrt{0.914\ \text{V} - 0} - 0.2\text{V}^{0.5}\cdot\sqrt{0.914\ \text{V}}\right)\sqrt{1+\frac{0\text{m}}{19.6\text{nm}}} - 0$$

$$+ 0.2\cdot\left(\sqrt{1+\frac{\text{LPE0}}{19.6\text{nm}}} - 1\right)\sqrt{0.914\ \text{V}} + (0+0)\frac{0.9\times e^{-9}}{W_{eff}' + 2.6\times e^{-6}\text{m}}\times 0.914\ \text{V}$$

$$- 0.5\cdot\left[\frac{0}{\cosh\left(0\times\frac{19.6\text{nm}\times W_{eff}'}{l_{tw}}\right)-1} + \frac{1}{\cosh\left(2\times\frac{19.6\text{nm}}{l_t}\right)-1}\right](1.1167\ \text{V} - 0.914\ \text{V})$$

$$- \frac{0.5}{\cosh\left(0.078\times\frac{19.6\text{n}}{6.025\text{n}}\right)-1}\left(0.0055 + 0\text{V}^{-1}.0\right)0.5$$

V_{th} = 0.2913 V at V_{DS} = 0.5 V.

$$V_{gsteff} = \frac{1.198\times 25.85\text{m}\times\ln\left\{1+\exp\left[\frac{0.515(0.499-0.2913)}{1.198\times 25.85\text{m}}\right]\right\}}{0.515 + 1.198\times 38.36\times e^{-15}\cdot\sqrt{\frac{2\times 0.914}{1.6\times 10^{-19}\times 6.5\times e^{18}\times 11.68}}\exp\left[-\frac{(1-0.515)(0.499-0.2913)-(-0.13)}{1.198\times 25.85\text{m}}\right]}$$

V_{gsteff} = 0.2095 V.

$$\mu_{eff} = \frac{0.02947}{1+\left(-5\times e^{-10}+0\cdot V_{bseff}\right)\left(\frac{0.2095+2\times 0.2913}{0.9\times e^{-9}}\right)+1.7\times e^{-18}\left(\frac{0.2095+2\times 0.2913}{0.9\times e^{-9}}\right)^2}$$

Effective mobility μ_{eff} = 0.0157 m^2/V-s.

$$E_{sat} = \frac{2\times 159550}{0.0157}$$

Saturation electric field $E_{sat} = 20324840.76$ V/m.

$$V_{dsat} = \frac{20324840.76\times 19.6n(0.2095+2\times 25.85m)}{1.2177\times 20324840.76\times 19.6n+0.2095+2\times 25.85m}$$

$V_{dsat} = 0.1737$ V.

The product of the last four terms in the equation for drain current (2.38) after simplification is (1.0644) (1.003) (1.018) (1.041) = 1.13. Since this value is approximately equal to 1, if the product of these four terms were substituted by 1 in the equation for drain current (2.38), drain current becomes I_D = 1.08 mA, which is very close to the simulation result (I_D = 1.028 mA from Figure 3.2). This simplification modifies the drain current equation (2.29) below:

$$I_{ds} = \frac{I_{ds0}\cdot NF}{1+\frac{R_{ds}I_{ds0}}{V_{dseff}}}$$

In the above equation, denominator = 1 from equation (2.38). Therefore,

$$I_{ds} = I_{ds0}\cdot NF$$

where, $I_{ds0} = \frac{W\mu_{eff}Q_{ch0}V_{ds}\left(1-\frac{V_{ds}}{2V_b}\right)}{L\left(1+\frac{V_{ds}}{E_{sat}L}\right)}$ and NF = number of fingers

Rearranging the above equation, $W = \frac{I_{ds0}L\left(1+\frac{V_{ds}}{E_{sat}L}\right)}{\mu_{eff}Q_{ch0}V_{ds}\left(1-\frac{V_{ds}}{2V_b}\right)}$

For $I_{ds} = 1.6$mA and NF = 10,

$$I_{ds0} = \frac{1.6m}{10}$$

$I_{ds0} = -0.16mA$. (Sign in accordance with equation (2.35a))

Substituting, $W = \dfrac{-0.16m \times 19.6n\left(1 + \dfrac{0.5}{20324840.76 \times 45n}\right)}{0.0157 \times 8.036\, e^{-3} \times 0.5\left(1 - \dfrac{0.5}{2 \times 0.2540}\right)}$

$W = 464.52nm$

For NF=10 fingers, total W = (464.52) (10).

Therefore, W = 4645.2 nm for every NMOS in the circuit. Simulation results for this dimension of the NMOS transistor yields a transconductance

$g_m = 0.0117A / V$

The input capacitance of the amplifier stage 1 is given by,

$C_{in} = C_{gs} + C_m$

$C_{in} = C_{gs} + (1 - A_{V1})C_{gd}$

For 10 transistors in parallel (Figure 6.3) for stage 1 of the amplifier,

$C_{in} = 10\left[C_{gs} + (1 - A_{V1})C_{gd}\right]$

In the saturation region, since the channel does not exist near the gate – drain interface,

$C_{gd} = 0$

$$C_{gs} = \left(\frac{2}{3}\right)WLC_{oxe}$$

$$C_{gs} = \left(\frac{2}{3}\right) \times 4645.2 \times 10^{-9} \times 45 \times 10^{-9} \times 38.36 \times 10^{-3}$$

$C_{gs} = 5.345 \times 10^{-15}F$

Therefore, $C_{in} = C_{gs} \times 10 = 53.45 \times 10^{-15}F$

The transconductance is given by,

$g_m = \omega_T \cdot (C_{gs} + C_{gd})$

Therefore, $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$

Substituting $g_m = 0.0117 A/V$ equivalent of 10 parallel MOSFETs in the above equation,

$$f_T = \frac{0.0117 \times 10}{2\pi(53.45 \times 10^{-15} + 0)}$$

$f_T = 348.34 GHz$ is the transition frequency of the 45 nm NMOS transistor.

The drain to body C_{db} capacitance of the stage 1, which is 0.8 fF as obtained by simulation is in parallel with the input capacitance of the stage 2:

For 5 transistors in parallel (Figure 6.4) for stage 2 of the amplifier,

C_{in2} = 5 C_{gs2} with C_{gd2} = 0 in the saturation region.

The width of each NMOS in stage 2 is the same as that of stage 1.

Therefore $C_{gs2} = C_{gs1}$ = 5.34 fF.

Hence the input capacitance of stage 2 is C_{in2} = 26.73 fF. This is in parallel with the feedback capacitance C_{F2} of the amplifier stage 2.

At the operating point, simulation gives the magnitude of the output impedance of stage 1 at 15 GHz as Z_{01} ~ 45 Ohms. From equation (5.9),

$$|A_{V2}| = -\frac{R_{F2}}{Z_{01} \cdot \sqrt{(R_{F2}\omega C_{F2})^2 + 1}}$$

Rearranging, $C_{F2} = \frac{1}{R_{F2}\omega}\left[\left(\frac{R_{F2}}{Z_{01}A_{V2}}\right)^2 - 1\right]^{1/2}$

Assuming R_{F2} = 150 Ohms,

$$C_{F2} = \frac{1}{150 \cdot 2\pi \cdot 15 \times 10^9}\left[\left(\frac{150}{45 \times 2.23}\right)^2 - 1\right]^{1/2}$$

$C_{F2} = 78.4 fF$

This capacitance acts like an equivalent miller capacitance in the feedback path and is amplified by the stage 2 inverting amplifier gain.

$C_{m2} = (1 - A_{v2})\, C_{F2}$

Therefore $C_{m2} = (1 – (-2.23))\ 78.4fF = 253.23\ fF$.

Hence, the equivalent capacitance at the input of the amplifier stage 2, which acts a load capacitor for the stage 1 is given by,

$C_{in2} = C_{m2} + 5\, C_{gs2} = 253.\ 23\ fF + 133.65\ fF = 386.88\ fF$.

The value of the load inductor L_1 to cancel out this capacitance at 15 GHz is given by,

$$L_1 = \frac{\left[\frac{1}{2\pi f_C}\right]^2}{C_{in2}}$$

$$L_1 = \frac{\left[\frac{1}{2\pi \times 15 \times 10^9}\right]^2}{386.88 \times 10^{-15}}$$

$L_1 = 0.29$ nH

The output capacitance of stage 2 is the equivalent miller capacitance from the feedback capacitor C_{F2}. Hence, $C_{out} = C_{m2} = 253.23$ fF. The load inductor of stage 2 is determined by,

$$L_2 = \frac{\left[\frac{1}{2\pi f_C}\right]^2}{C_{out}}$$

$$L_2 = \frac{\left[\frac{1}{2\pi \times 15 \times 10^9}\right]^2}{253.23 \times 10^{-15}}$$

$L_2 = 0.44$ nH.

5.5 Impedance Matching

Impedance matching is important to minimize signal reflections at the input and the output ports of the amplifier. For the desired wide bandwidth of 6 GHz (12-18 GHz), it is very difficult to model inductors and capacitors and get them to operate properly for the complete

bandwidth of interest. A simple matching network is designed using conventional methods. Some component values are optimized in ADS to achieve the desired results. Figures below show the component values of these matching networks obtained using the “L” matching circuit for which software is available at uta.edu [9]. The terminal impedances at the input and the output of the amplifier at 15 GHz are obtained from the simulation results (Figures 5.5).

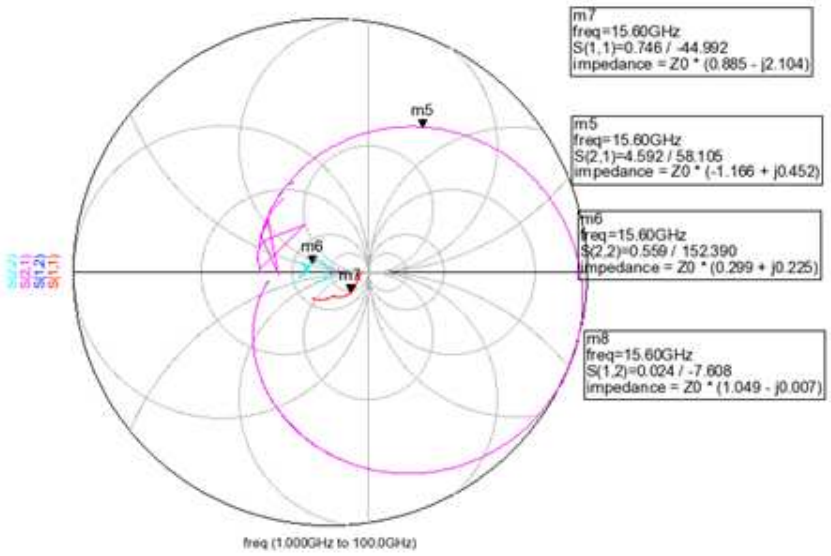
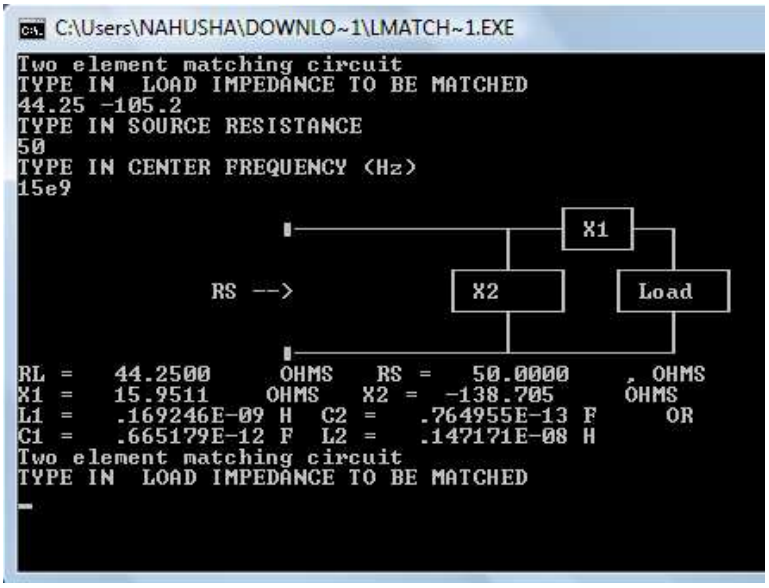


Figure 5.5 S parameters of the unmatched amplifier network. Z_0 =50 ohms.

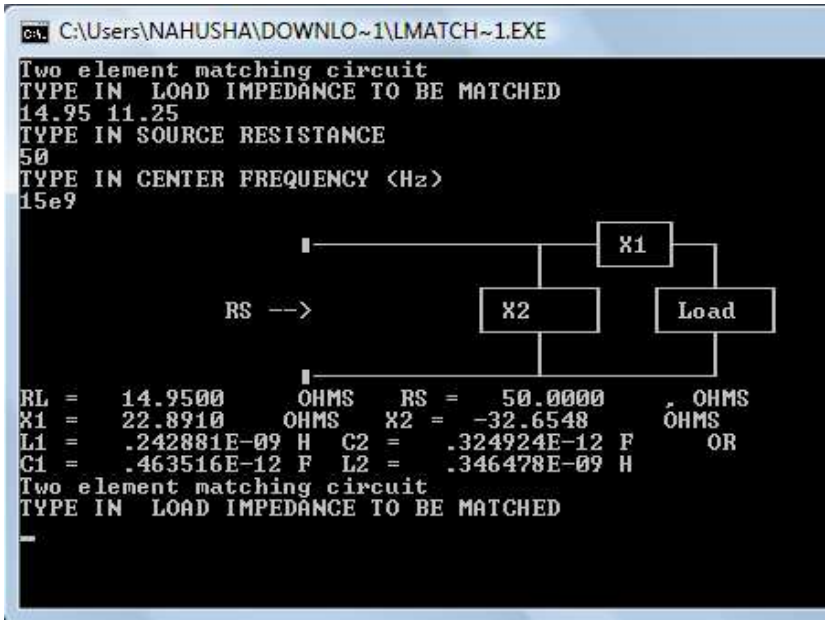
Figure 5.5 shows the plot of S parameters and the terminal impedances of the two port network model of the amplifier at the center frequency f_c = 15 GHz. From figure 5.5,

Input impedance of the two port network = 50 (0.885 – j2.104) = 44.25 – j105.2 Ohms.

Output impedance of the two port network = 50 (0.299 + j 0.225) = 14.95 + j 11.25 Ohms.



(a)



(b)

Figure 5.6 (a) Input Impedance matching (b) Output impedance matching

An additional Pi network (Figure 6.4) with an inductor of 0.26 nH and two capacitors of 400 fF is used to improve output impedance matching. These values are obtained by simulation through trial and error method.

CHAPTER 6

LNA SIMULATION IN ADS

The circuit is simulated in ADS with all the calculated component values and design criteria explained in the previous chapter. The stability of both stages are obtained by optimizing feedback elements to satisfy the Rollett stability criteria for unconditional stability [10] defined as

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \geq 1 \tag{6.1}$$

The following diagrams show the step by step simulation results obtained by ADS. The width of each NMOS is set to 4500 nm split into 10 fingers, and the circuit components are optimized to achieve the desired results. As a result some of the passive elements are L_1, L_2 = 0.22 nH, R_{F2} = 710 Ohms, C_{F2} = 40 fF with each NMOS driving a current of 1.8 mA.

A bandwidth of approximately 1.8 GHz from 14.4 – 16.6 GHz was achieved, although the gain of the amplifier is within 3 dB of its maximum value for the 6 GHz bandwidth from 12 – 18 GHz. The peak gain achieved is 19.2 dB centered at 15.4 GHz. The maximum noise figure in the circuit is 2.2 dB at 18 GHz, with a noise figure of 1.5 dB at 15.4 GHz. The total current consumption is nearly 27 mA, so the power consumption is 13.5 mW. The amplifier is completely stable in the 12-18 GHz bandwidth.

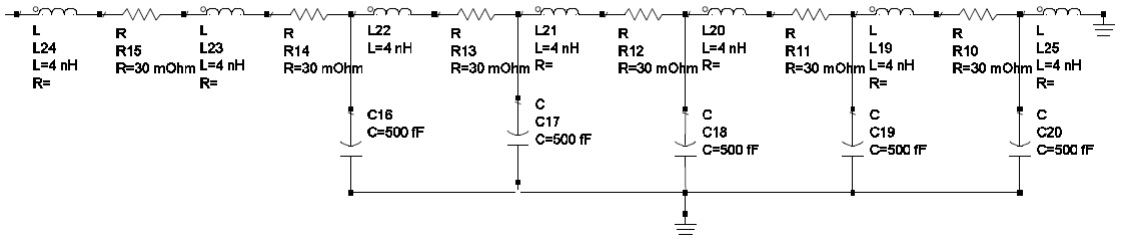


Figure 6.1 The effects of layout parasitics incorporated by equivalent RLC network connected to both supply and ground

The RLC network in figure 6.2 accounts for the signal degradation and layout parasitic effects that originate from the bonding pad connections of an IC. This network is used in the low noise amplifier circuit as shown in figure 6.4.

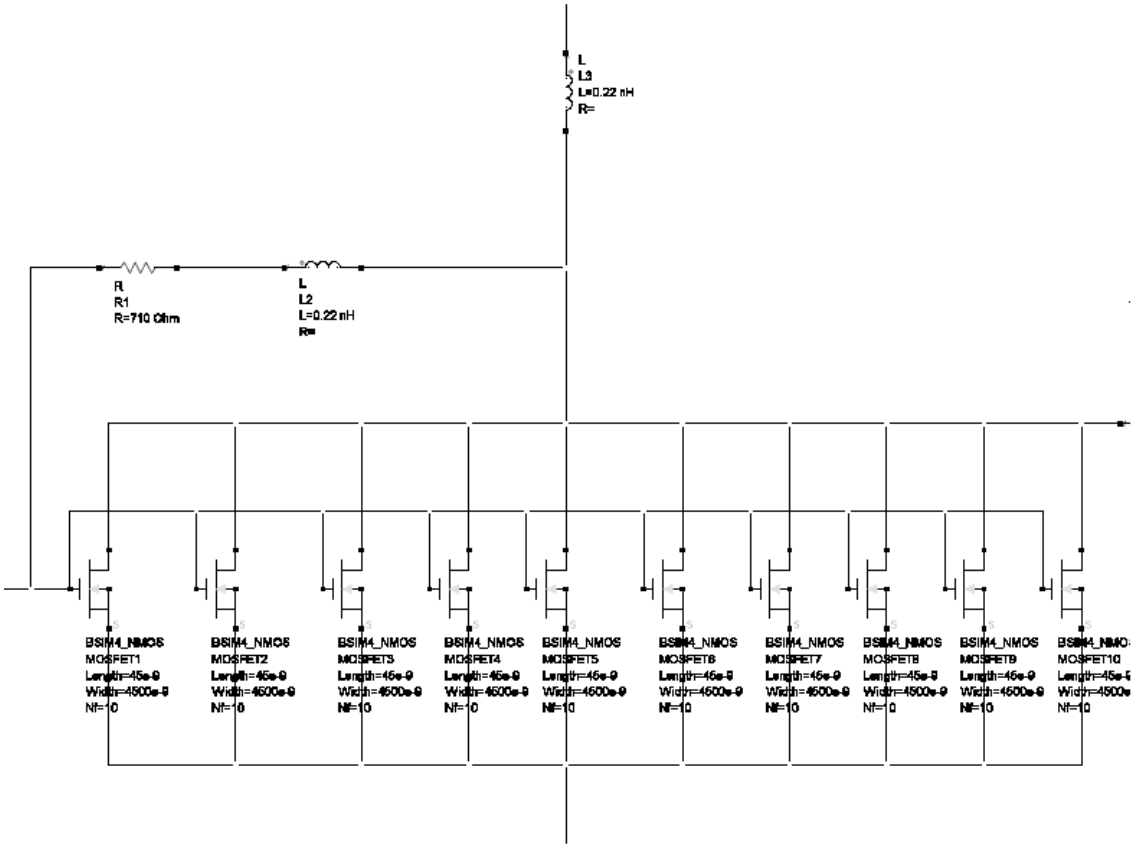


Figure 6.2 LNA circuit stage I

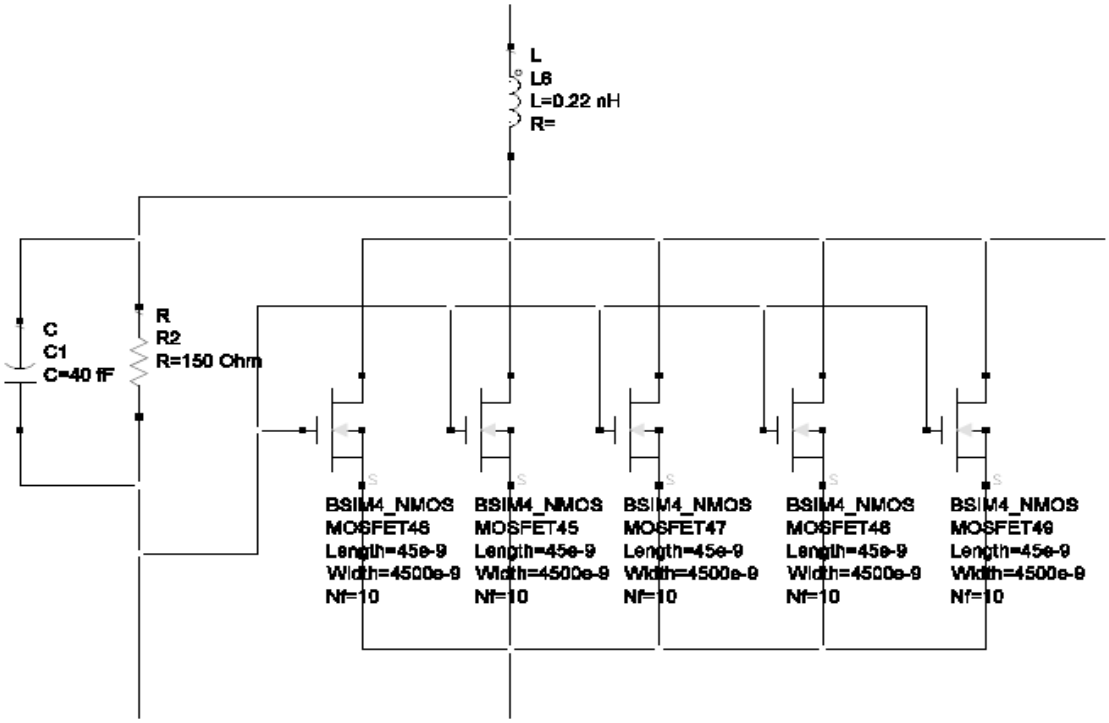


Figure 6.3 LNA circuit stage II

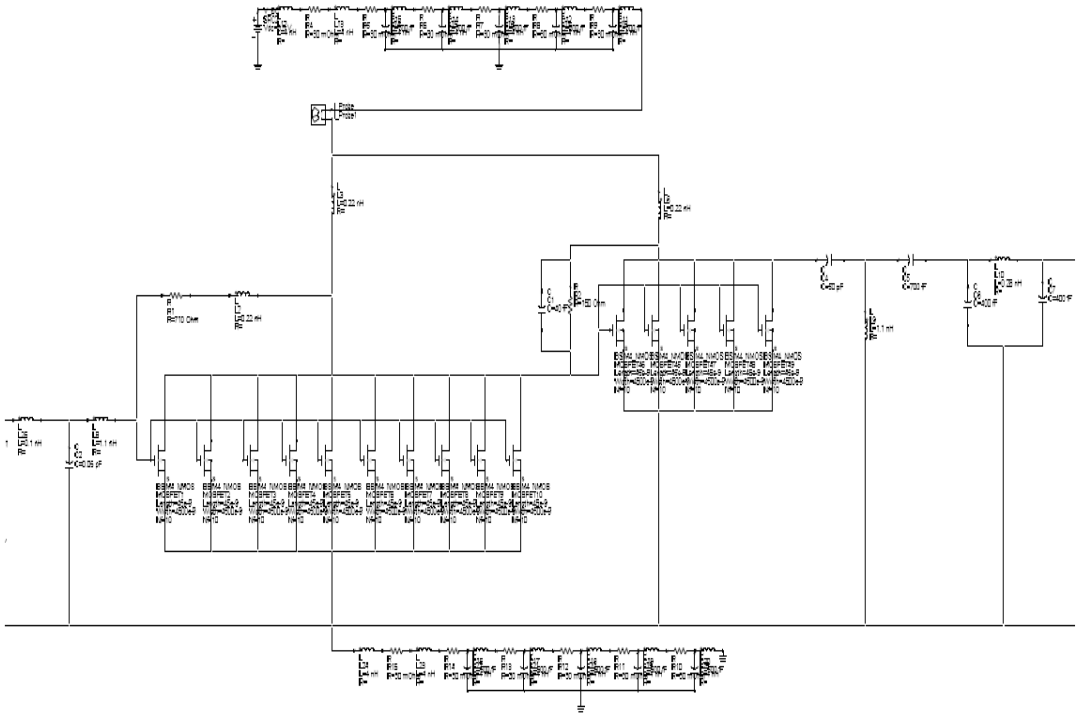


Figure 6.4 The complete LNA

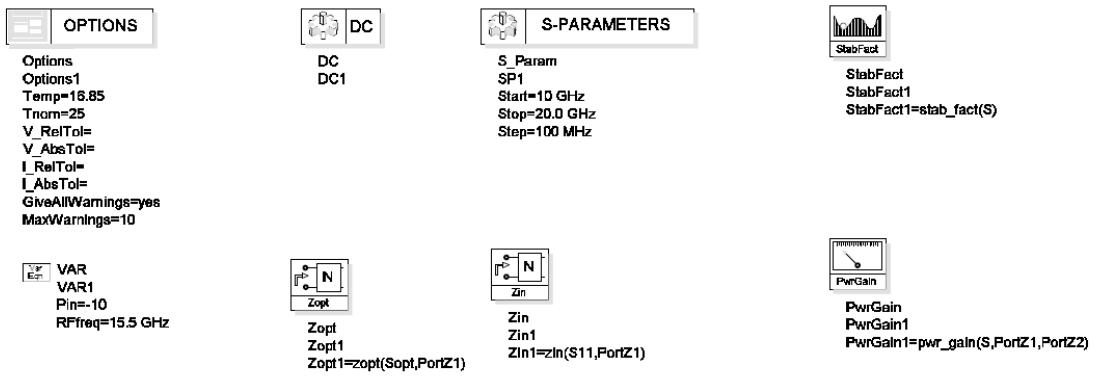


Figure 6.5 Simulation setup in ADS

Figure 6.6 LNA Gain S_{21} in dB

Figure 6.6 shows a plot with a voltage gain of the amplifier in dB in the frequency range of 12-18 GHz. The peak gain is 19.11 dB at the center frequency 15.4 GHz.

Figure 6.7 LNA noise figure in dB

Figure 6.7 shows a plot of the noise figure in dB measured at the output of the low noise amplifier for the frequency range of 12 to 18 GHz.

Figure 6.8 Stability Factor K >1

Figure 6.8 shows a plot of stability factor of the amplifier. From the above figure, It can be seen that stability factor is greater than 1 in the complete bandwidth of interest (12-18 GHz) and therefore satifies Rollett stability criteria (6.1).

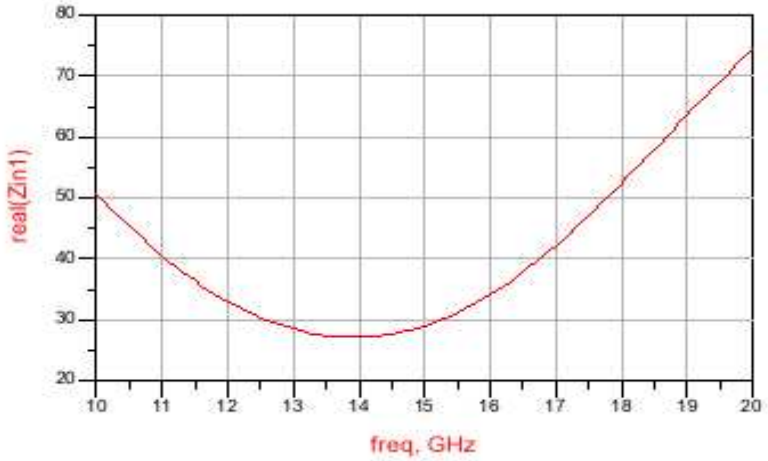


Figure 6.9 Input impedance

Figure 6.10 Output impedance

The input and the output impedance variations with the frequency of operation are plotted in figures (6.9) and (6.10). The impedance is matched to 50 ohms at the input and the output of the amplifier using an L matching network (figure 5.4).

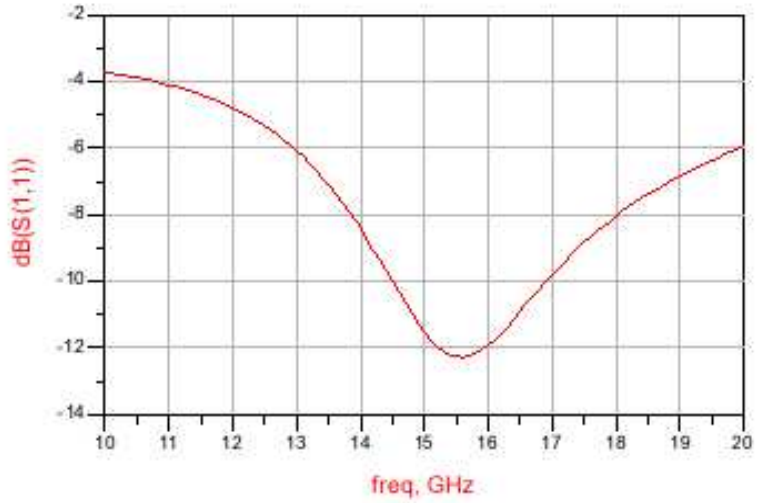


Figure 6.11 Input voltage reflection co-efficient S_{11} in dB

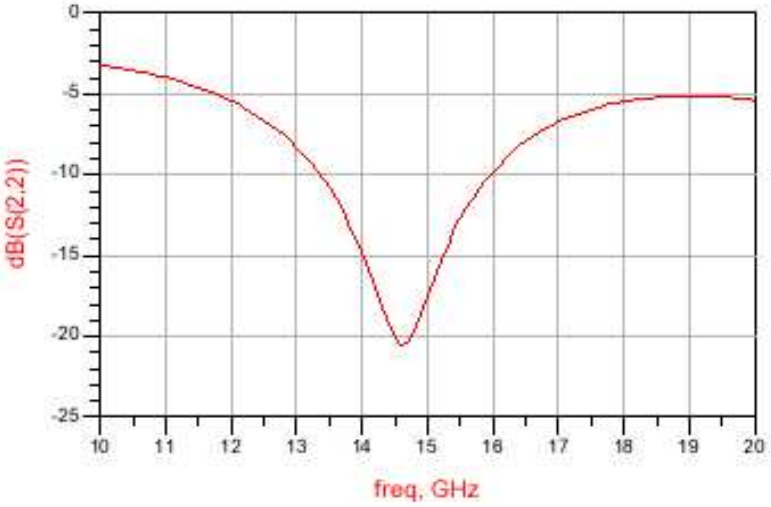


Figure 6.12 Output voltage reflection co-efficient S_{22} in dB

Figures (6.11) and (6.12) show the variation of input and output voltage reflection coefficients versus frequency. The parameters S_{11} and S_{22} are below -10 dB for a bandwidth of 1.8 GHz from 14.40 to 16.20 GHz, so this frequency range has a negligible return loss.

freq	DC.I_Probe1.i
0.0000 Hz	27.07 mA

Figure 6.13 Total Current consumption by the LNA

From figure (6.13), it can be seen that the total DC current consumed by the low noise amplifier is 27.02 mA. Therefore, total power consumption = (0.5 V) (27 mA) = 13.5 mW, where 0.5 V is the value of the power supply voltage.

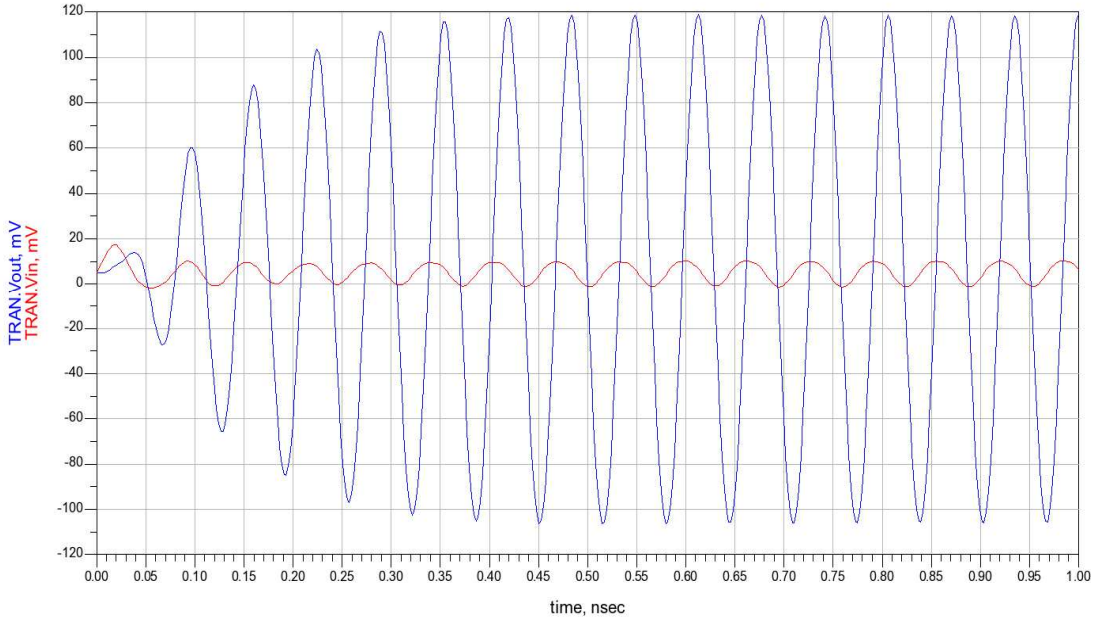


Figure 6.14 Transient analysis

Figure 6.14 shows a plot of the input and the output AC voltage waveforms. V_{in} is the input voltage in mV and V_{out} is the output voltage in mV.

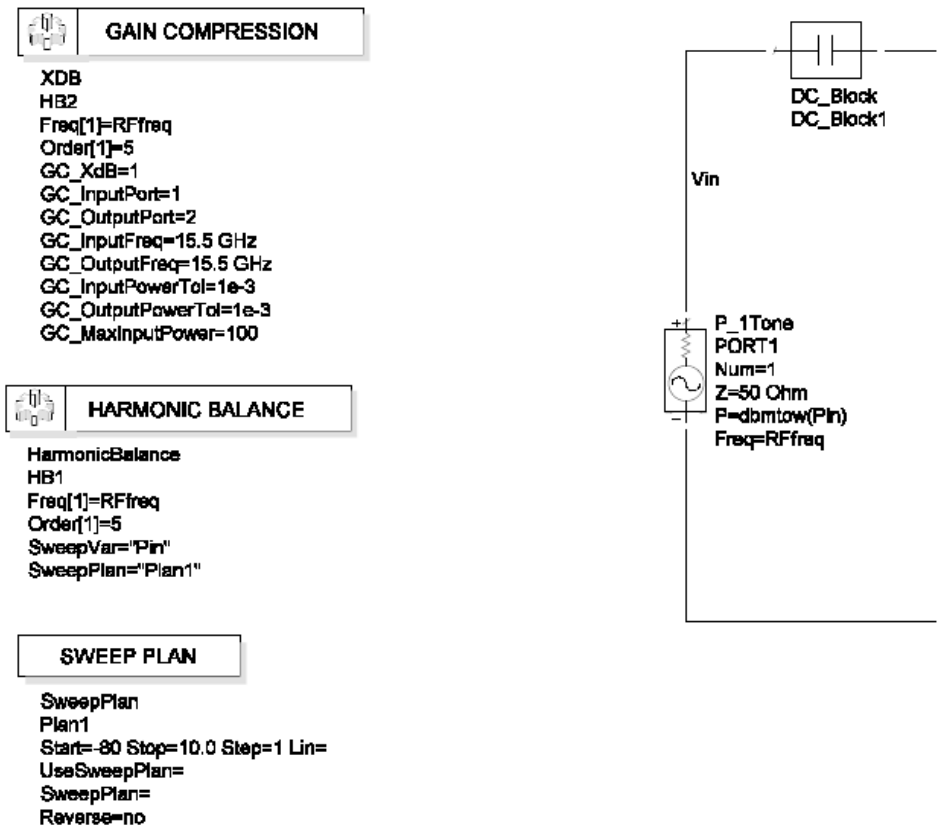


Figure 6.15 1 dB compression point simulation setup

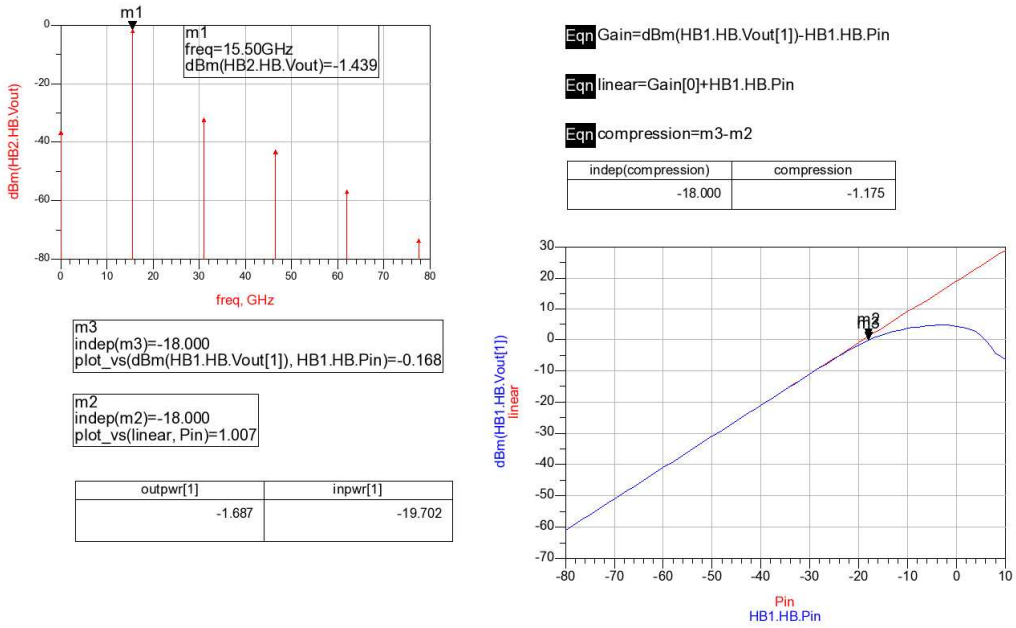
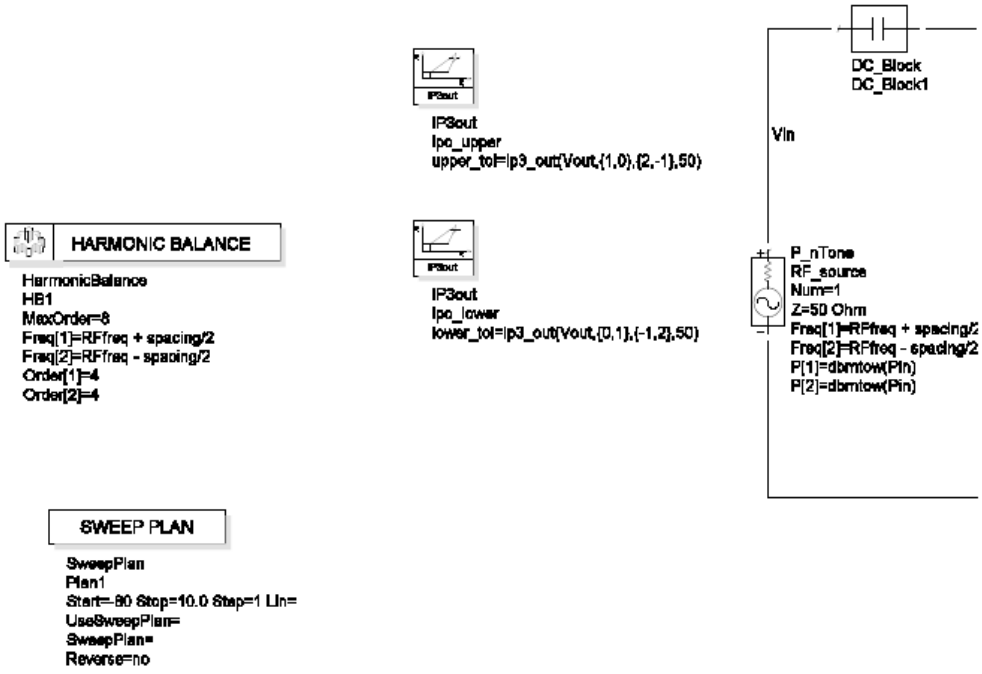


Figure 6.16 1 dB compression point and Harmonic analysis results

In the figure 6.16, the harmonic balance analysis shows the output power of the LNA decreases with the increase in the frequency of operation. Also, the 1 dB compression point for this LNA occurs when the input signal power is -18 dB. 1 dB compression point is defined as the input power at which the amplifier output power decreases by 1 dB.



lower_toi	HB.upper_toi
10.782	10.656

Figure 6.17 IIP3 measurement at 15.4 GHz

CHAPTER 7

CONCLUSIONS

A new two stage RL/RC feedback LNA architecture with parallel MOSFETs was defined, modeled and simulated with state-of-the-art standard 45 nm CMOS technology. A voltage gain of about 19 dB was well established in the frequency range 12 – 18 GHz, with a noise figure of about 2.2 dB. This LNA is capable of proper operation with a very low supply voltage of only 0.5 V. Mathematical predictions were fairly accurate and were verified with closely matched simulation results. The parasitic effects that come into the picture during layout design are taken into account (Figure 6.1) in the simulation by including RLC parasitic networks between the supply, circuit and the ground. To obtain an idea of the circuit performance degradation due to the layout parasitic effects, the simulation of the amplifier without the parasitic networks is presented in Appendix C.

A simple Impedance matching technique was used to match the amplifier terminals to the loads and the network elements were optimized to provide the best possible matching. The voltage reflection coefficients S_{11} and S_{22} are below -10 dB in the frequency range of 14.4 to 16.2 GHz. So, there is a minimal voltage reflection for about a bandwidth of 1.8 GHz around the center frequency f_c = 15 GHz. The two stage low noise amplifier is unconditionally stable over the complete 6 GHz bandwidth of interest and about 10 GHz around the center frequency.

APPENDIX A

INDUCTOR LAYOUT DESIGN TECHNIQUES THAT ENSURE THEIR PROPER OPERATION AT GHZ FREQUENCIES

One of the most challenging aspects of ultra wide band high frequency circuit and layout design is to make sure that the on chip inductors operate properly for the complete bandwidth of interest. The inductance value of an inductor used in a circuit plays an important role in determining the suitable layout design technique which ensures its proper operation in ultra wide band systems. The proper operation of other passive components in the circuit is important as well. In the GHz frequency range, it becomes more difficult to predict the proper operation of passive circuit elements.

All the feedback and load inductors used in this LNA are close to 0.22 nH. Inductors of this value can operate properly up to 60 GHz, when millimeter wave stacked inductor layout design techniques are implemented as described in [17]. This shows a comparison between different inductance values and their variation against frequency in the GHz range. It is also evident from this publication that the designed and measured values are close to within 10% for stacked inductor layout designs when measured at 40 GHz.

APPENDIX B

THE PREDICTIVE TECHNOLOGY MODEL NMOS 45 NM SPICE PARAMETER LIST

```
* PTM 45nm Metal Gate / High-K

.model  nmos  nmos level=54

+version = 4.0           binunit = 1           paramchk= 1           mobmod  = 0
+capmod  = 2             igcmod  = 1           igbmod  = 1           geomod  = 1
+diomod  = 1             rdsmod  = 0           rbodymod= 1           rgatemod= 1
+permod  = 1             acnqsmod= 0           trnqsmod= 0

+tnom    = 27            toxe    = 9e-010      toxp    = 6.5e-010    toxm    = 9e-010
+dtox    = 2.5e-010      epsrox  = 3.9         wint    = 5e-009      lint    = 2.7e-009
+ll      = 0             wl      = 0           lln     = 1           wln     = 1
+lw      = 0             ww      = 0           lwn     = 1           wwn     = 1
+lwl     = 0             wwl     = 0           xpart   = 0           toxref  = 9e-010
+dlcig   = 2.7e-009

+vth0    = 0.3423        k1      = 0.2         k2      = 0           k3      = 0
+k3b     = 0             w0      = 2.5e-006    dvt0    = 1           dvt1    = 2
+dvt2    = 0             dvt0w   = 0           dvt1w   = 0           dvt2w   = 0
+dsub    = 0.078         minv    = 0.05        voffl   = 0           dvtp0   = 1e-010
+dvtp1   = 0.1           lpe0    = 0           lpeb    = 0           xj      = 1.4e-008
+ngate   = 1e+023        ndep    = 6.5e+018    nsd     = 2e+020      phin    = 0
+cdsc    = 0             cdscb   = 0           cdscd   = 0           cit     = 0
+voff    = -0.13         nfactor = 1.9         eta0    = 0.0055      etab    = 0
+vfb     = -1.058        u0      = 0.02947     ua      = -5e-010     ub      = 1.7e-018
+uc      = 0             vsat    = 159550      a0      = 1           ags     = 0
+a1      = 0             a2      = 1           b0      = 0           b1      = 0
+keta    = 0.04          dwg     = 0           dwb     = 0           pclm    = 0.06
+pdiblc1 = 0.001         pdiblc2 = 0.001       pdiblcb = -0.005      drout   = 0.5
+pvag    = 1e-020        delta   = 0.01        pscbe1  = 2.0e+009    pscbe2  = 1e-007
+fprout  = 0.2           pdits   = 0.01        pditsd  = 0.23        pditsl  = 2300000
+rsh     = 5             rdsw    = 105         rsw     = 52.5        rdw     = 52.5
+rdswmin = 0             rdwmin  = 0           rswmin  = 0           prwg    = 0
+prwb    = 0             wr      = 1           alpha0  = 0.074       alpha1  = 0.005
+beta0   = 30            agidl   = 0.0002      bgidl   = 2.1e+009    cgidl   = 0.0002
+egidl   = 0.8           aigbacc = 0.012       bigbacc = 0.0028      cigbacc = 0.002
+nigbacc = 1             aigbinv = 0.014       bigbinv = 0.004       cigbinv = 0.004
+eigbinv = 1.1           nigbinv = 3           aigc    = 0.018029    bigc    = 0.0029
```

```
+cigc    = 0.002          aigsd   = 0.018029       bigsd   = 0.0029         cigsd   = 0.002
+nigc    = 1              poxedge = 1              pigcd   = 1              ntox    = 1
+xrcrg1  = 12             xrcrg2  = 5

+cgso    = 1e-010         cgdo    = 1e-010         cgbo    = 0              cgdl    = 7.5e-013
+cgsl    = 7.5e-013       clc     = 1e-007         cle     = 0.6            cf      = 1.1e-010
+ckappas = 0.6            ckappad = 0.6            vfbcv   = -1             acde    = 1
+moin    = 15             noff    = 1              voffcv  = 0

+kt1     = -0.154         kt11    = 0              kt2     = 0.022          ute     = -1.1
+ua1     = 1e-009         ub1     = -1e-018        uc1     = -5.6e-011      prt     = 0
+at      = 33000

+fnoimod = 1              tnoimod = 0              noia    = 6.25e+041      noib    = 3.125e+026
+noic    = 8.75e+009      em      = 41000000       af      = 1              ef      = 1
+kf      = 0              tnoia   = 1.5            tnoib   = 3.5            ntnoi   = 1

+jss     = 1.2e-006       jsws    = 2.4e-013       jswgs   = 2.4e-013       njs     = 1
+ijthsfwd= 0.1            ijthsrev= 0.1            bvs     = 10             xjbvs   = 1
+jsd     = 1.2e-006       jswd    = 2.4e-013       jswgd   = 2.4e-013       xjbvd   = 1
+pbs     = 1              cjs     = 0.0018         mjs     = 0.5            pbsws   = 1
+cjsws   = 1.2e-010       mjsws   = 0.33           cjswgs  = 2.1e-010       cjd     = 0.0018
+cjswd   = 1.2e-010       mjswd   = 0.33           pbswgd  = 1              cjswgd  = 2.1e-010
+mjswgd  = 0.33           tpb     = 0              tcj     = 0              tpbsw   = 0
+tcjsw   = 0              tpbswg  = 0              tcjswg  = 0              xtis    = 3

+dmcg    = 0              dmci    = 0              dmdg    = 0              dmcgt   = 0
+dwj     = 0              xgw     = 0              xgl     = 0

+rshg    = 0.4            gbmin   = 1e-010         rbpb    = 5              rbpd    = 15
+rbps    = 15             rbdb    = 15             rbsb    = 15             ngcon   = 1
```

APPENDIX C

SIMULATION OUTPUTS OF THE LNA WITHOUT THE RLC PARASITIC NETWORKS

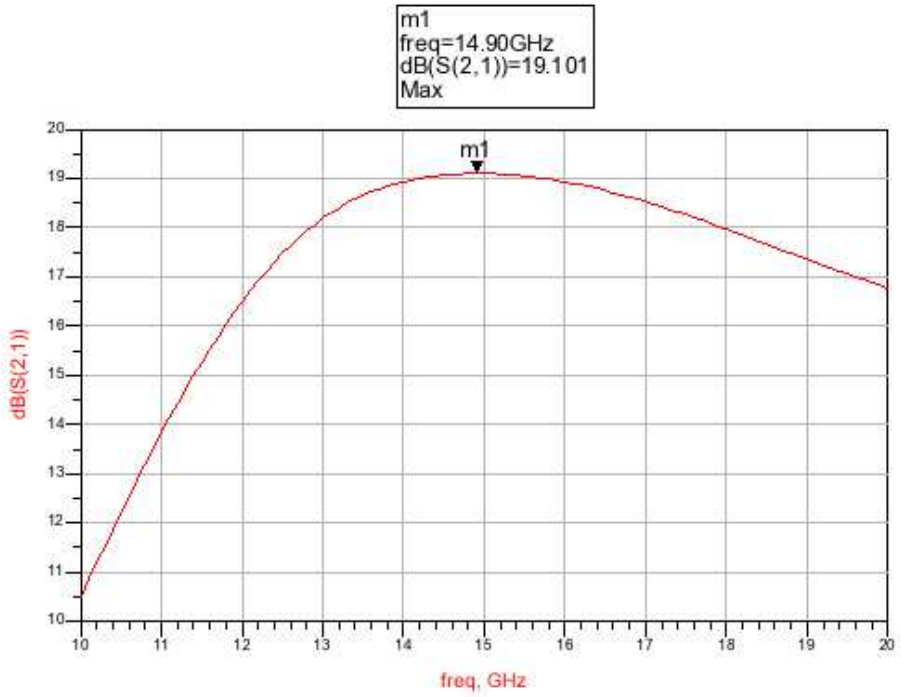


Figure C.1 Voltage gain of the LNA without the RLC parasitic networks.

From the figure C.1, the voltage gain has a relatively flat response (wider bandwidth at the maximum voltage gain) when compared to figure 6.6.

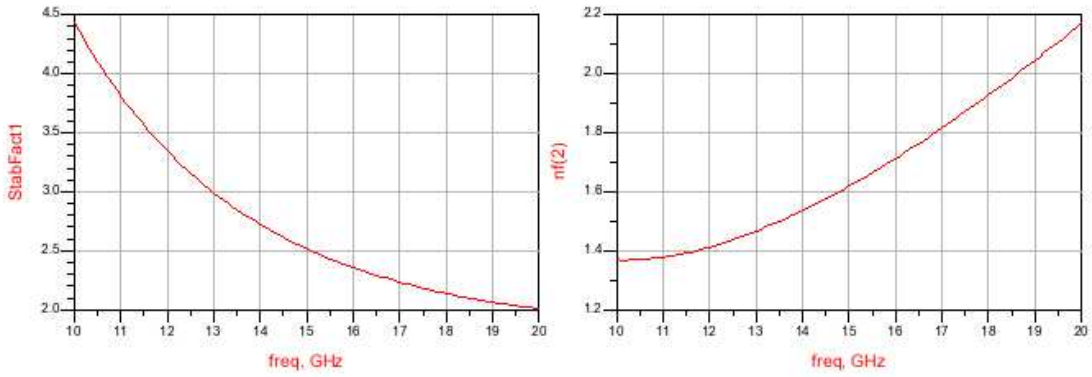


Figure C.2 The stability factor and the noise figure without the RLC parasitic networks.

From the figure C.2, the LNA seems to have better stability and noise figure as compared the figures 6.7 and 6.8.

REFERENCES

[1] Berkeley BSIM Group, *http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html.*

[2] Jung-suk goo, Stanford University, *http://www-tcad.stanford.edu/tcad/pubs/theses/goo.pdf.*, August 2001.

[3] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits,* chapter 10, Cambridge University Press, New York, NY, first edition, 1998.

[4] Behzad Razavi, *Design of Analog CMOS Integrated Circuits , chapter 7*, McGraw Hill , first edition,August 2000.

[5] Behzad Razavi, "*A 300-GHz fundamental oscillator in 65-nm CMOS technology*", IEEE symposium on VLSI circuits, pp.113-114, June 2010.

[6] W. Marshall Leach, JR. senior member IEEE, Georgia Tech University *http://users.ece.gatech.edu/mleach/papers/AnalogNoise.pdf.*

[7] Reinhold Ludwig, Gene Bogdanov, *RFCircuit Design: Theory and Applications*, chapter 9, Pearson Education Inc, New Jersy, second edition, 2009.

[8] Paul R. Gray, Paul J. Hurst, Robert G. Meyer, Stephen H. Lewis, *Analysis and Design of Analog Integrated Circuits*, chapter 8, Wiley India Pvt Limited, fourth edition, January 2008.

[9] RF Circuit Design Software, *http://www-ee.uta.edu/online/adavis/rfsoftware/index.htm.*

[10] Norman Dye, Helge Granberg, Larry Leighton, *Radio Frequency Transistors: Principles and Practical Applications,* chapter 13, Newnes, second edition, 2001.

[11] Tienyu Chang, Jinghong Chen, Riggie L.A;. Lin J, *"ESD Protected Wideband CMOS LNAs Using Modified Resistive Feedback Techniques With Chip-on Board Packaging"*, IEEE Transactions on Microwave Theory and Techniques, volume 56, issue 8, pp 1817-1826, July 2008.

[12] William Liu, *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*, John Wiley & Sons, New York, 2001.

[13] Cheng Yuhua; Hu, Chenming, *MOSFET Modeling BSIM3 User's Guide,* Kluwer Academic Publishers, third reprint, Massachusetts, 2001.

[14] Galup-Montoro and Schneider, *MOSFET Modeling For Circuit Analysis and Design,* World Scientific Publishing Co. pvt limited, Singapore.

[15] T. Ytterdal, Y. Cheng and T.A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*, John Wiley and Sons, Ltd third reprint, 2003.

[16] Qiang Li, Yue Ping Zhang, *"A 1.5 V 2-9.6 Ghz Inductorless Low-Noise Amplifier in 0.13-um CMOS"*, IEEE Transactions on Microwave Theory and Techniques, volume 55, issue 10, pp 2015-2023, October 2007.

[17] Dickson T.O; Lacroix, M -A., Boret S., Gloria D., Beerkens R., Voingescu S. P., *"30-100GHz Inductors and Transformers for Millimeter-wave(Bi)CMOS Integrated Circuits"* IEEE Transactions on Microwave Theory and Techniques, volume 53, issue 1, pp 123-133, January 2005.

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