FABRICATION OF MICROPATTERNS ON 3D SURFACES AND GENERATION OF LINKED ZnO NANOWIRES

by

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Finally, I dedicate this dissertation to my beautiful wife, Yana. I love you.

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ABSTRACT

FABRICATION OF MICROPATTERNS ON 3D SURFACES AND

GENERATION OF LINKED ZnO NANOWIRES

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Conventional lithographic approaches are good at fabricating structures on the top surfaces of substrates. They are not suited for 3D surface patterning due to the fact that vertical radiation exposure is employed to transfer patterns. In the meanwhile, patterns generated on 3D surfaces, such as the vertical sidewalls of silicon channels and the irregular surfaces of glass micropipettes may provide valuable applications in microfluidics, 3D circuits, bioengineering and so on. In this work, we developed new approaches to produce metal micropatterns on the vertical sidewalls of silicon channels as well as to fabricate two separated metal microlines on the tips of glass micropipettes. Using these approaches 10 μm Au dots and 20-μm-wide Au lines have been successfully produced on the sidewalls and two separated microlines have been fabricated on the outer surface of a glass micropipette with tip size down to 5 μm.

In the meantime, it was found in our experiments that ZnO nanowires may contact each other and become linked during hydrothermal growth. This phenomenon might be useful for building novel nanostructures. Accordingly, we monitored the process of nanowires growth and explained the formations of three types of linked nanowires.

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CHAPTER 1

INTRODUCTION AND DISSERTATION OVERVIEW

1.1 Introduction

Current micro/nanosystems mainly have a planar form. One layer of structures is built on the top surface of another layer of fabricated features. Multiple layers of these structures are stacked together to form numerous devices on a common substrate. Accordingly, current micro/nanofabrication skills are mainly focusing on producing patterns on flat surfaces [1-4].

On the other hand, when patterns are generated on the sidewalls, some good applications can be envisioned. The sidewall patterns could be used to build 3D circuits that might be required in electronic devices. Such a circuit might extend across a concave microstructure (for example, a channel) from one side of the microstructure to the opposite side via the sidewalls. In addition, nanowires and nanotubes are usually synthesized along the vertical directions through top templates. Additional electrical fields [5-9] or fluidic channels [10, 11], for instance, are needed to have the horizontal alignment of these 1D nanostructures. Consequently, they could be integrated into planar devices, making used of their specific mechanical or electrical properties. The sidewall patterns generated on a planar device might serve as templates to direct horizontal synthesis of nanowires or nanotubes such that they could be directly incorporated into the planar device, reducing the fabrication effort. In another case, two separate lines fabricated on a glass micropipette could serve as electrodes or interconnects [12]. The electrodes might be applied to record or stimulate neurons, and might also be employed to generate an electrical field to control drug delivery [13, 14]. The interconnects could be used to connect a power supply device with a conductive material coated on the end of the tip. After the power is supplied, this conducting material would provide

resistive heating. Accordingly, the micropipette could function as a heater to provide local heating [15].

Nevertheless, current photolithographic approaches, such as ultra-violet (UV), electron-beam, X-ray, and ion-beam, employ vertical radiation exposure to transfer patterns, not suited to patterning sidewalls. Existing three major non-photolithographic approaches use sharp tips (dip-pen [16, 17]), soft polydimethylsiloxane (PDMS) masters (soft lithography [18, 19]) or hard molds of flat bottom surfaces (nanoimprint lithography [20, 21]) to pattern the flat top surfaces. They are not good at transferring patterns to the sidewalls of microstructures either. In addition, an interesting approach was presented in [18] to fabricate 3D metal lines. In this approach, photoresist lines were first generated inside microchannels using UV lithography, and vertical metal lines were then fabricated on the channel sidewalls using the photoresist structures as a mask. This approach is good at generating lines on a sidewall. However, it might not be suitable to make dots or horizontal lines on sidewalls since the corresponding masking patterns (i.e., photoresist patterns) could not be fabricated on the sidewalls using UV lithography. Another technique to produce 3D interconnects was introduced in [19] based on diffraction of light by phase gratings. The phase gratings were incorporated into the photomask, resulting in inclined UV exposure. This technique is accurate in patterning. However, it is a challenge to fabricate the photomask with phase gratings. Previously, patterns have been fabricated on the sidewalls of polymer microchannels by our group using a hot-embossing approach [22, 23]. This approach requires the substrate material be a thermal polymer. It does not apply to the case when the substrate material is, for example, silicon, which is rigid. On the other hand, silicon is the most commonly used material in the fields of integrated circuits and MEMS.

Furthermore, it is also important to generate patterns on irregular surfaces, such as the sharp tip of a micropipette. A glass micropipette consists of a straight tube and a curved tip. The straight tube of a micropipette has a cylindrical outer surface. It is relatively easy to generate metal lines on this tube due to its relatively bigger size, usually 1 mm in diameter. Straight metal lines that are extended along the micropipette direction could be directly fabricated, for example,

using UV lithography. Coiling metal lines which are perpendicular to the micropipette axis, might be produced, for instance, employing microcontact approach of soft lithography [24]. In [24], a metal-coated straight tube was rolled on an array of ink-coated PDMS microlines. Through this rolling process, the ink was transferred to the tube, forming coiling microlines on the outer surface of the tube. With these ink microlines as a mask, coiling metal lines were further generated on the straight tube after wet etch of the metal coating. On the other hand, it still remains a challenge to generate metal lines on the curved tip of a glass micropipette. This tip has a conic shape and is curved along its longitudinal direction. Its outer surface is not developable. That is, a flat PDMS membrane could not be smoothly wrapped to cover every point on the tip surface. Therefore, the microcontact approach could not be applied to generate desired patterns on it. Conventional lithographic (UV, electron-beam, and X-ray) are also not suited for producing patterns on the curved tip, since they would encounter either alignment or intimate contact problems.

Therefore, in this work, we explored the possibilities of economical and efficient approaches to produce metal micropatterns on the sidewalls of silicon channels and two separated metal microlines on the tips of glass micropipettes.

Meanwhile, ZnO nanowires have been widely investigated for applications in optoelectronics, sensors, power generator, FET devices [25-35]. Most of these works focused on the process of synthesizing and utilizing ZnO nanowires. Although many efforts have been given to this area by a lot of researchers, there are still some issues in the field have not been discovered or discussed. For example, in our experiments, ZnO nanowires grow toward each other might link together. An intersection between the nanowires was formed. This phenomenon might be applied for building novel nanostructures. For this motivation, in this work, we also tried to understand the mechanism of the linked nanowires by monitoring the process of nanowire growth.

1.2 Dissertation Overview

Chapter 2 reviewed the current lithographic approaches that might be used to produce micropatterns on 3D surfaces. The shortcomings of each approach in its capability to generate patterns on vertical sidewalls of silicon channels and the tips of glass micropipettes were discussed.

Chapter 3e discussed two approaches to fabricate Au micropatterns on vertical sidewalls of silicon channels using a PDMS membrane as shadow mask. The first approach focused on producing micropatterns on a single sidewall of a silicon substrate. The second approach was good for fabricating micropatterns on the two sidewalls of a silicon channel.

Chapter 4 illustrated two new methods to generate two separated metal microlines from the straight section of a glass micropipette to the curved tip.

Chapter 5 demonstrated the formation process of linked ZnO nanowires during hydrothermal growth. SEM images were taken at different moments of the growth. The results were compared and analyzed.

Chapter 6 summarized and concluded this work.

CHAPTER 2

LITHOGRAPHIC TECHNIQUES REVIEW FOR 3D SURFACE PATTERNING

2.1 Introduction

Various lithographic techniques have been developed for 2D patterning, such as photolithography, atomic force microscope (AFM) and soft lithography. In this chapter, these main lithographic techniques are introduced, and their capabilities for 3D surface patterning are also discussed.

2.2 Photolithography

Photolithography in MEMS context is typically the transfer of patterns to a photosensitive material by selective exposure to a radiation source such as UV light using a photomask [36]. Photosensitive material, called photoresist, is an organic substance, which is sensitive to light. It has two kinds: positive and negative. A negative photoresist becomes less soluble in developer solution after exposure, while a positive photoresist becomes more soluble in developer solution after exposure [1]. Examples of positive photoresist include Shipley-S1800 series and AZ9260. SU-8 is one of the most popular used negative photoresist. Typical procedures of photolithography are shown in Fig. 2.1.

Traditional photolithography usually focuses on producing patterns on planar surfaces with these surfaces perpendicular to the exposure light, as in Fig 2.2. Due to the property of light propagation, which is straight in its path, surfaces that parallel to the light cannot be exposed. Therefore, traditional photolithographic technique is not suitable to pattern vertical sidewalls. For sloped sidewalls, it is possible to fabricate patterns on them using traditional photolithographic approach. However, several challenges still need to overcome. The first challenge is to obtain a uniform layer of photoresist. Spin coating is the most commonly used

method to obtain a uniform layer of photoresist for planar substrates. However, it is not possible to obtain the same result on a 3D surface as on a planar surface. As shown in Fig. 2.3, the force balance at different point of the surface is not the same, which leads to thickness variance. A simple model was further set up using FLUENT to visualize photoresist spreading on a substrate with 3D structures, Fig. 2.4. It can be observed that the thickness is different on the sidewalls that opposite to each other. The photoresist is thicker on the sidewalls that facing the spinning axis than the sidewalls that facing outward the spinning axis. For the corners, less photoresist is left on the top of the channel than those at the bottom. The second challenge is obtaining relative uniform amount of exposure dose. For two openings of the same size on the mask, the projected area on the sidewall is larger than the area on the planar surface, as shown in Fig. 2.5. It is difficult to find an appropriate amount of exposure dose that may crosslink the photoresist on these different locations, besides the thickness of photoresist at those locations is different, which brings in more challenges. Therefore, it is necessary to find substitute approaches for 3D surface patterning.

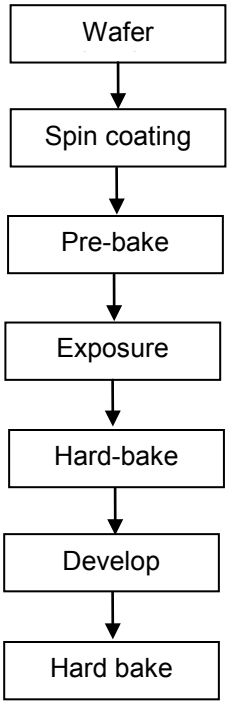


Figure 2.1 Steps of photolithographic process.

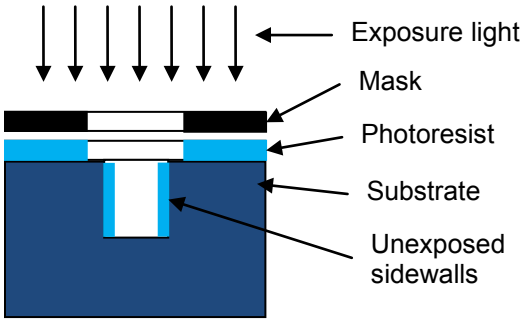


Figure 2.2 Exposure direction in traditional photolithography.

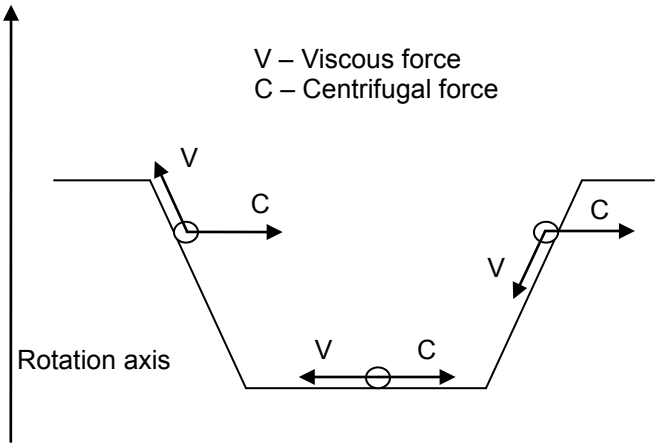


Figure 2.3 Force balance of photoresist on a 3D surface using spin coating (cross-section view).

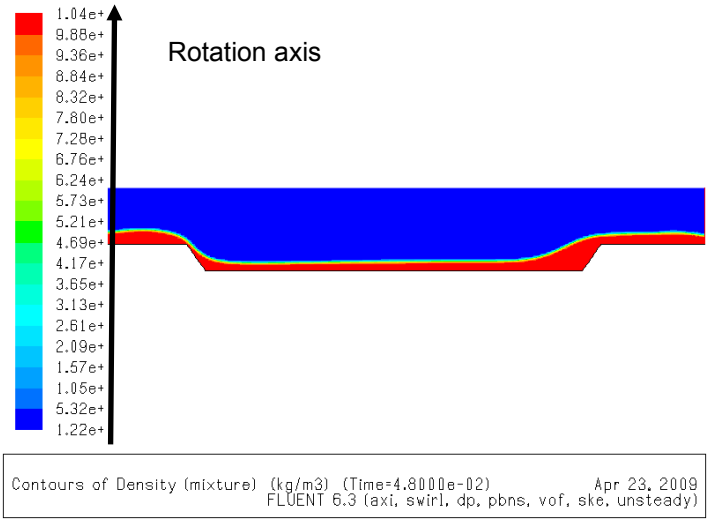


Figure 2.4 2D simulation of photoresist spreading on a 3D surface using FLUENT.

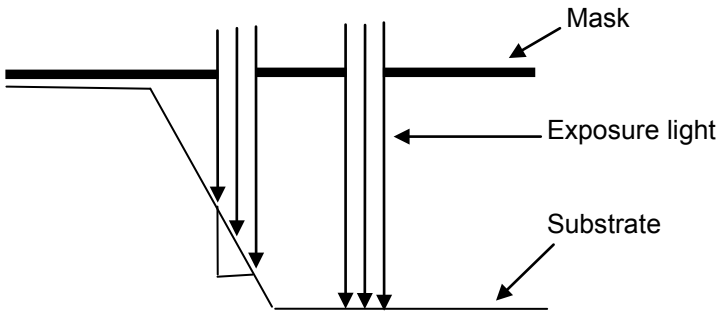


Figure 2.5 Exposed areas on the sloped sidewall and on the planar surface.

An interesting approach was presented in [37]. In this report, Al lines across 60-μm-deep cavities were fabricated using UV lithography with SU-8 as the photoresist. Unlike traditional lithographic approach, which needs a uniform and thin layer of photoresist to cover the substrate, in this report, SU-8 filled up the aluminum coated channel by spin coating. Followed by UV exposure and development, produced SU-8 patterns function as protection layer during aluminum etch, Fig. 2.6. Process of coating SU-8 was one of the key factors to obtain desired results. SU-8 viscosities, spin speed, channel size, pre-baking temperature and time were considered and tested to improve the cavity filling and step coverage. Direct exposure to produce line patterns on sloped sidewalls was investigated in [38-43]. However, these approaches might not suited for fabricating dots or horizontal lines on the sidewalls since the corresponding masking patterns (i.e., photoresist patterns) could not be fabricated on the sidewalls using UV lithography. To overcome this shortcoming, altered photolithographic approaches were developed by researchers to generate patterns on sidewalls, such as by inclined illumination or diffractive techniques [44].

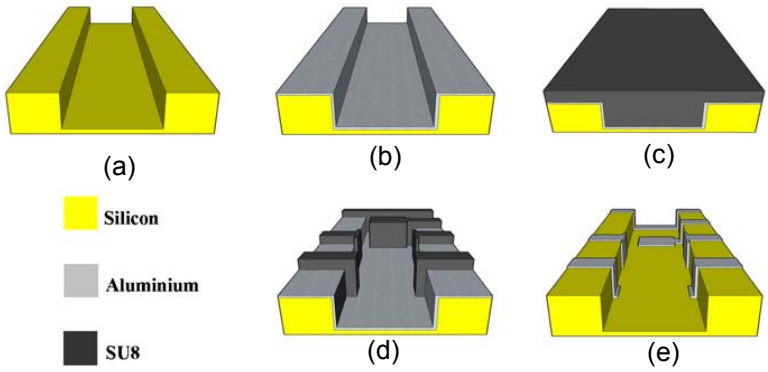


Figure 2.6 Schematic process flow of producing aluminum lines across a channel by direct exposure (a) cavity etch, (b) aluminum deposition, (c) SU-8 coating, (d) SU-8 exposure and development, (e) aluminum etch and SU-8 removal [37].

2.2.1. Inclined Illumination

Inclined illumination, also called inclined lithography. It is achieved by exposing the photoresist with exposure light under an inclined angle with the substrate using a conventional photo mask [44], as in Fig. 2.7. The exposure light is no longer vertical to the substrate. In such a way, the exposure light may reach the sidewall to be exposed. The stage that holds the substrate is usually rotated to form an inclined angle with the exposure light. Inclined lithography has been used in [45, 46] to fabricate 3D inclined structures applying thick photoresist. A simple setup of inclined lithography was given in Fig. 2.8 [45]. The first report of inclined lithography used a thick positive photoresist. Since the negative thick photoresist SU-8 was developed, it has been used in most of the work that used inclined lithography [45-47]. However, current efforts in inclined lithography are mostly given to the fabrication of 3D structures on a planar surface.

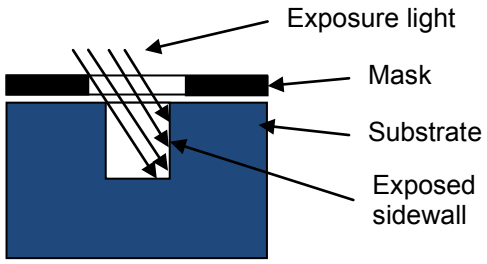


Figure 2.7 Inclined lithography.

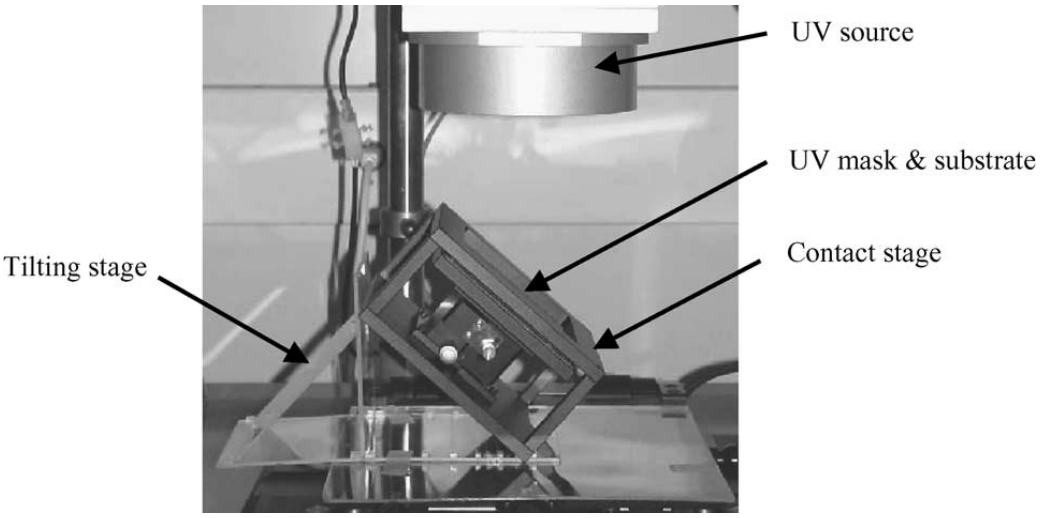


Figure 2.8 Basic setup of inclined UV lithography.

2.2.2. Diffraction Lithography

Diffraction lithography is realized by the diffraction of light when it passing through the phase gratings in the mask, Fig. 2.9. The phase gratings are incorporated into the photomask at discrete locations. They redirect the light towards the sidewalls when the photomask is exposed at perpendicular incidence [48]. However, it is time consuming and not economical to fabricate this kind of masks.

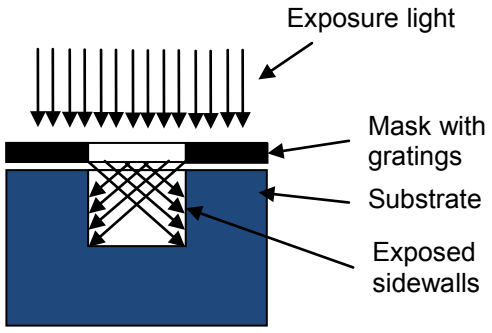


Figure 2.9 Diffractive photolithography.

For cylindrical substrate patterning, UV lithography was used in [49] with a flexible mask. Projection lithography has been applied to produce patterns on them [50, 51]. The reticle was scanned in the direction perpendicular to the rotated sample axis. Patterns on conic surfaces were also investigated in [51] with sample tilted according to the cone angle to make

the exposed surface parallel to the mask. Besides traditional UV lithography, X-Ray [52] and laser-beam [53, 54] lithographic techniques were also employed for the patterning of cylindrical substrates. By applying photolithographic approach, patterns can be precisely produced on the cylindrical surfaces. However, it is time consuming for conducting alignment, especially for the tips of glass micropipette, which are not fit into traditional substrate holder of the mask aligner.

2.3 AFM-Based Lithography

AFM is one of the foremost tools for imaging, measuring, and manipulating mater at the nanoscale. It consists of a cantilever, typically made of silicon or silicon nitride, with a sharp tip (probe) at its end that is used to scan the specimen surface. Upon proximity of the tip with the specimen surface, force is produced and bended the cantilever. The deflection of the cantilever may be detected through optical, capacitive, or piezoresistive approaches [55]. Setup of AFM using an optical detection method is shown in Fig. 2.10.

AFM lithography functions as ploughing, which employs the tip to scratch and remove the resist on the substrate. It has the advantages of precise alignment, nondamaging definition process compared to electron- or ion-beam, and absence of additional processing steps, such as the development of a photoresist [56].

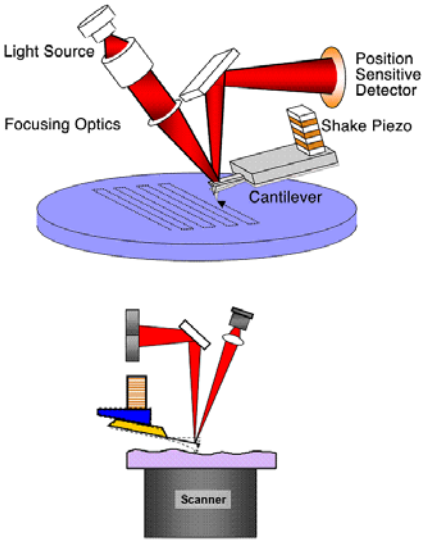


Figure 2.10 Setup of an AFM using an optical sensing approach.

AFM lithography can be applied in varies ways, such as fabrication of nanochannels within a poly (methyl methacrylate) (PMMA) layer. These channels were used in electrochemical synthesis of polypyrrole nanowires. In [57], AFM lithography was applied to make local anodic oxidation of surfaces through non-contact mode. DC voltage pulsed between tip and sample oxidized the Al that has been deposited on a SOI wafer. Al in the scanning path was oxidized and provided as mask for further silicon processing. Non-oxidized Al was removed through wet etch.

AFM is traditionally employed for planar surface characterization. It is difficult to use AFM to scan over vertical surfaces of 3D structures [58]. Attempts to overcome this limitation include tilted sample, and tilted tip [59, 60]. In the approach of tilted tip, the tip was pre-set at a certain angle from the horizontal direction, and approaches the sample non-vertically. Under-cuts and vertical sidewall shapes have been measured using a tilted AFM tip in [60]. However, the working distance of AFM in vertical direction is limited to 10-20 μm. That is AFM cannot be used to characterize patterns that have steps more than 20 μm high. Besides, the serial working mode of AFM makes it extremely time consuming for patterning.

2.4 Soft Lithography

Soft lithography refers to a family of techniques to fabricate or replicate structures using elastomeric stamps, molds, and conformable photomasks. It includes: microcontact printing, replica molding, microtransfer molding, micromolding in capillaries and solvent-assisted molding [18]. In soft lithography, an elastomeric stamp with patterned relief structures on its surface is used to generate patterns and structures with feature sizes ranging from 30 nm to 100 μm [18].

Typical processes of soft lithography include: 1. Etch desired patterns onto a substrate (usually silicon). 2. Form the stamp (usually PDMS) by molding using the patterns etched on the substrate. 3. Ink the stamp by placing it in the ink solution. 4. Bring the stamp into contact with the substrate and transfer ink molecules onto the substrate (Fig. 2.11). Soft lithography has been widely used to obtain patterns on planar substrates [61-65]. In [66, 67], soft lithography was also applied for the patterning of cylindrical surfaces. Yet the stencil used in soft lithography

is usually thick. It cannot be bended naturally to follow the shape change of the vertical step, or the shape of the fragile tip of the glass micropipette. Besides, the stencil should be placed on the target substrate at one time. Further adjustment may destroy the patterns.

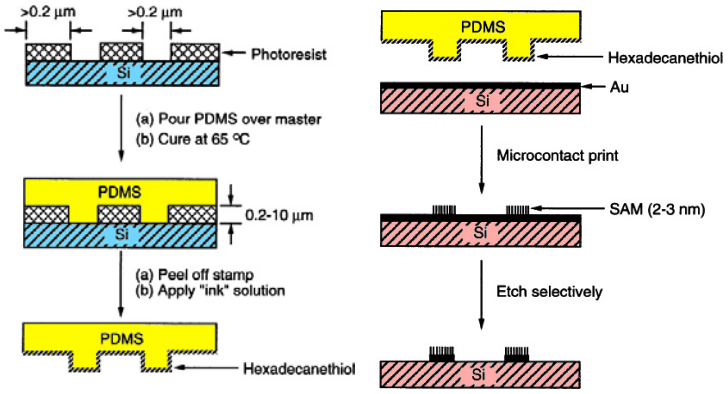


Figure 2.11 Procedures of soft lithography.

2.5 Summary

In this chapter, main approaches that could be potentially used for 3D surfaces patterning were briefly reviewed. Among the lithographic approaches introduced above, photolithography and AFM approaches are not cost-effective. For soft lithography, the thickness of the stencil is large, which makes it hard to bend and not flexible enough for 3D surface patterning. Therefore, it is necessary to explore new approaches that both time and economical effective for producing patterns on vertical sidewalls and the outer surfaces of glass micropipettes.

CHAPTER 3

FABRICATION OF AU MICROPATTERNS ON VERTICAL SILICON SIDEWALLS

3.1 Introduction

In this chapter, two approaches were introduced to generate patterns on a single and/or two vertical sidewalls of a silicon channel, respectively, using PDMS membranes as shadow masks. PDMS membrane with hollow structures was chosen as the shadow mask mainly because of its capability of bonding to a silicon substrate naturally. This eliminated the use of any extra bonding method.

In the first approach, a thin PDMS membrane with hollow structures was first placed against a silicon sidewall. A layer of Au was then thermally deposited on the substrate using the PDMS membrane as shadow mask. Finally, after removal of the PDMS membrane, Au patterns were left on the silicon sidewall. Using this method, we have successfully produced 10 μm Au dots and 20-μm-wide Au lines on vertical silicon sidewalls. In the second approach, a thin PDMS membrane with hollow structures was placed over a silicon channel. Au films were coated on the substrate through two processes of thermal evaporation using the PDMS membrane as a shadow mask. In these two processes, the substrate was tilted towards the Au source to ensure that Au was coated on either sidewall. Finally, after the removal of this PDMS membrane, Au patterns were generated on the channel sidewalls. 3D geometric models were also set up for the second approach. Based on the understanding gained from these geometric models, we then applied the approach to produce 10 μm Au dots and 20-μm-wide Au lines, respectively, on two sidewalls of a silicon microchannel.

Shadow mask technology is usually used in the case that the materials to be patterned are not compatible with traditional lithographic processes, such as organic materials [68-70], and also in the case that substrates have already had fragile and delicate patterns, such as

electronic devices or micro-machined structures [71, 72]. Further lithographic processes might damage those devices or structures.

Currently shadow mask technique is usually used for 2D patterning [68-71, 73]. In addition to applying shadow mask technique for 2D patterning, there are also reports of employing shadow effect for 3D patterning. By applying shadow-mask technique, electrical wafer feed-through was fabricated in [74]. A simple equation to calculate the enlargement of fabricated patterns on planar surface based on the geometry of evaporation equipments was given. Metal patterns on a tip of AFM was generated [75]. 10 nm scale devices were directly evaporated on the curved surface of the AFM tip. Combining plasma treatment, self-assembled monolayer coating and contact displacement electroless plating, line patterns were generated on both sloped sidewall and nearly vertical sidewall in [76] by using suspended silicon dioxide structures as shadow mask. In addition, 3D shadow masks made of silicon were developed in [77] for patterning deeply recessed surfaces for increased patterning resolution. However, these 3D patterning works using shadow mask mainly focus on fabricating patterns on sloped sidewalls. The potential of using shadow mask technique to generate patterns on vertical sidewalls has not been well developed.

Shadow masks are usually made of rigid materials [74, 77, 78], such as silicon, which needs complicated fabrication processes, including dry etch or wet etch. Besides, current applications of shadow mask technology on 3D surface patterning mainly focus on fabricating lines, which could function as interconnects. The possibility of generating other patterns, such as dots, has not been explored yet. Therefore, in this work, we adopted PDMS membranes as shadow mask, and explored the feasibility of fabricating not only vertical lines, but also an array of dots on vertical sidewalls of a silicon channel. For this purpose, we also developed 3D geometric models to direct experimental conduction in the second approach.

3.2 Generation of Au Micropatterns on a Single Sidewall of a Silicon Substrate

3.2.1 Experimental Procedures

Taking the generation of Au microdots on a vertical silicon sidewall as an example, the fabrication procedure in the developed approach involved four steps (Fig. 3.1): (1) prepare a substrate with a vertical sidewall through anisotropic potassium hydroxide (KOH) etch of a <110> silicon wafer (Fig. 3.1a); (2) fabricate a thin PDMS membrane with through-holes and place it over the vertical sidewall (Fig. 3.1b); (3) thermally deposit a layer of Au on the silicon sidewall (Fig. 3.1c); and (4) remove the PDMS membrane from the substrate, completing the generation of Au patterns on the silicon sidewall (Fig. 3.1d).

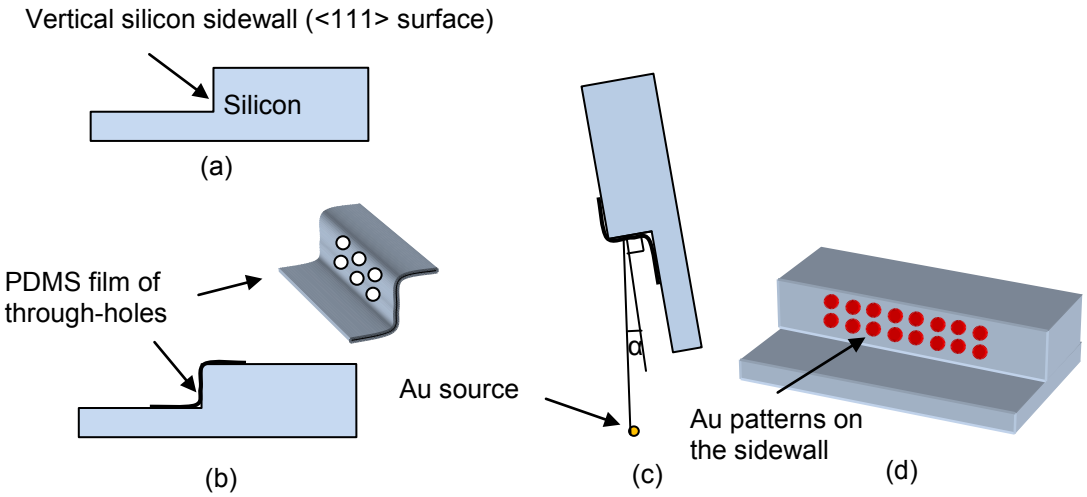


Figure 3.1 Schematics of the fabrication procedure: (a) fabricate a silicon structure with a vertical sidewall, (b) place a PDMS membrane across the silicon sidewall, (c) generate a thin film of Au using thermal evaporation, and (d) remove the PDMS membrane, completing the generation of Au patterns on the silicon sidewall.

3.2.1.1 Substrate Preparation by KOH Wet Etch

In the first step, a vertical silicon sidewall was obtained using KOH etch. KOH solution is prepared by dissolving KOH pellets into DI water and heating up to a certain temperature. KOH pellets are added to DI water slowly and stirred the solution with a Teflon coated magnetic bar at the same time. The dissolution of KOH in water produces heat, and gets the solution warms up quickly. Wait till the temperature of the solution stabilized at operation temperature

before put the sample into the solution for etch. There are several factors that affect the etch rate, such as crystallographic orientation of silicon, concentration of the solution, operation temperature, and concentration of doping in silicon. Because potassium ion (K+) is an extremely fast diffusing metal alkali metal ion, it is extremely important that do not let it contaminate the metal ion sensitive processes or structures. For our case, since we are just interested in the etched structures, metal ion is compatible with our processes. Otherwise, dry etch may replace KOH etch to obtain silicon channels.

The doping concentration of the silicon to be etched may impact etch rate strongly. If the boron doping concentration exceeds 10^{19} cm^{-3}, boron doped silicon forms borosilicate glass on the surface may acts as etch stop.

Among all factors that affect etch rate, temperature should be noticed particularly, since once concentration of the solution and the etch target were fixed, temperature becomes the only controllable factor that may affect the etch rate. Besides, temperature also relates to the surface roughness of etched results. Fig. 3.2 shows the relations between etch rate and operation temperature for <110> silicon wafer. It can be observed that etch rate increases with enhanced temperature. Meanwhile, higher concentration leads to slower etch rate. Such as at 70 ^{o}C, for 30% solution, the etch rate is around 65 μm/hr; for 40% solution, the etch rate is around 55 μm/hr; and for 50% solution, the etch rate decreases to 40 μm/hr. However, the concentration is not the less the better. Experimentation has found that solutions less than 30% KOH yields rough etch for <110> silicon etch [79]. To avoid the possibility of resulted rough etch, in this work, a 40% KOH solution was chosen for etch.

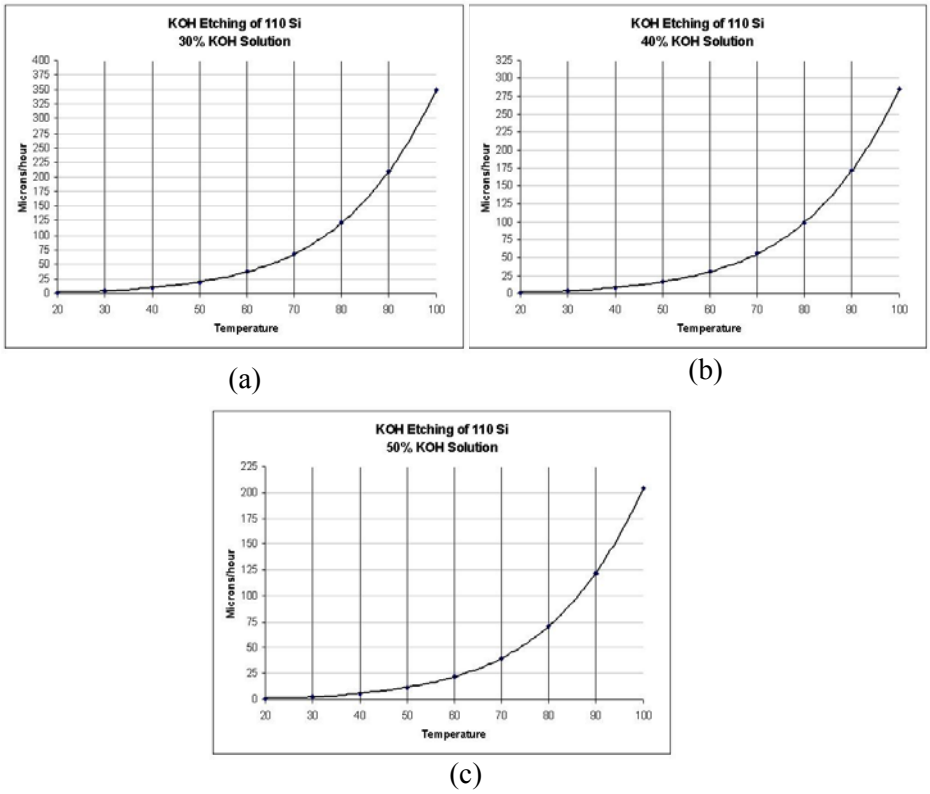


Figure 3.2 KOH etch rate vs. temperature for solution concentration at (a) 30%, (b) 40% and (c) 50% [79].

Anisotropic etch was obtained in <110> silicon wafer due to high selectivity of etch rates between <110> and <111> crystal planes in alkaline etchants. Along the directions, respectively, perpendicular to these two planes, the ratios of the corresponding etch rates range between 180:1 and 200:1 [79]. As in Fig. 3.3, a trench is formed on <110> wafer in KOH etch. The etch is first performs at the rate of <110>, after reaching an apex, etch rate slows down and at the rate of projected rate of <311> plane [80]. Relations between etch rates, and time to reach an apex can be expressed through equations 3.1-3.3.

$$R_{<110>} > R_{<311>} \cos\alpha \tag{3.1}$$

$$t_{apex} = \frac{w_{channel} \tan\alpha}{2(R_{<100>} - R_{<311>} \cos\alpha)} \tag{3.2}$$

$$d_{apex} = t_{apex} R_{<110>} \tag{3.3}$$

where, R represents the etch rate in according orientation, α is the angle between <110> and <311> planes, $w_{channel}$ is the width of the channel, t_{apex} is the time to reach the apex, and d_{apex} is the depth of the apex that is first formed.

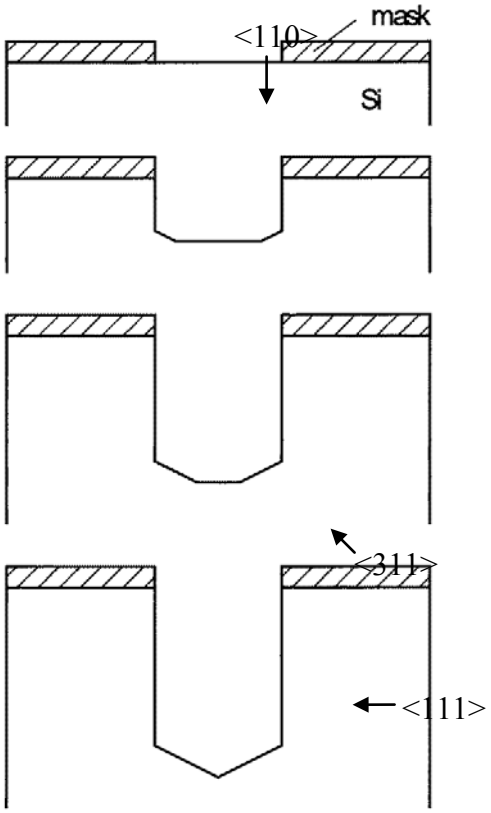


Figure 3.3 Development of the channel cross-section until an apex forms in KOH for <110> silicon wafer [80].

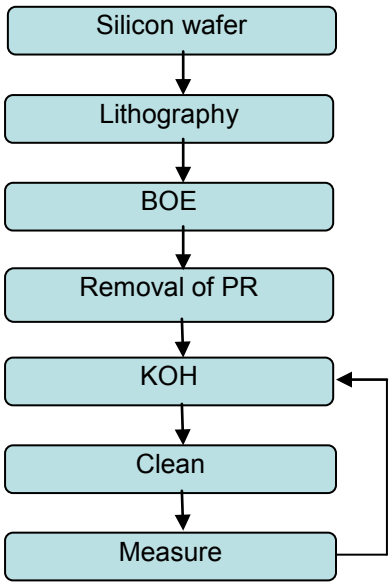


Figure 3.4 Procedures of KOH etch.

The operation procedures of KOH etch is shown in Fig. 3.4. Before the KOH etch, a 1-μm-thick film of SiO_2 on the <110> silicon wafer was patterned with straight lines using UV lithography and buffered oxide etch (BOE). During the UV lithography, the line patterns on the mask should be aligned parallel to the major flat of the <110> silicon wafer. The patterned SiO_2 layer was then employed as a mask during the KOH etch of the silicon wafer. In our experiments, the silicon wafer was etched using a 40% KOH solution at 70 ^{o}C. After the KOH etch, the SiO_2 layer was removed employing BOE. Fig. 3.5 gives a representative sidewall that was fabricated. It can be observed that the <311> and bottom <110> surfaces were rough after the KOH etch, while the vertical <111> surface and the top <110> surface were flat and smooth. This work focuses on the generation of good patterns on the vertical silicon sidewalls, i.e., on the <111> surfaces. Therefore, the roughness on the bottom <110> and <311> surfaces did not affect the testing results. On the other hand, if needed, a dry-etch approach can be adopted to generate silicon structures. This approach employs a technique of deep reactive ion etch, making both side and bottom surfaces of the silicon structures relatively smooth [81].

Etch was conducted for 100 min. 110-μm-deep vertical silicon structures were produced (Fig. 3.5). The <110> surface at the bottom appeared rough, while <111> and <110> surfaces

on the top were clean and uniform. During lithography, line patterns should be kept parallel to the major flat on the <110> silicon wafer. If the line patterns were kept vertical to the major flat, smooth surfaces cannot be obtained, as in Fig. 3.6.

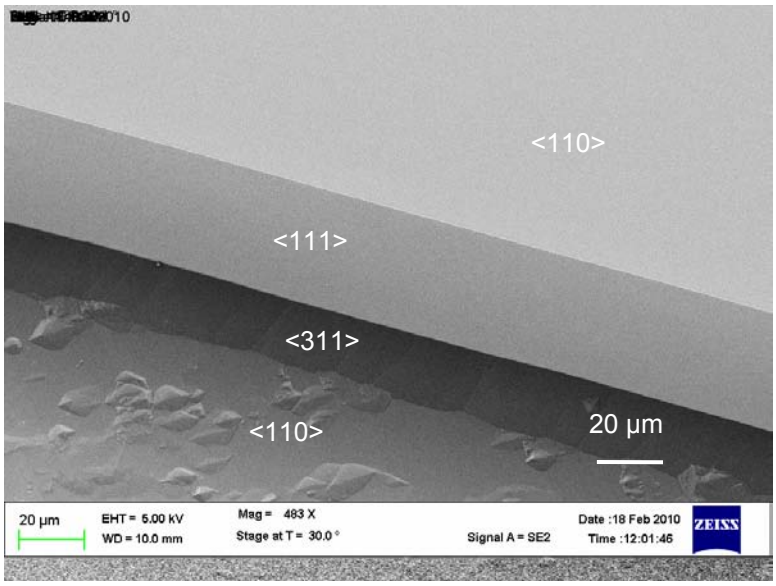


Figure 3.5 A vertical silicon sidewall (i.e., <111> surface) produced after the first fabrication step.

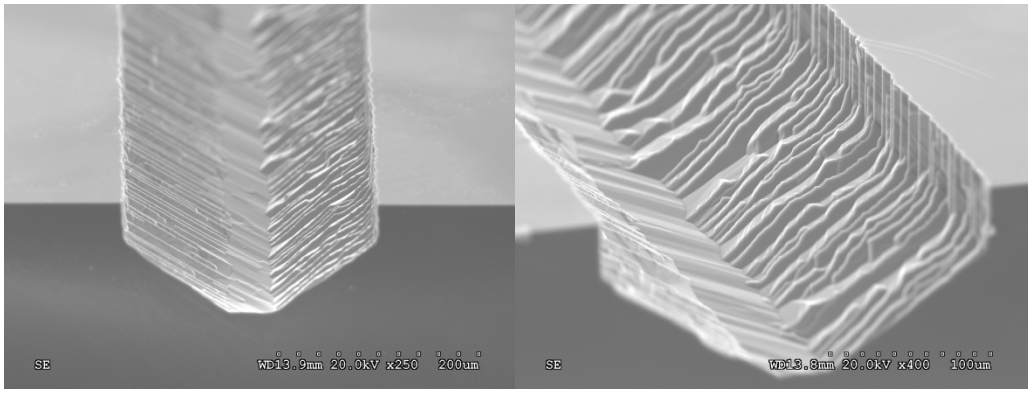


Figure 3.6 Structures obtained through KOH etch on <110> silicon wafer (lines vertical to the major flat).

3.2.1.2 Fabrication of PDMS Membranes with Hollow structures

A PDMS membrane of hollow structures was generated in the second step. This generation includes five sub-steps (Fig. 3.7): (1) spin-coat S1813 (Shipley Company) on a SU-8 mold (Fig. 3.7b), (2) spin-coat PDMS (ratio between PDMS and its curing agent is 10:1) on the

S1813-coated SU-8 mold (Fig. 3.7c), (3) drop hexane on top of the spin coated PDMS to remove the residual layer, followed by baking to cure (Fig. 3.7d) and (4) release the thin PDMS film from the SU-8 mold by etching S1813 with acetone, completing the generation of the PDMS film of through-holes (Fig. 3.7e). The released PDMS membrane was placed on a clean glass slide for later use.

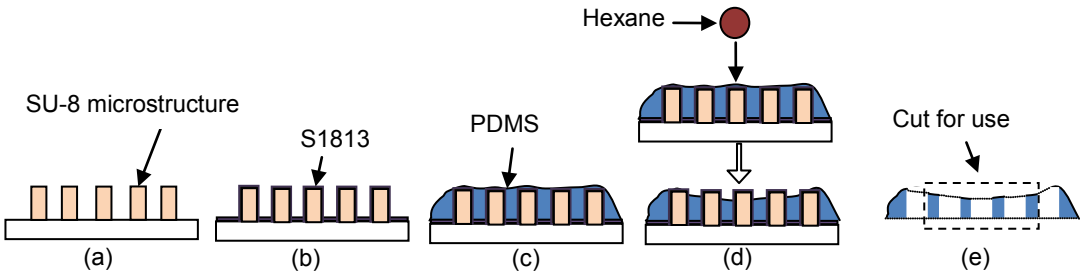
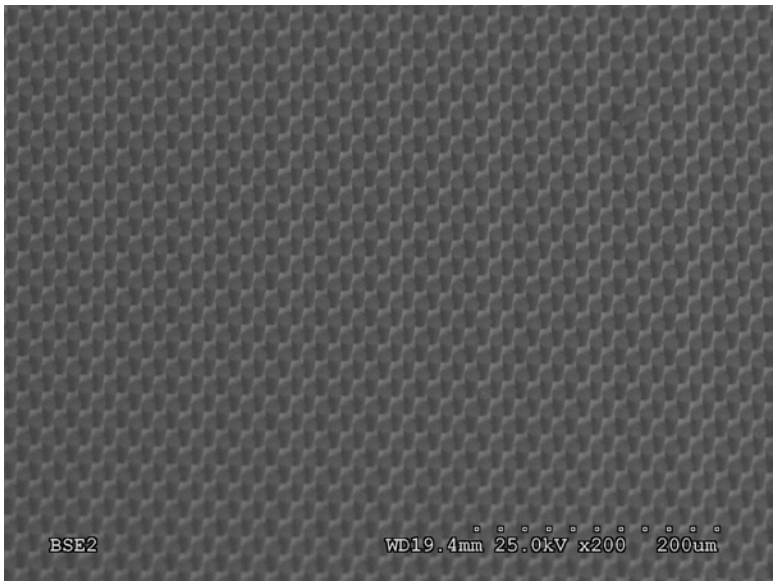


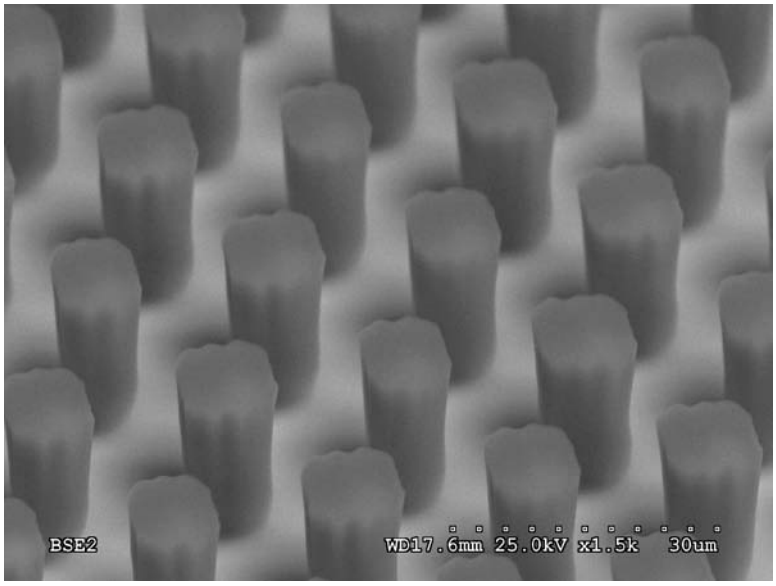
Figure 3.7 Fabrication of a PDMS membrane with hollow structures: (a) generate SU-8 microstructures, (b) spin-coat a positive PR (S1813), (c) spin-coat PDMS solution, (e) apply liquid hexane to remove the PDMS residue layer above the SU-8 microstructures, and (e) cure the PDMS, remove the PDMS membrane from the substrate, and cut off the central area of this membrane for later use.

The SU-8 mold included a SU-8 layer and a silicon substrate. SU-8 was a negative photoresist. Square micropillars were generated in the SU-8 layer using a conventional UV lithographic approach [82]. S1813 was a positive photoresist. It was employed in this work as a sacrificial material for easily removing the PDMS from the SU-8 mold. A thin film of S1813 was spin-coated not only on the top surfaces of the SU-8 layer, but also at the sidewalls and bottoms of the SU-8 square pillars. Due to the surface tension, this S1813 coating would make the sharp edges and corners of the SU-8 structures become rounded, as discussed in a related work [83]. Accordingly, the PDMS holes generated out of such a mold would have approximately circular cross-sections. SU-8 2015 (MicroChem Company) was adopted to fabricate these pillars. Before processing, a silicon wafer was immersed in a 10:1 hydrofluoric acid (HF) solution for 2 min to remove the native oxide layer coated on the silicon wafer. Subsequently, this wafer was rinsed with DI water and baked for 5 min at 200 ^{o}C on a hotplate. A 23-μm-thick layer of SU-8 was then obtained by spin-coating SU-8 at 3000 rpm for 30 s. After spin-coating, the substrate

was pre-baked for 1 min at 65 ^{o}C, followed by 3 min at 95 ^{o}C. The SU-8 layer was exposed through a mask using UV light of 145 mW dose. After that, the sample was baked first for 1 min at 65 ^{o}C and then for 3 min at 95 ^{o}C. The fabrication of the SU-8 mold was completed after the sample had been developed for 4 min using SU-8 developer and rinsed with isopropyl alcohol, Fig. 3.8.



(a)



(b)

Figure 3.8 Fabricated SU-8 pillars (a) 3D view and (b) close-up view.

PDMS membranes with hollow structures are crucial for certain microfabrication applications, such as in microfluidics and cell biology [84-86]. Due to the limitations in PDMS properties, such as no sensitivity to light, traditional photolithography methods cannot be used to fabricate PDMS features. PDMS patterns are generally produced using a molding approach, as illustrated in Figs. 3.7(a), 3.7(b) and 3.7(d). However, a residual layer of PDMS is usually formed on top of the mold even after long time of spinning. Many approaches have been developed to fabricate through-hole patterns in PDMS, including mechanical removal of excessive PDMS layer using a blade [87], and dry etch of PDMS using gas plasma [88, 89]. The mechanical scrubbing approach requires good handling skills, and may not be capable of removing all extra PDMS due to the facts that the blade is not perfectly flat, and that the mold structures are not perfectly uniform in their heights. The dry-etch method needs adjustment of etch recipes, and the etch rate is normally low. Hence, a new approach was developed in this work to fabricate hollow structures in PDMS membrane. This approach does not need any special handling skills, and is easy to realize. In the approach, a droplet of liquid hexane was placed at the center of the spin-coated PDMS before baking to cure (Fig. 3.7c). Hexane dissolved and pushed away the top layer of PDMS from the center towards the edge of the substrate (Fig. 3.7d). The PDMS membrane formed in this way was thin at the center and thick at the edge. For example, the thickness across the membrane ranged from 5 μm at the center to over 100 μm at the edge when the volume of the hexane droplet was ~30 μL. The thick edge made it convenient to hold and separate the membrane from the SU-8 mold. The thickness of the PDMS membrane in its central area decreased with the increase in the volume of hexane used. The hollow patterns were located in the central area of a PDMS membrane, and this area was cut off from the membrane (Fig. 3.7e). The cut-off membrane served as the shadow mask in the fabrication. It had a rectangular shape of dimensions 5×5 mm^2, and was aligned on the silicon substrate with one edge of this membrane placed over the sidewall (Fig. 3.1b).

The membrane should not be too thick, over 20 μm, otherwise, the bending moment of the membrane will be large, and the membrane could not deform naturally to follow the shape

change of the silicon stage as in Fig. 3.9. In this case, a gap emerges between the membrane and the sidewall. The shape and position of the patterns produced on the sidewall will be different.

The PDMS membrane with hollow lines should not be too thin either, less than 5 μm. The first reason is that if the membrane was too thin, it will be hard for membrane transferring. The other reason is that when the membrane was too thin, the strength of the PDMS lines between the hollow patterns will be reduced, and may not be able to keep the shape of the patterns as designed, Fig. 3.10. In Fig. 3.10, the thickness of the PDMS membrane is about 4 μm. Neighboring PDMS lines were stuck together. During experiments, this kind of situation happened many times. If the PDMS membrane is thick, around 10 μm, once the peeled off PDMS was soaked into IPA, the PDMS lines will restore their shape and become separated. However, for thin PDMS membrane, less than 5 μm, the shape of the PDMS lines did not restore after soaking the membrane into IPA. For PDMS membrane with hollow dots, the second issue is no longer exists due to its nearly circular shape of the hollow patterns.

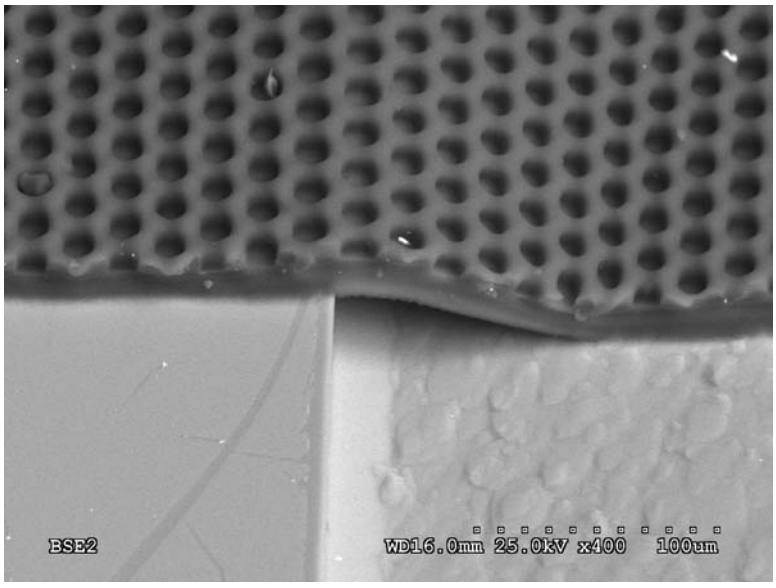
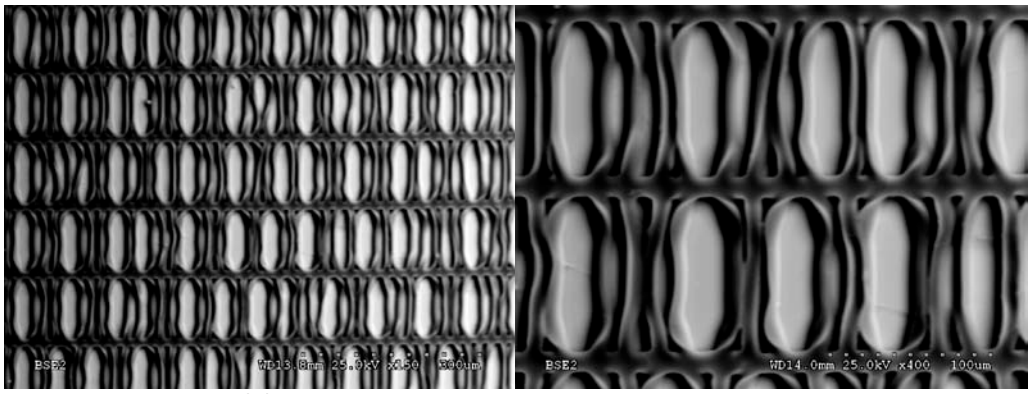


Figure 3.9 A piece of thick PDMS membrane placed on a silicon stage.



(a) (b)

Figure 3.10 Thin PDMS membrane with hollow lines (a) overview and (b) close-up view.

The alignment was conducted under an optical microscope according to relative positions between the hollow patterns of the cut-off membrane and the top edge of the silicon sidewall. During the alignment, a small amount of isopropyl alcohol (IPA) was added to the substrate to make it easy to move the PDMS membrane around. After the evaporation of IPA, the PDMS membrane was tightly bonded to the silicon substrate.

3.2.1.3 Metal Deposition

In the third step (Fig. 3.1c), using the cut-off PDMS membrane as a shadow mask, a Au film was generated on the silicon substrate in a thermal evaporator. To ensure that Au could be coated on the silicon sidewall, the substrate was tilted during the deposition. The direction perpendicular to the sidewall formed an angle, α (which ranges between 0^0 and 90^0), with the vertical direction, as illustrated in Fig. 3.1(c). Let t_1 denote the thickness of a Au layer generated on the silicon substrate when α is 90^0, i.e., when the substrate is not tilted. The value of t_1 is provided by the thermal evaporator during the deposition. Set t_2 to be the corresponding thickness of the Au film coated on the silicon sidewall if α is not 90^0, i.e., if the substrate is tilted. According to [4], we have

$$t_2 = t_1 \cos\alpha \,. \tag{3.4}$$

By this equation, no Au is coated on the silicon sidewall when the substrate is not tilted, and the thickness of the Au film coated on the silicon sidewall increases with the decrease in the value of α .

3.2.2 Experimental Results and Discussions

Using the fabrication procedure illustrated in Fig. 3.1, two types of Au micropatterns, dots and lines, were generated on 110- and 70-μm-high vertical silicon sidewalls, respectively (Figs. 3.11 and 3.12). The height of the sidewall refers to the etched depth along the <111> surface.

3.2.2.1 Fabrication of Au Dots on Sidewall

The mask design of dot patterns is shown in Fig. 3.11(a). An individual pattern has a square shape (10 × 10 μm^2). The pitch between two neighboring dots in a row is 36 μm, and that between two neighboring dots in a column is 20 μm. Fig. 3.11(b) shows a generated PDMS membrane with through-holes that was used as a shadow mask during the Au deposition. The membrane was about 10 μm thick. The through-holes in this generated PDMS membrane had approximately circular cross-sections due to the capillary effect involved in the fabrication. Our focus was to generate Au dots on the sidewall. Hence, during the process of depositing Au, α was set to be 10^o, which made the sidewall almost perpendicular to the vertical direction. Consequently, Au dots appeared mainly on <111>, <311> and bottom <110> surfaces, and only few dots were seen at the edge of the top <110> surface (this edge was close to the <111> surface). t_1 was 5 nm. By equation (3.4), the thickness of the generated Au dots was 4.9 nm. The etched depth along the <111> surface was 110 μm. Nine rows of Au dots have been properly generated on the <111> surface (Fig. 3.11c). The average diameter of the generated Au dots was 10 μm. The Au dots in a vertical column were not aligned exactly perpendicular to the <110> surface because of the error of alignment, which was about 4^o. The average distance between two neighboring dots in a horizontal row was 37 μm, while that in a vertical column was 21 μm. Both distances were larger than the designed ones by 1 μm. The increase in the

distances might be caused by the stretch of the PDMS membrane when this membrane was placed on the silicon sidewall.

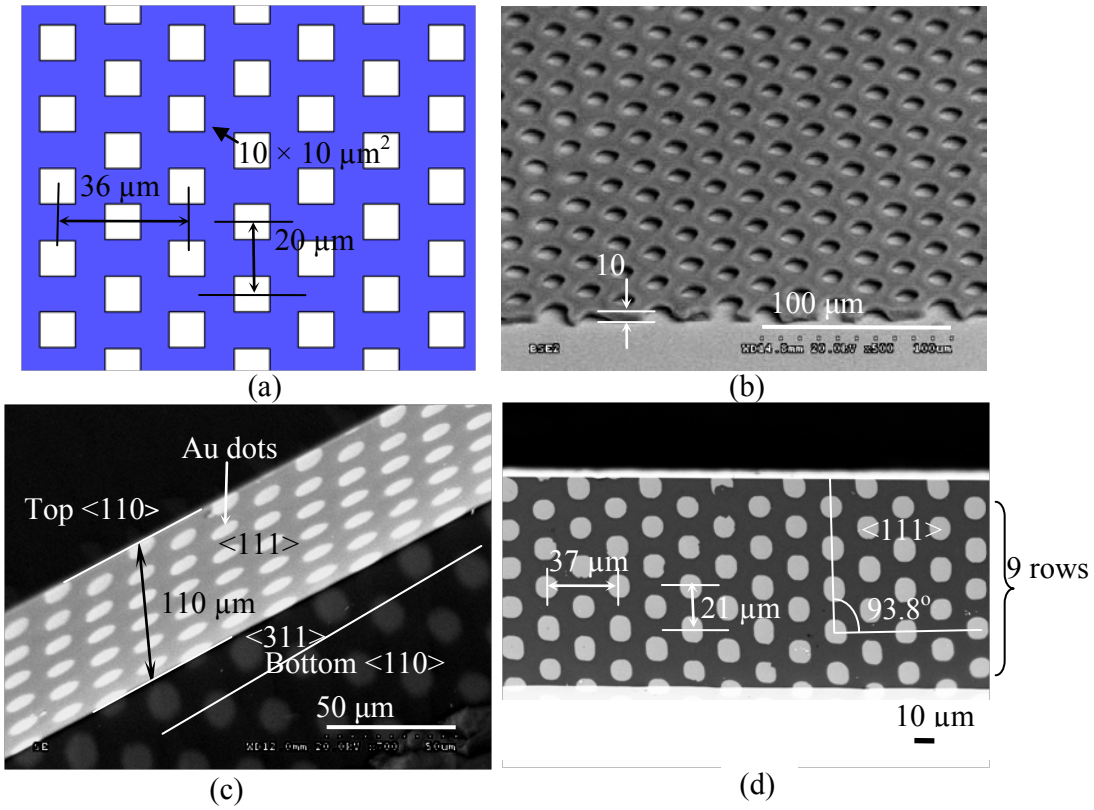


Figure 3.11 Fabrication of Au dots on sidewall (a) designed dot patterns on the mask, (b) a fabricated PDMS membrane with 10 μm through-holes, (c) 3D and (d) side views of 10 μm Au dots generated on a vertical silicon sidewall (i.e., <111> surface).

3.2.2.2 Fabrication of Au Lines on Sidewall

The mask design of line patterns is shown in Fig. 3.12(a). Each individual line was 100 μm long and 20 μm wide. The horizontal distance between two neighboring lines was 40 μm. Fig. 3.12(b) shows a fabricated PDMS membrane that was used as a shadow mask during the Au deposition. This membrane had hollow lines, and was about 15 μm thick. The etched depth along the <111> surface for Au lines was 70 μm (Fig. 3.12c). The Au lines generated on a silicon sidewall could potentially serve as interconnects between the circuits located at the top and bottom surfaces beside the sidewall. For this purpose, these Au lines should run across the

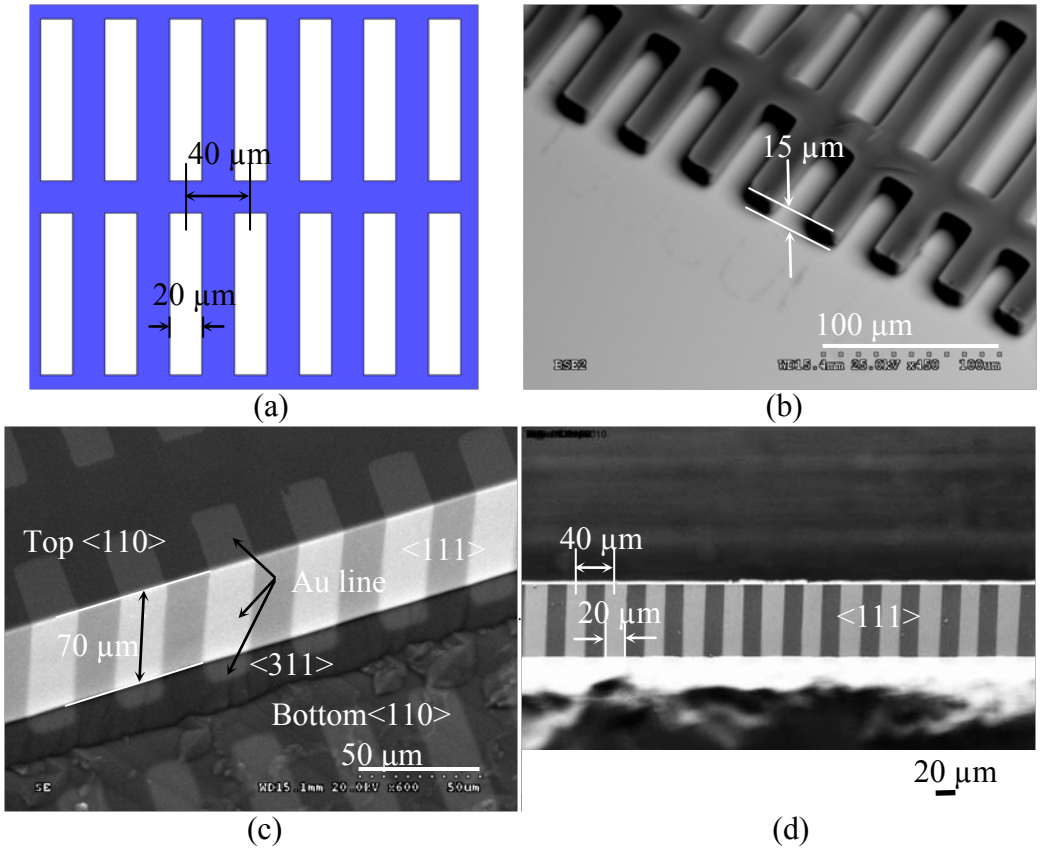


Figure 3.12 Fabrication of Au lines on sidewall (a) designed line patterns on the mask, (b) a reprehensive PDMS membrane with hollow lines that served as a shadow mask, (c) 3D and (d) side views of 20-μm-wide Au lines generated on a vertical silicon sidewall (i.e., <111> surface).

sidewall and have contact with both top and bottom surfaces. Therefore, during the thermal deposition, α was set as 45^0 to ensure that Au would be coated on all these three surfaces. t_1 was also 5 nm. By equation (3.4), the thickness of the generated Au lines was 3.5 nm. The average distance between two neighboring lines was 40 μm, and the average width of the generated lines was 20 μm. These two dimensions were the same as the designed ones. The generated lines were oriented vertically, and ran across the sidewall (i.e., <111> surface) (Fig. 3.12d). These lines also extended to the top surface (i.e., top <110> surface) and the bottom surface (i.e., <311> surface). Part of structures on the top and bottom surfaces could be subsequently generated on the extended portions of these sidewall lines using, for example, UV lithography with the

alignment accuracy of 1 μm. Consequently, the planar devices on both the top and bottom surfaces would be connected through the sidewall lines. It would be better to have sidewall lines generated before the production of the planar devices. Otherwise, the pre-existing planar devices might be damaged by the PDMS shadow mask when this mask is placed on the substrate to generate the sidewall lines.

3.3 Generation of Micropatterns on Both Sidewalls of a Silicon Channel

3.3.1 Experimental Procedures

We have previously explored the possibility of fabricating patterns on the sidewalls of polymer microstructures using hot embossing processes [22, 23] and strain-recovery property of a thermal shape-memory polymer [90]. Furthermore, in last section [91], we have developed an approach to produce Au patterns on a single silicon sidewall using PDMS shadow mask. In the approach, a thin PDMS membrane with hollow structures was first placed against the sidewall. Au film was then thermally coated on the substrate using this flexible PDMS membrane as a shadow mask. Finally, after the removal of the PDMS membrane, Au patterns were left on the silicon sidewall. This approach is applicable when there is only a single sidewall on the substrate. As examined in [91], a flexible PDMS membrane could be folded against this sidewall. However, it is difficult to place a PDMS membrane directly on multiple sidewalls of a concave microstructure (such as two vertical sidewalls of a microchannel) due to the small size of the concave microstructure. On the other hand, functional components in a MEMS device may include multiple sidewalls. Therefore, in this work, we explored the feasibility of fabricating not only vertical lines, but also an array of dots on vertical sidewalls of silicon microchannels. For this purpose, we also developed 3D geometric models to direct experimental conduction. Based on the understanding gained from these 3D geometric models, we have produced 10 μm Au dots and 20-μm-wide Au wires on vertical sidewalls of silicon microchannels.

Experimental setup for generating metal micropatterns on both sidewalls of a silicon channel was given in Fig. 3.13. Using a PDMS membrane with hollow structures as a shadow mask, a silicon channel was coated with Au twice in a thermal evaporator. To ensure that Au

can be coated on either sidewall, the substrate was tilted at an angle, θ, during the first deposition (Fig. 3.13a). To also coat Au on the other sidewall, the substrate had been rotated by 180^0 on its wedge-shaped stage such that this sidewall would also face the incoming Au vapor at the angle of θ during the second deposition (Fig. 3.13b). The fabrication processes for silicon channel and PDMS membrane with through-structures are the same as illustrated in last section. The silicon channel had two vertical sidewalls, which was 70 μm deep, 113 μm wide and 1 cm long.

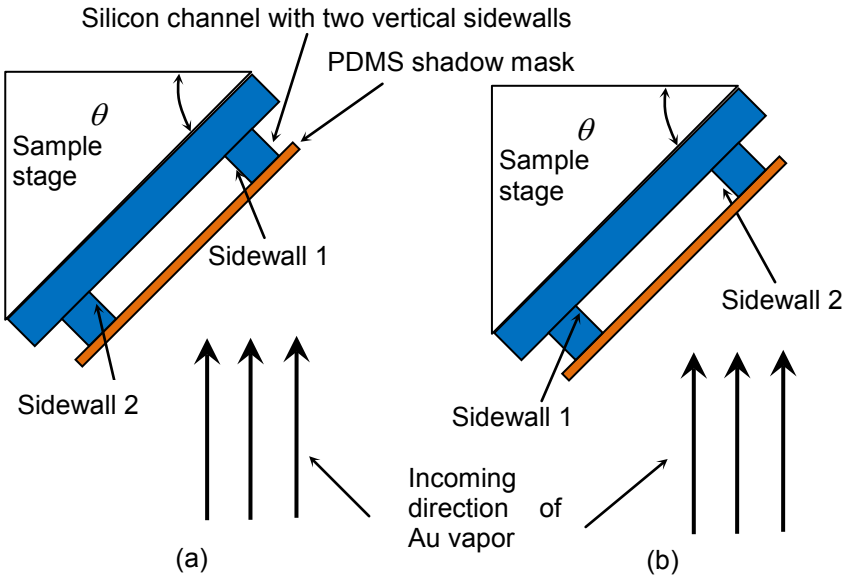


Figure 3.13 Schematics of experimental setup: (a) a silicon substrate with channels covered by a PDMS shadow mask is tiltled at an angle of θ during the first deposition of Au and (b) the substrate is rotated by 180^0 on the sample stage before the second deposition.

3.3.2 Geometric Models of Generating Micropatterns on Vertical Sidewall Using Shadow Mask

Due to large mean free paths of gas molecules at low pressure, evaporation techniques tend to be directional in nature, and shadow of patterns may occur [92]. Based on shadow effect, micro/nanopatterns have been generated on top surfaces of substrates [92]. 2D models have also been developed in these references to address the shadow effect. Since our goal is to fabricate patterns on channel sidewalls, 3D geometric models are established accordingly to

find shapes, thicknesses and dimensions of Au patterns generated on a channel sidewall (Fig. 3.14).

3.3.2.1 Location of a Generated Au Dot

As illustrated in Fig. 3.13(a), let *A* denote a representative hollow point in the PDMS membrane that is suspended above a silicon channel as the shadow mask. Set A' to be the corresponding Au point, which is formed on a channel sidewall after Au vapor goes through the point *A* and has contact with the sidewall. Set up a rectangular coordinate system. The origin is located at the top right corner of the channel sidewall (Fig. 3.14a). The *x*-axis is perpendicular to the channel sidewall, *y*-axis lies along the vertical direction of the substrate, and *z*-axis is along the channel direction. Let (x_A, y_A, z_A) denote the coordinates of *A*. Use $A'B$, $A'D$ and *AC* to denote the projections of line $A'A$ on the sidewall, the surface parallel to *x*-*z* plane, and the surface parallel to *y*-*z* plane, respectively. The angle formed by *AD* and *AC* is α, and that subtended by $A'B$ and *CB* is β. Then, according to geometric analysis, the coordinates ($x_{A'}$, $y_{A'}$, $z_{A'}$) of A' are

$$x_{A'}=0,\ y_{A'}=-x_A\cot\alpha,\ z_{A'}=z_A+x_A\cot\alpha\tan\beta. \tag{3.5}$$

The coordinates of *B* are calculated to be (0, 0, z_A). Although the line *AB* is parallel to *x* direction, the line $A'B$ is not along *y* direction. Instead, the latter line lies on the channel sidewall and forms an angle of β with the *y* direction.

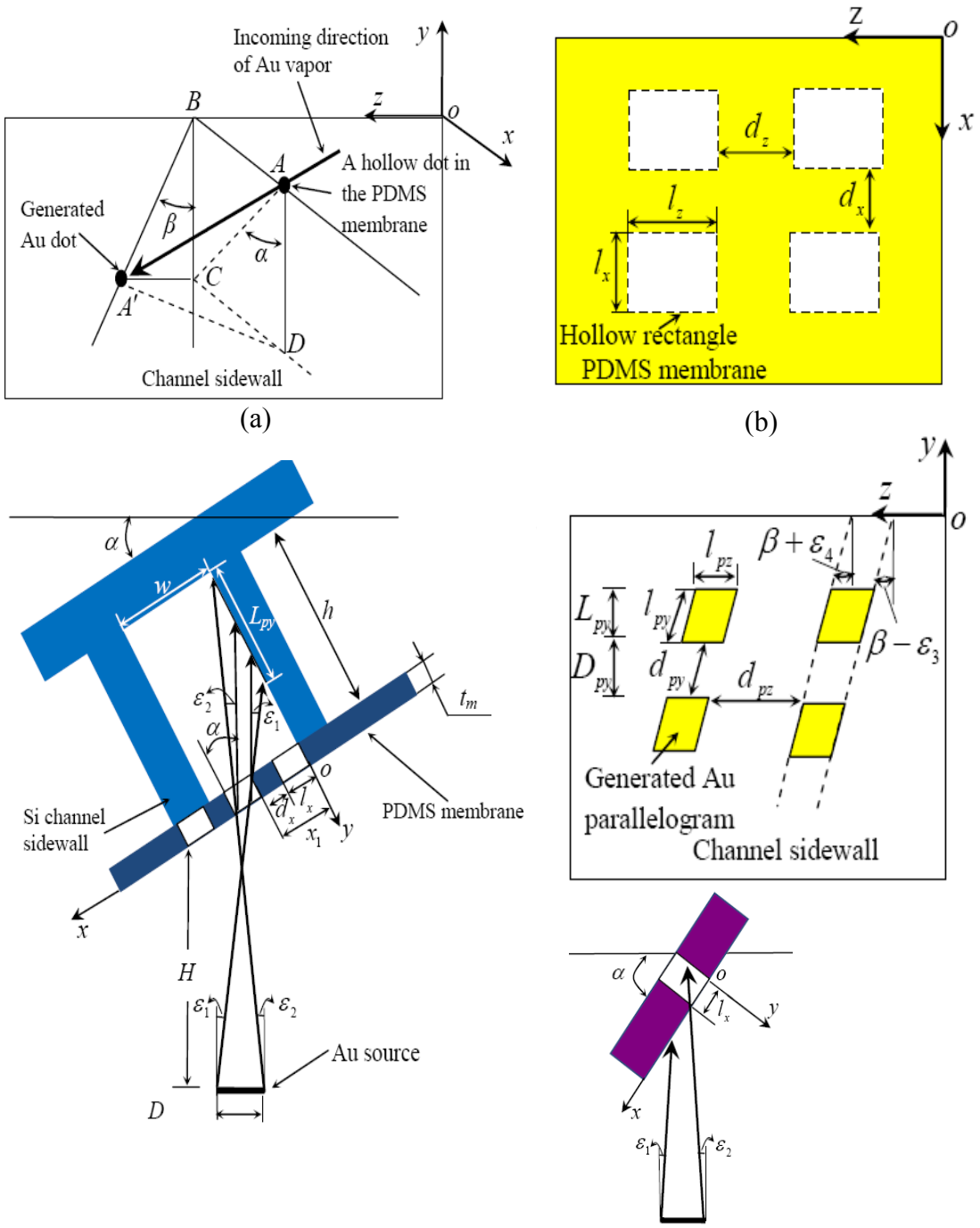


Figure 3.14 Geometric models of shadow mask patterning (a) 3D illustration of generating a Au dot on a vertical channel sidewall, (b) 2D illustration of masking structures, (c) Side view of Au vapor penetrating a hollow structure in the PDMS membrane, (d) 2D illustrations of generated Au trapezoids and (e) Side view of a case that Au vapor cannot penetrate a hollow structure of the PDMS membrane.

3.3.2.2 Shapes and Dimensions of Generated Au Patterns

Suppose that the PDMS membrane includes an array of hollow rectangles (Fig. 3.14b). Let l_x and l_z denote the dimensions of a hollow rectangle along the *x*- and *z*-axes, respectively. Set d_x and d_z to be the distances between two neighboring hollow rectangles along the *x*- and *z*-axes, separately. Suppose that the Au source has a circular shape with a diameter of *D* (which is our case), and the vertical distance between this source and the substrate is *H*. The silicon channel was suspended right above the Au source. Consider a representative hollow pattern in the PDMS membrane (Fig. 3.14c). Let x_1 denote *x*-coordinate of its right edge. The *x*-coordinate of its left edge is $(x_1 + l_x)$ accordingly. Set t_m to be the thickness of the shadow mask. As shown in Fig. 3.14(c), Au vapors that come from the left and right edges of the Au source in the *x*-*y* plane and go through the representative hollow pattern might form angles of ε_1 and ε_2, respectively, with the vertical direction. Based on equation (3.5) and geometric analysis, the array of hollow rectangles in the shadow mask may result in the generation of an array of Au trapezoids on a channel sidewall after thermal evaporation of Au (Fig. 3.14d). The top and bottom edges of each trapezoid are parallel to the *z*-axis, while the left and right side edges form angles of $(\beta + \varepsilon_4)$ and $(\beta - \varepsilon_3)$, respectively, with the *y* direction. Naturally, when both ε_3 and ε_4 are 0^0, the two side edges are parallel to each other, and each Au trapezoid becomes a parallelogram. Furthermore, if β is also 0^0, then the two side edges of the parallelogram are both parallel to the *y*-axis, but perpendicular to the top and bottom edges. Subsequently, the parallelogram becomes a rectangle. Let l_{pz} denote the length of the top edge of a Au trapezoid (Fig. 3.14d). Set l_{py} to be the distance between the top and bottom edges of a Au trapezoid along the direction that forms an angle of β with the *y*-axis. Use L_{py} to represent the height of the Au trapezoid along *y* direction. Also, let d_{pz} be the

distance between two neighboring trapezoids along the *z*-axis, and set d_{py} to be the distance between two neighboring trapezoids along the direction that forms an angle of β with the *y*-axis. Use D_{py} to represent the distance between these two neighboring trapezoids along *y* direction.

Based on equation (3.5), as well as geometric analysis, we have

$$l_{pz} = x_1 \cot\alpha \tan(\beta + \varepsilon_4) - x_1 \cot\alpha \tan(\beta - \varepsilon_3) + l_z - t_m \tan(\beta - \varepsilon_3),$$

$$l_{py} = [\frac{x_1 + l_x}{\tan(\alpha - \varepsilon_2)} - \frac{x_1}{\tan(\alpha + \varepsilon_1)}]\sec\beta - t_m \sec\beta,\ L_{py} = \frac{x_1 + l_x}{\tan(\alpha - \varepsilon_2)} - \frac{x_1}{\tan(\alpha + \varepsilon_1)} - t_m,$$

$$d_{pz} = x_1 \cot\alpha \tan(\beta - \varepsilon_3) - x_1 \cot\alpha \tan(\beta + \varepsilon_4) + t_m \tan(\beta - \varepsilon_3) + d_z,$$

$$d_{py} = [\frac{x_1}{\tan(\alpha + \varepsilon_1)} - \frac{x_1 - d_x}{\tan(\alpha - \varepsilon_2)} + t_m]\sec\beta,\ D_{py} = \frac{x_1}{\tan(\alpha + \varepsilon_1)} - \frac{x_1 - d_x}{\tan(\alpha - \varepsilon_2)} + t_m.$$

(3.6)

3.3.2.3 Limits of Two Projected Angles

In order to generate an array of patterns on the channel sidewall, α has to meet two requirements: Au vapor should be able to go through the PDMS mask, and should also be able to further reach the channel sidewall. Based on geometric analysis (Figs. 3.14c and 3.14e), to ensure that Au vapor goes through the PDMS mask, α needs to satisfy the inequality:

$$\alpha < \arctan\frac{l_x}{t_m} + \varepsilon_2. \tag{3.7}$$

To enable Au vapor to further reach the bottom edge of the channel sidewall, α needs to further satisfy the inequality:

$$\alpha < \arctan\frac{w}{h + t_m} + \varepsilon_2. \tag{3.8}$$

where *w* is the width of the channel, and *h* is the depth of the channel. Therefore, to generate an array of patterns on the channel sidewall, α should meet the two inequalities given in (3.7) and (3.8), respectively.

On the other hand, in order to fabricate an array of patterns on the channel sidewall, β just needs to meet one requirement since the channel sidewall is long: Au vapor should be able to go through the PDMS mask. Subsequently, based on geometric analysis, β has to satisfy the following conditions:

$$-\arctan\frac{l_y}{t_m}-\varepsilon_3<\beta<\arctan\frac{l_y}{t_m}+\varepsilon_4. \tag{3.9}$$

3.3.2.4 Thickness of Generated Au Patterns

The thickness of the generated Au patterns is related to the incoming direction of Au vapor [4]. Let t_1 denote the thickness of the Au layer generated on the channel sidewall when the incoming direction of the Au vapor is perpendicular to the channel sidewall (i.e., α = 90^o and β =0^o). The value of t_1 is provided by the thermal evaporator during the deposition. Set t_2 to be the corresponding thickness of the Au film coated on the channel sidewall if the incoming direction of Au vapor is not perpendicular to the channel sidewall. Based on the conservation of mass, the total amount of Au vapor penetrating the shadow mask should equal that reaching the sidewall. Neglecting the inclination effect of the incoming Au vapor (i.e., set ε_1, ε_2, ε_3 and ε_4 all to be 0^0), it can be readily derived that

$$t_2 = t_1 \sin\alpha\cos\beta. \tag{3.10}$$

By this equation, the thickness of the Au patterns generated on the channel sidewall increases with the increase in α and decrease in β.

3.3.3 Geometric Models of Generating Micropatterns on Sloped Sidewall

This work focused on patterning of vertical sidewalls. The geometric models developed for vertical sidewall patterning could be easily generalized for the case of sloped sidewall. Let

φ denote the angle between the sloped sidewall and the vertical direction, Fig. 3.15. Set *A"* to be the corresponding Au point, which formed on this sloped sidewall after Au vapor goes through the point *A* and deposits on the sidewall. Using the same coordinate system and definitions of α and β, the relationships given in (3.7), (3.9) and (3.10) still hold. However, those listed in equations (3.5), (3.6) and (3.8) need to be modified. According to geometric analysis, the coordinates ($x_{A"}$, $y_{A"}$ $z_{A"}$) of *A"* are

$$x_{A"} = \frac{x_A \tan\varphi}{\tan\alpha + \tan\varphi},\ y_{A"} = -\frac{x_A}{\tan\alpha + \tan\varphi},\ z_{A"} = z_A + \frac{x_A \cot\alpha \tan\beta}{1 + \tan\varphi \cot\alpha}. \qquad (3.11)$$

These relationships indicate that, as φ increases, *x* coordinate of A'' increases while the absolute values of y and z coordinates of A'' decrease.

Defining l^s_{pz}, l^s_{py}, L^s_{py}, d^s_{pz}, d^s_{py} and D^s_{py} in the same ways as l_{pz}, l_{py}, L_{py}, d_{pz}, d_{py} and D_{py}, respectively, we have

$$l^s_{pz} = \frac{x_1 \cot\alpha \tan(\beta + \varepsilon_4)}{1 + \tan\varphi \cot\alpha} - \frac{x_1 \cot\alpha \tan(\beta - \varepsilon_3)}{1 + \tan\varphi \cot\alpha} + l_z - t_m \tan(\beta - \varepsilon_3),$$

$$l^s_{py} = [\frac{x_1 + l_x}{\tan(\alpha - \varepsilon_2) + \tan\varphi} - \frac{x_1}{\tan(\alpha + \varepsilon_1) + \tan\varphi}]\sec\beta - t_m \sec\beta,$$

$$L^s_{py} = \frac{x_1 + l_x}{\tan(\alpha - \varepsilon_2) + \tan\varphi} - \frac{x_1}{\tan(\alpha + \varepsilon_1) + \tan\varphi} - t_m,$$

$$d^s_{pz} = \frac{x_1 \cot\alpha \tan(\beta - \varepsilon_3)}{1 + \tan\varphi \cot\alpha} - \frac{x_1 \cot\alpha \tan(\beta + \varepsilon_4)}{1 + \tan\varphi \cot\alpha} + d_z + t_m \tan(\beta - \varepsilon_3),$$

$$d^s_{py} = [\frac{x_1}{\tan(\alpha + \varepsilon_1) + \tan\varphi} - \frac{x_1 - d_x}{\tan(\alpha - \varepsilon_2) + \tan\varphi} + t_m]\sec\beta,$$

$$D^s_{py} = \frac{x_1}{\tan(\alpha + \varepsilon_1) + \tan\varphi} - \frac{x_1 - d_x}{\tan(\alpha - \varepsilon_2) + \tan\varphi} + t_m. \qquad (3.12)$$

Furthermore, to ensure Au vapor also reaches the bottom edge of the sloped sidewall, the condition given in (3.8) is modified as

$$\alpha < \arctan\frac{w - h\tan\varphi}{h + t_m} + \varepsilon_2 \tag{3.13}$$

When φ is zero, geometric models for sloped sidewall are reduced to their counterparts in the case of vertical sidewall.

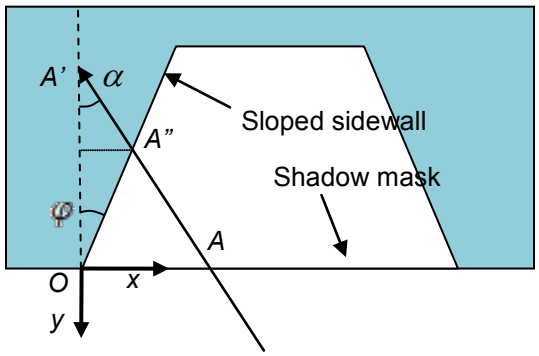


Figure 3.15 Demonstration of generating a pattern on sloped sidewall.

3.3.4 Experimental Results and Discussions

Based on the understanding gained from the geometric models, we produced 10 μm Au dots and 20-μm-wide Au wires, respectively, on vertical sidewalls of a silicon channel (Figs. 3.16 and 3.17). These results were also employed to validate the theoretical relationships given in (3.6). The silicon channel used in this work was 70 μm deep, 113 μm wide and 1 cm long. In this work, the values of *D* and *H* were 8 mm and 32 cm, respectively. According to geometric analysis, ε_1, ε_2, ε_3 and ε_4 were all equal to 0.7^0. As seen from Fig. 3.14(c), the inclination of incoming vapor can be further reduced by increasing the value of *H*, as well as by decreasing the value of *D*. Consequently, as discussed in the previous section, the generated patterns would have the shapes of parallelograms.

During the first thermal deposition of generating Au dots, the value of α was 35^o, which met conditions (3.7) and (3.8). In the second deposition, the value of α remained the same, while the other sidewall of a channel was facing the arriving Au vapor. α was obtained by

attaching the sample to the inclined surface of a wedge-shaped Al stage using a double-sided tape. The incline surface formed an angle of 35^{o} with the bottom surface of the Al stage. The stage was fixed to the bottom surface of a flat holder, which was located at a place 32 cm right above the Au source in the thermal evaporator. β was approximately 0^{0}.

3.3.4.1 Fabrication of Au Dots on Sidewalls

The mask design of dot patterns is shown in Fig. 3.16(a). An individual pattern has a square shape (10 × 10 μm^2). The distance between two neighboring dots in a horizontal row is 10 μm. The distance between two neighboring horizontal rows is 8 μm. Fig. 3.16(b) shows a PDMS membrane with through-holes that was used as a shadow mask in this work. The thickness of the PDMS membrane was 4 μm.

Two rows of Au dots have been properly generated on either sidewall of the silicon channel (Figs. 3.16c-3.16e). t_1 was 5 nm. By equation (3.10), the thickness of the generated Au dots was 2.9 nm. Since the hollow dots in the shallow mask had round corners (Fig. 3.16b), the corners of the generated Au dots were round accordingly. The generated dots were not in the form of trapezoids as illustrated in Fig. 3.16(d). Instead, the generated dots had approximately rectangular shapes, since β, ε_3 and ε_4 were small (they were 0^{0}, 0.7^{0} and 0.7^{0}, respectively).

On the left sidewall of the silicon channel (Fig. 3.16e), the average size of the generated Au dots along the *y* direction (i.e., L_{py}) was 12.0 μm in the top row. The theoretical value predicted by equation $(3.6)_3$ was 11.9 μm. The average dimension of the generated Au dots along *y* direction was 13.7 μm in the bottom row, while the theoretical value predicted by equation $(3.6)_3$ was 13.4 μm. The average size of the generated Au dots along the *z* direction (i.e., l_{pz}) was 10.8 μm in the top row. The theoretical value predicted by equation $(3.6)_1$ was

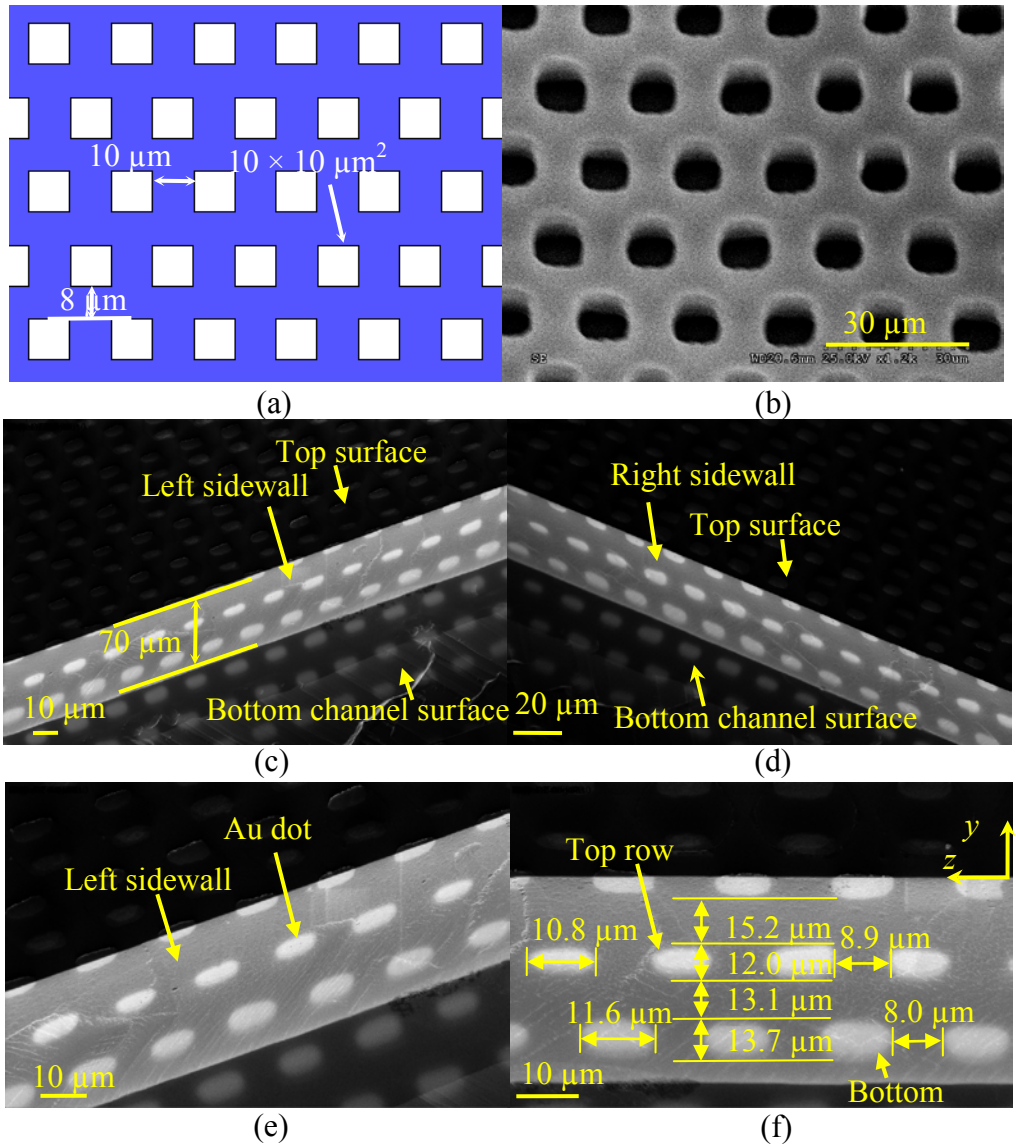


Figure 3.16 Fabrication of Au dots on two sidewalls (a) designed dot patterns on the mask, (b) a representative PDMS membrane of through-holes, 3D views of 10 µm Au dots generated on (c) left and (d) right sides of the silicon channel, (e) close-up and (f) front views of Au dots generated on left side of the silicon channel. The dimensions of the Au dots fabricated on the two sidewalls were measured using a Scanning Electron Microscope (SEM) machine. The image viewing direction was located inside the *x*-*y* plane, while formed an angle of 25^0 with the *y* direction. Accordingly, real dimensions of the fabricated Au dots along the *y* and *z* directions were, respectively, 2.1 times as large as and equal to the corresponding dimensions measured directly using the SEM machine. The real dimensions were marked on the SEM images. The same measurement technique was also applied to the fabricated Au lines.

10.6 µm. The average dimension of the generated Au dots along *z* direction was 11.6 µm in the bottom row. The theoretical value predicted by equation $(3.6)_1$ was 11.3 µm. In conclusion, the

errors in predicting the dimensions of Au dots using the theoretical relationships given in (3.6) along both *y* and *z* directions were within 0.3 μm.

The distance between Au dots along the *y* direction (i.e., D_{py}) was 15.2 μm in the top row. The theoretical value predicted by equation $(3.6)_6$ was 14.5 μm. The distance between Au dots along the *y* direction was 13.1 μm in the bottom row. The theoretical value predicted by equation $(3.6)_6$ was 13.0 μm. The distance between Au dots along the *z* direction (i.e. d_{pz}) was 8.9 μm in the top row, while the theoretical value predicted by equation $(3.6)_4$ was 9.4 μm. The distance between Au dots along the *z* direction was 8.0 μm in the bottom row. The theoretical value predicted by equation $(3.6)_4$ was 8.7 μm. In conclusion, the errors in predicting the distances between neighboring Au dots using the relationships in (3.6) along both *y* and *z* directions were within 0.7 μm. The same results applied to the right sidewall of the silicon channel.

3.3.4.2 Fabrication of Au Lines on Sidewalls

The mask design of line patterns is shown in Fig. 3.17(a). Each individual line was 100 μm long and 20 μm wide. The horizontal distance between two neighboring lines was 20 μm. Fig. 3.17(b) shows a PDMS membrane that was placed above a channel as a shadow mask during Au deposition. This membrane had hollow lines, and was about 8 μm thick. During the thermal deposition, α was also set as 35^0 to ensure that Au would be coated on a channel sidewall. β was approximately 5^0, which met the requirement given in (3.9).

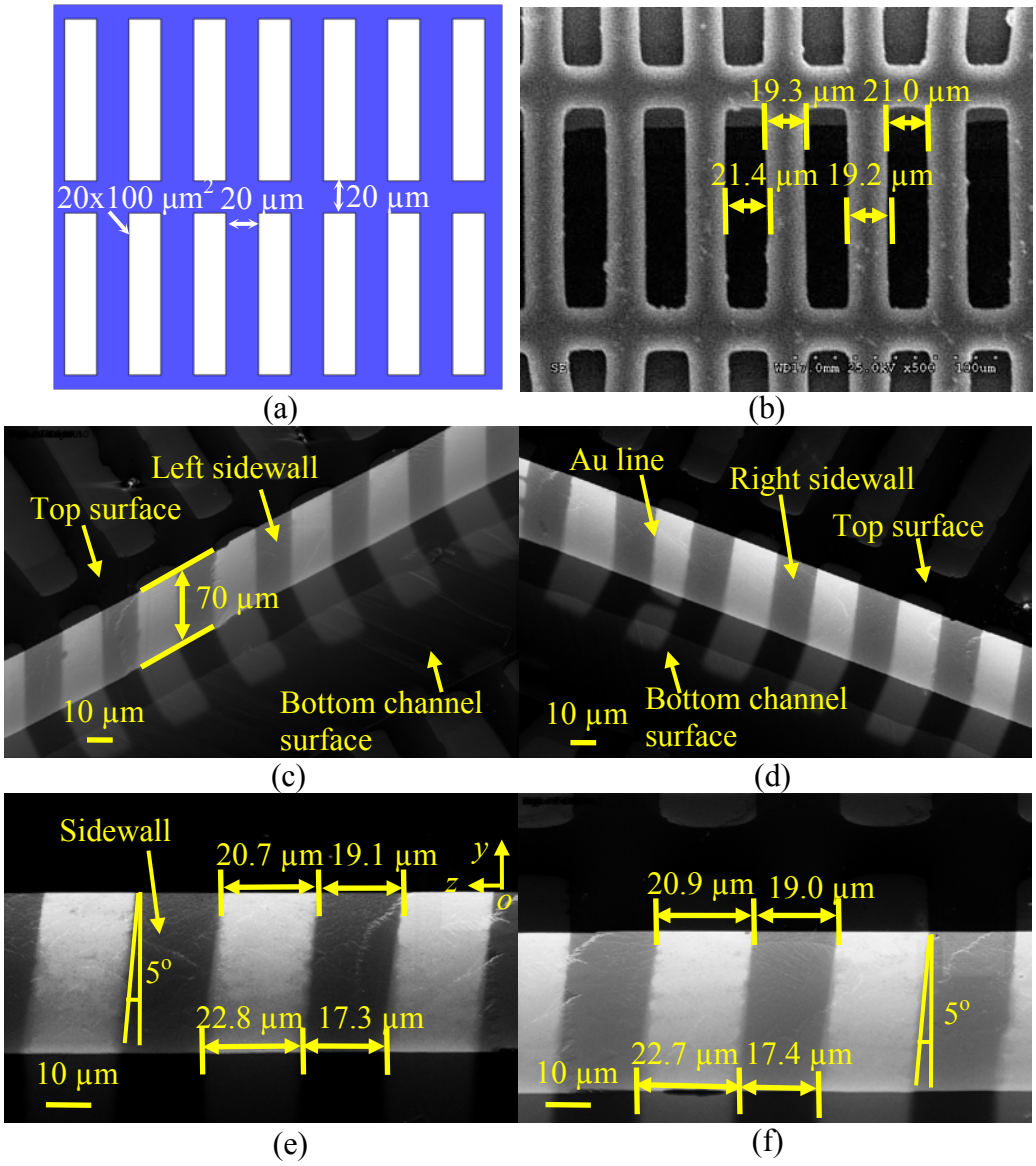


Figure 3.17 Fabrication of Au lines on two sidewalls (a) designed line patterns on the mask, (b) a reprehensive PDMS membrane of hollow lines placed on the silicon channel, 3D views of Au lines generated on (c) left and (d) right sides of the silicon channel and front views of Au lines on the (e) left and (f) right sidewalls.

An array of Au lines was generated on either channel sidewall (Figs. 3.17c-3.17f). t_1 was also 5 nm. By equation (3.10), the thickness of the generated Au lines was 2.9 nm as well. It was found that the size of the features in the PDMS shadow mask has relatively large variance comparing with their counterparts in the designed mask (Fig. 3.17b). The average width of the hollow lines was 21.0 μm at the end of the line feature, and was 21.4 μm in the

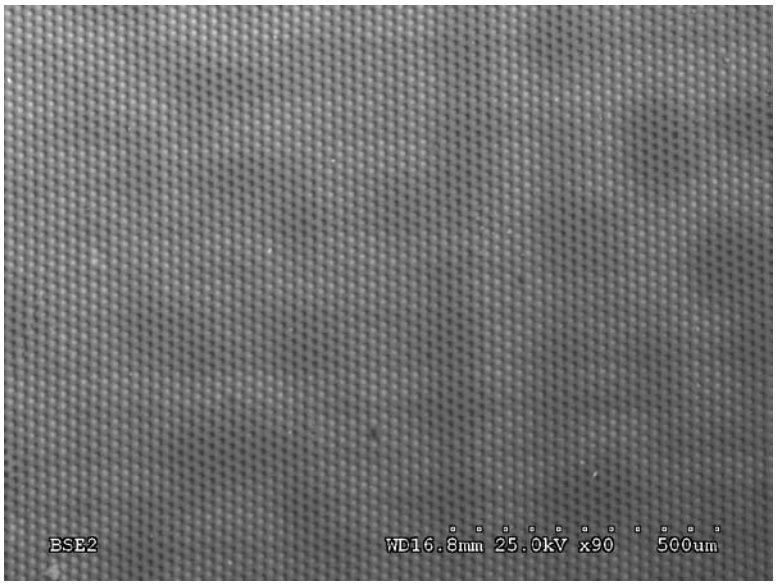
middle. The average width of the PDMS line was 19.3 μm at the end of the line feature, and was 19.2 μm in the middle. These values were applied during theoretical prediction.

The average width of a generated Au line (i.e., l_{pz}) at the top edge of the channel sidewall was 20.7 μm on the left sidewall (Fig. 3.17e), and 20.9 μm on the right sidewall (Fig. 3.17f). Accordingly, the theoretical value of the width of Au line (i.e., l_{pz}) at the top edge of the channel predicted by equation $(3.6)_1$ was 20.4 μm. The average distance between Au lines at the top edge of the channel sidewall was 19.1 μm on the left sidewall (Fig. 3.17e), and 19.0 μm on the right sidewall (Fig. 3.17f). The theoretical value predicted by equation $(3.6)_4$ was 19.9 μm.

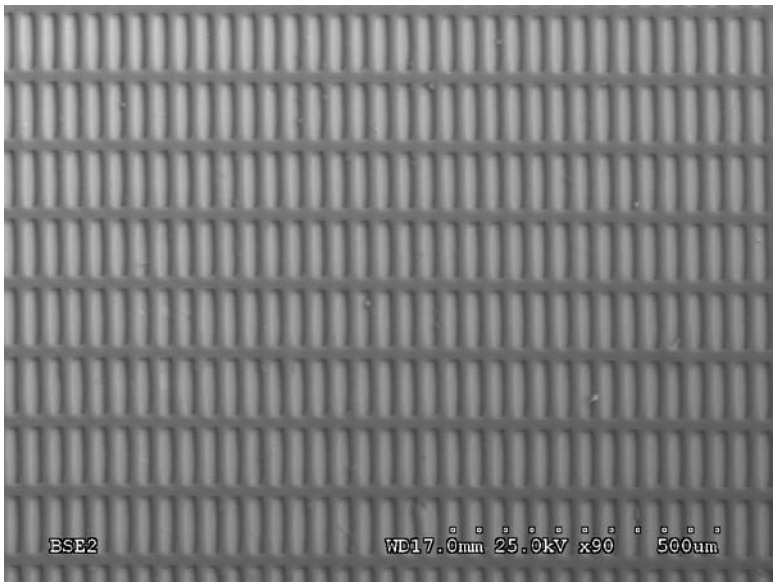
The average width of a generated Au line at the bottom edge of the channel sidewall was 22.8 μm on the left sidewall (Fig. 3.17e), and 22.7 μm on the right sidewall (Fig. 3.17f). The theoretical value predicted by equation $(3.6)_1$ was 22.5 μm. The average distance between Au lines at the bottom edge of the channel sidewall was 17.3 μm on the left sidewall (Fig. 3.17e), and 17.4 μm on the right sidewall (Fig. 3.17f). The theoretical value predicted by equation $(3.6)_4$ was 18.1 μm.

In conclusion, the errors in predicting the dimensions of Au lines using the theoretical relationships given in (3.6) along both *z* direction was within 0.5 μm at the top edge, and 0.3 μm at the bottom edge. The errors in predicting the distance between Au lines using the theoretical relationships given in (3.6) along both *z* direction was within 0.9 μm at the top edge, and 0.8 μm at the bottom edge.

The peeled off membranes for dots and lines after evaporation were shown in Fig. 3.18. The membranes were still in good shape, only contained with some stains.



(a)



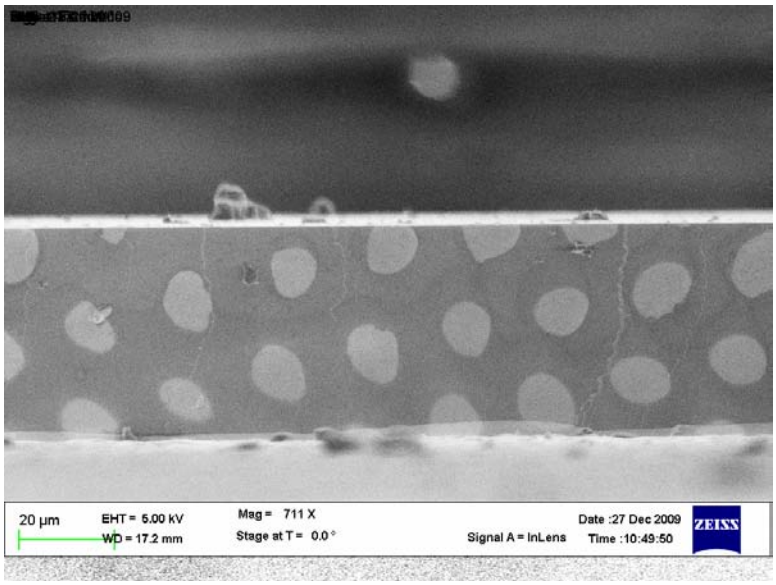
(b)

Figure 3.18 Membranes after using (a) for dots and (b) lines.

3.3.4.3 Alignment

Alignment is an important issue during microfabrication. Bad alignment may lead to the failure of devices. As shown in Fig. 3.19, when the alignment is not conducted properly, the lines are no longer vertical to the edge of the channel as expected. Another case is that if the

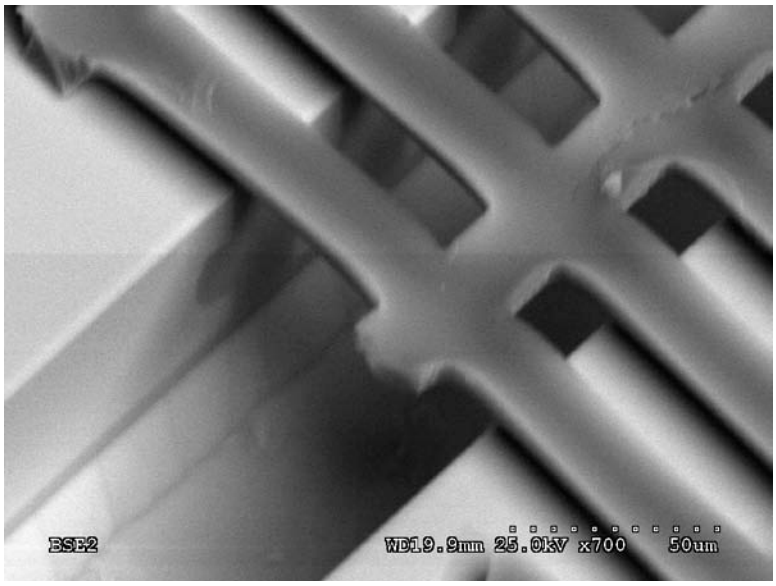
PMDS line in the horizontal direction locates right above the channel as in Fig. 3.19(a), the lines produced on the sidewall might not be continued due to shadow effect, Fig. 3.19(b). The horizontal lines blocked the Au vapor.



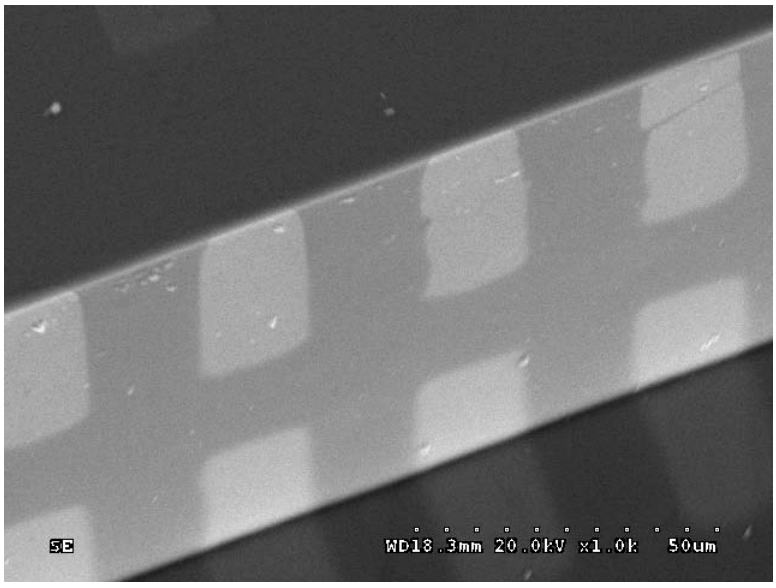
(a)

(b)

Figure 3.19 Misalignment for (a) dots and (b) lines.



(a)



(b)

Figure 3.20 (a) Horizontal PDMS line above the channel and (b) discontinuous Au lines produced on the sidewall.

A so called self-alignment technology in shadow mask technology was reported in [77]. As shown in Fig. 3.21, 3D structures were etched on the shadow mask, which were fitted into the cavities on the substrate. The materials of the shadow mask and the substrate were silicon.

SU-8 pillars were used in [93] to limit the movement of parylene-C shadow mask for multilayer evaporation purpose, Fig. 3.22. In this approach, SU-8 pillars were first fixed on the substrate serving as positioning posts. Shadow mask was limited to move in between the posts.

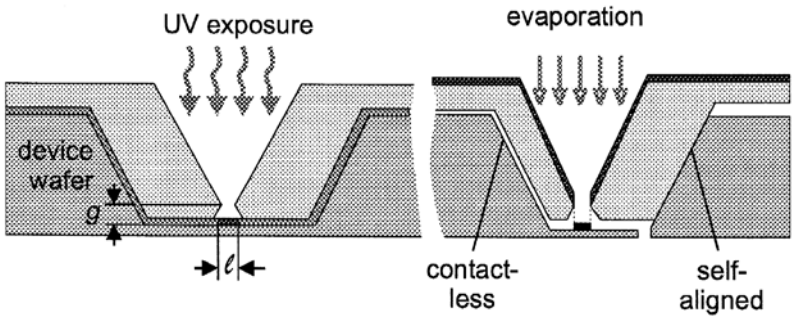


Figure 3.21 Self-aligned shadow mask [77].

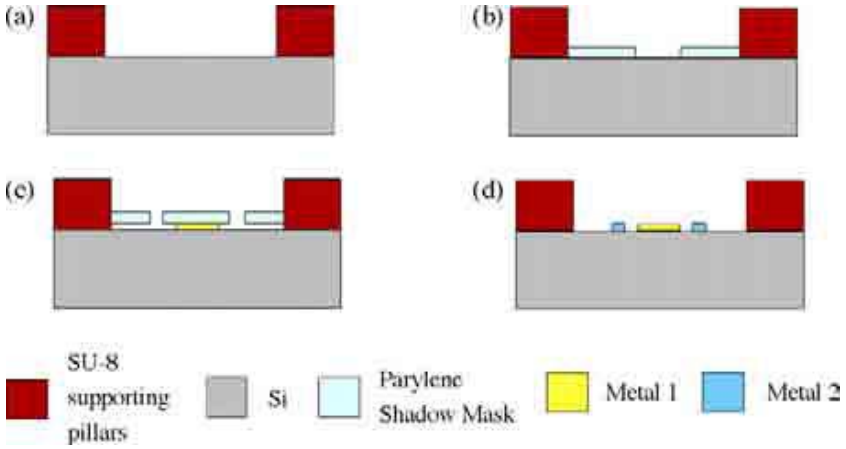


Figure 3.22 Using SU-8 pillars for multilayer shadow mask alignment: (a) fabricate 250 μm thick SU-8 pillars, (b) place the first shadow mask, (c) deposit metal and then peel off the first shadow mask and place the second shadow mask, and (d) peel off the second shadow mask [93].

In our work, the alignment currently was conducted under a microscope by manual manipulation using tweezers. IPA was added to the sample to keep the membrane wet and therefore to make it moving freely. The membrane bonded with the substrate tightly after IPA evaporating out. To further increase the accuracy of alignment, an alignment step may be added to the PDMS membrane, Fig. 3.23. The step is at one end of the membrane. During alignment, the step may be aligned with one sidewall of the etched features thus to increase the

accuracy of alignment. To fabricate the PDMS step, a channel is suggested to be etched in silicon substrate before generating SU-8 structures, Fig. 3.24.

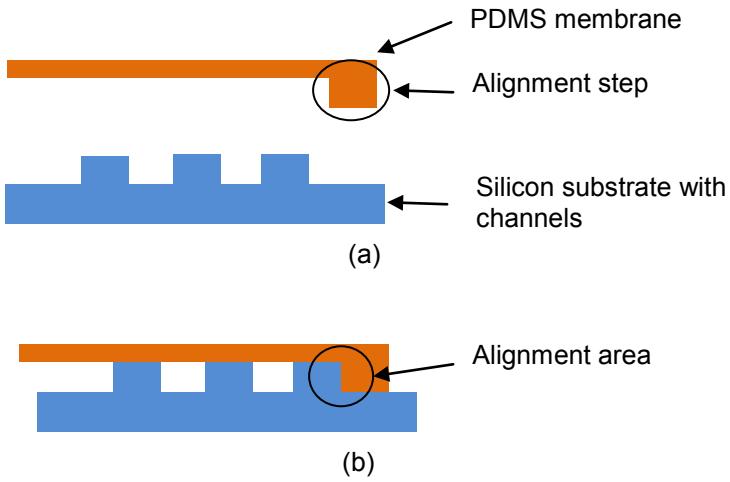


Figure 3.23 Suggested alignment approach (a) before contact and (b) after contact.

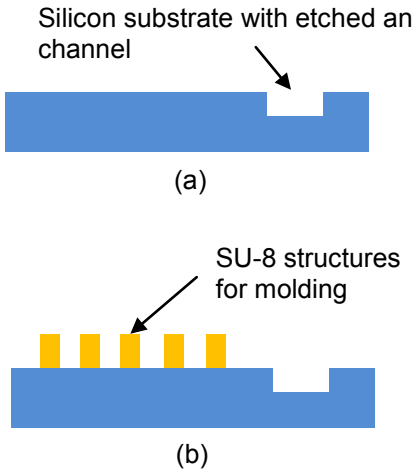


Figure 3.24 Substrate for fabricating PDMS membrane with alignment step (a) silicon substrate with an etched channel and (b) SU-8 structures for molding.

3.4 Summary

This chapter demonstrated two approaches to fabricate Au microdots and microlines on vertical silicon sidewalls using PDMS membrane with hollow structures as shadow mask. The PDMS membrane was placed against the sidewall in the first approach. 10 μm Au dots and 20-μm-wide Au lines have been produced on 110- and 70-μm-high silicon sidewalls, respectively.

Different with the first approach, the PDMS membrane was placed over the channels in the second approach. 10 μm Au dots and 20-μm-wide Au lines have been produced on 70-μm-high silicon sidewalls, respectively. 3D geometric models were established to predict shapes, thicknesses and dimensions of generated patterns for the second approach.

The Au dots generated on the vertical silicon sidewalls could be potentially applied as seed patterns to guide the horizontal growth of, for example, ZnO nanowires [94], which could directly serve as nanocantilevers. In the meanwhile, the vertical Au lines produced could potentially function as interconnects to link the circuits located on the top and bottom surfaces, forming 3D circuits.

CHAPTER 4

FABRICATION OF METAL MICROLINES ON THE OUTER SURFACES OF GLASS MICROPIPETTES

4.1 Introduction

This chapter addresses the fabrication of patterns on irregular surfaces, particularly the sharp tip of a glass micropipette. A glass micropipette includes a straight part and a curved tip, Fig. 4.1. It is manufactured from a straight tube of cylindrical cross sections. One end of the tube is heated and pulled to form a curved tip. The end of this tip could be made very small and may have an outer diameter down to 2 μm. Due to the small sizes of their tips, the glass micropipettes have been applied for electrochemical microboring [95], pH measurements [96-98], creation of non-thermal plasma [99], destruction of bacteria [14], recording of membrane potential [12, 100, 101], creation of well-defined electric field patterns [102], and detection of L-glutamate release from mouse brain slices [103].

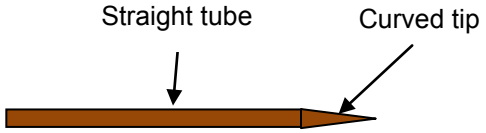


Figure 4.1 Schematic of a micropipette.

Take the generation of a metal line as an example. In either approach, a force is applied to make a PR-coated membrane have local contact with the metal-coated tip. As this force moves along the tip direction, the membrane contacts the tip from the beginning to the end of this tip, transferring a continuous PR line to the tip. A metal line is subsequently generated on the curved tip after removing extra metal using the PR line as a masking pattern in metal etch solution. The two approaches mainly differ in the ways of making the PR-coated membrane have intimate contact with the curved tip. A clip is used in the first approach to push

the PR-coated membrane, while in the second approach a nitrogen flux is applied for this purpose.

4.2 Design Criteria

Fig. 4.2 gives the configuration when a PR–coated membrane was pressed against a metal-coated micropipette to generate a continuous PR line on the micropipette. Let *d*, *t*, *w* and *h* denote the outer diameter of the micropipette at the point of contact, the thickness of PR, the width of the contact line, and the maximum depth that the micropipette penetrated into the membrane. It can be readily shown that

$$w = 2\sqrt{(h+t)(d-h-t)}\,. \tag{4.1}$$

It is observed from equation (4.1) that *w* is related to *d*. The curved tip has a non-uniform cross section, i.e., that value of *d* is not constant along the tip of the micropipette. To make a PR line have a uniform width, by equation (4.1), the only possibility is to vary the value of $(h+t)$ at different contact points of the PR-coated membrane and the micropipette. This appears difficult to realize since currently no instrument could change either *h* or *t* in such a way. On the other hand, the metal lines finally generated on the micropipette would serve as, for example, interconnects, and would not necessarily have uniform widths. Hence, in this work, we focused on fabricating two separate Au microlines on a micropipette, instead of controlling their widths. The same applies to the two PR lines.

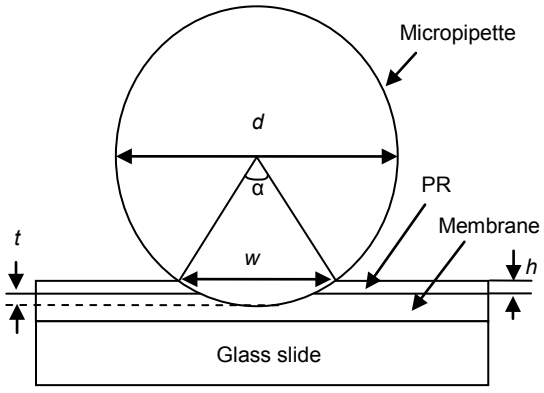


Figure 4.2 Schematic of the contact between a PR-coated membrane and a micropipette (cross-sectional view).

In the case of patterning the straight tube, *d* is fixed and much larger than *h* and *t*. Accordingly, *w* can be re-written as

$$w = 2\sqrt{d(h+t)}\,. \tag{4.2}$$

It can be seen from this equation that, for a fixed *d*, *w* is related to both *h* and *t*, and linearly increases with $\sqrt{(h+t)}$. In order to fabricate two separate lines on the straight tube which has a diameter of, for instance, 1 mm (i.e., *d*=1 mm), the width of either line should be less than 1 mm to avoid the contact with each other. Thus, the maximum value of *w* should be less than 1 mm. By equation (4.2), $(h+t)$ should be less than 0.25 mm. According to our preliminary tests, when the PR was more than 0.5 μm thick, it could be transferred from the membrane to the micropipette after they had contact. That is, *t* should be 0.5 μm or above. In this work, the spin-coated PR was 1 μm thick. Accordingly, the maximum allowable depth of penetration is 249 μm, i.e., $h = 249$ μm. This requirement of penetration would be relatively easy to meet with the careful control of the penetration.

In the case of patterning the curved tip, whose end may have an outer diameter as small as, for example, 5 μm, by equation (4.1), two requirements have to be satisfied in order to generate two separate PR lines on the curved tip: $(h+t)$ should be less than 5 μm to make the term inside the square root of equation (1) have a positive value; and *w*<5 μm. With the aid of equation (4.1), the second requirement implies

$$(h+t-2.5)^2 \geq 0\,. \tag{4.3}$$

This equation indicates that the second requirement is always met no matter what value $(h+t)$ has. In summary, to generate two separate lines on a curved tip, $(h+t)$ should be less than 5 μm. Since *t*=1 μm, *h* should be less than 4 μm. The maximum depth of penetration *h* is influenced by both the stiffness of the membrane and the force used to press the membrane. In this work, small depth of penetration was produced by making the contact force as small as possible.

According to the above consideration, it would be relatively easy to fabricate two separate PR lines on the straight part of a micropipette, while difficult to do so on the curved tip due to two concerns: (i) the tip has a non-uniform cross section, and (ii) the diameters of the curved tip are smaller than that of the straight part. The successful generation of two separate PR lines on the curved tip would depend on whether the PR-coated membrane could have intimate contact with the curved tip, and whether the contact force could be controlled to be small. These two points were particularly investigated in the experiments.

4.3 Experimental Procedures and Results

The straight part of a micropipette used in this work has an outer diameter of 1 mm, an inner diameter of 0.75 mm and a length between 40 mm and 50 mm. The length of the tip is between 7 and 12 mm. The outer diameter of the tip opening ranges from 50 μm to 5 μm. The PR used is S1813 (Shipley Company). The membrane employed to transfer PR to the micropipette is a single-sided tape (Ultratape #1310, Delphon Industries). It is 75 μm thick**.** The used membrane should be thin and soft such that it could be locally bent to have intimate contact with a curved tip at each point of this tip, and should also be compatible with a PR such that the PR could be spin-coated on this membrane.

4.3.1 First Approach to Fabricate Au Lines on Glass Micropipettes

In the first approach, a bulldog clip is adopted to press the PR-coated membrane against the curved tip, making them have local contact. Six basic steps are included in the fabrication of two separate Au lines on a micropipette (Fig. 4.3).

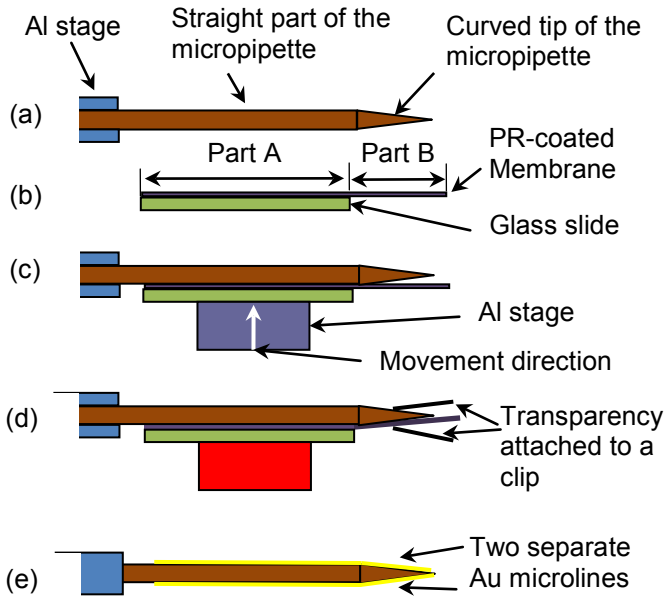


Figure 4.3 Schematics of fabrication procedures of the first approach (top views): (a) deposit 100-nm-thick Au on the micropipette, and fix it between two Al stages, (b) attach a membrane to a glass slide and spin-coat PR on the membrane, (c) push Part A of the PR-coated membrane against the micropipette, transferring PR to the micropipette at the contact place (a PR line is formed on the straight tube of the micropipette after the contact), (d) press Part B of the membrane against the curved tip using a transparency-covered clip to form a PR line on this tip, and (e) fabricate another PR line on the other side of the micropipette using the same process, etch the Au film using the two PR lines as masking patterns, and generate two separate Au lines on the micropipette after the removal of the two PR lines.

First, deposit a 100-nm-thick Au film on the micropipette, and fix the straight end of the micropipette between two Al stages (Fig. 4.3a). The micropipette is horizontally oriented and suspended about 5 mm above the bottom surfaces of the Al stages.

Second, place a membrane on a glass slide, spin-coat a layer of PR on this membrane, and fix the glass slide on a third Al stage using a double-sided tape (Scotch Company) (Fig. 4.3b). Part of the membrane lies on the glass slide, and for simplicity is called Part A. The other part is extended outside, and is called Part B.

Third, slowly push the third Al stage horizontally towards the micropipette, and stop whenever a small resistance is sensed, which indicates Part A of the membrane has contact with this micropipette (Fig. 4.3c). This step is used to create a straight PR line on the straight part of the micropipette.

Fourth, push Part B of the PR-coated membrane against the tip portion of the micropipette using a clip. The clip is moved horizontally along the micropipette direction all the way from the beginning to the end of the tip to ensure that the whole tip has contact with Part B of the membrane (Fig. 4.3d).

Fifth, detach the membrane from the micropipette, leaving a continuous PR line on the micropipette.

Sixth and finally, repeat the above five steps to generate a PR line on the other side of the micropipette. After the Au film is etched using the two PR lines as masking patterns, followed by the removal of the PR using acetone, two separate Au lines are produced on the outer surface of a micropipette (Fig. 4.3e).

In the fourth step, soft transparencies (commonly used as projector films) are attached to both sides of the clip using double-sided tape. The transparencies are used to avoid the direct contact of the rigid clip with the tip, which may damage the tip. The transparency, pushed by the clip, presses the PR-coated membrane against the curved tip at the contact point. The force generated through this approach is small, which avoids cracking the brittle tip. On the other hand, this force is large enough to make the membrane have good contact with this curved tip. Besides, the transparency on the opposite side of the micropipette also provides a force to the tip, which prevents the tip from breaking due to the uneven force. The clip is moved horizontally along the curved tip. Accordingly, the membrane and this tip have intimate contact along this moving path, leaving a continuous PR line on the outer surface of the curved tip.

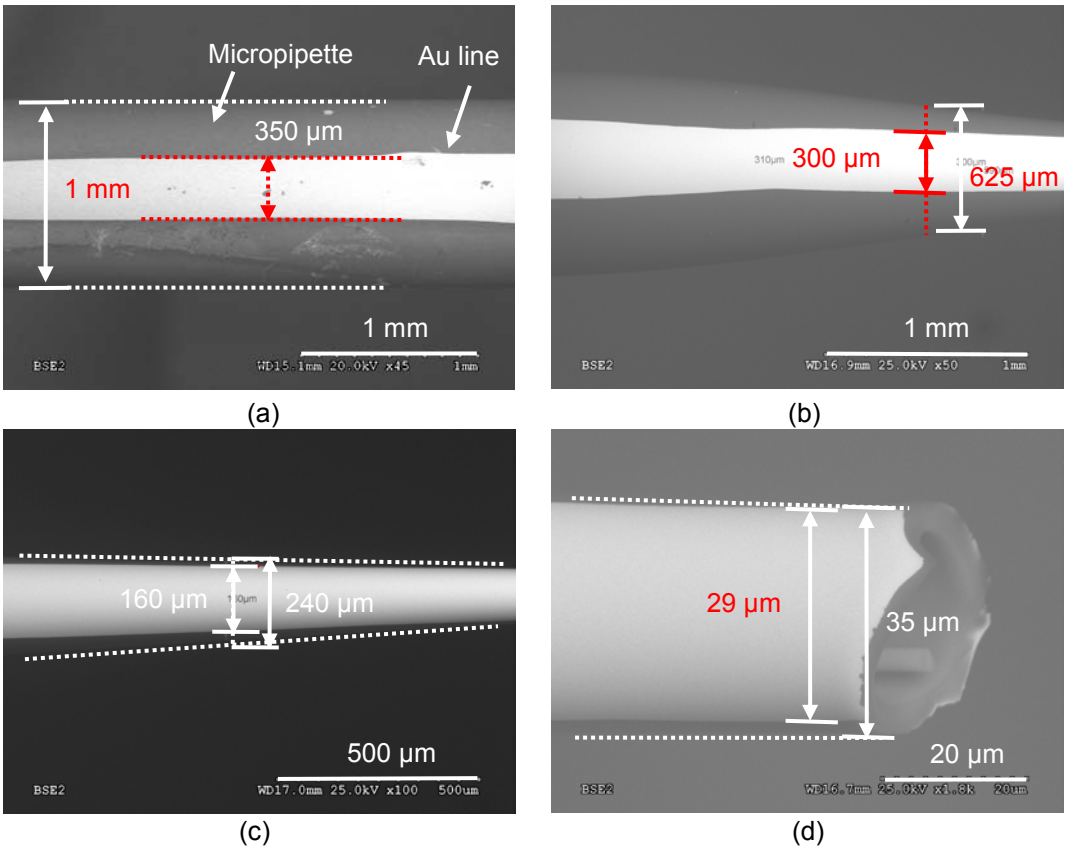


Figure 4.4 SEM images of a generated Au line at (a) the straight tube, (b) the intersection between the straight and tip portions, (c) the middle of the tip, and (d) the end of the tip of a micropipette. It was fabricated using the first approach.

Figure 4.4 shows SEM images of a Au microline fabricated on the straight part, intersection of the straight tube and the tip, the middle of the tip, and the end of the tip of a micropipette. The average width of the Au line was 350 μm at the straight part of the micropipette. The width of the line was not uniform at the intersection since different forces might be applied in the third and fourth steps, which resulted in different depths of penetration. The width of the Au line on the tip gradually decreased from 300 μm at the intersection of the straight tube and curved tip to 29 μm at the end of the tip due to the decrease in the outer diameter of the tip, as observed from equation (4.2). The outer diameter of the micropipette is 35 μm at the end of the tip. This is also the smallest tip on which we have successfully fabricated two separate Au lines using the first approach. Due to its small size, the curved tip

was easy to break at its end due to a relatively large contact force that was generated using the clip, particularly when the end had an outer diameter below 10 μm.

4.3.2 Second Approach to Fabricate Au Lines on Glass Micropipettes

The second approach was developed to reduce the possibility of breaking a small tip. In order to decrease the contact force, a nitrogen flux, instead of a clip, was adopted to press the PR-coated membrane against the curved tip of a micropipette. In this approach, four basic steps are involved (Fig. 4.5).

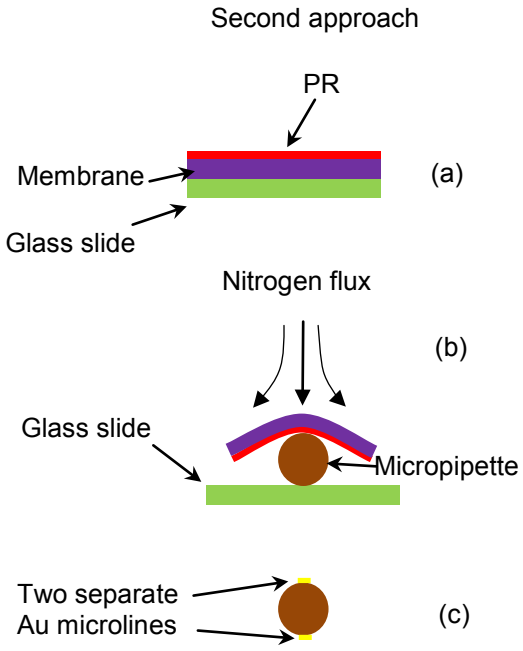


Figure 4.5 Schematics of fabrication procedures of the second approach (a) spin-coat a layer of PR on a membrane, (b) place the PR-coated membrane over the micropipette and blow nitrogen to press this membrane against the micropipette (a PR line is formed on the micropipette after the separation of the membrane and the micropipette), and (c) fabricate another PR line on the other side of the micropipette using the same process, etch the Au film using the two PR lines as masking patterns, and generate two separate Au lines on the micropipette after the etch of the two PR lines.

First, place a membrane on a glass slide, and spin-coat a layer of PR on this membrane (Fig. 4.5a).

Second, remove the PR-coated membrane from the glass slide and place it over a PR-coated micropipette, which is fixed on another glass slide using double-sided tape (Fig. 4.5b).

Third, blow nitrogen gas along the micropipette direction to make the PR-coated membrane have intimate contact with the micropipette (Fig. 4.5c).

Fourth, detach the membrane from the micropipette, leaving a continuous PR line on the outer surface of the micropipette. This PR line was extended from the straight tube to the end of the tip.

Fifth and finally, repeat the above four steps to generate another PR line on the other side of the micropipette. After the Au film is etched using the two PR lines as masking patterns, followed by the removal of the PR using acetone, two separate Au lines are produced on the outer surface of a micropipette (Fig. 4.5c).

Figure 4.6 shows SEM images of two Au microlines fabricated on a glass micropipette whose tip opening had an outer diameter of 5 μm. This is also the smallest tip on which we have successfully generated two separate Au lines using the second approach. The average widths of the two Au lines were 320 μm and 250 μm, respectively, at the straight tube of the micropipette. The widths of both Au lines gradually decreased from over 200 μm at the intersection of the straight tube and curved tip to less than 5 μm at the end of the tip. The tip was not broken during the fabrication process. The contact force generated by the nitrogen flux in the second approach was smaller than that produced by the clip in the first approach. Accordingly, Au lines could be generated on a micropipette of a smaller tip using the second approach. On the other hand, the first approach might be applied to fabricate Au lines on multiple micropipettes during a single fabrication process. In the first fabrication step of the first approach (Fig. 4.3a), several micropipettes, instead of a single micropipette, could be placed between two Al stages. The third Al stage and the clip have flat surfaces and straight edges, respectively. They have direct contact with the PR-coated membrane, thus restricting vertical and horizontal movements of the PR-coated membrane during the subsequent patterning steps. This might ensure the PR-coated membrane to have intimate contact with each micropipette. Consequently, two separate Au lines would be generated on each micropipette at the end of the fabrication. However, the second approach is better used for patterning a single micropipette

during a fabrication process. The nitrogen flux covers a large area, and the flux pressure is not uniform across the covered area. Due to lack of constraints in the movements, the PR-coated membrane might not have good contact with each micropipette if multiple micropipettes were patterned simultaneously.

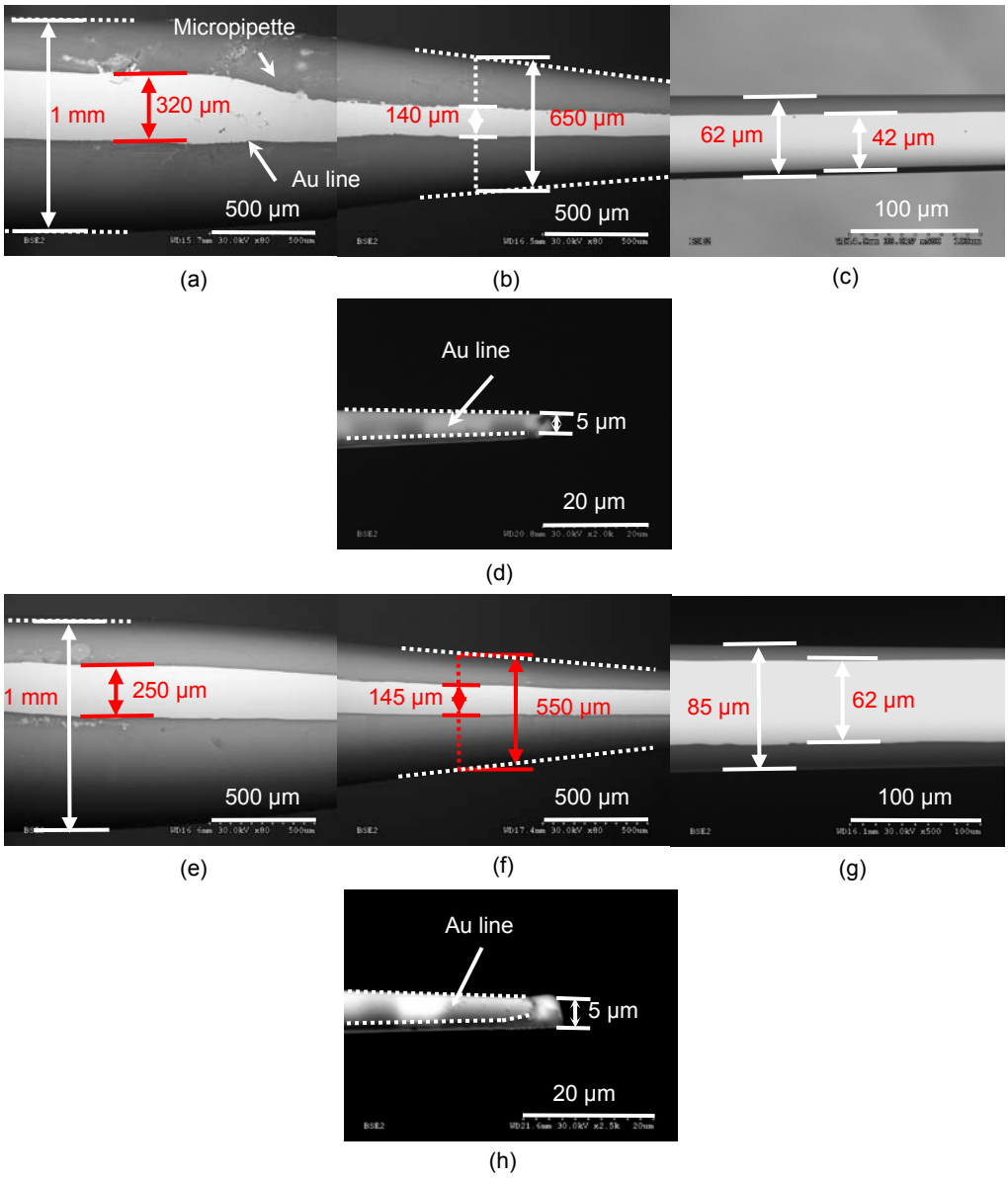


Figure 4.6 SEM images of two Au lines fabricated on a micropipette using the second approach. The first line at (a) the straight part and the intersection between the straight and tip portions, (b, c) the middle of the tip, and (d) the end of the tip of a micropipette; and the second line at (e) the straight tube and the intersection between the straight and tip portions, (f, g) the middle of the tip, and (h) the end of the tip of the micropipette.

The conductivity between the two Au lines generated a micropipette was measured. The current was zero, which further demonstrated that they were separate. To measure the resistance of these two Au lines, the end of the tip was dipped in a conducting silver epoxy. The silver epoxy coated on the end of the tip connected the two Au lines together. Their resistance was subsequently detected on a probe station using an electrical meter (model: Agilent 4155C LCR). Probes were attached to the Au lines at the straight tube of the micropipette. The resistances of the Au lines on the micropipettes of 35 μm and 5 μm tip openings were measured to be 95 and 140 Ω, respectively.

4.4 Failure Analysis

The pressure applied on the membrane is an important factor that affects final results. If the pressure is too large, the tip might break at the end as in Fig. 4.7. The large pressure can also create excessive deformation of the membrane with wet photoresist, which may make the tip fully covered with photoresist. Once the tip was fully covered with photoresist, the Au layer underneath cannot be etched off in the following step. No separated Au lines will be formed at the tip in this case, Fig. 4.8. It can also be observed from Fig. 4.8 that residues appeared at the tip after the final step. The residues were formed due to the chemicals left inside the micropipette. During Au etch process, some etch solution went into the micropipette due to capillary effect. If the sample was not cleaned enough after etch, the etch solution left inside the micropipette may come out after a while and contaminates the tip. To avoid the contamination, it is suggested that the sample should be thoroughly flushed after etch, and left in DI water for half hour or longer to remove possible chemicals inside the tube.

On the other hand, if the pressure applied on the membrane is too small. No enough pressure will be generated on the membrane for photoresist transfer. Therefore, the Au film on the micropipette is left without the coverage of photoresist during Au etch process. This usually happened at the tip end of the micropipette. The Au at tip was totally etched off as in Fig. 4.9.

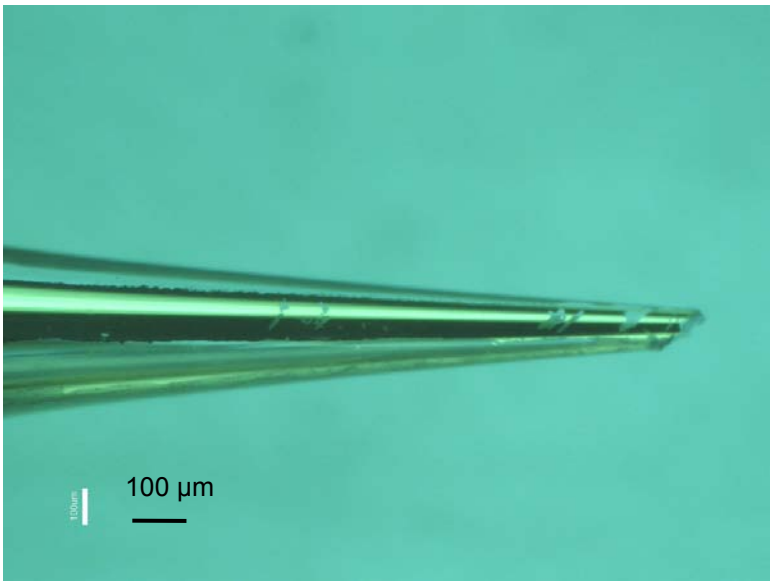


Figure 4.7 A broken tip due to exceeded pressure.

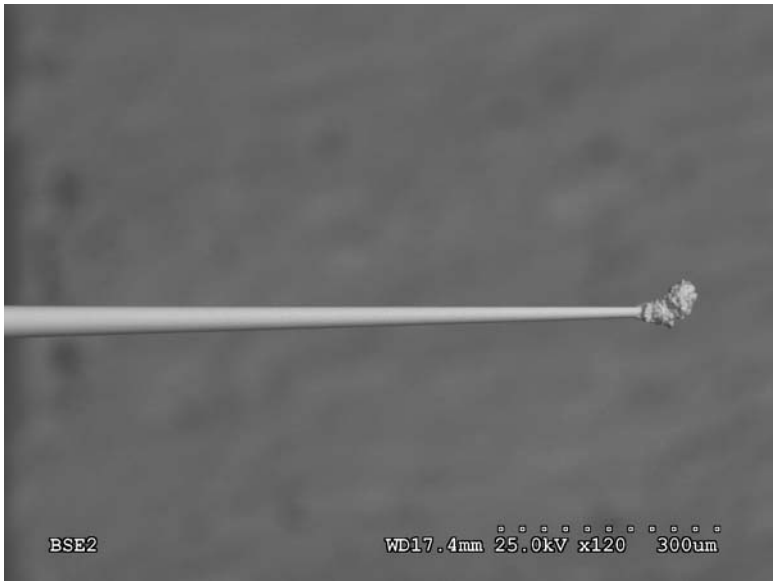


Figure 4.8 A tip fully covered with Au and contaminated by chemical residues.

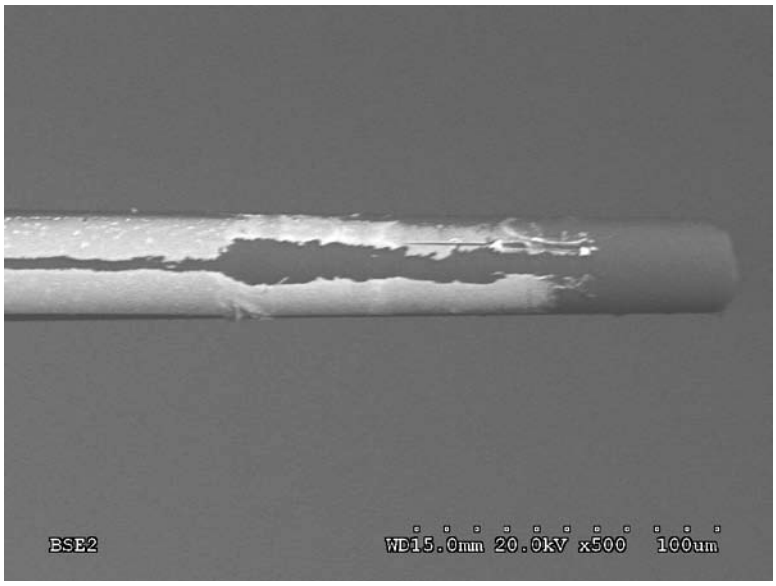


Figure 4.9 A tip without Au coverage.

4.5 Summary

In this chapter, two approaches have been developed to fabricate Au microlines on the outer surfaces of glass micropipettes. Using either approach, two separate microlines have been successfully fabricated on the outer surface of a glass micropipette. Either line was extended from the straight tube to the curved tip of the micropipette. Resistances of the generated Au lines were in the order of 100 Ω. These approaches are easy to apply since no sophisticated equipment is required. They could also be potentially applied to fabricate line patterns on other irregular surfaces.

CHAPTER 5

GENERATION OF LINKED ZnO NANOWIRES

5.1 Introduction

ZnO nanowire has many good features, such as wide band-gap of 3.34 eV at room temperature, large excitation energy (60 meV), piezoelectric, and bio-safe. Each of these properties may lead to different kinds of potential applications [104-106]. The wide band-gap at room temperature and large excitation energy make ZnO nanowire a good candidate for opto-electronic devices including light emitting diodes (LED) and laser diodes [105]. Piezoelectric effect of ZnO nanowire is mainly applied in sensor and power generation applications. For a vertical ZnO wire, once it is bent by an external force, a potential drop is created across the wire, with the stretched surface being positive and compressed surface being negative [107].

For solar purpose, ZnO nanowire layer based solar cells was reported in [108]. PN junction was formed by ZnO and polymer. Since the distance between nanowires was smaller than mean free path of electrons almost all emitted electrons are collected. Hybrid polymer solar cells based on zinc oxide is introduced in [109]. Hybrid polymer solar cells use polymer and inorganic semiconductor to convert sunlight into charges. It may has advantages of being morphologically more stable and being able to utilize the high charge carrier mobility of the inorganic material [109]. ZnO nanowires imbedded in PDMS film served as antireflection layer in solar system was reported in [110]. ZnO nanowires were firstly synthesized on silicon dioxide substrate through hydrothermal approach. Uncured PDMS solution was spread on the substrate with ZnO nanowires and cured. Finally, PDMS film was mechanically detached from the substrate with ZnO nanowires imbedded inside. Besides, ZnO nanowire-based dye-sensitized solar cell was described in [111].

For sensing purpose, ZnO nanowire based strain sensor was introduced in [112]. In this paper, the sensor was fabricated by bonding a ZnO piezoelectric fine wire laterally on a polystyrene substrate. Nanoforce sensor was illustrated in [113], which was composed of a ZnO nanowire bridging across two ohmic contacts. External force triggered field-effect transistor based on ZnO nanowire was introduced in [114]. This device consists of an Ag source electrode and Au drain electrode at each end of a ZnO nanowire, separated by PDMS. The configuration of most of these sensors is that a single ZnO nanowire is connected at the two ends. By applying a bending force to the nanowire, a potential is created across the bended nanowire due to piezoelectric effect. Meanwhile, [104] utilizes ZnO nanowire coated capillary for intracellular pH detection. Two electrodes have been used. One is coated with ZnO nanowires as working electrode, the other one, Ag/AgCl as reference electrode. Electrochemical potential difference between these two electrodes may be recorded using this configuration. An advantage of ZnO nanowire sensors is their small size, which allows intracellular sensing of physiological and biological species in nano-environments, and provides a strong, stable, and reversible signal with respect to pH changes. The detection sensitivity may reach single-molecule level [104].

For energy generation purpose, the potential of using ZnO nanowires as nanogenerators was explained in [115]. P-type ZnO nanowire produces positive voltage pulse when contacted by AFM tip. Voltage pulse was generated when the tip contacts the stretched side of the nanowire. In contrast, n-type ZnO nanowire produces negative output voltage, and when the tip contacts the compressed side of the nanowire. Nanogenerator driven by ultrasonic waves to produce continuous direct current output was developed in [116]. The Nanogenerator was fabricated with vertically aligned ZnO nanowires beneath a zigzag metal electrode with a small gap. The up and down movement of the electrode driven by the wave bend and/or vibrate the nanowires creates power due to the piezoelectric factor of ZnO nanowires. The main limitation of building nano-electronics by nano-components is it is not yet possible to selectively grow semiconducting or metallic nanowires or nanotubes [117].

In our experiments, it is interesting to find that in some cases two nanowires growing toward each other may link together. An intersection is formed between the nanowires. This phenomenon can be potentially used to build up novel nanostructures, such as two nanowires growing from each sidewall of a microchannel in the opposite direction may connected and be used for sensing and other purposes. Therefore in this chapter we aim to explore the mechanism of this phenomenon by observing and analyzing of the growing processes. A brief review of ZnO nanowire growing methods is provided, followed by the reports of growing linked ZnO nanowires through hydrothermal approach.

5.2 Methods to Grow ZnO Nanowires

Several approaches have been reported to fabricate ZnO nanowires, such as vapor-liquid-solid (VLS), hydrothermal, thermal evaporation, template-based growth, chemical vapor deposition, and pulsed laser deposition [118], among which VLS and hydrothermal are the two mostly investigated approaches in the area.

5.2.1 VLS Growth of ZnO Nanowires

The growth mechanism of VLS method was first proposed in 1964 by R. S. Wagner and W. C. Ellis [119]. It includes three stages (Fig. 5.1):

a. Formation of the liquid alloy droplet on the substrate where the wire is going to be grown from.

b. Introduction of the substance to be grown in vapor format.

c. Supersaturation and nucleation at the liquid/solid interface of the alloy droplet, which leads to nanowire growth [120].

In the first stage, alloy droplets are formed either by laser ablation or by annealing the very thin layer metallic film. The diameter of the droplets are usually around 10-20 nm. The alloy droplets act as catalyst for the growth, and determine the diameter of the nanowires. The metal should be physically active, while chemically stable [121]. Au is the most frequently used metal for the VLS process. Other metals, such as Al, Ag and Fe, that are used as catalysts have also been reported.

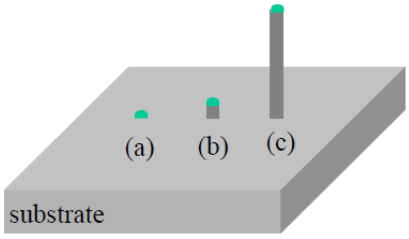


Figure 5.1 VLS ZnO nanowire growth (a) formation of catalyst drops, (b) precipitation and (c) grown nanowire.

In the second stage, source substances, usually contained inside aluminum crucible, are heated up to reaction temperature, which forms matters in gas format and are transported to substrate surfaces with inert gas, such as Ar.

The last stage, alloy droplets adsorb source gas and become supersaturated, which leads to the growth of nanowires.

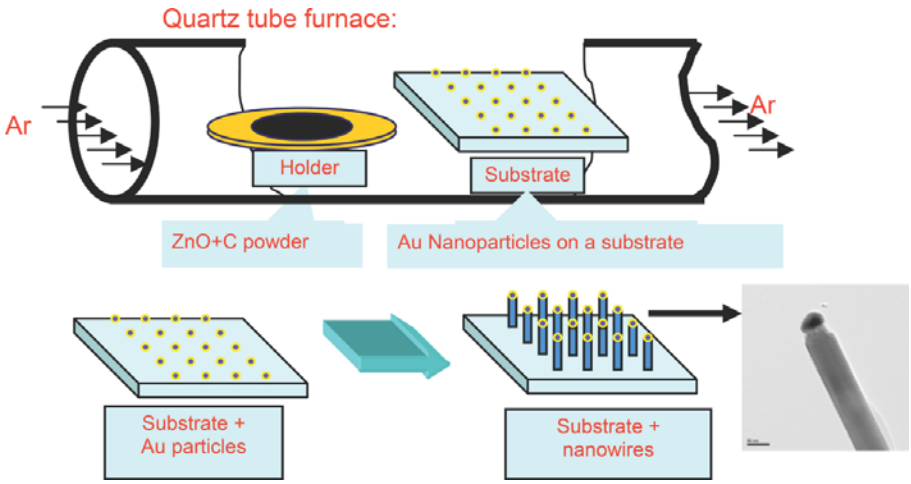


Figure 5.2 Setup of using VLS method to grow ZnO nanowires.

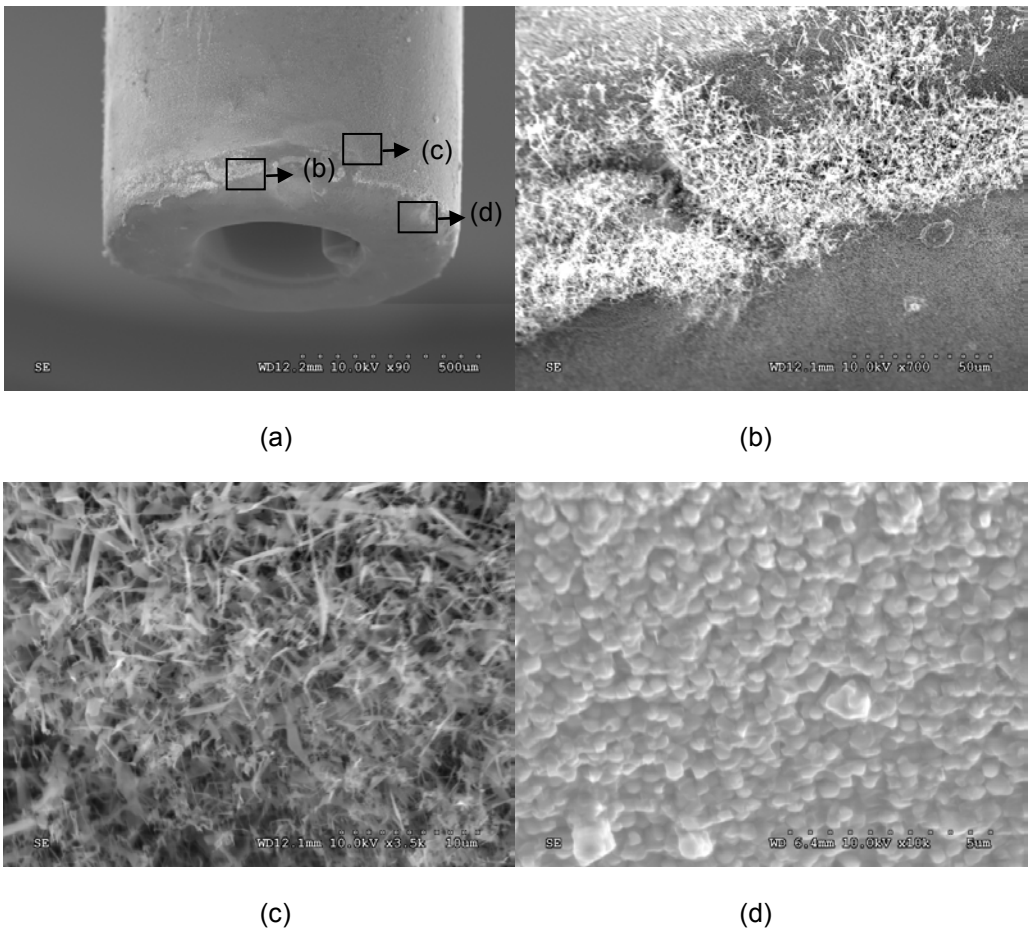
The setup of VLS growth is shown in Fig. 5.2. ZnO powder and graphite powder is mixed at 1:1 weight ratio in an alumina crucible and is put upstream of the sample in the furnace tube [122]. Samples with Au patterns are placed on the downstream from the crucible. Temperature for growth ranges from 800 to 1000 ^{o}C. ZnO powder is reduced by graphite to form zinc and CO vapors. Corresponding chemical reactions are expressed as

$$ZnO(s) + C(s) \rightarrow Zn(g) + CO(g)$$
$$CO(g) + ZnO(s) \rightarrow CO2(g) + Zn(g)$$

Meanwhile, Ar gas flows through the tube to carry the zinc, CO and CO2 vapors to the samples. Catalyzed by Au-silicon alloy, the following reactions took place at solid-liquid interface and obtained zinc oxide nanowires.

$$Zn(g) + CO(g) \rightarrow ZnO(nanowire) + C(s)$$
$$C(g) + CO2(g) \rightarrow 2CO(g)$$

Flow rate of Ar should not be too high, or zinc vapors will be taken away, and leading to low possibility of nanowire growth[122].



(a) (b)

(c) (d)

Figure 5.3 ZnO nanowires grown on Au coated glass tube by VLS method (a) overview, (b) zoom in at the cylindrical surface, (c) zoom in at the edge and (d) zoom in at the end of the tube.

ZnO nanowire growth using VLS approach has been tested. 0.3 g ZnO and 0.3 g C powders were placed in the aluminum crucible and located at the center of the furnace tube. Sample was placed downstream of Ar gas, and located at the edge of heating units. Temperature of the furnace was set at 925 ^{o}C and lasted for 2 hrs. Temperature at the sample was around 400 ^{o}C. To place sample at a lower temperature was for the purpose of ZnO vapor condense.

Fig 5.3 gives the results of the ZnO nanowire grown on a Au coated glass cylinder. The glass cylinder is 1 mm in outer diameter. Thickness of Au layer deposited is 4 nm. Because glass cylinder was horizontally placed in thermal evaporator for Au deposition, no Au has been deposited on the two ends of the glass cylinder. Therefore, no nanowires have been grown on the ends. While on the cylindrical surfaces, while Au has been deposited, nanowires have been densely grown.

5.2.2 Hydrothermal Growth of ZnO Nanowires

Hydrothermal approach growing of ZnO nanowires/rods has drawn a lot attention due to its low cost and low operation temperature, less than 100 ^{o}C, even at room temperature. On the contrary, VLS approach requires high growth temperature, 800-1000 ^{o}C. The low temperature requirement of hydrothermal approach opens gates to grow nanowires on substrates that cannot stand high temperatures, such as polymers. Besides, hydrothermal growth method does not need complicated facilities. VLS approach needs tools to deposit catalyst metals, growing furnace, and hydrothermal growth requires minimum facilities, usually beakers, balance and hotplate.

Hydrothermal growth includes two steps, substrate seeding and nanowire growth. In the first step, sample is usually seeded by spin coating the seed solution on the substrates. In the second step, samples are immerged in growth solution and heated up to growth temperature on a hot plate.

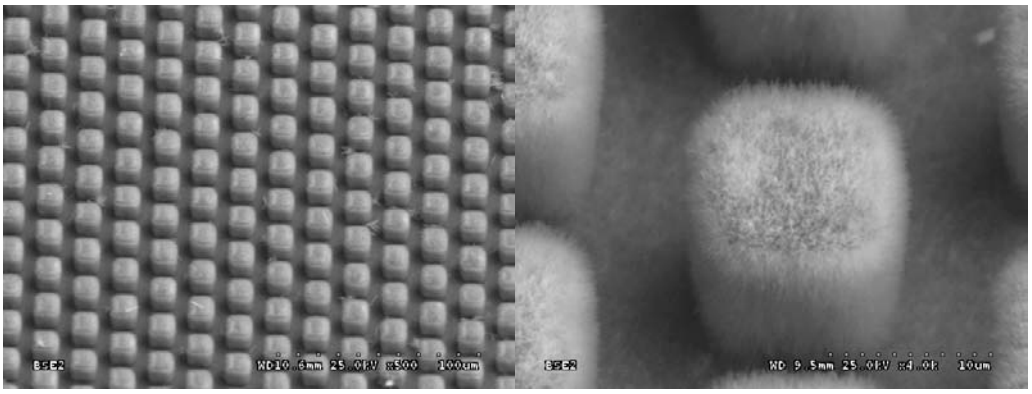
Different ways of preparing seed solution have been reported, such as

- NaOH solution in methanol (0.03 M) was added to zinc acetate dehydrate ($C_4H_6O_4Zn{\cdot}2(H_2O)$, 0.01M) in methanol solution at 60 ^oC and stirred for two hours [123].
- 0.01 M zinc acetate dehydrate in 1-propanol [124].
- 0.0055 M zinc acetate dehydrate in pure ethanol [104].
- 0.001 M zinc acetate and 0.0016 M NaOH at 35 ^oC with IPA [125].

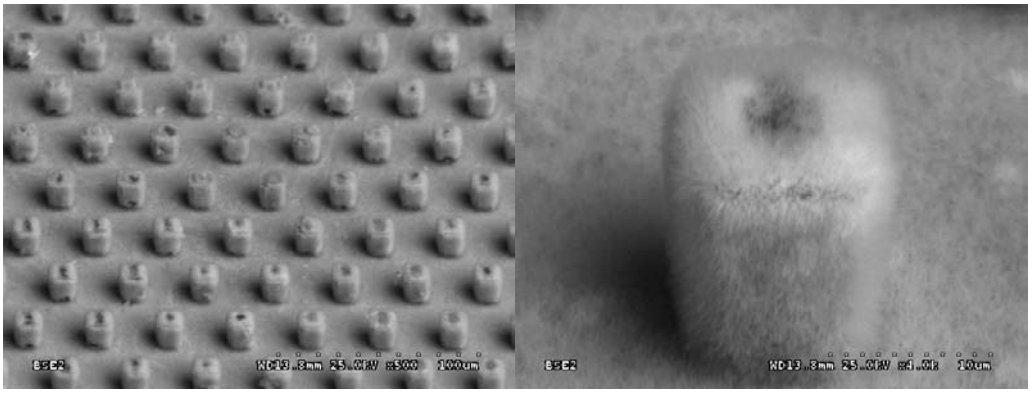
Sputtering [126] and CVD [110] methods for seeding were also reported. Meanwhile, unseeded substrate for growing was also reported [127].

Growth solution is usually prepared by equal mole zinc nitrate hexahydrate ($Zn(NO_3)_2{\cdot}6H_2O$) and hexamethylenetetramine ($C_6H_{12}N_4$) in DI water. Concentration varies from 0.005 to 0.025 M. Growing temperature ranges from room temperature to 95 ^oC. Growth time is from 15 min to days depending on the size of nanowires going to obtain [104, 110, 123-126, 128-132].

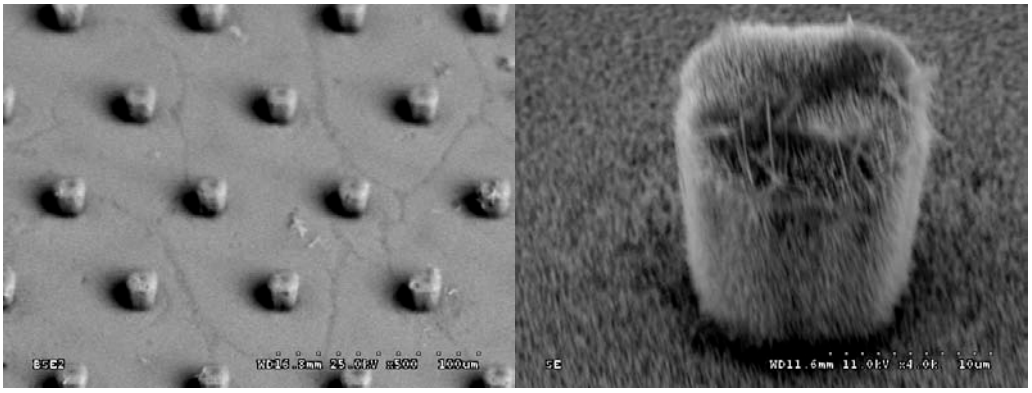
We have explored the possibility of growing ZnO nanowires on different kinds of substrates, such as silicon and SU-8. ZnO nanowires have successfully grown on SU-8 pillars, which could be used for superhydrophobic surfaces, Fig. 5.4. Two steps growing processes were applied as introduced above. Prior to spin coating, substrate was cleaned with acetone and IPA. Seed solution was prepared with 5 mM zinc acetate dehydrate in ethanol, and was continued stirred with a magnetic bar at 5000 rpm for half an hour. Spin speed was 2000 rpm for 30 s. If thick seed layer is desired, spin cycles may be repeated. Anneal the substrate on a hot plate at 100 ^oC for one minute after each spin to increase the adhesion between the nanocrystals and the substrate. Growth solution was prepared with equal mole (25 mM) zinc nitrate hexahydrate ($Zn(NO_3)_2{\cdot}6H_2O$, Sigma-Aldrich) and hexamethylenetetramine ($C_6H_{12}N_4$, HMT, Sigma-Aldrich) in DI water. HMT functions to adjust pH value of the solution. Growing temperature was 95 ^oC, for 12 h. Substrate was kept straight in the growth solution. After growth, substrate was rinsed with water, and baked dry on a hotplate at 100 ^oC for 5 min.



(a)



(b)



(c)

Figure 5.4 ZnO nanowires grown on SU-8 pillars of pitch size (a) 20, (b) 40 and (c) 60 μm.

The solution becomes blurt as the temperature increases. Once the temperature reaches 80 ^{o}C, the reaction becomes strong, and the solution looks milky. If the sample was put

in the solution earlier or at this moment, the particles in the solution might attach to the substrate and hard to remove. Hence, it is better to put the sample in the solution when the reaction is less strong. In our case the sample was put in the solution after 10 min as it reached 95 ^{o}C.

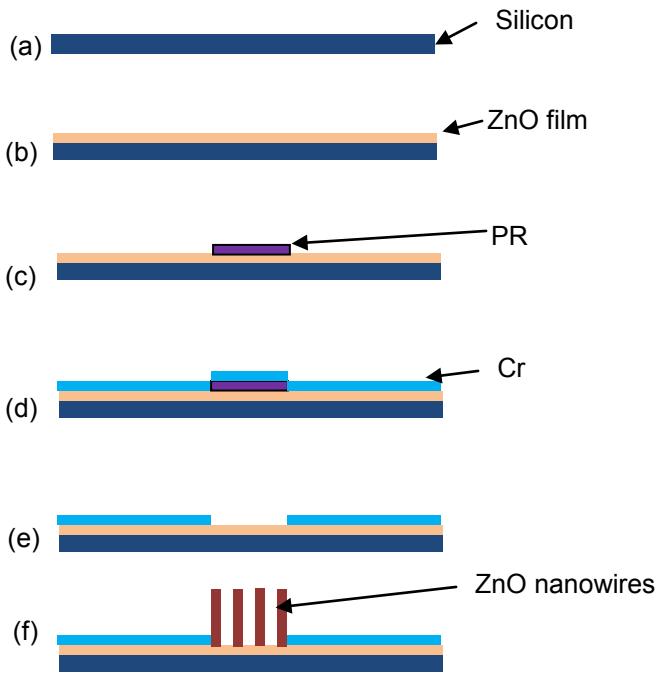
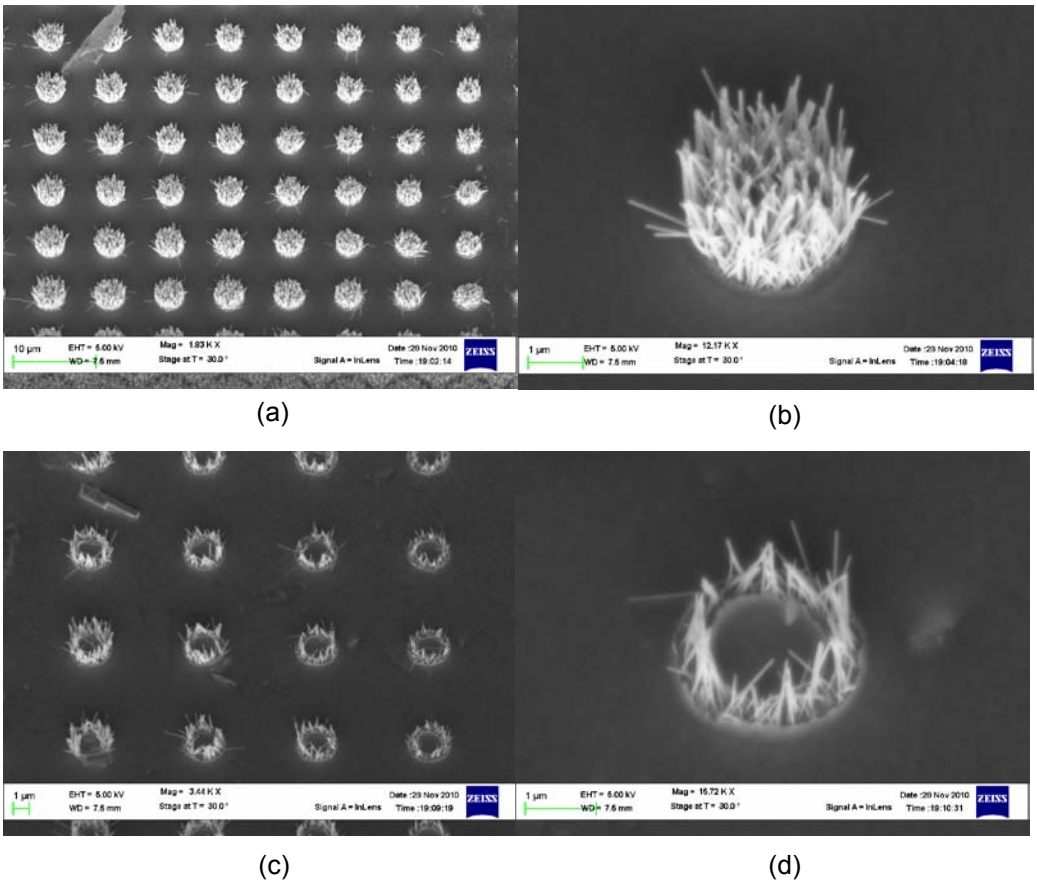


Figure 5.5 Procedures for selective growth of ZnO nanowires (a) silicon substrate, (b) deposition of ZnO seed layer, (c) photolithography, (d) Cr deposition, (e) liftoff and (f) Growth of ZnO nanowires.

ZnO nanowires were also grown selectively on silicon substrate using Cr as stopping layer. Growing procedures was shown in Fig. 5.5. Silicon substrate was sputtered with 100 nm thick of ZnO as seed layer, Fig. 5.5(b). Photolithography was conducted to define patterns on the sputtered ZnO layer, Fig. 5.5(c). 5 nm thick of Cr layer was thermal evaporated on the substrate functioned as stoppying layer during nanowire growth, Fig. 5.5(d). Acetone cleaning was introduced to remove the photoresist and the Cr above the photoresist, therefore to define the opening areas on the substrate, Fig. 5.5(e). Finally, Fig. 5.5(f), ZnO nanowires were selectively grown in the opening areas. The growth results were shown in Fig. 5.6. The dimater of the opening holes were 3 μm. For selective area growth, the mass of ZnO nanowires grown

per unit area for exposed surface increases as the distance between the exposed growth areas is increased and as the width of the exposed lines is decreased [127].



(a) (b)

(c) (d)

Figure 5.6 Selective growth of ZnO nanowires (a) in opening holes, (b) zoom in of (a), (c) in circular rings and (d) zoom in of (c).

5.3 Generation of Linked ZnO Nanowires through Hydrothermal Approach

As introduced above, nanowires may become linked during hydrothermal growth. To explore the mechanism of this phenomenon, it is important to understand the mechanism of ZnO single crystal growth under hydrothermal circumstance and to visualize the process of nanowire growth.

5.3.1 Growth Mechanism of ZnO Nanowire under Hydrothermal Circumstance

Growth mechanism of ZnO single crystals has been reported in [133-139]. It has been pointed out that the growth mechanism of oxide crystals contains two main steps: the formation

of growth units and the incorporation of growth units into the crystal lattice by a dehydration reaction [133]. The process of formation of growth units is also known as crystallization, where solute molecules dispersed in solvent start to gather into clusters. The process of incorporation of growth units into the crystal lattice then forms new growth interfaces.

Supersaturation is the driving force of the crystallization, since it represents the difference between the chemical potentials of a hydrate building unit in the solution and in the hydrate crystal [140]. Once the supersaturation is exhausted nucleation and growth stops. Diameters of the ZnO nanocrystals are dependent on the concentration of the aqueous solution [31, 141]. By decreasing the concentration of the precursors by one order of magnitude, the diameter of the rods shall decrease likewise by about an order of magnitude, due to the critical diffusion of the monomers and the subsequent limited growth. Microrods 1-2 μm wide were obtained at a concentration of 0.1 M zinc nitrate/methenamine, and therefore nanorods about 100-200 nm at 0.01 M, as well as nanowires about 10-20 nm wide at 0.001 M are targeted [141].

It has been pointed out that the growth kinetics of the ZnO particles follows diffusion-limited ripening process [142, 143]. The possible reaction steps from reactants to products in solution including [127]:

$$Zn^{+2} + H_2O \text{ — } ZnOH^+ + H^+$$

$$ZnOH^+ + H_2O - Zn(OH)_2 + H^+$$

$$Zn(OH)_2 - ZnO + H_2O.$$

These intermediate steps happen not only at the surfaces of growing ZnO nanowires but also in the bulk of the solution. So a major drawback of the hydrothermal approach is that ZnO forms both the seeded substrates and in the bulk solution simultaneously [144]. The formation of ZnO in the bulk solution results in rapid depletion of reactants and slows down the growth rate of nanowires [144].

ZnO crystal has a hexagonal wurtzite structure, Fig. 5.7. Regarding the growth rate, [136] claimed that ZnO structure has both polar and non-polar faces. The morphology of a

particular crystal is determined by the slowest growing faces. Polar faces with surface dipoles are thermodynamically less stable than non-polar faces and often undergo rearrangement to minimize the surface energy, which grows faster. [133] pointed out that the growth habit of crystals is mainly determined by the internal structure of a given crystal, and affected by external conditions such as temperature, supersaturation and pH value of the solution. It considered the relationship between the growth rate and the orientation of the coordination polyhedron at the interface, which led to the conclusion that the direction of the crystal face with the corner of the coordination polyhedron occurring at the interface has the fastest growth rate. Both works demonstrated that the growth rate at {0001} plane is faster than the growth rate at {0110} plane, which also confirms with our experimental observation.

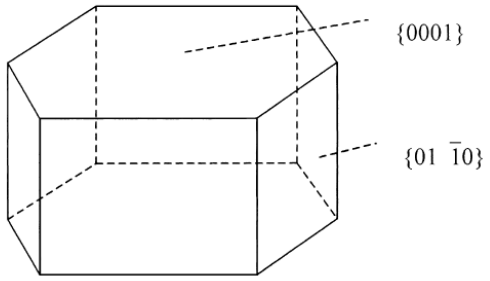


Figure 5.7 Hexagonal structure of ZnO crystal.

5.3.2 Experimental Results

According to the contact approach of the nanowires, we classified the linked nanowires into three categories. First, contact was formed due to the width expansion of the nanowires, Fig. 5.8(a). Second, contact was introduced due to the elongation of the nanowire(s), Fig. 5.8(b). Third, contact was introduced due to width expansion and elongation of the nanowires. For convenience, we call the first and second cases as case ‘A’ , case ‘B’, and case ‘C’, respectively.

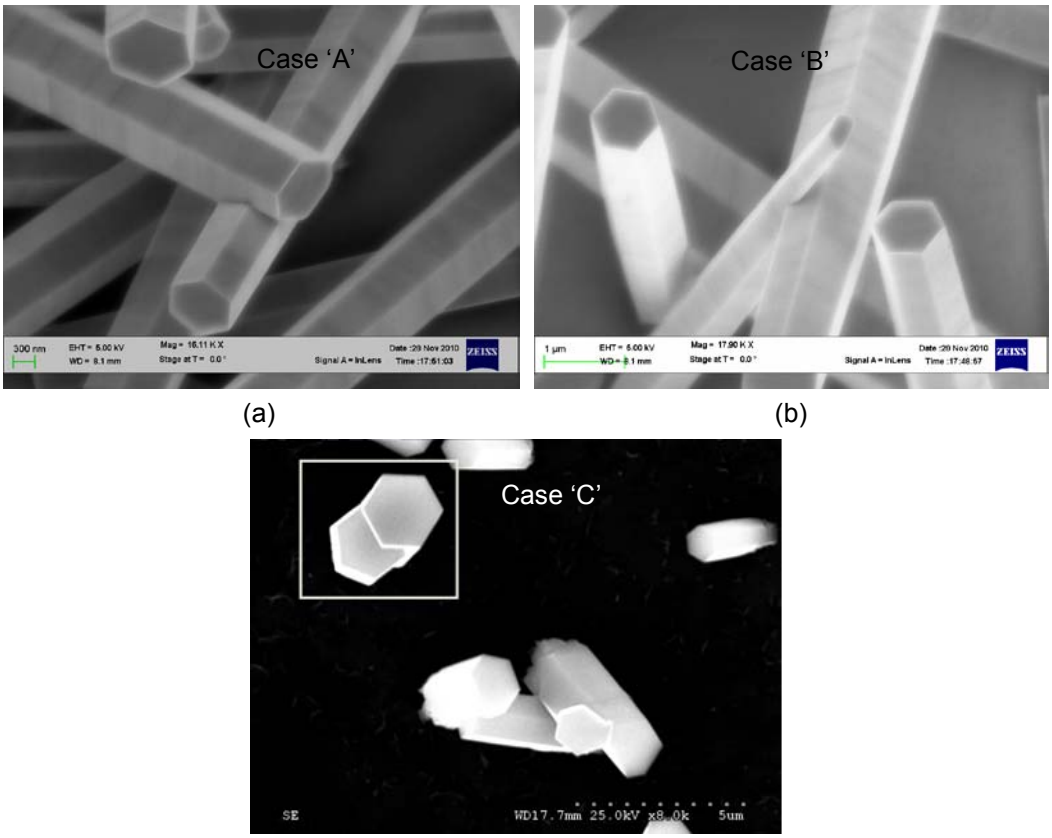


Figure 5.8 Linked ZnO nanowires (a) case ‘A’, (b) case ‘B’ and (c) case ‘C’.

The size of nanowires keeps expanding both in length and width as growth continuing. For case ‘A’, the contact was introduced due to width expansion of nanowires, such as in Fig. 5.9(a), the two nanowires form a cross in the front view. While, a tiny space still exists between the two nanowires, as in the side view, Fig. 5.9(b). As growth continues, the nanowires become longer as well as thicker. The tiny space between the two nanowires at the cross reduces as diameter of the nanowires increases, till the two nanowires begin to touch each other, Fig. 5.9(d). According to the growth mechanism, the growth process is the incorporation of growth units into the crystal lattice [133]. Once physical contact exists, growth units are no longer be able to deposit on the contact area. Thereby, the growth at the contact area stops, and continues at the non-contacted area at certain rate, which depends on the growth rate of the crystal plane.

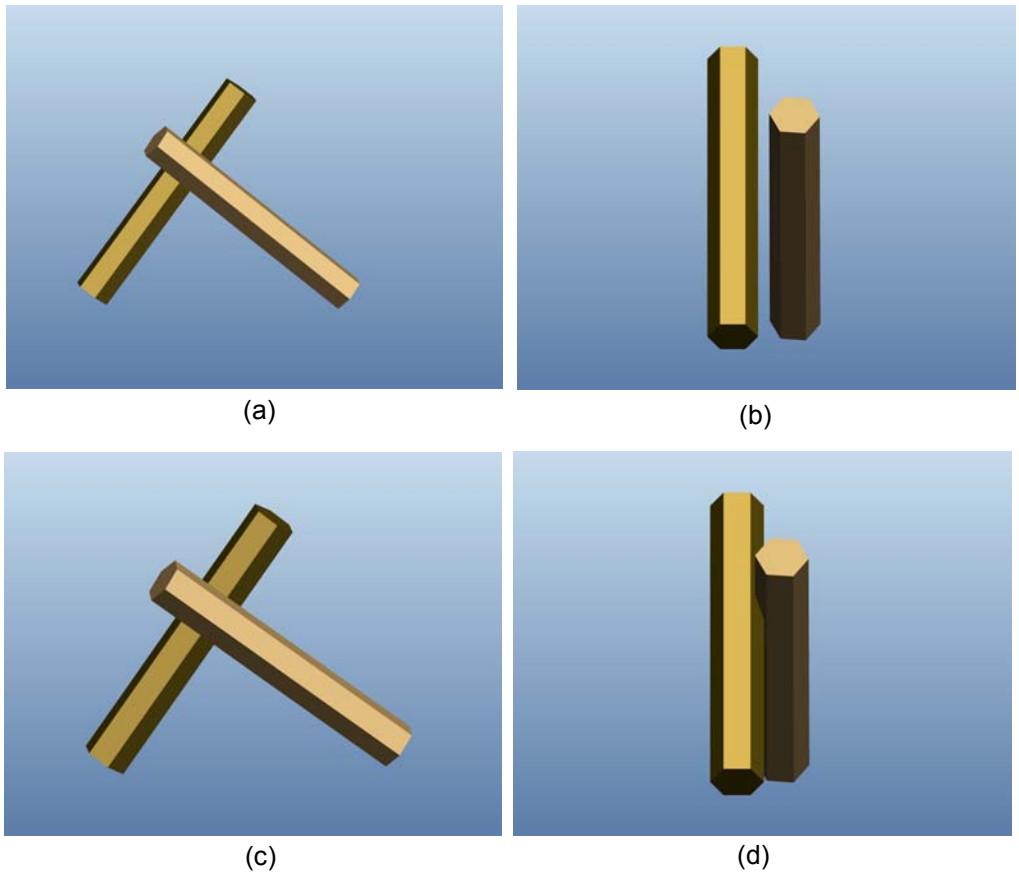


Figure 5.9 Demonstration of two linked nanowires in case 'A': (a) front view before linked, (b) side view before linked, (c) front view after linked and (d) side view after linked.

To support the assumption made above, experiments were conducted aiming to find out formation process of the linked nanowires. Growth solution was prepared with equal mole (25 mM) zinc nitrate hexahydrate and hexamethylenetetramine in DI water. Growing temperature was 95 ^{o}C. Growth solution was replaced every time after the sample was taken out for SEM imaging. Since there is no effective ways for in-situ recording of the nanowire growing process in aqueous solution, sample was taken out for imaging after certain period of growth under SEM (ZEISS Supra 55 VP Scanning Electron Microscope). Particular locations were marked for tracking purpose.

As in Fig. 5.11(b), after 50 min growth, the two nanowires in the marked area 'A' were still separated from each other. The gap between them was 40 nm. In Fig. 5.10(d), after 170

min growth, the two nanowires in area ‘A’ began to touch each other. When the growth continued for 590 min, Fig. 5.11(f), an overlap between the two nanowires showed up. While, the top of the nanowires were not affected by the intersection, and still kept their hexagonal shape.

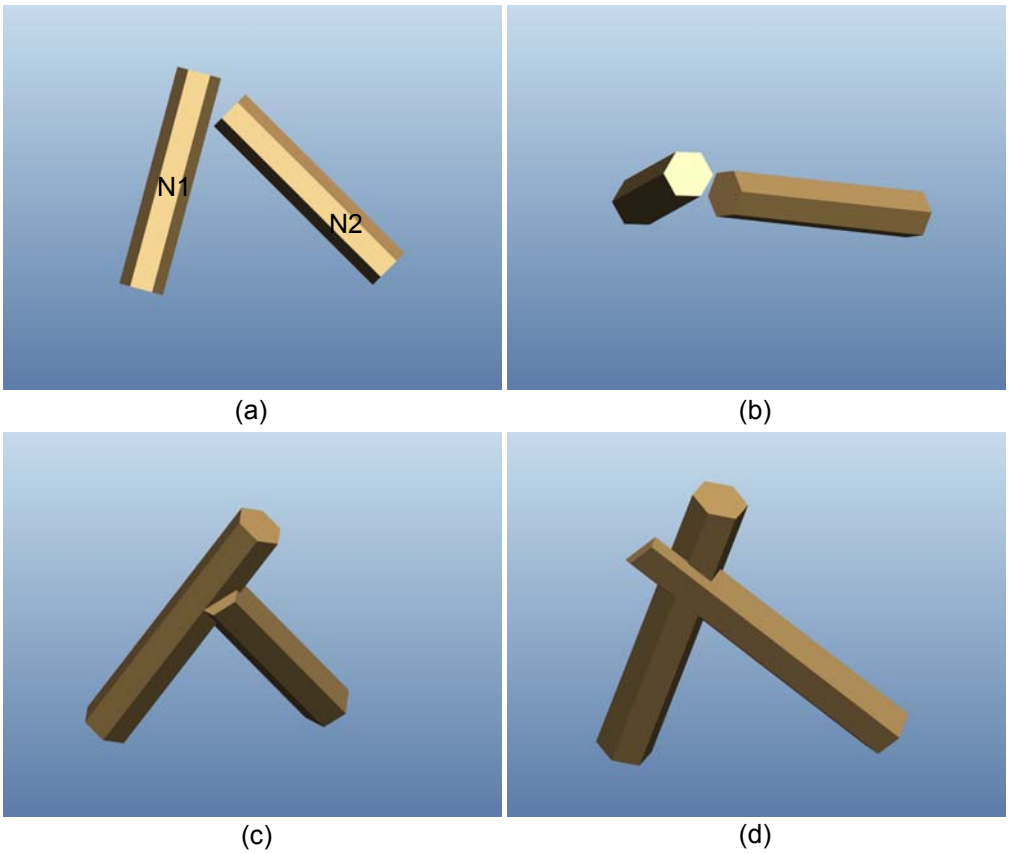


Figure 5.10 Demonstration of two linked nanowires in case ‘B’: (a) front view before linked, (b) top view before linked, (c) 3D view growth at the intersection, and (d) 3D view growth beyond the intersection.

For case ‘B’, contact was formed due to elongation of nanowires. For example, in Fig. 5.10(a), nanowire ‘N1’ is in the growth pass of ‘N2’. In the top view, Fig. 5.10(b), part of the hexagonal growing surface of ‘N2’ is blocked by ‘N1’. As growth continues, Fig. 5.10(c), an intersection is formed between the two nanowires. Since ‘N2’ is blocked by ‘N1’ partially, fully hexagonal shape of ‘N2’ cannot be formed after the intersection, Fig. 5.10(d).

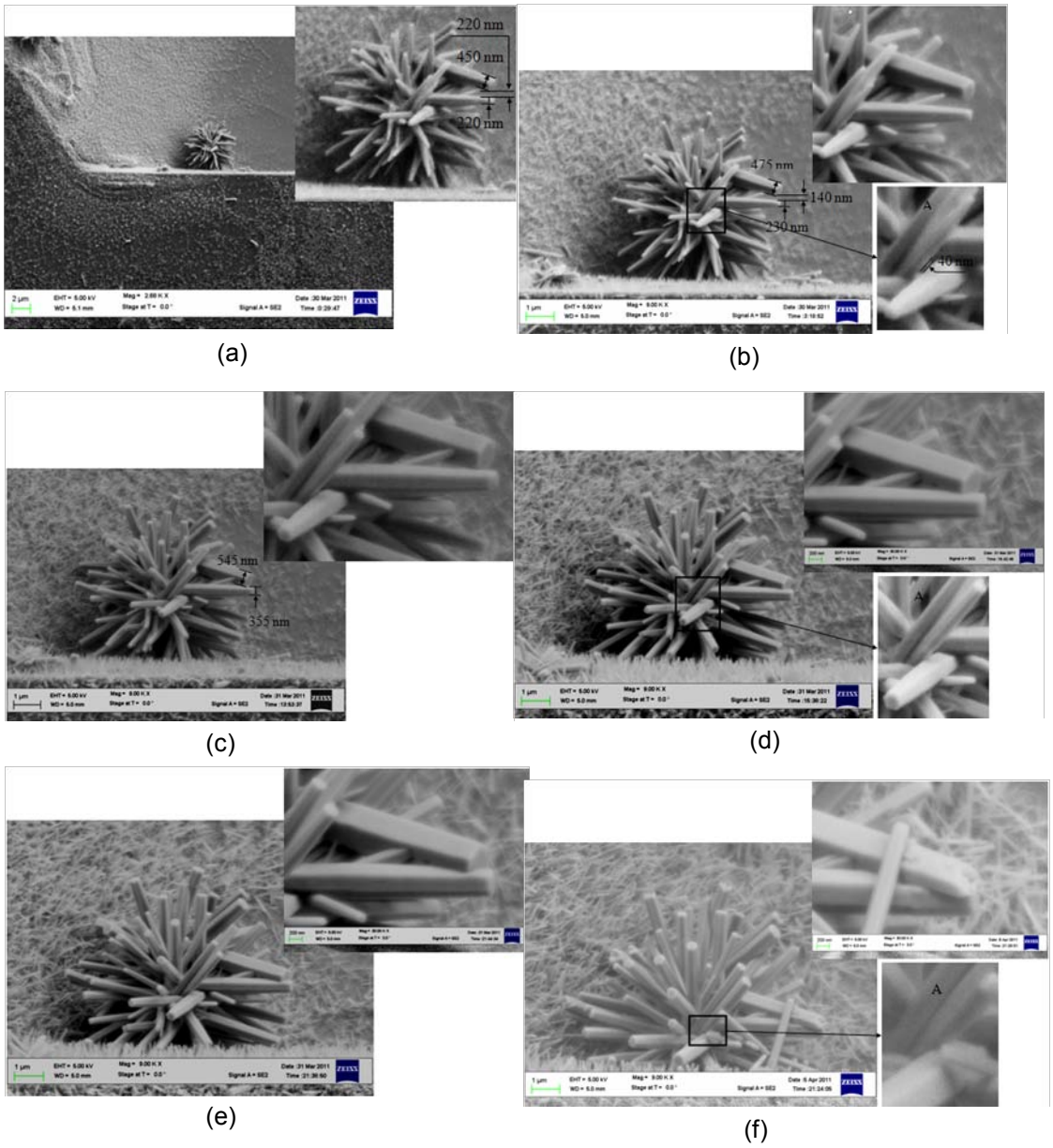
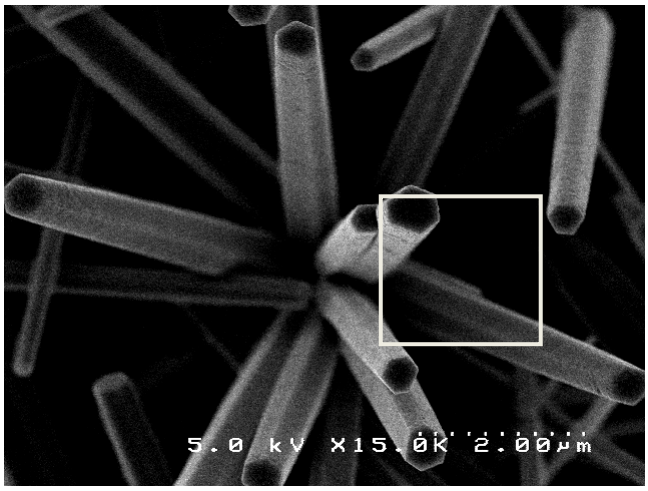


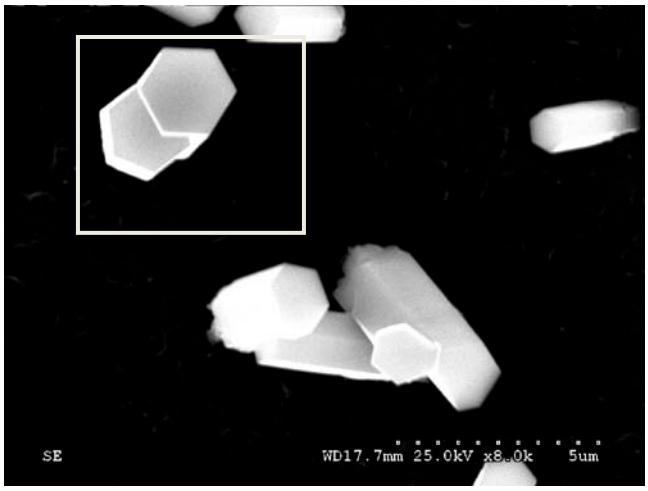
Figure 5.11 Growth of nanowires after (a) 30, (b) 50, (c) 110, (d) 170, (e) 230, and (f) 590 min.

Fig. 5.11 was recorded to approve the assumption of case 'B'. SEM images were taken after growth was conducted for 30, 50, 110, 170, 230 and 590 min, respectively. The two nanowires were separated at 30 min growth. The diameters at the tip of the nanowires were 450 and 220 nm, respectively. The gap between the nanowires was 220 nm, Fig. 5.11(a). After 20 min, totally 50 min growth, the gap between the two nanowires was reduced to 140 nm, Fig.

5.11(b). The diameters at the tips of the nanowires were increased to 475 and 230 nm, respectively. After another hour, totally 110 min growth, the two nanowires touched each other and became linked, Fig. 5.11(c). The diameters of the two nanowires at the tips were 545 and 355 nm, respectively. With the increasing of growth time, after 170 and 230 min, the overlapped part of the nanowires increased, Fig. 5.11(d) and (e). As growth conducted for 590 min, Fig. 5.11(f), the nanowire at the top exceeded the intersection and kept uncompleted hexagonal shape.



(a)



(b)

Figure 5.12 Linked nanowires in parallel direction (a) 3D view and (b) top view.

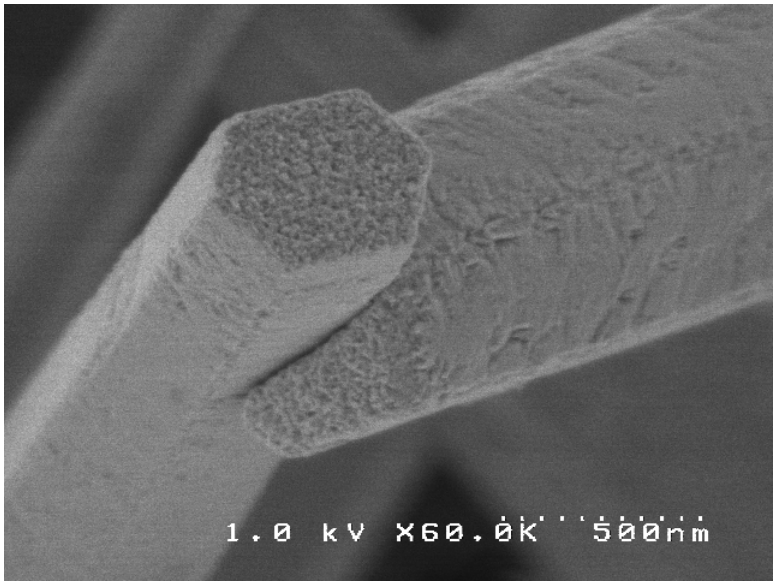
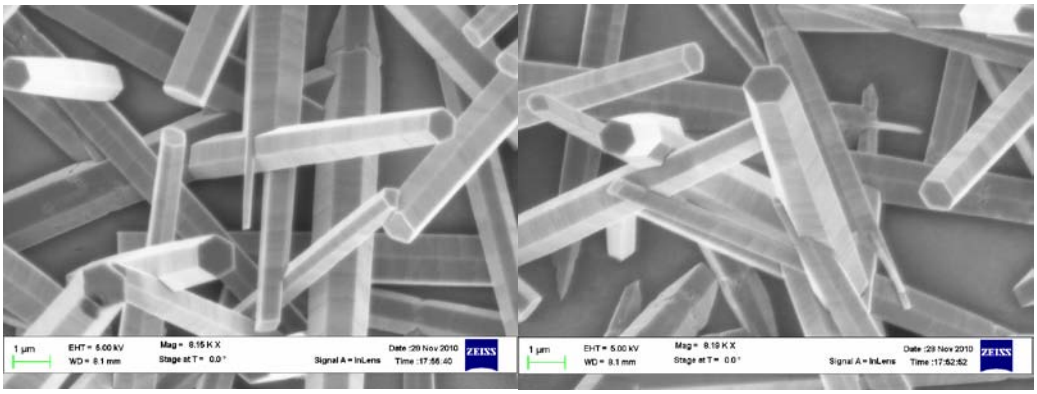


Figure 5.13 Linked nanowires.

Linked nanowires may appear in many forms, such as fork shape nanowire in Fig. 5.14(a), and multiple linked nanowires in Fig. 5.14(b). EDS was taken to prove the chemical components of the nanowires, Fig. 5.15. Three elements were detected: silicon, oxygen and zinc, where silicon is the substrate material. The ratio between zinc and oxygen atoms equals to one, which means the nanowires were made of ZnO.



(a) (b)

Figure 5.14 Different forms of linked nanowires (a) fork shape nanowire and (b) multiple linked nanowires.

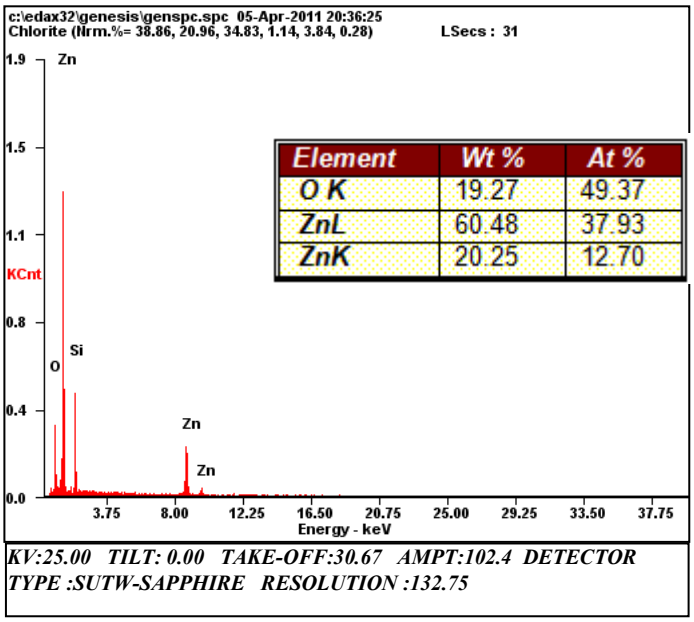


Figure 5.15 EDX analysis of nanowires.

5.4 Summary

It was found that ZnO nanowires may link together during hydrothermal growth. An intersection was formed at the linked area. The shapes of nanowires after the intersection may appear different forms, hexagonal or partially hexagonal. The formation processes of the linked nanowires were proposed. The shape of nanowire after the intersection is mainly decided by the contact approach between the nanowires. By applying SEM imaging, the processes of the formation of linked nanowires were recorded, which proved the proposed explanations.

CHAPTER 6

CONCLUSIONS AND FUTURE DIRECTIONS

6.1 Conclusions

This work aimed to develop new approaches to fabricate micropatterns on 3D surfaces, including irregular surfaces and vertical sidewalls of silicon channels. Au microdots and microlines on vertical sidewalls of silicon microchannels were produced by applying PDMS membrane with hollow structures as shadow mask. Two methods were developed for generating metal microlines on the outer surfaces of glass micropipettes. Meanwhile the mechanism of the formation of linked nanowires during hydrothermal growth was also explored.

In chapter 3, two approaches for generating Au micropatterns on vertical silicon sidewalls using PDMS membrane as shadow mask were introduced. In the first approach, PDMS membrane was placed against the sidewall directly. Au micropatterns were generated on the vertical silicon sidewall during the metal deposition on the silicon sidewall. Four rows of 10 μm Au dots were properly patterned on a 110-μm-deep silicon vertical sidewall. In the second approach, PDMS membrane was placed over the silicon channels. Au films were then coated on the substrate through two processes of thermal evaporation using the PDMS membrane as a shadow mask. In these two processes, the two sidewalls of the Si channel were tilted towards the Au source, respectively, to ensure that Au was coated on either sidewall. Finally, after the removal of this PDMS membrane, Au patterns were generated on the channel sidewalls. 3-D geometric models for the new approach were setup accordingly to find shapes, thicknesses and dimensions of Au patterns generated on the sidewall. Based on the understanding gained from these geometric models, we then applied this approach to produce 10 μm Au dots and 20-μm-wide Au lines, respectively, on two sidewalls of a Si microchannel. Comparing the two approaches, the first approach is good at generating micropatterns on a single sidewall, while

the second approach is good at generating micropatterns on the two sidewalls of a silicon channel. These Au dots might serve as catalysts for VLS growth of ZnO nanowires, which can be potentially employed as functional components in 3D electronic circuits. In addition, a new method to fabricate PDMS membranes of hollow structures was developed. A hexane droplet was applied on the PDMS film to remove the PDMS residue layer that had been created on a SU-8 mold before PDMS was cured. The thickness of the finally generated PDMS membrane of hollow structures can be adjusted by changing the amount of hexane used.

In chapter 4, two methods for producing metal microlines on the outer surfaces of micropipettes were developed. In either approach, the outer surface of the glass micropipette was first thermally coated with a thin Au film. A PR-coated membrane was then pushed against this glass micropipette when the PR was still wet. During the contact, part of the PR was transferred from the membrane to the micropipette. After the membrane was removed, a continuous PR line was left on the outer surface of the glass micropipette. This line extended from the straight tube to the end of the curved tip. Another PR line was further generated on the other side of this micropipette using the same process. Finally, after the Au film was etched using the two PR lines as the masking patterns, followed by the removal of the PR using acetone, two Au lines were generated on the outer surface of the glass micropipette. The two approaches mainly differed in the ways of pressing the PR-coated membrane against the curved tip of the micropipette. In the first approach, a clip was applied for this purpose, while in the second approach a nitrogen flux was employed to make the membrane have intimate contact with the curved tip. To date, we have successfully fabricated Au lines on glass micropipettes of tip sizes down to 35 μm and 5 μm, respectively, using the two approaches.

In chapter 5, the formation processes of linked ZnO nanowires were explored. Growing images of linked nanowires at different stages were recorded under SEM. The shapes of nanowires after the intersection may appear different forms, hexagonal or partially hexagonal, which were mainly decided by the encounter form of the nanowires. This phenomenon can be potentially used for building new nanostructures.

6.2 Future Directions

In the near future, we would like to continue our work on the introduced projects in following aspects.

For sidewall patterning, it is worth to continue the work on fabricating sidewall patterns on smaller channels, such as channels of 10 μm wide. In such a case, ZnO nanowires grow from the opposite sidewalls may linked and generate valuable applications. Meanwhile, the alignment feature on the PDMS membrane should be added, which will reduce the work labor of alignment procedure greatly.

For the project of micropipette, devices, such as microelectrodes, based on the fabricated samples may be fabricated and tested. It is also very interesting that if ZnO nanowires may be grown at the tip of the micropipette and linked together, which can be used for sensing purpose.

For the work on linked ZnO nanowires, an approach need to be developed for separating the linked nanowires to observe the interface and further approve the proposed explanations. By manipulating single nanowire to make them grow toward each other, new nano/microstructures may be fabricated.

REFERENCES

1. S M Sze, *Vlsi Technology*. 2nd ed. 1988, New York: McGraw-Hill Book Company.
2. G T Kovacs, *Micromachined Transducers Sourcebook*. 1998, New York: McGraw-Hill.
3. J M Bustillo, R T Howe and R S Muller. *Surface Micromachining for Microelctromechanical Systems*. in *Proceedings of the IEEE*. 1998.
4. M J Madou, *Fundamentals of Microfabrication*. 1997, New York: CRC Press.
5. D L Fan, F Q Zhu, R C Cammarata and C L Chien, *Manipulation of Nanowires in Suspension by Ac Electric Fields.* Applied Physics Letters, 2004. **85**(18): p. 4175-4177.
6. J Chung, K-H Lee, J Lee and R S Ruoff, *Toward Large-Scale Integration of Carbon Nanotubes.* Langmuir, 2004. **20**(8): p. 3011-3017.
7. O Englander, D Christensen, J Kim, L Lin and S J S Morris, *Electric-Field Assisted Growth and Self-Assembly of Intrinsic Silicon Nanowires.* Nano Letters, 2005. **5**(4): p. 705-708.
8. Z Chen, W Hu, J Guo and K Saito, *Fabrication of Nanoelectrodes Based on Controlled Placement of Carbon Nanotubes Using Alternating-Current Electric Field.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, 2004. **22**(2): p. 776-780.
9. P A Smith, C D Nordquist, T N Jackson, T S Mayer, B R Martin, J Mbindyo and T E Mallouk, *Electric-Field Assisted Assembly and Alignment of Metallic Nanowires.* Applied Physics Letters, 2000. **77**(9): p. 1399-1401.
10. B Messer, J H Song and P Yang, *Microchannel Networks for Nanowire Patterning.* Journal of the American Chemical Society, 2000. **122**(41): p. 10232-10233.
11. Y Huang, X Duan, Q Wei and C M Lieber, *Directed Assembly of One-Dimensional Nanostructures into Functional Networks.* Science, 2001. **291**(5504): p. 630-633.

12. H M Fishman, *Low-Impedance Capillarry Electrode for Wide-Band Recording of Membrane Potential in Large Axons.* IEEE Transactions on Biomedical Engineering, 1973. **BME-20**(5): p. 380-382.

13. M Zhong and S M Lunte, *Integrated on-Capillary Electrochemical Detector for Capillary Electrophoresis.* Analytical Chemistry, 1996. **68**(15): p. 2488-2493.

14. K Becker, N Abramzon, N S Panikov, R Crowe, P J Ricatto and C Christodoulatos. *Destruction of Bacteria Using an Atmospheric-Pressure Dielectric Capillary Electrode Discharge Plasma*. in *Plasma Science, 2002. ICOPS 2002. IEEE Conference Record - Abstracts. The 29th IEEE International Conference on*. 2002.

15. H M Pollock and A Hammiche, *Micro-Thermal Analysis: Techniques and Applications.* Journal of Physics D: Applied Physics, 2001. **34**(9): p. 23-53.

16. R D Piner, J Zhu, F Xu, S Hong and C A Mirkin, *"Dip-Pen" Nanolithography.* Science, 1999. **283**(5402): p. 661-663.

17. X Wang, K S Ryu, D A Bullen, J Zou, H Zhang, C A Mirkin and C Liu, *Scanning Probe Contact Printing.* Langmuir, 2003. **19**(21): p. 8951-8955.

18. Y Xia and G M Whitesides, *Soft Lithography.* Angewandte Chemie International Edition, 1998. **37**(5): p. 550-575.

19. Y Xia, J A Rogers, K E Paul and G M Whitesides, *Unconventional Methods for Fabricating and Patterning Nanostructures.* Chemical Reviews, 1999. **99**(7): p. 1823-1848.

20. S Y Chou, P R Krauss and P J Renstrom, *Imprint Lithography with 25-Nanometer Resolution.* Science, 1996. **272**(5258): p. 85-87.

21. S Y Chou, P R Krauss and P J Renstrom, *Nanoimprint Lithography.* J. Vac. Sci. Technol., 1996. **14**(6): p. 5.

22. X Liu and C Luo, *Fabrication of Au Sidewall Micropatterns Using Si-Reinforced Pdms Molds.* Sensors and Actuators A: Physical, 2009. **152**(1): p. 96-103.

23. X Liu and C Luo, *Fabrication of Super-Hydrophobic Channels.* Journal of Micromechanics and Microengineering, 2010. **20**(2): p. 025029.

24. K Nakajima, T Yamagiwa, A Hirano and M Sugawara, *A Glass Capillary Microelectrode Based on Capillarity and Its Application to the Detection of L-Glutamate Release from Mouse Brain Slices.* Analytical Sciences 2003. **19**: p. 55-60.

25. B Zhang, S Zhou, B Liu, H Gong and X Zhang, *Fabrication and Green Emission of Zno Nanowire Arrays.* Science in China, Series E: Technological Sciences, 2009. **52**(4): p. 883-887.

26. M Li, H-Y Zhang, C-X Guo, J-B Xu and X-J Fu, *The Research on Suspended Zno Nanowire Field-Effect Transistor.* Chinese Physics B, 2009. **18**(4): p. 1594-1597.

27. O Lupan, T Pauporte, B Viana, I M Tiginyanu, V V Ursaki and R Cortes, *Epitaxial Electrodeposition of Zno Nanowire Arrays on P-Gan for Efficient Uv-Light-Emitting Diode Fabrication.* ACS Applied Materials and Interfaces. **2**(7): p. 2083-2090.

28. C Soci, A Zhang, B Xiang, S A Dayeh, D P R Aplin, J Park, X Y Bao, Y H Lo and D Wang, *Zno Nanowire Uv Photodetectors with High Internal Gain.* Nano Letters, 2007. **7**(4): p. 1003-1009.

29. S Hur, K-H Lee, Y-B Hahn, W-D Kim and H Choi. *Power Generation Using Piezoelectric Zno Nanowires for Nano-Scale Devices*. Ilsan, Gyeonggi-Do, Korea, Republic of: IEEE Computer Society.

30. J Wang, H Li, Y Huang and Y Zhang. *Fabrication and Optical Properties of Mn-Doped Zno Nanowires*. 2009. Qingdao, China: Trans Tech Publications.

31. J-H Kim, D-S Kang, S-K Hong, H Kim, D Kim, J W Lee and J Y Lee. *Investigations on Growth and Hydrogen Gas Sensing Property of Zno Nanowires Prepared by Hydrothermal Growth*. Hongkong, China: IEEE Computer Society.

32. L Li, H Yang, H Zhao, J Yu, J Ma, L An and X Wang, *Hydrothermal Synthesis and Gas Sensing Properties of Single-Crystalline Ultralong Zno Nanowires.* Applied Physics A: Materials Science and Processing. **98**(3): p. 635-641.

33. S Todros, C Baratto, E Comini, G Faglia, M Ferroni, G Sberveglieri, S Lettieri, A Setaro, L Santamaria and P Maddalena. *Optical Gas Sensing Properties of Zno Nanowires*. Pavia, Italy: Springer Verlag.

34. D Y Kim and J Y Son, *Horizontal Zno Nanowires for Gas Sensor Application: Al-Doping Effect on Sensitivity.* Electrochemical and Solid-State Letters, 2009. **12**(12): p. J109-J111.

35. M K Singh, E Titus and J Gracio. *Uv Emission from Patterned Growth of Zno Nanowires*. 26650 The Old Road, Valencia, California, 91381-0751, United States: American Scientific Publishers.

36. M Museau, C Masclet and S Tichkiewitch, *Integrated Design of Mems: Aiming at Manufacturability.* International Journal on Interactive Design and Manufacturing, 2007. **1**(3): p. 127-134.

37. T M Verhaar, J Wei and P M Sarro, *Pattern Transfer on a Vertical Cavity Sidewall Using Su8.* Journal of Micromechanics and Microengineering, 2009. **19**(7): p. 074018.

38. C Christensen, P Kersten, S Henke and S Bouwstra, *Wafer through-Hole Interconnections with High Vertical Wiring Densities.* Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on, 1996. **19**(4): p. 516-522.

39. P P Nga, J N Burghartz and P M Sarro, *Spray Coating of Photoresist for Pattern Transfer on High Topography Surfaces.* Journal of Micromechanics and Microengineering, 2005. **15**(4): p. 691.

40. P Nga Phuong, E Boellaard, J N Burghartz and P M Sarro, *Photoresist Coating Methods for the Integration of Novel 3-D Rf Microstructures.* Microelectromechanical Systems, Journal of, 2004. **13**(3): p. 491-499.

41. S Linder, H Baltes, F Gnaedinger and E Doering. *Photolithography in Anisotropically Etched Grooves*. in *Micro Electro Mechanical Systems, 1996, MEMS '96, Proceedings. 'An Investigation of Micro Structures, Sensors, Actuators, Machines and Systems'. IEEE, The Ninth Annual International Workshop on*. 1996.

42. N P Pham, T L Scholtes, R Klerk, B Wieder, P M Sarro and J N Burghartz. *Direct Spray Coating of Photoresist for Mems Applications*. in *Micromachining and Microfabrication Process Technology VII*. 2001. San Francisco, CA, USA: SPIE.

43. M Heschel and S Bouwstra, *Conformal Coating by Photoresist of Sharp Corners of Anisotropically Etched through-Holes in Silicon.* Sensors and Actuators A: Physical, 1998. **70**(1-2): p. 75-80.

44. M d Samber, T Nellissen and E v Grunsven, *Through Wafer Interconnection Technologies for Advanced Electronic Devices*, in *Electronics Packaging Technology Conference*. 2004: Singapore.

45. M Han, W Lee, S-K Lee and S S Lee, *3d Microfabrication with Inclined/Rotated Uv Lithography.* Sensors and Actuators A: Physical, 2004. **111**(1): p. 14-20.

46. Z Zhen, Z-F Zhou, Q-A Huang and W-H li, *Modeling, Simulation and Experimental Verification of Inclined Uv Lithography for Su-8 Negative Thick Photoresists.* Journal of Micromechanics and Microengineering, 2008. **18**(12): p. 125017.

47. H Sato, D Yagyu, S Ito and S Shoji, *Improved Inclined Multi-Lithography Using Water as Exposure Medium and Its 3d Mixing Microchannel Application.* Sensors and Actuators A: Physical, 2006. **128**(1): p. 183-190.

48. T Nellissen, M Botermans, M Burghoorn, J V Delft, E V Grunsven, J Scheer and M D Samber, *Development of an Advanced Three-Dimensional Mcm-D Substrate Level Patterning Technique.* European Microelectronics and Packaging Symposium, 2004: p. 459-464.

49. W J Li, J D Mai and C-M Ho, *Sensors and Actuators on Non-Planar Substrates.* Sensors and Actuators A: Physical, 1999. **73**(1-2): p. 80-88.

50. T Horiuchi and N Hayashi, *Projection Lithography onto Small-Diameter Copper Shafts and Fabrication of a Micro-Axial Pump.* Microelectronic Engineering. **86**(4-6): p. 1176-1178.

51. K Hashimoto, Y Kaneko and T Horiuchi, *Projection Lithography onto Overall Cylindrical Surfaces.* Microelectronic Engineering. **83**(4-9): p. 1312-1315.

52. A D Feinerman, R E Lajos, V White and D D Denton, *X-Ray Lathe: An X-Ray Lithographic Exposure Tool for Nonplanar Objects.* Journal of Microelectromechanical Systems, 1996. **5**(4): p. 250-255.

53. G Lullo, C Arnone and C G Giaconia, *Technologies for the Fabrication of Cylindrical Fine Line Devices.* Microelectron. Eng., 1997. **35**(1-4): p. 417-420.

54. C G Giaconia, G Grasso and C Arnone, *Resist Coating of Cylindrical Samples for 3-D Lithography.* Microelectronics International, 1995. **12**(1): p. 22-24.

55. F J Giessibl, *Advances in Atomic Force Microscopy.* Reviews of Modern Physics, 2003. **75**(3): p. 949.

56. S W Park, H T Soh, C F Quate and S I Park, *Nanometer Scale Lithography at High Scanning Speeds with the Atomic Force Microscope Using Spin on Glass.* Applied Physics Letters, 1995. **67**(16): p. 2415-2417.

57. Z J Davis, G Abadal, O Hansen, X Boris, N Barniol, F P 閘 ez-Murano and A Boisen, *Afm Lithography of Aluminum for Fabrication of Nanomechanical Systems.* Ultramicroscopy. **97**(1-4): p. 467-472.

58. J H Jang, W Zhao, J W Bae, D Selvanathan, S L Rommel, I Adesida, A Lepore, M Kwakernaak and J H Abeles, *Direct Measurement of Nanoscale Sidewall Roughness of Optical Waveguides Using an Atomic Force Microscope.* Applied Physics Letters, 2003. **83**(20): p. 4116-4118.

59. Y Martin and H K Wickramasinghe, *Method for Imaging Sidewalls by Atomic Force Microscopy.* Applied Physics Letters, 1994. **64**(19): p. 2498-2500.

60. S G Ken Murayama, Hajime Koyanagi, Tsuneo Terasawa and Sumio Hosaka *Side-Wall Measurement Using Tilt-Scanning Method in Atomic Force Microscope.* Japanese Journal of Applied Physics, 2006. **45**: p. 6.

61. A d Campo, I Alvarez, S Filipe and M Wilhelm, *3d Microstructured Surfaces Obtained by Soft-Lithography Using Fast-Crosslinking Elastomeric Precursors and 2d Masters.* Advanced Functional Materials, 2007. **17**(17): p. 3590-3597.

62. A S M Chong, L K Tan, J Deng and H Gao, *Soft Imprinting : Creating Highly Ordered Porous Anodic Alumina Templates on Substrates for Nanofabrication*. Vol. 17. 2007, Weinheim, ALLEMAGNE: Wiley-VCH. 7.

63. C N LaFratta, T Baldacchini, R A Farrer, J T Fourkas, M C Teich, B E A Saleh and M J Naughton, *Replication of Two-Photon-Polymerized Structures with Extremely High Aspect Ratios and Large Overhangs.* The Journal of Physical Chemistry B, 2004. **108**(31): p. 11256-11258.

64. C Y Hui, A Jagota, Y Y Lin and E J Kramer, *Constraints on Microcontact Printing Imposed by Stamp Deformation.* Langmuir, 2002. **18**(4): p. 1394-1407.

65. A Bietsch and B Michel, *Conformal Contact and Pattern Stability of Stamps Used for Soft Lithography.* Journal of Applied Physics, 2000. **88**(7): p. 4310-4318.

66. R J Jackman, S T Brittain, A Adams, M G Prentiss and G M Whitesides, *Design and Fabrication of Topologically Complex, Three-Dimensional Microstructures.* Science, 1998. **280**(5372): p. 2089-2091.

67. J A Rogers, R J Jackman and G M Whitesides, *Constructing Single- and Multiple-Helical Microcoils and Characterizing Their Performance as Components of Microinductors and Microelectromagnets.* Journal of microelectromechanical systems, 1997. **6**(3): p. 184-192.

68. J Kohler, M Albrecht, C R Musil and E Bucher, *Direct Growth of Nanostructures by Deposition through an Si3n4 Shadow Mask.* Physica E: Low-dimensional Systems and Nanostructures, 1999. **4**(3): p. 196-200.

69. S M Yi, S H Jin, J D Lee and C N Chu, *Fabrication of High Aspect Ratio Metal Shadow Mask for Otfts.* Journal of Micromechanics and Microengineering, 2005. **15**: p. 263-269.

70. S M Yi, M S Park, Y S Lee and C N Chu, *Fabrication of a Stainless Steel Shadow Mask Using Batch Mode Micro-Edm.* Microsyst. Technol., 2008. **14**(3): p. 411-417.

71. M Graff, S K Mohanty, E Moss and A B Frazier, *Microstenciling: A Generic Technology for Microscale Patterning of Vapor Deposited Materials.* Microelectromechanical Systems, Journal of, 2004. **13**(6): p. 956-962.

72. A Tixier, Y Mita, J P Gouy and H Fujita, *A Silicon Shadow Mask for Deposition on Isolated Areas.* Journal of Micromechanics and Microengineering, 2000. **10**(2): p. 157-162.

73. G Kim, B Kim and J Brugger, *All-Photoplastic Microstencil with Self-Alignment for Multiple Layer Shadow-Mask Patterning.* Sensors and Actuators A: Physical, 2003. **107**(2): p. 132-136.

74. G J Burger, E J T Smulders, J W Berenschot, T S J Lammerink, J H J Fluitman and S Imai, *High-Resolution Shadow-Mask Patterning in Deep Holes and Its Application to an Electrical Wafer Feed-Through.* Sensors and Actuators A: Physical, 1996. **54**(1-3): p. 669-673.

75. A R Champagne, A J Couture, F Kuemmeth and D C Ralph, *Nanometer-Scale Scanning Sensors Fabricated Using Stencil Lithography.* Applied Physics Letters, 2003. **82**(7): p. 1111-1113.

76. W-S Su, M-S Tsai and W Fang, *A Three-Dimensional Microfabrication Technology on Highly Structured Surfaces.* Electrochemical and Solid-State Letters, 2007. **10**(1): p. H16-H19.

77. J Brugger, C Andreoli, M Despont, U Drechsler, H Rothuizen and P Vettiger, *Self-Aligned 3d Shadow Mask Technique for Patterning Deeply Recessed Surfaces of Micro-Electro-Mechanical Systems Devices.* Sensors and Actuators A: Physical, 1999. **76**(1-3): p. 329-334.

78. S Morishita, J H Kim, F Marty, Y Li, A J Walton and Y Mita, *A Three-Dimensional Silicon Shadowmask for Patterning on Trenches with Vertical Walls*, in *Transducers*. 2009: Denver, CO, USA. p. 1608-1611.

79. H Seidel, L Csepregi, A Heuberger and H Baumgartel, *Anisotropic Etching of Crystalline Silicon in Alkaline Solutions.* Journal of The Electrochemical Society, 1990. **137**(11): p. 3612-3626.

80. A Holke and H T Henderson, *Ultra-Deep Anisotropic Etching of (110) Silicon.* Journal of Micromechanics and Microengineering, 1999. **9**(1): p. 51-57.

81. R B Gmbh, *Method for Anisotropically Etching Silicon*.

82. C Luo, A Govindaraju, J Garra, T Schneider, R White, J Currie and M Paranjape, *Releasing Su-8 Structures Using Polystyrene as a Sacrificial Material.* Sensors and Actuators A: Physical, 2004. **114**(1): p. 123-128.

83. C Luo, F Meng and A Francis, *Fabrication and Application of Silicon-Reinforced Pdms Masters.* Microelectronics Journal, 2006. **37**(10): p. 1036-1046.

84. A L Thangawng, M A Swartz, M R Glucksberg and R S Ruoff, *Bond-Detach Lithography: A Method for Micro/Nanolithography by Precision Pdms Patterning.* small, 2005. **3**(1): p. 132-138.

85. Y Luo and R Zare, *Perforated Membrane Method for Fabricating Three-Dimensional Polydimethylsiloxane Microfluidic Devices.* Lab Chip, 2008. **8**(10): p. 1688-1694.

86. J H Kang, E Um and J-K Park, *Fabrication of a Poly(Dimethylsiloxane) Membrane with Well-Defined through-Holes for Three-Dimensional Microfluidic Networks.* Journal of Micromechanics and Microengineering, 2009. **19**: p. 045027.

87. J Zou and P Y Wong. *Thermal Effects in Plasma Treatment of Patterned Pdms for Bonding Stacked Channels*. in *Mat. Res. Soc. Symp. Proc.* 2004.

88. S R Oh, *Thick Single-Layer Positive Photoresist Mold and Poly(Dimethylsiloxane) (Pdms) Dry Etching for the Fabrication of a Glass Pdms Glass Microfluidic Device.* Journal of Micromechanics and Microengineering, 2008. **18**(11): p. 115025.

89. S J Hwang, D J Oh, P G Jung, S M Lee, J S Go, J-H Kim, K-Y Hwang and J S Ko, *Dry Etching of Polydimethylsiloxane Using Microwave Plasma.* J. Micromech. Microeng, 2009. **19**: p. 095010.

90. X Liu, A Chakraborty and C Luo, *Fabrication of Micropatterns on the Sidewalls of a Thermal Shape Memory Polystyrene Block.* Journal of Micromechanics and Microengineering, 2010. **20**(9): p. 095025.

91. H Wang and C Luo, *Fabrication of Au Micropatterns on Vertical Si Sidewalls Using Pdms Membranes as Shadow Masks.* JMM, 2010.

92. C J Richard, *Introduction to Microelectronic Fabrication*. Modular Series on Solid State Devices. 2001, New Jersey: Prentice Hall. 1.

93. S Selvarasah, S H Chao, C L Chen, S Sridhar, A Busnaina, A Khademhosseini and M R Dokmeci, *A Reusable High Aspect Ratio Parylene-C Shadow Mask Technology for Diverse Micropatterning Applications.* Sensors and Actuators A: Physical, 2008. **145-146**: p. 306-315.

94. P Yang, H Yan, S Mao, R Russo, J Johnson, R Saykally, N Morris, J Pham, R He and H J Choi, *Controlled Growth of Zno Nanowires and Their Optical Properties.* Advanced Functional Materials, 2002. **12**(5): p. 323-331.

95. I Gavrilas, C Opran and I D Marinescu. *Electrochemical Microboring with a Capillary Electrode Made of Glass*. 1985. Stuttgart, Austria: Springer-Verlag.

96. Y Okada and A Inouye, *Ph-Sensitive Glass Microelectrodes and Intracellular Ph Measurements.* European Biophysics Journal, 1976. **2**(1): p. 21-30.

97. R N Khuri, S K Agulian, H Oelert and R I Harik, *A Single Unit Ph Glass Ultramicro Electrode.* Pflügers Archiv European Journal of Physiology, 1967. **294**(4): p. 291-294.

98. R H Wilkinson, *Capillary Ph Electrode.* Journal of Scientific Instruments, 1959. **36**(10): p. 424.

99. H S Park, S J Kim, H M Joh, T H Chung, S H Bae and S H Leem, *Optical and Electrical Characterization of an Atmospheric Pressure Microplasma Jet with a Capillary Electrode.* Physics of Plasmas. **17**(3): p. 033502-10.

100. K-M Yin, *A Theoretical Model of the Membrane Electrode Assembly of Liquid Feed Direct Methanol Fuel Cell with Consideration of Water and Methanol Crossover.* Journal of Power Sources, 2008. **179**(2): p. 700-710.

101. T Gotow, M Ohba and T Tomita, *Tip Potential and Resistance of Micro-Electrodes Filled with Kcl Solution by Boiling and Nonboiling Methods.* IEEE Transactions on Biomedical Engineering, 1977. **BME-24**(4): p. 366-371.

102. J Olofsson, M Levin, A Stromberg, S G Weber, F Ryttsen and O Orwar, *Generation of Focused Electric Field Patterns at Dielectric Surfaces.* Analytical Chemistry, 2005. **77**(14): p. 4667-72.

103. K Nakajima, T Yamagiwa, A Hirano and M Sugawara, *A Glass Capillary Microelectrode Based on Capillarity and Its Application to the Detection of L-Glutamate Release from Mouse Brain Slices.* Analytical Sciences, 2003. **19**(1): p. 55-60.

104. M Willander, P Klason, L L Yang, M A-H Safaa, Q X Zhao and O Nur, *Zno Nanowires: Chemical Growth, Electrodeposition, and Application to Intracellular Nano-Sensors.* physica status solidi (c), 2008. **5**(9): p. 3076-3083.

105. J J Cole, X Wang, R J Knuesel and H O Jacobs, *Integration of Zno Microcrystals with Tailored Dimensions Forming Light Emitting Diodes and Uv Photovoltaic Cells.* Nano Letters, 2008. **8**(5): p. 1477-1481.

106. S W Yoon, J H Seo, K-H Kim, J-P Ahn, T-Y Seong, K B Lee and H Kwon, *Electrical Properties and Microstructural Characterization of Single Zno Nanowire Sensor Manufactured by Fib.* Thin Solid Films, 2009. **517**(14): p. 4003-4006.

107. J Zhou, P Fei, Y Gao, Y Gu, J Liu, G Bao and Z L Wang, *Mechanical-Electrical Triggers and Sensors Using Piezoelectric Micowires/Nanowires.* Nano Letters, 2008. **8**(9): p. 2725-2730.

108. W S Jirí Podzemský, *Organic Solar Cells Based on Zno Nanowires Layer.*

109. W J E Beek, M M Wienk and R A J Janssen, *Hybrid Polymer Solar Cells Based on Zinc Oxide.* Journal of materials Chemistry, 2005. **15**: p. 4.

110. M K Kim, D K Yi and U Paik, *Tunable, Flexible Antireflection Layer of Zno Nanowires Embedded in Pdms.* Langmuir.

111. J B Baxter and E S Aydil, *Nanowire-Based Dye-Sensitized Solar Cells.* Applied Physics Letters, 2005. **86**(5).

112. J Zhou, Y Gu, P Fei, W Mai, Y Gao, R Yang, G Bao and Z L Wang, *Flexible Piezotronic Strain Sensor.* Nano Letters, 2008. **8**(9): p. 3035-3040.

113. X Wang, J Zhou, J Song, J Liu, N Xu and Z L Wang, *Piezoelectric Field Effect Transistor and Nanoforce Sensor Based on a Single Zno Nanowire.* Nano Letters, 2006. **6**(12): p. 2768-2772.

114. P Fei, P-H Yeh, J Zhou, S Xu, Y Gao, J Song, Y Gu, Y Huang and Z L Wang, *Piezoelectric Potential Gated Field-Effect Transistor Based on a Free-Standing Zno Wire.* Nano Letters, 2009. **9**(10): p. 3435-3439.

115. M-P Lu, J Song, M-Y Lu, M-T Chen, Y Gao, L-J Chen and Z L Wang, *Piezoelectric Nanogenerator Using P-Type Zno Nanowire Arrays.* Nano Letters, 2009. **9**(3): p. 5.

116. X Wang, J Song, J Liu and Z L Wang, *Direct-Current Nanogenerator Driven by Ultrasonic Waves.* Science, 2007. **316**(5821): p. 102-105.

117. X Duan, Y Huang, Y Cui, J Wang and C M Lieber, *Indium Phosphide Nanowires as Building Blocks for Nanoscale Electronic and Optoelectronic Devices.* Nature, 2001. **409**(6816): p. 66-69.

118. S Bu, C Cui, Q Wang and L Bai, *Growth of Zno Nanowires in Aqueous Solution by a Dissolution-Growth Mechanism.* J. Nanomaterials, 2008. **2008**(1): p. 1-5.

119. R S Wagner and W C Ellis, *Vapor-Liquid-Solid Mechanism of Single Crystal Growth.* Applied Physics Letters, 1964. **4**(5): p. 89-90.

120. J K Jian, C Wang, Z H Zhang, X L Chen, L H Xu and T M Wang, *Necktie-Like Zno Nanobelts Grown by a Self-Catalytic Vls Process.* Materials Letters, 2006. **60**(29-30): p. 3809-3812.

121. Y Civale, L K Nanver, P Hadley and E J G Goudena, *Aspects of Silicon Nanowire Synthesis by Aluminum-Catalyzed Vapor-Liquid-Solid Mechanism.*

122. S Y Cortes-Jimenez, *Site Specific Nanowire Growth.* MATERIALS • NNIN REU 2006 Research Accomplishments, 2006.

123. E G Lori, L Matt, G Joshua, K Franklin, C J Justin, Z Yanfeng, J S Richard and Y Peidong, *Low-Temperature Wafer-Scale Production of Zno Nanowire Arrays.* Angewandte Chemie International Edition, 2003. **42**(26): p. 3031-3034.

124. U Husnu Emrah, H Pritesh, R Nalin, D Sharvari, I M William and A J A Gehan, *Rapid Synthesis of Aligned Zinc Oxide Nanowires.* Nanotechnology, 2008(25): p. 255608.

125. Y Nakamura, *Solution-Growth of Zinc Oxide Nanowires for Eye-Sensitized Solar Cells.* MATERIALS • NNIN REU 2006 Research Accomplishments, 2006: p. 74-75.

126. Y Qin, X Wang and Z L Wang, *Microfibre-Nanowire Hybrid Structure for Energy Scavenging.* Nature, 2008. **451**(7180): p. 809-813.

127. M E Coltrin, J W P Hsu, D A Scrymgeour, J R Creighton, N C Simmons and C M Matzke, *Chemical Kinetics and Mass Transport Effects in Solution-Based Selective-Area Growth of Zno Nanorods.* Journal of Crystal Growth, 2008. **310**(3): p. 584-593.

128. L E Greene, B D Yuhas, M Law, D Zitoun and P Yang, *Solution-Grown Zinc Oxide Nanowires.* Inorganic Chemistry, 2006. **45**(19): p. 7535-7543.

129. L Vayssieres, K Keis, A Hagfeldt and S-E Lindquist, *Three-Dimensional Array of Highly Oriented Crystalline Zno Microtubes.* Chemistry of Materials, 2001. **13**(12): p. 4395-4398.

130. S-Y Liu, T Chen, J Wan, G-P Ru, B-Z Li and X-P Qu, *The Effect of Pre-Annealing of Sputtered Zno Seed Layers on Growth of Zno Nanorods through a Hydrothermal Method.* Applied Physics A: Materials Science & Processing, 2009. **94**(4): p. 775-780.

131. H Yang, J-S Lee, S Bae and J H Hwang, *Density-Controlled Growth of Zno Nanorods Using Zno Nanocrystals-Embedded Polymer Composite.* Current Applied Physics, 2009. **9**(4): p. 797-801.

132. L W Ji, S M Peng, T H Fang, C H Liu, W H Hsieh and W Y Jywe. *Well-Aligned Zno Nanowire Arrays Grown on Zno/Glass Substrates*. in *Taiwan & Mainland China, Summit of University Principals, 2008*. 2008. Tai Wan.

133. W-J Li, E-W Shi, W-Z Zhong and Z-W Yin, *Growth Mechanism and Growth Habit of Oxide Crystals.* Journal of Crystal Growth, 1999. **203**(1-2): p. 186-196.

134. L Demianets, D Kostomarov, I Kuz'mina and S Pushko, *Mechanism of Growth of Zno Single Crystals from Hydrothermal Alkali Solutions.* Crystallography Reports, 2002. **47**(0): p. S86-S98.

135. L N Demianets and D V Kostomarov, *Mechanism of Zinc Oxide Single Crystal Growth under Hydrothermal Conditions.* Annales de Chimie Science des Mat 閌 iaux. **26**(1): p. 193-198.

136. K Govender, D S Boyle, P B Kenway and P O'Brien, *Understanding the Factors That Govern the Deposition and Morphology of Thin Films of Zno from Aqueous Solution.* Journal of materials Chemistry, 2004. **14**(16): p. 2575-2591.

137. H Wang, J Xie, K Yan and M Duan, *Growth Mechanism of Different Morphologies of Zno Crystals Prepared by Hydrothermal Method.* Journal of Materials Science and Technology. **27**(2): p. 153-158.

138. B G Wang, E W Shi and W Z Zhong, *Understanding and Controlling the Morphology of Zno Crystallites under Hydrothermal Conditions.* Crystal Research and Technology, 1997. **32**(5): p. 659-667.

139. T Maruo, N Ueno, S Ichikawa, N Nishiyama, Y Egashira and K Ueyama, *Transmission Electron Microscopy Study on the Growth of Zinc Oxide Crystals under Hydrothermal Conditions.* Materials Letters, 2009. **63**(27): p. 2373-2376.

140. D Kashchiev and A Firoozabadi, *Driving Force for Crystallization of Gas Hydrates.* Journal of Crystal Growth, 2002. **241**(1-2): p. 220-230.

141. L Vayssieres, *Growth of Arrayed Nanorods and Nanowires of Zno from Aqueous Solutions.* Advanced Materials, 2003. **15**(5): p. 464-466.

142. E M Wong, J E Bonevich and P C Searson, *Growth Kinetics of Nanocrystalline Zno Particles from Colloidal Suspensions.* The Journal of Physical Chemistry B, 1998. **102**(40): p. 7770-7775.

143. Z Hu, D J Escamilla Ramirez, B E Heredia Cervera, G Oskam and P C Searson, *Synthesis of Zno Nanoparticles in 2-Propanol by Reaction with Water.* The Journal of Physical Chemistry B, 2005. **109**(22): p. 11209-11214.

144. C Xu, P Shin, L Cao and D Gao, *Preferential Growth of Long Zno Nanowire Array and Its Application in Dye-Sensitized Solar Cells.* The Journal of Physical Chemistry C, 2009. **114**(1): p. 125-129.

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