ESTIMATION OF THERMAL IMPEDANCE PARAMETERS OF SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

by

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ABSTRACT

ESTIMATION OF THERMAL IMPEDANCE PARAMETERS OF SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

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Silicon Germanium (SiGe) hetero junction bipolar transistors (HBTs) are used in a variety of circuits like analog mixed signal and RF(radio frequency) circuits. As the device gets smaller these days the self heating affects the performance of the SiGe HBTs. This paper uses theoretical methods based on device geometry and material properties to calculate the thermal resistance and thermal capacitance of SiGe HBT. In addition to theoretical estimations time domain, frequency domain and DC measurements are done on National Semiconductor's CBC8 HBTs which is used to extract the values of thermal impedance parameters.

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CHAPTER 1

INTRODUCTION

High bandwidth and throughput requirements for communication systems have called for increased use of high speed transistors in circuits. New fabrication technologies along with miniaturized circuit designs have helped in reducing the size of mobile handsets and other electronic equipments. These 'state of the art' devices are meant to be operated at higher frequency ranges (GHz ranges) and therefore the basic active devices used in these circuits should be capable of operating at GHz range. The Silicon-Germanium (SiGe) Hetero-junction Bipolar Transistor (HBT) is one such device which is capable of operating at such high frequencies.

Silicon-Germanium (SiGe) Hetero-junction Bipolar Transistor (HBT) has been used in a variety of circuit applications such as analog, mixed signal and RF circuits. It is observed that SiGe HBTs with a peak unity gain in the GHz range are capable of operating at higher frequency bands. The compatibility of SiGe with Si permits design of highly complex circuits which can be used in high speed mixed signal applications. The SiGe HBT used with BiCMOS technology enables the manufacture of high performance "system-on-a-chip" (SoC) architectures with reduced chip count, power consumption, packing complexity and cost [2].

The performance of SiGe HBTs is affected by the operating temperature of the device. The change in operating temperature is usually caused by self heating or adjacent heating. The small size of the device along with the advanced isolation technique of silicon-on-insulator (SOI) and deep trench oxide isolation (DTI) traps more heat within the active operating region of the device. The low thermal conductivity of the oxide layers further adds to the heat trapping

problem. The self heating of the HBT is characterized as thermal spreading impedance. The thermal impedance parameters of the device can be determined using device geometry and material properties [3]. It is reported [3] that the effect of self-heating is more prominent with transistors with reduced geometries. This thesis deals with the study of self-heating aspects of HBTs and characterization of SiGe HBTs from the CBC8 process of National Semiconductor.

The HBT provides better gain and frequency range of operation compared to the BJT. The emitter in the HBT is made of a different material than the base. The emitter material has a larger band gap compared to the base which causes the electrons injected across the junction from the emitter to have high potential energy. This leads to high current gain. However, the current gain is limited by the recombination in the base region. The current gain can further be increased by making the base narrower. The base width is inversely proportional to the operating frequency. Hence there is a tradeoff between the gain and frequency of operation. In a SiGe HBT, incorporation of material like Ge into the crystal lattice of the silicon creates a compressive strain in the material (because the Ge atom requires a larger atomic separation), and as a result, reduces the band gap of the material of the base. Figure 1.1 shows of the energy bands of an HBT.

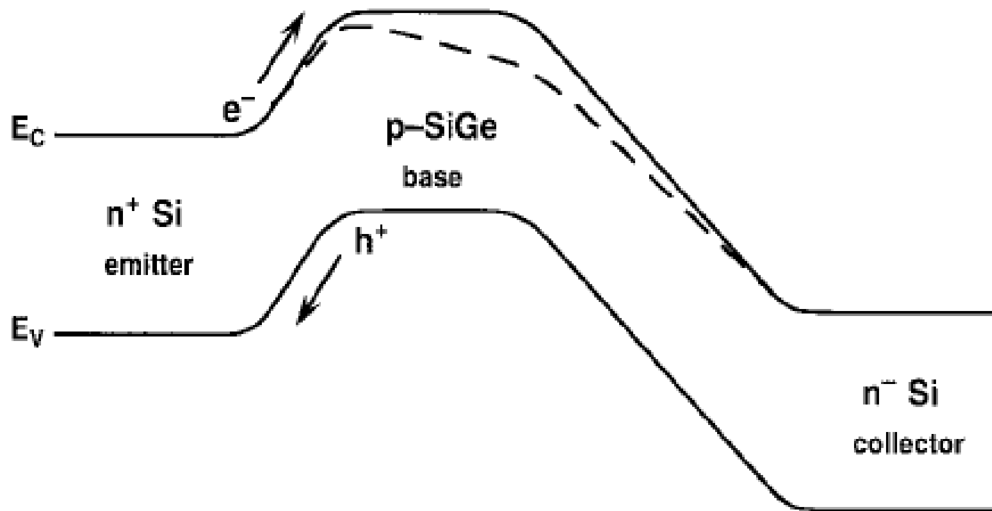

Figure 1.1 Energy band diagram of an HBT [2].

HBTs are used in applications like power amplifiers and oscillators due to high power density and low phase noise. Materials used for making HBTs are Si/Ge, AlGaAs/GaAs, InGaP/GaAs, and InP/InGaAs. The SiGe HBT contains a SiGe alloy in the base. The amount of Ge introduced in the base varies from process to process, but it is usually in the interval from 8 to 15 % [4]. Lattice mismatch and traps are minimized by having a graded doping profile in the base between the emitter edge and collector edge.

1.1 Self-heating of the transistor

The power dissipated across the pn junctions results in self heating of the transistor. Device isolation techniques used makes the heat spreading difficult and traps the heat produced within the device. The self heating of the HBT can be characterized as thermal resistance and thermal capacitance. This can be modeled as a single pole RC network or a multi pole RC network. The thermal spreading impedance can be determined using the material properties and geometric dimensions of the device.

1.1.1 Definition of thermal Parameters

1.1.1.1 Thermal resistance [5]

Thermal resistance is defined as the ratio of the difference in temperatures between two isothermal surfaces to the total heat flow between them. Thermal resistance R_{TH} can be expressed as [5]

$$R_{TH} = \frac{T_J - T_A}{P} \tag{1.1}$$

where T_J is the junction temperature, T_A is the ambient temperature, and P is the heat flow rate[5].

The unit for R_{TH} is K/W.

1.1.1.2 Thermal capacitance [5]

Thermal capacitance (C_{TH}) is the amount of heat energy that can be stored and dissipated in a device. The unit for C_{TH} is J/K.

1.1.2. Thermal-Electrical analogy [6]

The rise in temperature ΔT, can be written as

$$\Delta T = R_{TH} \times P \quad (1.2)$$

where P is the power dissipation.

Temperature rise in the thermal network is analogous to the voltage rise in an electrical network. Table 1.1 summarizes this analogy between thermal and electrical networks.

Table 1.1 Thermal – Electrical analogy [5]

Thermal		**Electrical**	
Temperature	T in K	Voltage	V in Volt
Heat flow	P in W	Current	I in Amp
Thermal resistance	R_{TH} in K/W	Resistance	R in Ohm
Thermal capacitance	C_{TH} in J/K	Capacitance	C in Farad

1.2 A Simple Thermal Network

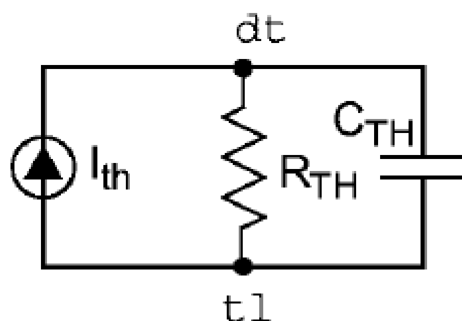

Figure 1.2 The thermal network in VBIC Model [14].

The simple thermal network shown in figure 1.2 is that used by a VBIC model to model the thermal characteristics of a transistor. A detailed description of the VBIC model is given in section 1.3.5. The thermal network models the interaction between electrical characteristics and the thermal effects. In the above thermal network I_{th} corresponds to dissipated power in the thermal domain. The node dt represents the temperature node at which the voltage rise will happen in electrical which corresponds to a temperature rise in the thermal domain. Thus, from equation 1.2 the voltage at the temperature node dt (as per VBIC syntax) is numerically equal to the local temperature rise in K.

1.3 Modeling of HBTs

A transistor model can describe the operational behavior of a transistor in a circuit. This helps in optimum design of circuits.There are various categories of transistor models today. They are explained below:

1.3.1 Physics Based Models

These models are derived based on device physics knowledge. They take into account the material properties, device dimensions, doping profiles, drift-diffusion equations, Schrodinger equation and thermal diffusion equations. Physics based models are the most accurate models. Errors in the model can be caused due to lattice imperfections or crystal defects. An example of a physical model is given in [7]. However such models require large

simulation times. When used in large complex circuits such long simulation times are disadvantageous.

1.3.2 Physics Based Analytical Models

Device equations are analytically solved and simplified to remove the discontinuities in the functions and their derivations. The final equations could be solved with a computer and a circuit model based on the analytical solutions is derived. A one-dimensional representation can be used as a good approximation to the intrinsic behavior of a bipolar junction transistor. Using several assumptions, these equations can be simplified resulting in ordinary differential equations and solutions obtained using the appropriate boundary conditions. A circuit model can be found by combining several nonlinear resistors, capacitors and controlled current and voltage sources. Two good examples of this kind of modeling are the Ebers-Moll model [8] and the Gummel-Poon model [9]. HICUM (High Current Model) [10-12], Philips MEXTRAM [13], and VBIC-95 (Vertical Bipolar Intercompany) model [14] are other popular models that fall under this category.

These models have short simulation time and high accuracy. Optimizations and simulations using large RF signals can be done easily. It is also easy to understand the behavior of models which are built up this way. However the validity of the model depends on the validity of the physical analysis of the device and the validity of all the approximations made during the process to derive the final circuit model. Other limitations include limited bandwidth and the limited area of active region where the model can be used.

1.3.3 Black Box Analytical Models (Empirical Model)

These models are based on measurement data. The model is derived by use of mathematical equations representing the relationship between input and output responses to known excitations. The main disadvantage with this kind of model is the lack of physical parameters so that it cannot give direct physical explanations of device properties. Also the validity of the model depends on how the mathematical equations fit the measured data.

Theoretically, one should use an infinite number of responses to ensure a valid model for all possible kinds of excitations.

1.3.4 Models based on Look up Tables

The measurement results are tabulated in a look up table from which model values are obtained. The model uses interpolation to get intermediate model values. The model has a short simulation time. Also the model is process independent. Almost any device can be modeled with this model, as long as all the necessary measurements can be made. The model measurements used should cover a wide range of DC biases, frequencies and power levels. The main limitation with this kind of model is insufficient physical parameters and it cannot explain device properties accurately. Also the measurements may get very complex and might require specialized measurement equipment to find certain properties of the device.

1.3.5 The VBIC Model

The thesis focuses on thermal characteristics as modeled by the VBIC model. The VBIC model [14] was developed by a consortium of large companies in the BJT industry including Motorola, Texas Instruments, Analog Devices, Hewlett-Packard, IBM, etc. Figure 1.3 shows the schematic of the VBIC model.

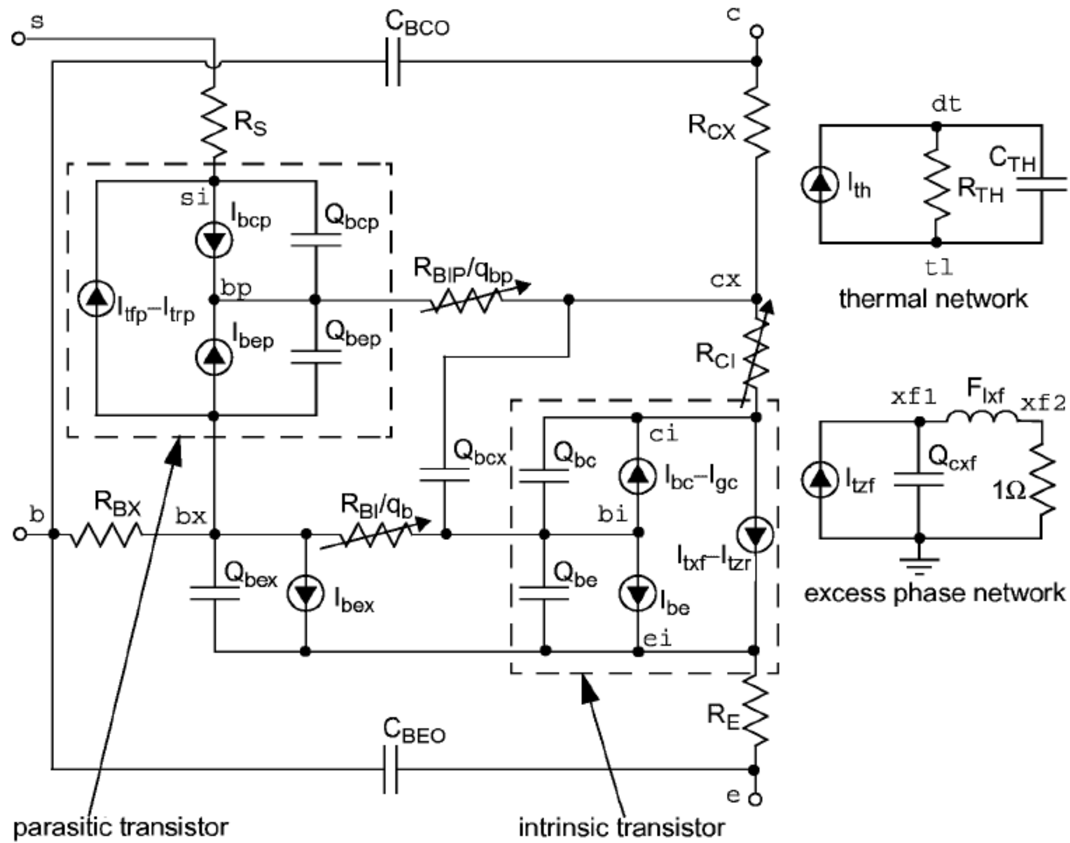

Figure 1.3 Schematic of the VBIC Model [14].

The VBIC model is an improved version of Gummel Poon(GP) model. The main advantage of VBIC over GP is the ability to model self heating which was not present in GP. Furthermore, VBIC include full parasitic substrate transistor modeling, separation of I_c and I_b without being empirically related through β_F, Early effect modeling based on depletion charge, constant overlap capacitances, base emitter break down modeling and improved depletion and diffusion charge models. The VBIC model can be used for BJTs and HBTs. VBIC has several temperature parameters. The parameters which model the self heating are R_{TH} and C_{TH}. The major temperature dependent parameter is the saturation current I_S. The other temperature parameters include temperature exponent X_{IS} of the forward saturation current I_S, the

temperature exponent X_{II} of the saturation currents I_{BEI}, I_{BCI}, I_{BEIP}, $I_{BCIP,}$ the temperature coefficient T_{NF} of N_F, temperature exponents of the base, collector and emitter resistances X_{RB}, X_{RC}, and $X_{RE,}$ temperature coefficient T_{AVC} of the base collector weak avalanche parameters A_{VC1} and A_{VC2} and temperature exponent X_{VO} of the epitaxial drift saturation voltage V_o. At normal operating temperatures only $R_{TH,}$ C_{TH} and I_S plays a significant role and the temperature dependence of all other parameters are negligible. The thesis deals with characterizing the thermal behavior of HBTs and discusses means of extraction of $R_{TH,}$ C_{TH} of VBIC model of HBT through theoretical calculations, measurements and simulations.

CHAPTER 2

THEORETICAL ESTIMATIONS OF THERMAL IMPEDANCE PARAMETERS

The geometrical information of the device can be used to find the thermal impedance parameters. The physics based models which depend on the solution of numerous complex equations, which are again dependent on different boundary conditions, takes a long time to be solved and does not convey any useful information about the geometry of the system. The model presented here overcomes these limitations. Masana's method is used to derive the thermal impedance parameters of the Si-tub and oxide layers of the SiGe HBT.

2.1 Masana's Method of Thermal Impedance estimation

2.1.1 Derivation of Thermal Impedance parameters [16]

The time dependent equation of conduction of heat in an isotropic medium is given by

$$\nabla^2 T = \frac{1}{\alpha_p}\frac{\partial T}{\partial t} \tag{2.1}$$

where T is the temperature, α_p is the thermal diffusivity at constant pressure and ∇^2 is the Laplacian operator,

$$\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}$$

In the electrical domain, the corresponding basic equation for the potential is the wave equation

$$\nabla^2 V = \frac{1}{v^2}\frac{\partial^2 V}{\partial t^2} \tag{2.2}$$

where v is the velocity of voltage waves and V is the potential.

It is evident from equations 2.1 and 2.2 that the heat diffusion equation depends on the first derivative with respect to time, while in the wave equation has voltage depends on the second

derivative with respect to time. Thus, in the electric equivalent circuit there will be two different types of energy storage elements, while in the thermal equivalent circuit there will be only one. The resistance to the heat flow through a medium which depends on its thermal conductivity is called thermal resistance and the capacity to store heat within the medium is called the thermal capacitance. There is nothing similar to the magnetic field in heat transfer, so there is no thermal inductance.

The thermal resistance is defined as a lumped model obtained by the integrating over the distributed volume with certain boundaries. Consider a volume shown in Figure 2.1 with constant cross-section, S, constant temperature across S, constant and uniform heat flux q across S, zero heat flux flowing out of the vertical walls.

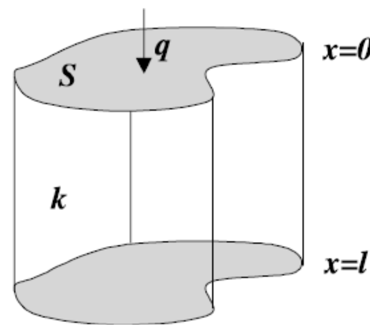

Figure 2.1 Volume for the calculation of thermal resistance [16].

Equation 2.1 is integrated in one-dimension, and the constant of integration is obtained by applying the boundary conditions. Thus the equation 2.1 reduces to [16]

$$\frac{dT}{dx} = -\frac{q}{k} \tag{2.3}$$

where k is the thermal conductivity of the medium. The rate of heat input to the volume is W=qS watts. Integrating once more and substituting for q as q=W/S gives

$$\frac{T_0 - T_l}{W} = \frac{l}{kS} = R_{TH} \tag{2.4}$$

where T_0 and T_l are the temperatures at x=0 and x=l respectively. Thus the thermal resistance between any two isothermal surfaces can be obtained, by solving equation 2.1 by applying suitable boundary conditions and dividing the temperature difference by the rate of heat flow

between the surfaces. The thermal resistance is found by integration along a path of length l with a cross-section S. The relevant characteristic of the medium filling the volume is the thermal conductivity k. Thermal capacity is a magnitude associated with heat storage and accordingly the integration has to be performed for the volume V=lS, with the heat capacity c_p as the relevant characteristic of the medium filling that volume. With these considerations [16]

$$C_{TH} = V\rho c_p \tag{2.5}$$

where ρ is the density of the medium with units kg/ m^3, V is the volume in m^3 , and c_p is the specific heat with units J/kg-K.

The SiGe transistor can be considered to be divided into different layers of materials. Here each layer can be represented using different RC networks. The variable angle method (VAM) [17] is used to calculate the thermal resistance of the volume sketched below. The heat source, its projection on the next layer boundary and the edges defined by the spreading angles α_1, α_2, β_1 and β_2 delimit this volume as shown in figure 2.2. These angles are associated with the source dimensions x and y respectively. In the general case, the spreading is different for each side of the heat source according to its placement with respect to the substrate.

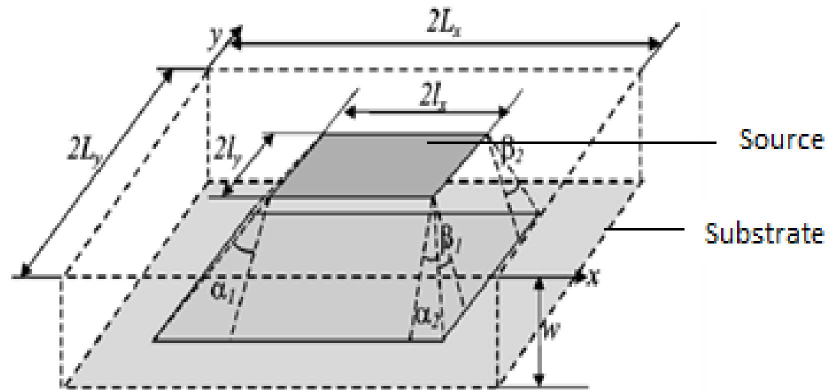

Figure 2.2 Volume for applying VAM [17].

Using equation 2.4 the thermal resistance for that particular volume is given by [19]

$$R_{TH} = \frac{1}{k}\int_0^W \frac{dz}{[(l_x+z\ tan\alpha_1)+(l_x+z\ tan\alpha_2)][(l_y+z\ tan\ \beta_1)+(l_y+z\ tan\beta_2)]} \tag{2.6}$$

Integrating equation 2.6,

$$R_{TH} = \frac{1}{4kl_x}\frac{1}{(\gamma_e \tan\alpha - \tan\beta)} ln \frac{l_x + w\ tan\ \alpha}{l_x + w\ tan\ ^{\beta}/_{\gamma_e}} \tag{2.7}$$

where $\gamma_e = l_y/l_x$ and $\gamma_s = L_y/L_x$ are the aspect ratios of the heating element and substrate respectively. The spreading angles are given by [19]

$$(\tan\alpha)_i = \frac{(\tan\alpha_1 + \tan\alpha_2)_i}{2} = \left(1 + \frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_x^2}\right)\frac{w_n + [\rho_s/(1+\rho_s)]l_{xn}}{w_n + [1/(1+\rho_s)]l_{xn}}\bigg|_i$$

$$(\tan\beta)_i = \frac{(\tan\beta_1 + \tan\beta_2)_i}{2} = \left(1 + \frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_y^2}\frac{\gamma_e}{\gamma_s}\right)\frac{w_n + [\rho_s/(1+\rho_s)]l_{xn}\gamma_e}{w_n + [1/(1+\rho_s)]l_{xn}\gamma_e}\bigg|_i \tag{2.8}$$

where its boundary dependence comes through ρ_s and ρ_L which are constants used in equations 2.6 and equation 2.8. ρ_s and ρ_L are defined as

$$\rho_s = \frac{k_i}{k_{i+1}}; \rho_L = \frac{k_i}{k_L} \tag{2.9}$$

In equation (2.9), k_i and k_{i+1} are the thermal conductivity of the present and the next layer respectively, and k_L represents the thermal conductivity of the lateral boundary of the system.

The source to substrate offset is taken into consideration by the aspect ratios γ_e and γ_s, the normalized dimensions $l_{xn}=l_x/L_x$ and $w_n=w/L_x$ and the eccentricity parameters given by [19]

$$\varepsilon_x = \frac{\sqrt{L_{x1}L_{x2}}}{L_x}; \varepsilon_y = \frac{\sqrt{L_{y1}L_{y2}}}{L_y}$$

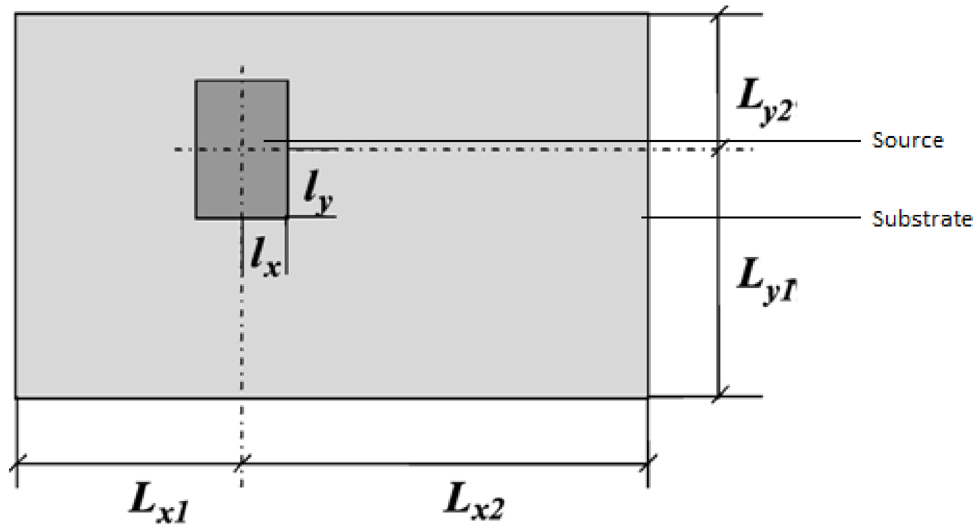

Figure 2.3 Source to substrate offset definition [17].

The side walls of the volume are assumed to be adiabatic, so heat flow takes place only inside the volume from top to bottom. This approximation is valid because the influence of the outer volume will be negligible in the overall heat conduction. Consequently, the same volume considered for the calculation of thermal resistance has to be used for the calculation of thermal capacitance in equation (2.5). The volume is calculated as [17]

$$V = 4\left[l_x l_y w + (l_x \tan\beta + l_y \tan\alpha)\frac{w^2}{2} + \tan\beta \tan\alpha \ \frac{w^3}{3}\right] \tag{2.11}$$

Since the expressions forming R_{TH} and C_{TH} are closed form equations, a spreadsheet has been used to perform the calculations.

2.2 Joy and Schlig's Method of thermal Impedance Estimation [18]

The wafer layer thermal impedance is estimated using the Joy and Schlig's method of thermal impedance estimation. Joy and Schlig's paper gives a mathematical model of the three dimensional transient heat flows which takes into account the physical structure of the device and the actual region of power dissipation. The model predicts the time-dependent temperature response to power dissipation as a function of time within the device. The effect of all chip boundaries except the one closest to the device is neglected. The top surface of the chip is

assumed to be adiabatic, that is there is no heat flow perpendicular to the boundary at that surface. This analysis assumes that the medium is a semi-infinite homogeneous half space.

The power dissipation in a bipolar transistor occurs mainly in the collector base depletion region. In this region the carriers gain high energy that involves phonon interactions with the lattice thereby giving up thermal energy. A solid rectangular parallelepiped submerged beneath the surface of the semi-infinite medium, as shown in Figure 2.4, can be used as an approximation of the heat source region in the device.

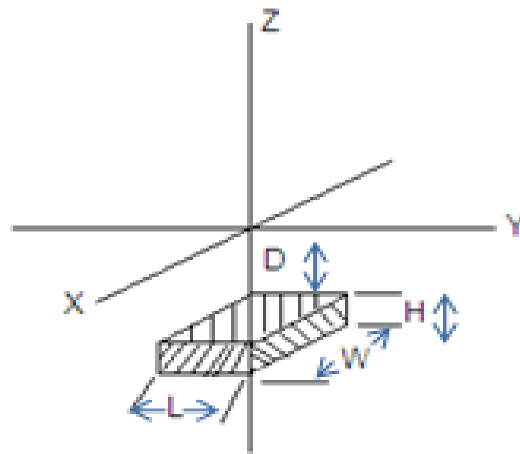

Figure 2.4 Heat source, simulating transistor power dissipation located below the surface of a semi-infinite medium [18].

The shaded region of dimensions $L \times W \times H$ located at a depth D below the surface shows volume in which the power is dissipated. For a transistor L and W would correspond to the length and width of the emitter stripe, H the approximate thickness of the depletion region, and D the depth of the collector base depletion junction below the surface [18]. The expression for temperature of an instantaneous point source is derived and then integrated throughout the volume of the heat source. The increase in temperature at any point in the semi-infinite medium to a step increase in power, P at time=0 is given by [18]

$$T(x,y,z,t) =$$

$$\frac{P}{8C}\int_0^t \left[erf\left(\frac{W/_2+x}{\sqrt{4ku}}\right)+erf\left(\frac{W/_2-x}{\sqrt{4ku}}\right)\right].\left[erf\left(\frac{L/_2+y}{\sqrt{4ku}}\right)+\right.$$

$$\left.erf\left(\frac{L/_2-y}{\sqrt{4ku}}\right)\right].\left[erf\left(\frac{z+D+H}{\sqrt{4ku}}\right)+erf\left(\frac{-D-z}{\sqrt{4ku}}\right)+\left[erf\left(\frac{z-D}{\sqrt{4ku}}\right)+erf\left(\frac{D+H-z}{\sqrt{4ku}}\right)\right]\right]du \tag{2.12}$$

where C=ρcV and V=L×W×H. Here ρ represents the density of the solid and c represents the specific heat of the solid. The thermal resistance is the ratio of the final value of the temperature increase to the power dissipated given by [18]

$$R_{TH}(x,y,z) = {}^{T(x,y,z,\infty)}/_{P} \tag{2.13}$$

2.3 Network Topologies used to model the thermal Impedance

There are primarily two network topologies that can be used to represent the thermal impedance of different layers of a device namely the Foster network and the Cauer network. Figure 2.5 shows the Foster and Cauer networks with RC elements representing each individual layer of the device.

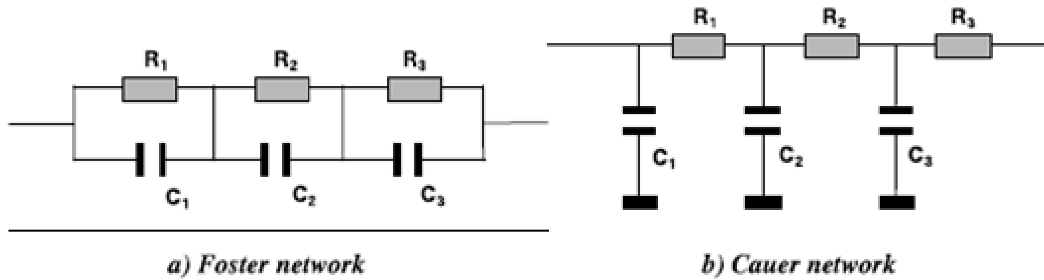

Figure 2.5 Foster and Cauer network representation [16].

In the Foster network, the time constants coincide with the RC products of each section whereas in the Cauer network, each time constant has contributions from all the R's and C's of the circuit. Thus calculating the R and C values from the time constants is not an easy task in the case of the Cauer network. However, it is possible to convert from Cauer to Foster and vice versa by considering equal driving point impedance for both networks. Though it is possible to

model the thermal network using either networks, it is found that the Cauer network closely models the physical representation of the thermal network. In an electrical circuit, the effective flow of ac current through a capacitor is by the accumulation of equal and opposite charges on its plates. In a thermal system heat flows only in one direction. There is no negative heat particle. Hence in the thermal regime there is no entity analogous to the negative charges in electrical circuits.

Consider the block of solid shown in figure 2.6 with temperatures T_1 K and T_2 K on the top and bottom surfaces respectively. In the electrical domain the nodes T1 and T2 correspond to voltages with numerical values equal to the temperature at the top and bottom surfaces of the solid respectively. R_{th} represents the thermal resistance to the heat flow from node T1 to T2 and C_{th} represents the heat capacitance of the solid which can be split equally between the two nodes. Thus the Cauer network explains electro-thermal analogy more accurately.

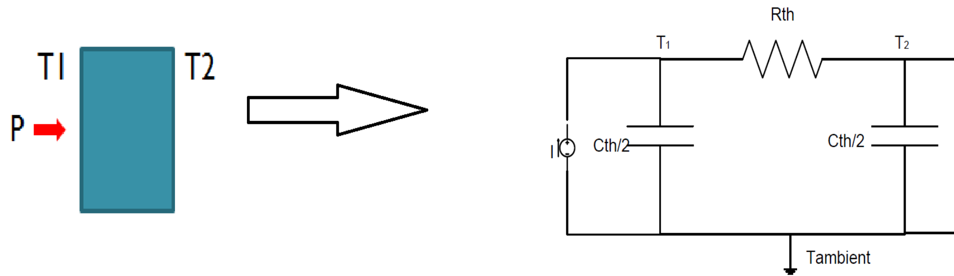

Figure 2.6 Cauer network representation of block of solid(on left) in the electrical domain(on right).

2.4 Conversion of the Foster network to the Cauer network [5]

The input impedance expression is found for the Foster network. The input impedance of a 3-pole Foster network in the Laplace domain is given by

$$Z_{in}(s) = \frac{R_1}{1+sR_1C_1} + \frac{R_2}{1+sR_2C_2} + \frac{R_3}{1+sR_3C_3} \quad (2.14)$$

Here s is the Laplace variable, all the R's and C's here are of the Foster network. This can be written as,

$$Z_{in}(s) = \frac{s^2(R_1R_2R_3C_2C_3 + R_1R_2R_3C_1C_3 + R_1R_2R_3C_1C_2)}{s^3(R_1R_2R_3\,C_1C_2C_3) + s^2(R_1R_3C_1C_3 + R_2R_3C_2C_3 + R_1R_2C_1C_2) + s(R_1C_1 + R_2C_2 + R_3C_3) + 1} +$$

$$\frac{s(R_1R_3C_3 + R_1R_2C_2 + R_2R_3C_3 + R_2R_1C_1 + R_3R_1C_1 + R_3R_2C_2) + (R_1 + R_2 + R_3)}{s^3(R_1R_2R_3C_1C_2C_3) + s^2(R_1R_3C_1C_3 + R_2R_3C_2C_3 + R_1R_2C_1C_2) + s(R_1C_1 + R_2C_2 + R_3C_3) + 1} \quad (2.15)$$

The Cauer method for synthesis of passive electrical networks can be applied to the input impedance expression to get the individual circuit element values of the corresponding Foster network. For this the below following algorithm is used [19].

1. $i = 1,2,3$ Since here a 3- pole circuit is considered.

2. $Z_1(s) = Z_{in}(s)$

Since the denominator of Zin(s) is one order higher than the numerator, start with the admittance expression.

3. $\frac{1}{Z_i(s)} = sC_{i,cauer} + Y_i^{'}(s)$

4. $\frac{1}{Y_i^{'}(s)} = R_{i,cauer} + Z_{i+1}(s)$

5. Repeat steps 3 and 4 until the remainder is zero either for step 3 or step 4.

A similar approach of conversion of Cauer to Foster topology is derived in Appendix A using the driving point impedance equivalence method.

2.5 Steps involved in the thermal modeling of a device

The steps involved in modeling the thermal network of a device are mentioned in this section.

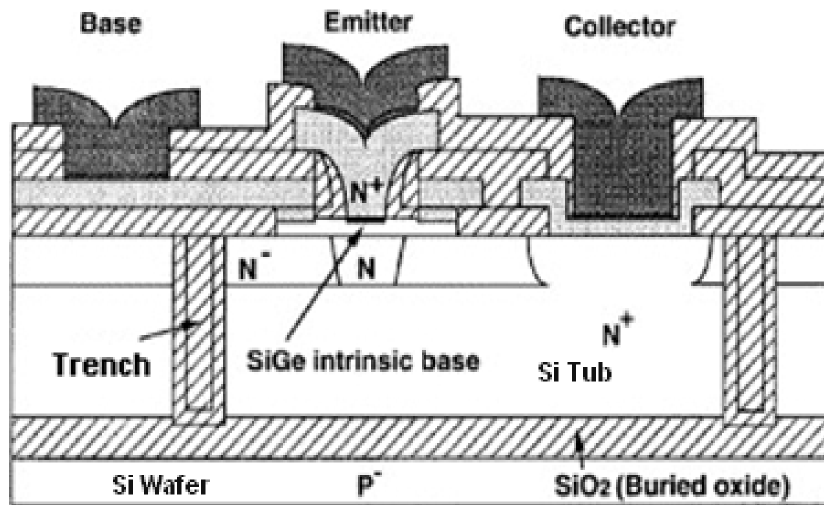

Figure 2.7 Typical structure of a SiGe HBT [22].

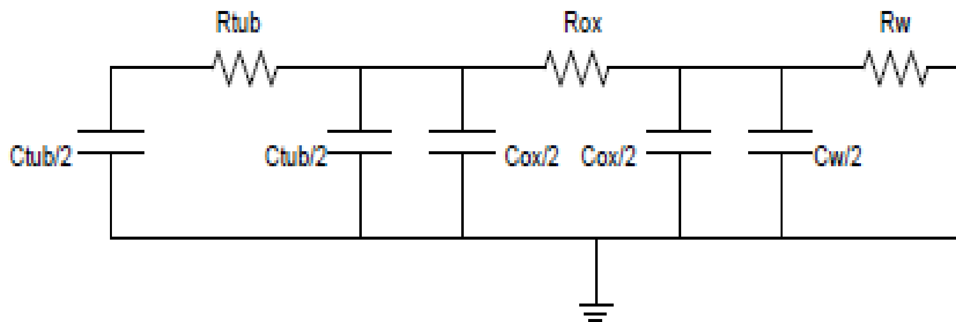

Figure 2.8 Cauer network representing the thermal circuit of SiGe HBT.

1. Find the R's and C's of the Cauer Network representation using the material property and geometry information of each layer using the method described in sections 2.1 and 2.2.The tub and oxide thermal impedances are determined using the Masana's calculations in section 2.1. The thermal impedance estimation for the wafer is done using Joy and Schlig's method in section 2.2. Figure 2.6 shows the typical structure of a SiGe HBT which is divided into 3 layers namely Si-tub, oxide and wafer layers for thermal impedance calculations.

2. The Cauer is shown in Figure 2.7. Here R_{tub}, C_{tub}, R_{ox}, C_{ox}, R_w and C_w denote the thermal resistance and capacitance of the Si-tub, oxide and wafer layers respectively.

2.6 Example Calculations of SiGe HBT from CBC8 process

The steps explained in 2.5 are used to estimate the Cauer circuit values of the thermal impedance network. Here a device with dimensions emitter length (Le) = 5um and emitter width (We) = 0.25um is used as a sample device to estimate the thermal impedance. A spreadsheet has been prepared for the implementing the mathematical formulae used for the calculations of thermal impedances of each layer. Masana's method is used for the Si-tub and Oxide layers. Joy and Schilg's method is used for wafer layer. The final Cauer network derived is as shown in Figure 2.8.

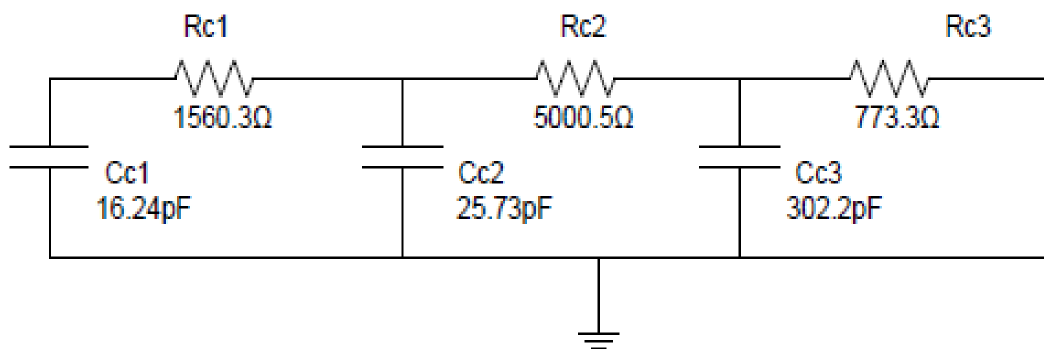

Figure 2.9 Cauer network representation of thermal impedance for a device with Le = 5um and We = 0.25um.

The above Cauer network is converted into Foster network and is as shown in Figure 2.10. The conversion formula is implemented in the spreadsheet calculator shown in Appendix B.

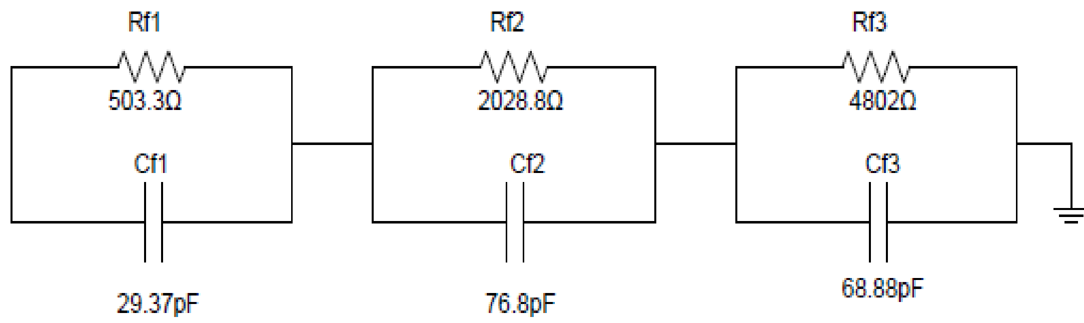

Figure 2.10 Foster network representation of thermal network for a SiGe HBT.

These thermal impedance values derived using the above methods are used as initial values for characterization of CBC8 device measurements.

CHAPTER 3

TIME DOMAIN MEASUREMENTS OF CBC8 DEVICES

There are various ways by which the thermal impedance of a given device can be measured and characterized. One such method is by taking time domain measurements on the devices. Here a 5um low voltage NPN device has been chosen for taking such measurements.

A pulse input is applied between the base and emitter of the HBT and the response at the emitter is observed. The pulse input results in a temperature change in the reverse biased collector base junction. The heat generated at this junction flows down though the tub and oxide layers to the wafer layer of the device at a rate determined by the thermal time constant of the device. The thermal time constant can be split into two major components namely, thermal resistance and thermal capacitance. The thermal resistance offers a resistance to heat flow in the device from the from heat source (collector-base junction) to the wafer where as the thermal capacitance indicates the ability to store heat in the device. The V_{be} of a device decreases with increase in temperature almost linearly [20]. This causes the V_{be} voltage to decrease at a rate dependent on the thermal time constant.

3.1 Circuit Description

There are restrictions on the amount of the current that can flow through the smaller devices. As the device used here is a 5um SiGe HBT it is important to limit the currents through the device and ensure that it is operating in the safe operating area (SOA).Different amplifier configurations have been studied. The popular common emitter configuration requires larger emitter resistance to be used to limit the current through smaller device. This large resistance along with the input capacitance of the oscilloscope causes low pass filtering of the V_{be} voltage.

This can cause a higher slope for V_{be} measured in the oscilloscope than the actual slope when the input pulse to the transistor goes from a low level to a high level. This results in incorrect readings of peak values for V_{be} and a wrong measurement of the thermal impedance. Therefore common base configuration is selected for measurements to avoid the use of large resistances when smaller dimension devices are used. The common base configuration used for the time domain measurement is as shown in Figure 3.1.

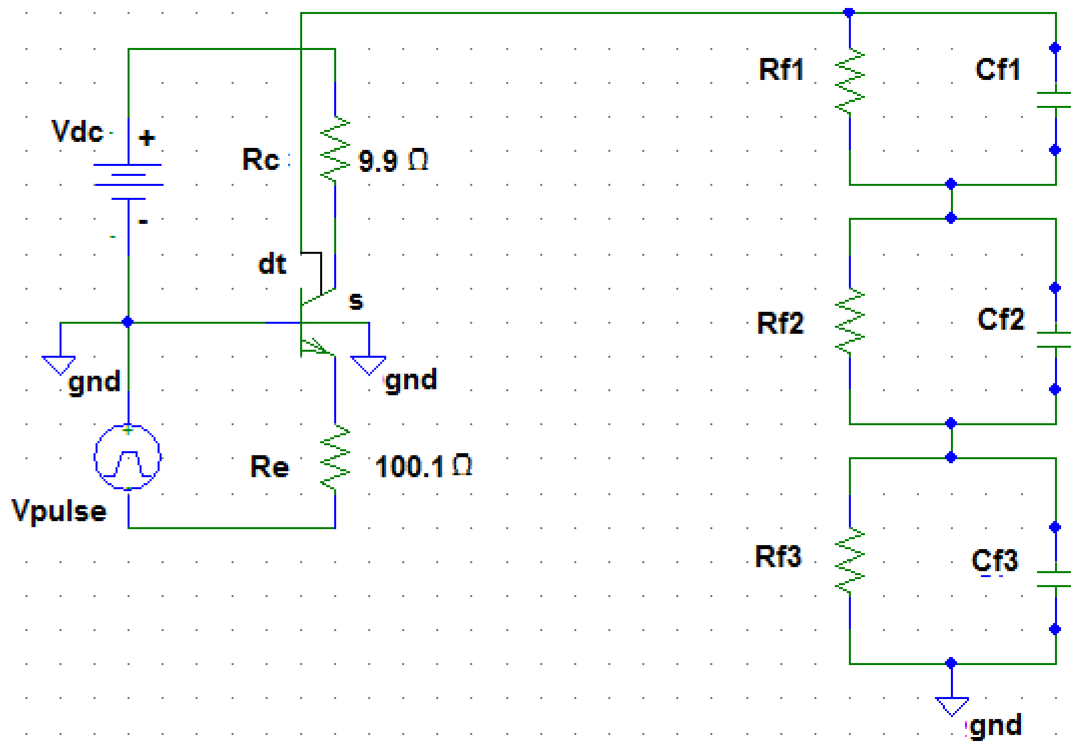

Figure 3.1 Common base setup for time domain measurements.

Figure 3.2 Connecting the Infinity Probe to the connector's circuit board.

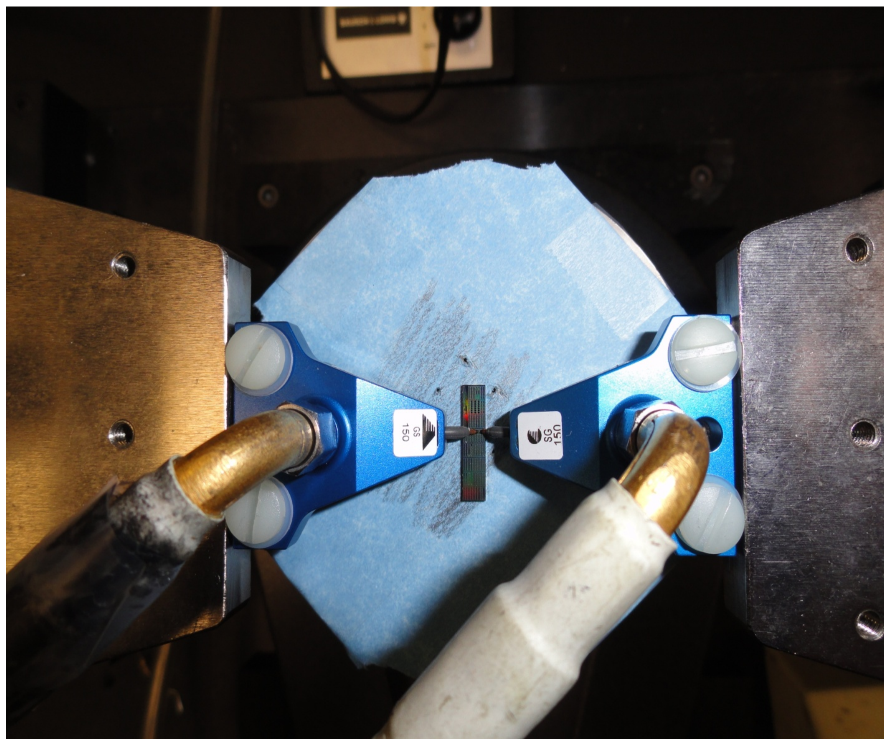

Figure 3.3 Cascade infinity probe connections on the wafer.

The wafers are probed using Cascade Infinity probes with 150 um pitch as shown in the Figure3.3. An Agilent 6000 series oscilloscope and function generator is used in the

measurement. The circuit is probed at four points. The pulse input from the function generator is fed between the base and emitter. The response at the emitter of the device is observed to see the thermal transient responses in the two half cycles of the pulse. The Cauer or Foster network derived through theoretical estimations in chapter 2 is used as starting values in the simulations used to optimize and match the measured responses. The simulations are done in ICCAP using the spmodeads simulator. The data taken from the measurement is given as input to ICCAP which then optimizes the R_{TH} and C_{TH} values to get the best fit between the measured and simulated curves. The bias levels for the device are chosen after simulations in-order to maintain the device in the safe operating area (SOA) limits provided by National Semiconductor.

Figure 3.4 The DC source and square pulse generator.

3.2 Processing and Optimization of time domain measurements

The time domain data captured from the oscilloscope is then saved as the output measured data in ICCAP. The delay, period, rise and fall times of the input pulse in the simulation is adjusted to exactly match that of the measurement setup. The spice model file for

the 5um low voltage NPN device is used to get the simulated response to the pulse input. The simulated response is then optimized using ICCAP optimization tool with Cauer or Foster network parameters as the optimization variables.

The ICCAP modeling software is used to measure a semiconductor device, model the device characteristics and analyze the resulting data. The general functional flow of a typical ICCAP system is shown in figure 3.5. There are various simulators like spectre, ADS, hpspice, spmodeads etc. that can invoked from ICCAP during simulations.

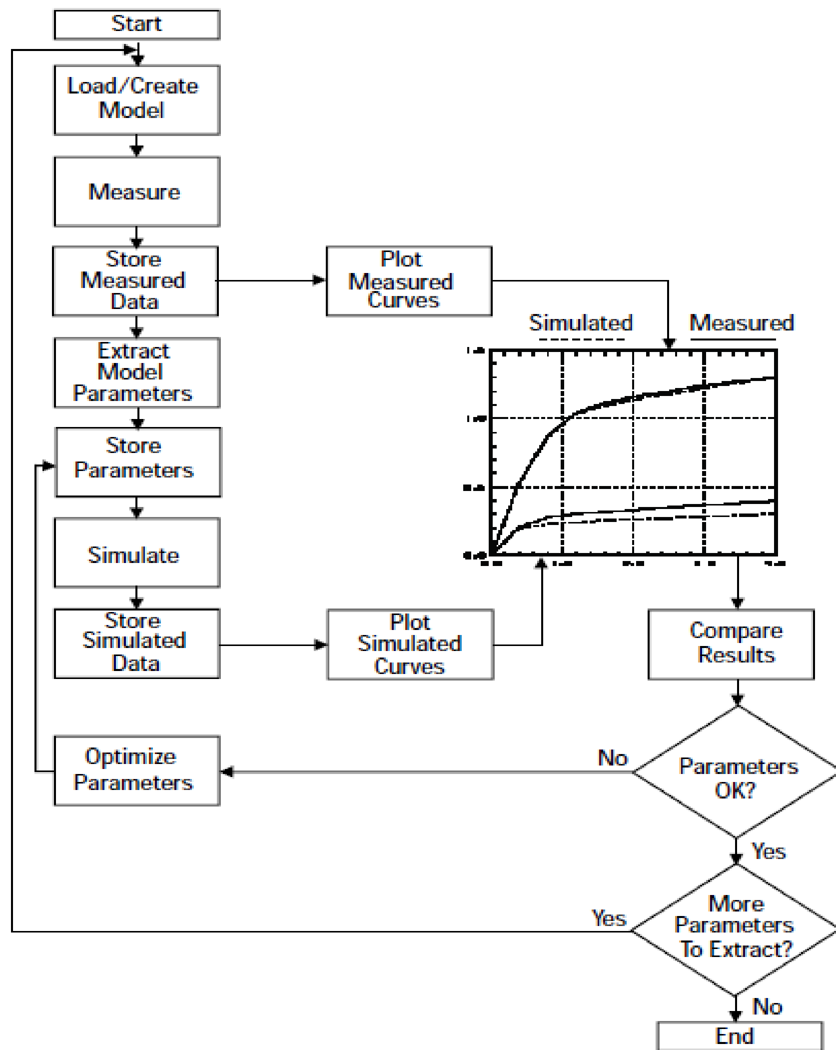

Figure 3.5 General functionality of ICCAP system [21].

Once the simulation is done using the model parameters and the appropriate input conditions the next step is to optimize the thermal response so as to match with the measured response. The optimization procedure followed by ICCAP is as shown in figure 3.6. The ‘Optimize’ function in ICCAP is used to do the optimization by setting the ‘X’ and ‘Y’ data ranges. The parameters to be used for the optimization are also specified in the ICCAP. The optimizer iteratively solves for a set of model parameters which produce simulated data that optimally matches with the measured data. There are different algorithms used for optimizations in ICCAP. The suitable algorithm is chosen depending upon the goal of optimization and nature of the model equations involved. If the model is well behaved and local minima are not a problem, the Levenberg-Marquardt optimization is used. The Levenberg-Marquardt method is a non-linear, least squares fit algorithm. It is a combination of steepest descent and Gauss-Newton methods. It calculates the specified model parameters in each iteration until the RMS error between measured and simulated data is minimized. Random optimization is used in the initial phase before a Levenberg-Marquardt optimization to reduce the error to an acceptable limit. Random optimization makes random guesses of the parameter values until the specified RMS error value is obtained. Hybrid optimization is a combination of the random and Levenberg-Marquardt optimizers.

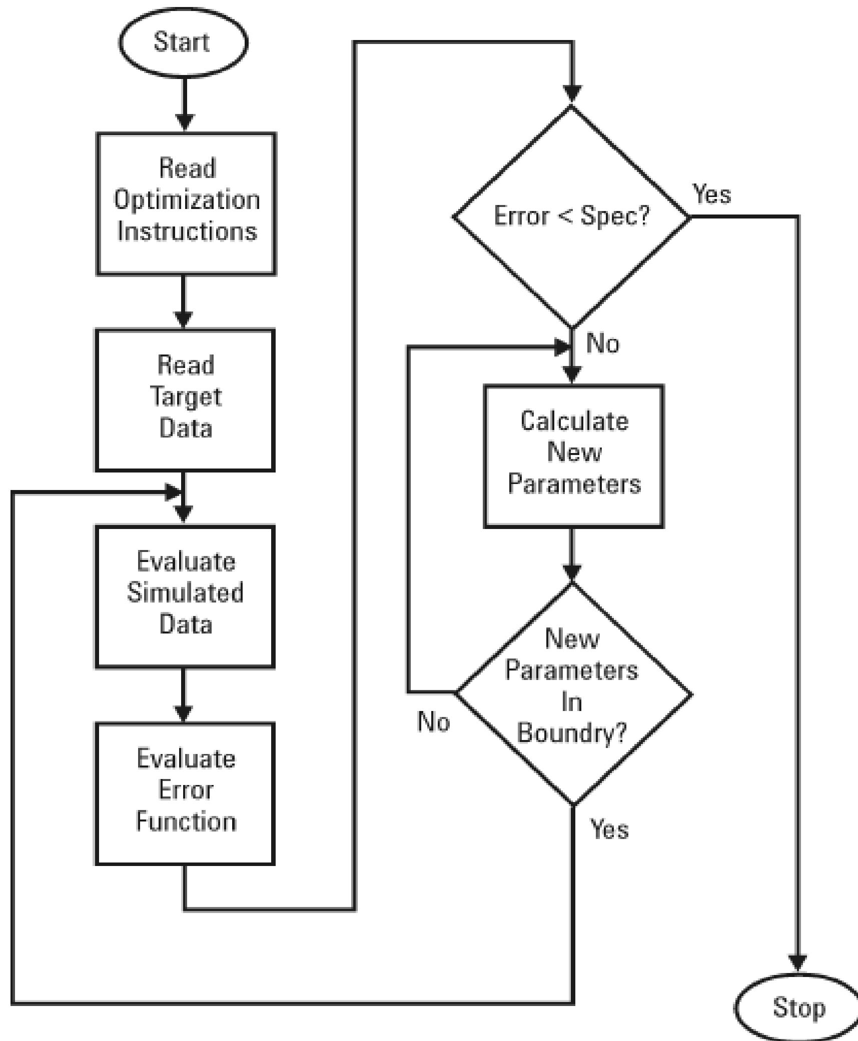

Figure 3.6 Optimization flow diagram [21].

3.3 Time domain measurement example of a 5um low voltage NPN SiGe HBT

The time domain measurements are done on a 5um low voltage NPN device from CBC8 process. The ICCAP optimization tool is used to match the simulated data to the measured data keeping the R and C values of the Foster network as the optimization parameters.

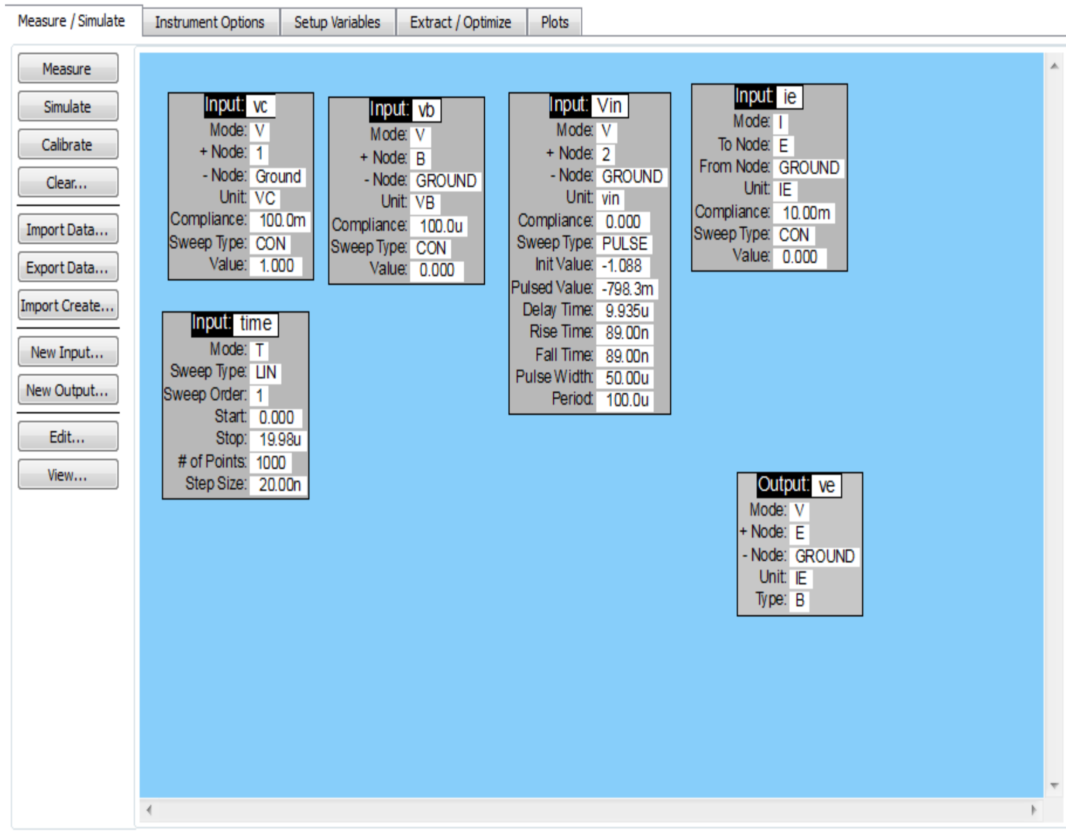

Figure 3.7 Measure/Simulate configurations in ICCAP.

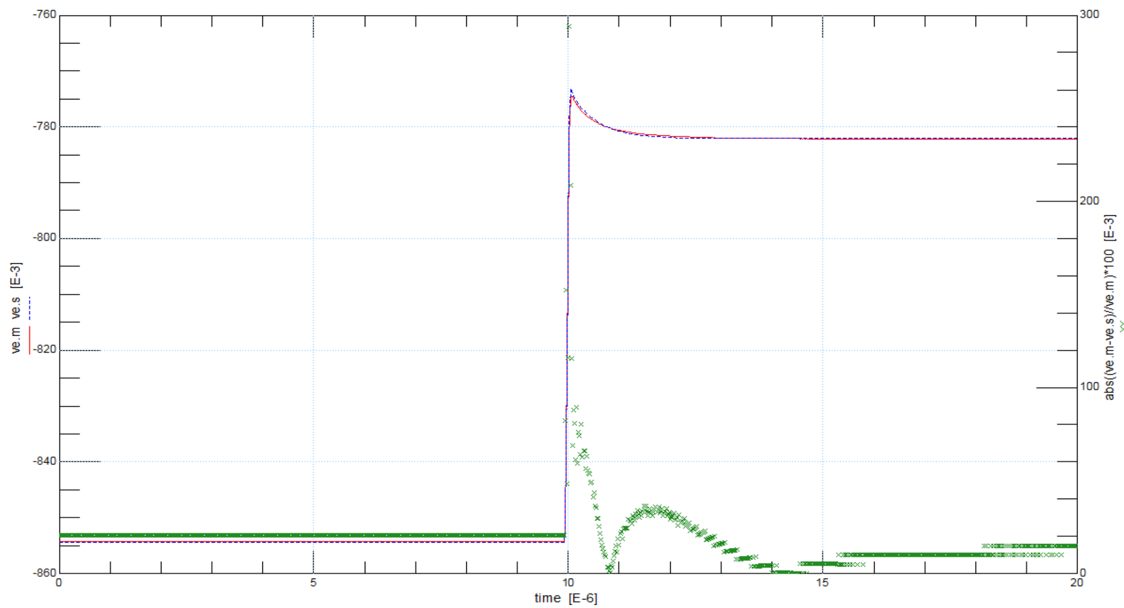

Figure 3.8 Rising edge after optimization.

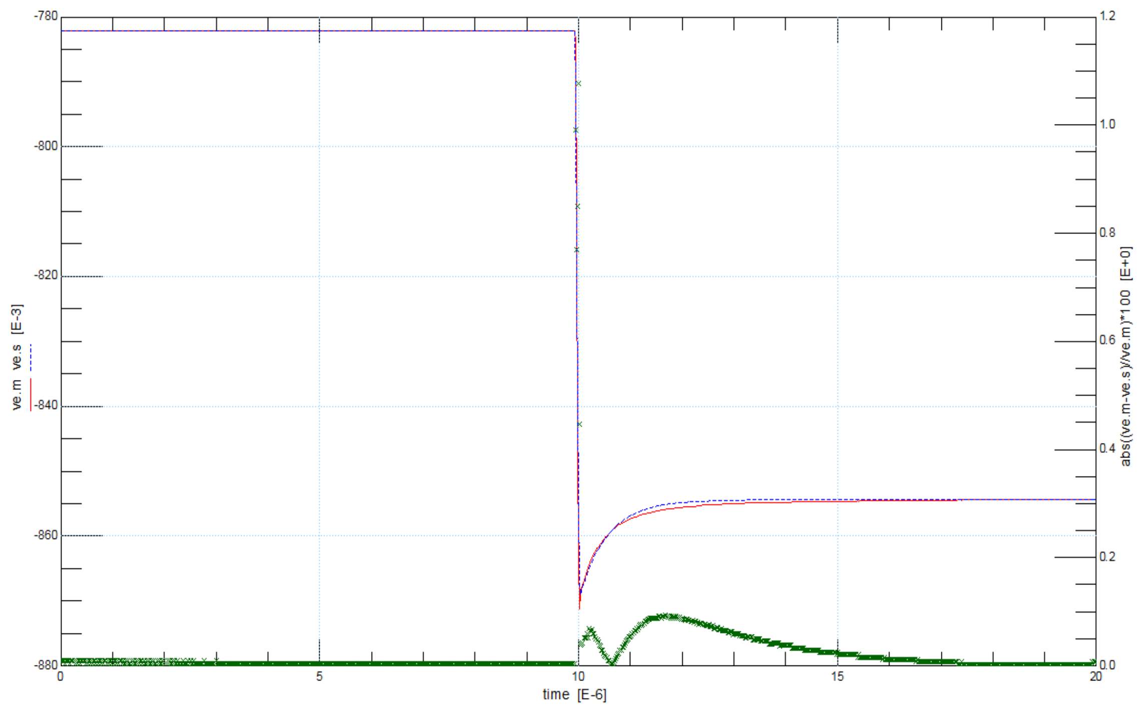

Figure 3.9 Falling edge after optimization.

Select Transform:

Optimize

Function: Optimize | Browse...

Algorithm: Levenberg-Marquardt | Error: Absolute

Inputs | Parameters | Options

Group: -- Select Group -- | Insert: -- Select from list -- | Clear Table | Autoset | Reset

Name	Min	Value	Max	Sto:
R1.r	20.1400	502.3	503.500	50:
C1.c	10.3900p	95.31p	259.700p	29
R2.r	852.600	4.458K	21.3200K	2.(
C2.c	7.52000p	116.5p	188.000p	76
R3.r	336.800	336.8	8.42000K	4.:
C3.c	68.8800p	1.343n	1.72200n	68
	1.00000f		1.00000MEG	0.(

Figure 3.10 Optimization window used for time domain optimizations in ICCAP showing the optimized values of Foster network resistors and capacitors.

3.4 Results and Discussion

Table 3.1 Table of initial and final values of foster network optimizations in time domain

	Rf1	Cf1	Rf2	Cf2	Rf3	Cf3
Initial Value	**503.3**	**29.37p**	**2.029K**	**76.8p**	**4.802K**	**68.88p**
Optimized Value	**502.3**	**95.31p**	**4.458K**	**116.5p**	**336.8**	**1.343n**

The time domain measurements on 5um HBT device were captured and used for extracting the values of the Foster network components. Optimizations are performed in the time range where the simulated trace is used to fit the measured trace both in the thermal tail region and also in the dc regions of the waveform. The theoretically estimated values of Foster network are used as initial values for optimizations. From the optimized values of R and C components it is observed that the the total optimized thermal resistance of the foster network matches with the total theoretical thermal resistance. The values of thermal capacitances of the foster network are also extracted in this method. Thus it is possible to extract both the thermal resistance and thermal capacitance of distributed network (Foster network) using the time domain measurement data.

CHAPTER 4

DC MEASUREMENTS OF CBC8 DEVICES

The DC measurements are performed on the 0.25um by 5 um HBT device to estimate the VBIC parameters R_{TH} and I_S. Forward active common base DC setup is used to capture the measurements. The wafers are probed with the cascade infinity (pitch150um) probes. DC source 4142 from Agilent and ICCAP software are used in the measurement setup. In the standard Forward active common base setup the collector and base are held at the same potential and base emitter voltage is swept between the permissible safe operating limits of the transistor. The plots of collector current versus base-emitter voltage and base current versus base-emitter voltage are plotted for various values of collector-base potentials. It is observed that the junction temperature of the HBT rises from the ambient temperature and as a result there is a significant difference in the currents between the simulated and measured Forward active common base plots. A setup is made in ICCAP in which first optimization is carried out so as to extract the exact value of I_S which will match the simulated current curve to measured currents.

4.1 Forward active common base circuit configuration and Optimizations

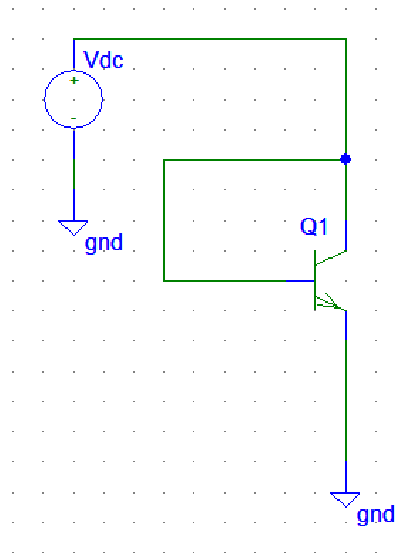

Figure 4.1 Forward active common base configuration.

The basic idea of the DC measurement is to extract the value of R_{TH} by varying the power dissipated at the junction and measuring the temperature change in each case. It is important to note that the collector-base voltage should remain constant for each setup so as to reduce the Early effect.

The typical Forward active common base circuit configuration is as shown in the figure 4.1. In this setup the collector and base terminals of the transistor are held at the same potential. The base-emitter voltage is varied to get plots of I_C and I_B versus V_{BE} voltage. The modular DC source 4142B drives the S-parameter ports of 8753ES from which the probe cable connections come out as shown in figure 4.4. Figure 4.2 shows the top view of the probe connections on the wafer and figure 4.3 shows the lateral view of the probe station setup with microscope and thermometer. The entire measurement setup is configured in ICCAP and the current curves are plotted. The ambient temperature at which the measurements are taken is noted using a thermometer.

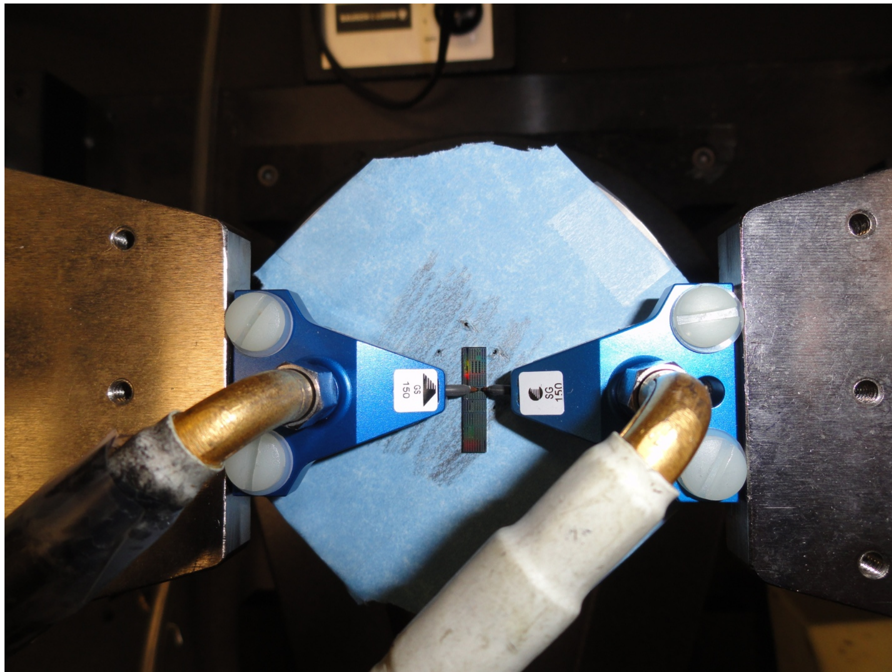

Figure 4.2 Probe connections on the wafer (Top view).

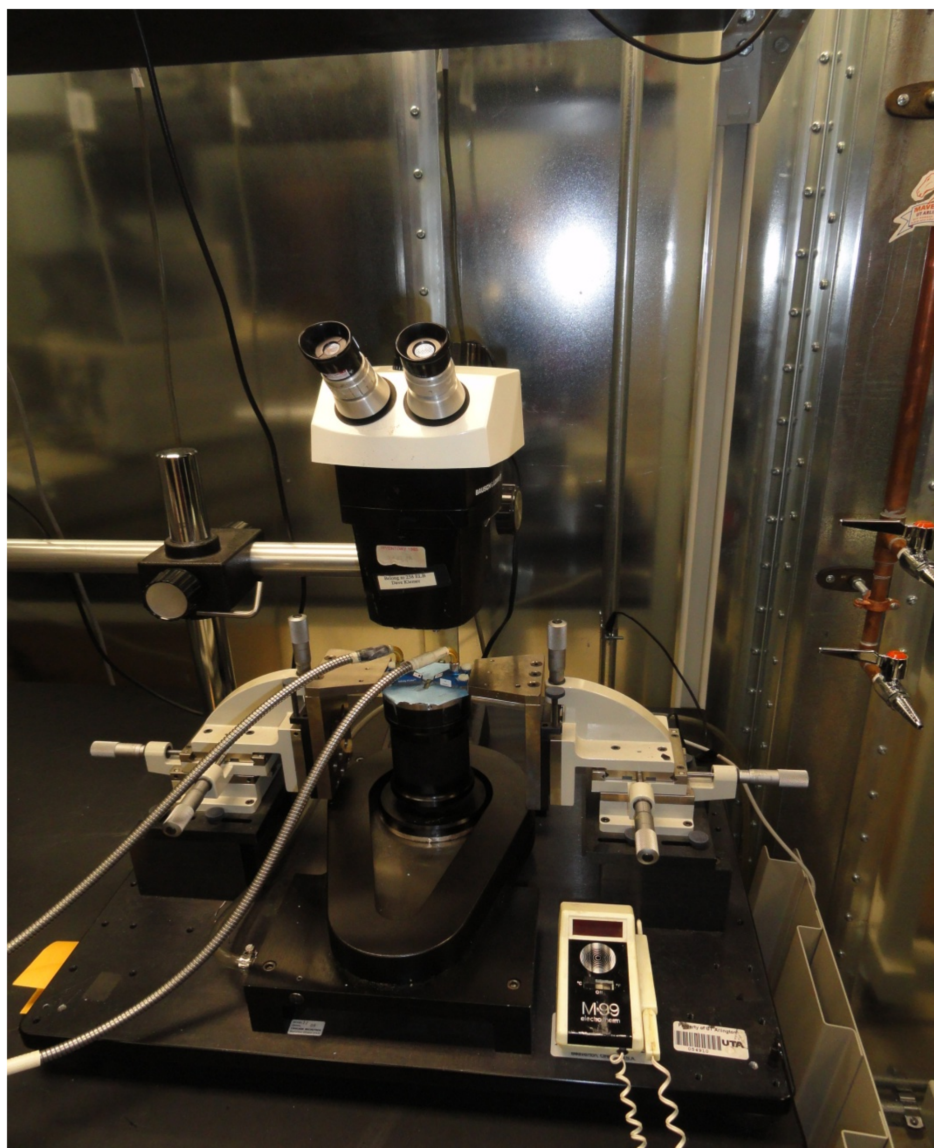

Figure 4.3 Probe station setup with microscope and thermometer.

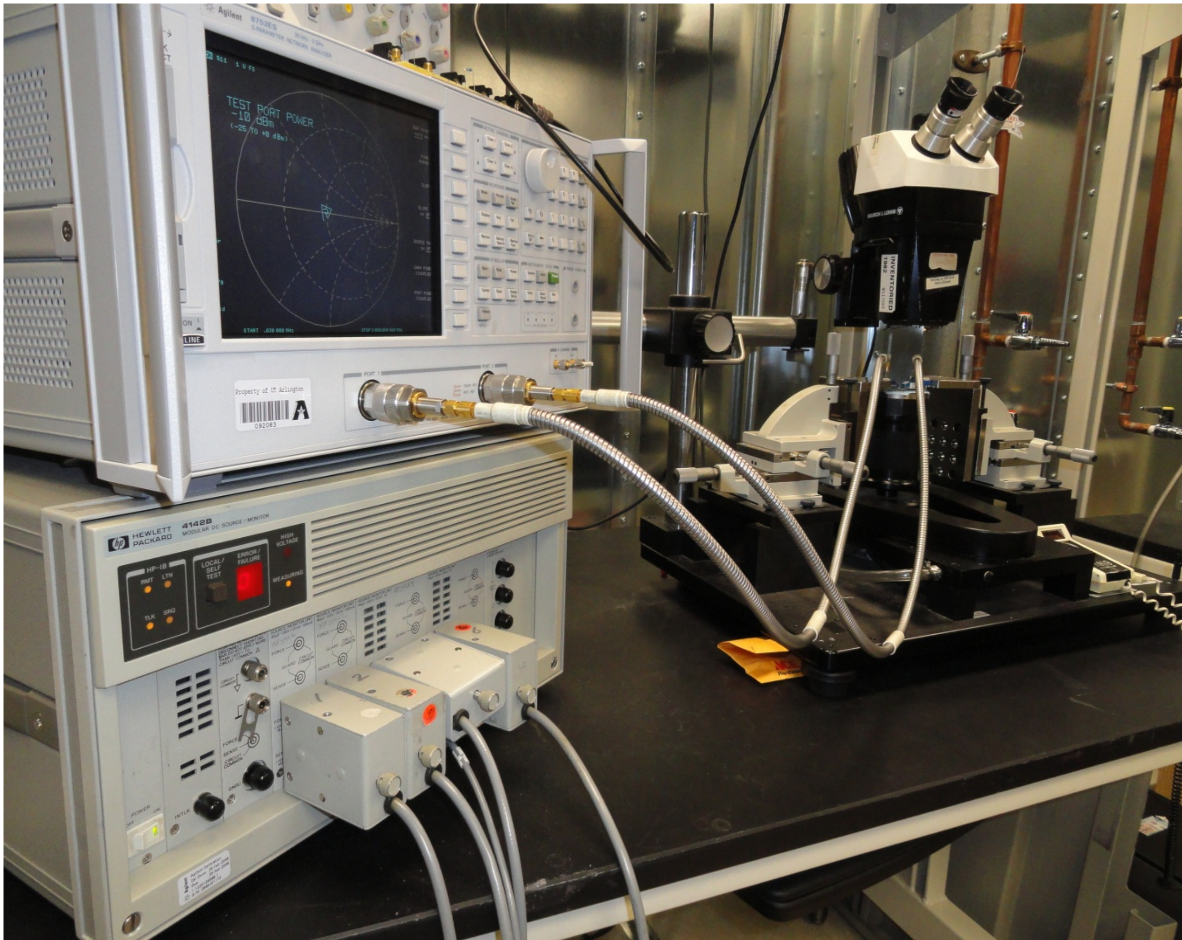

Figure 4.4 Connections between HP 4142B, Agilent 8753ES and probe station.

The VBIC model file is used to do simulation of the Forward active common base setup in ICCAP. The simulator spmodeads is invoked from ICCAP for running the simulations. During the simulations the ambient temperature variable TEMP in ICCAP is set to the corresponding measured ambient temperature. From the simulations and measurements it is observed that there is significant difference in the measured and simulated current curves. In the first round of optimization and extraction the simulated current curves are optimized to match the measured current curves to give the accurate value of I_S. After extracting the value of I_S, the TEMP variable is used as the optimization parameter to optimize the simulated currents to the

measured currents. In this optimization the value of TEMP is optimized and extracted for each value of base-emitter voltage. The rise in junction temperature for base-emitter voltage point or power dissipation point is obtained as difference between the optimized TEMP value and initial ambient temperature. After obtaining the temperature rise at each power dissipation point, the rise in temperature, dT (K) versus power dissipated, P (W) is plotted for each value of V_{CB}. A polynomial curve fitting is used to get the value of temperature as a function of power dissipated. The slope of this curve gives the thermal resistance at that particular value of dissipated power.

4.2 Forward active common base measurement example on a 5um low voltage NPN SiGe HBT

The procedure explained in section 4.1 is used to capture the DC measurements of a 5um low voltage NPN SiGe HBT.The ICCAP setup used to take Forward active common base plots is shown in figure 4.5.This setup is repeated for different values of V_{CB} ranging from 0 to 0.5V. The Forward active common base plot of I_C vs V_{BE} and I_B vs V_{BE} is as shown in the figure 4.6.

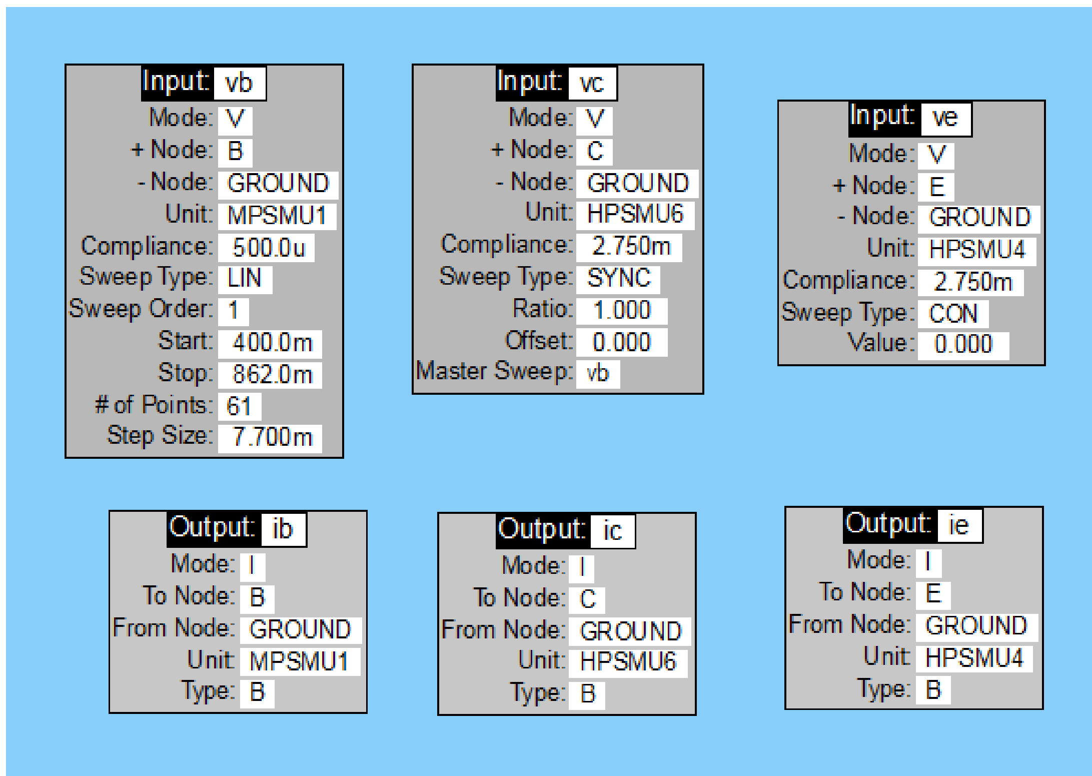

Figure 4.5 ICCAP setup used to take Forward active common base measurements(V_{CB} = 0V).

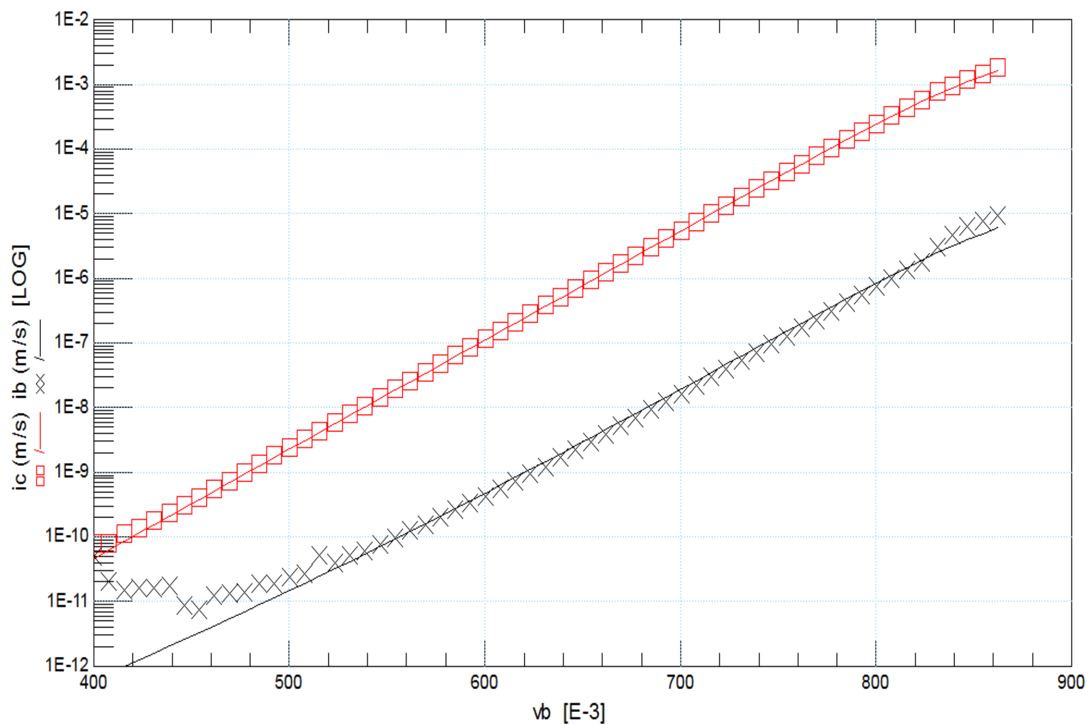

Figure 4.6 Forward active common base plot of I_C vs V_{BE} and I_B vs V_{BE} at V_{CB} =0 and V_E =0.

An example snapshot of input range and parameters used for optimization are shown in figures 4.7 and 4.8 respectively.This process is repeated for different values of V_{BE} keeping the V_{CB} constant in each setup.

Function Optimize Browse...

Algorithm: Levenberg-Marquardt Error: Absolute

Inputs Parameters Options

Target	ic.m	ib.m	
Simulated	ic.s	ib.s	
Weight	10.00	10.00	1.000
Target Min	0.000	0.000	0.000
Target Max	0.000	0.000	0.000
X Min	844.5m	844.5m	0.000
X Max	846.5m	846.5m	0.000
Curve Min			
Curve Max			
X Data Ref			
Reference SetUp			

Figure 4.7 An example snapshot of the input range used for optimization of TEMP variable.

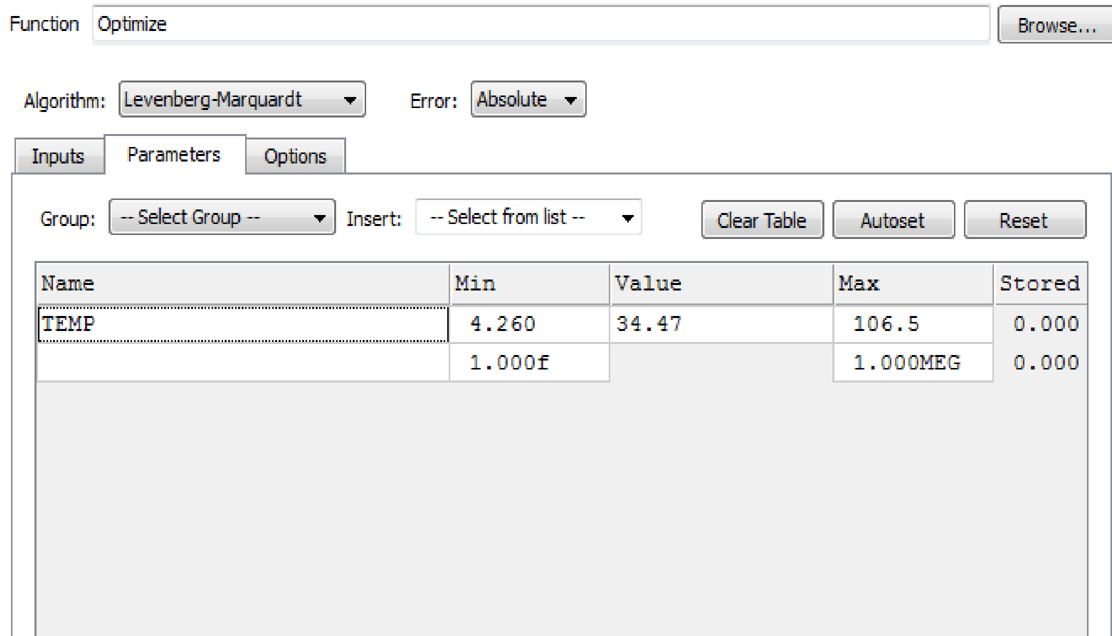

Figure 4.8 An example snapshot of parameter used for optimization.

The dT versus P curves for different values of V_{CB} ranging from 0V to 0.5V are plotted. A trendline is used to make a polynomial curve fitting on these curves to get the expression of rise in temperature as a function of dissipated power.The dissipated power in each case is calculated as:

$$P = I_C V_{CE} + I_B V_{BE} \tag{4.1}$$

The variation of Rth with temperature is also studied and plot of Rth versus temperature is plotted for each value of V_{CB}.Below are the plots of dT versus P and R_{TH} versus temperature curves obtained for various values of V_{CB}.

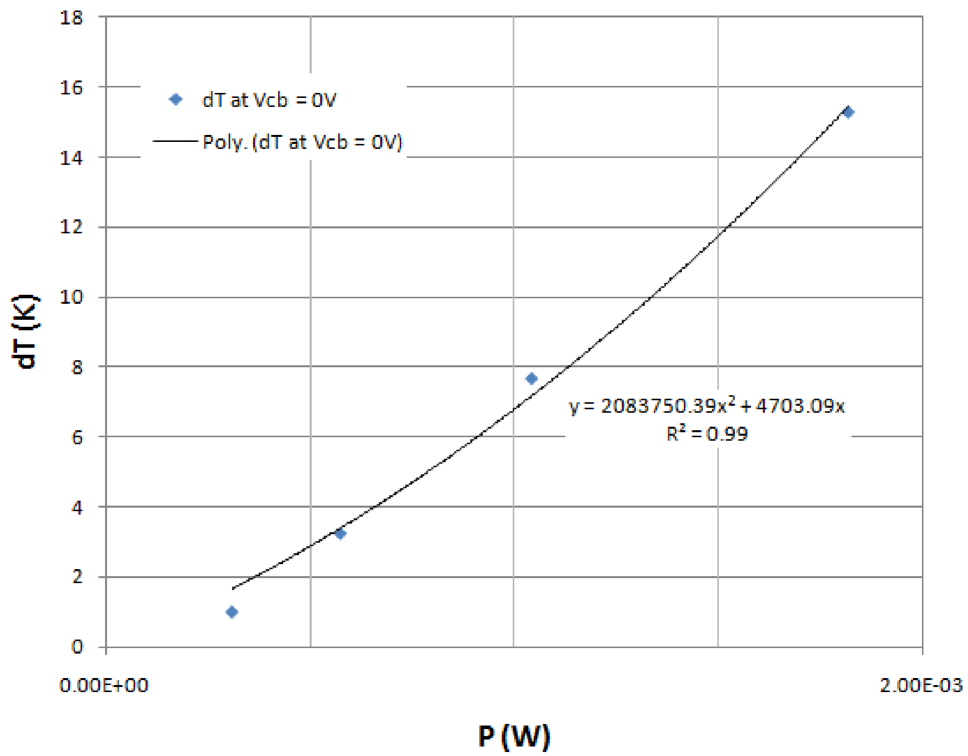

Figure 4.9 Polynomial curve fitting for dT versus P for V_{CB} = 0V.

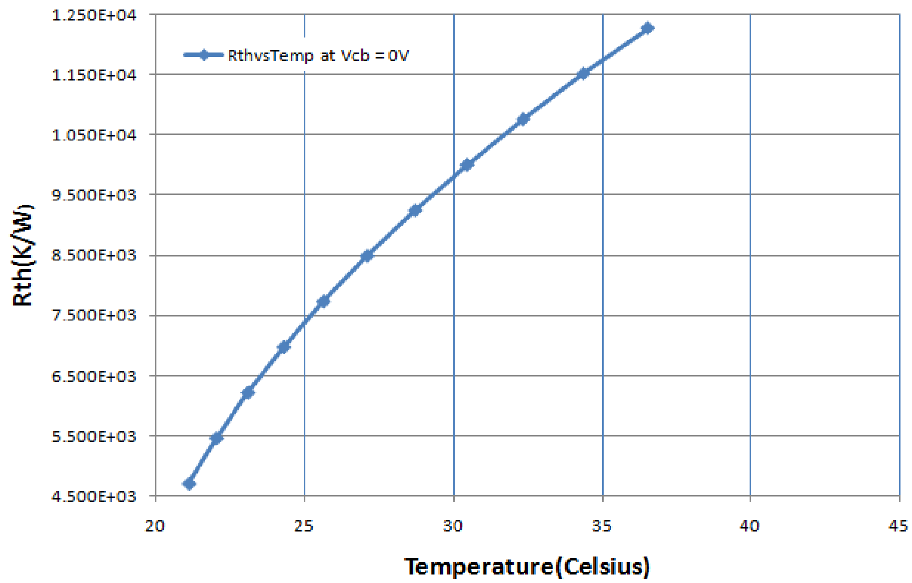

Figure 4.10 Plot of Rth versus temperature for V_{CB} = 0V.

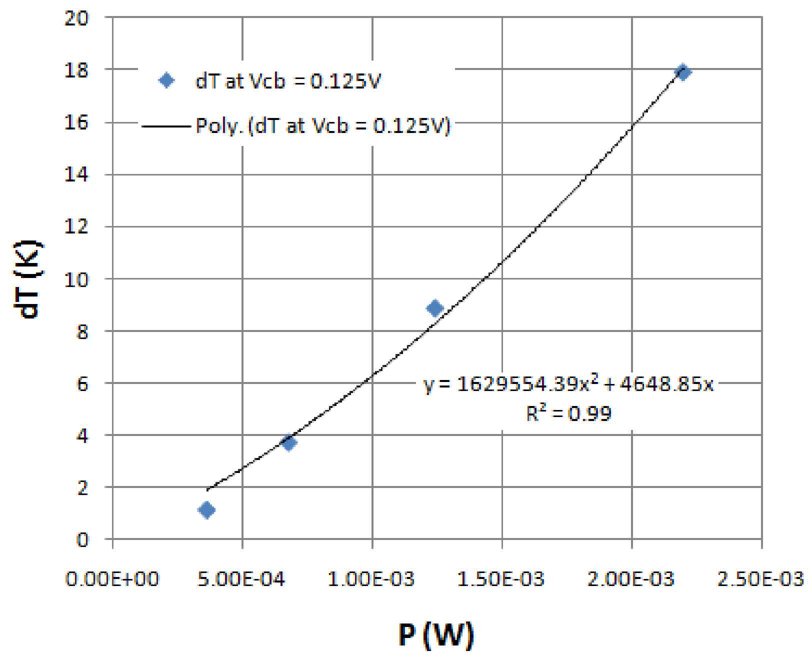

Figure 4.11 Polynomial curve fitting for dT versus P for V_{CB} = 0.125V.

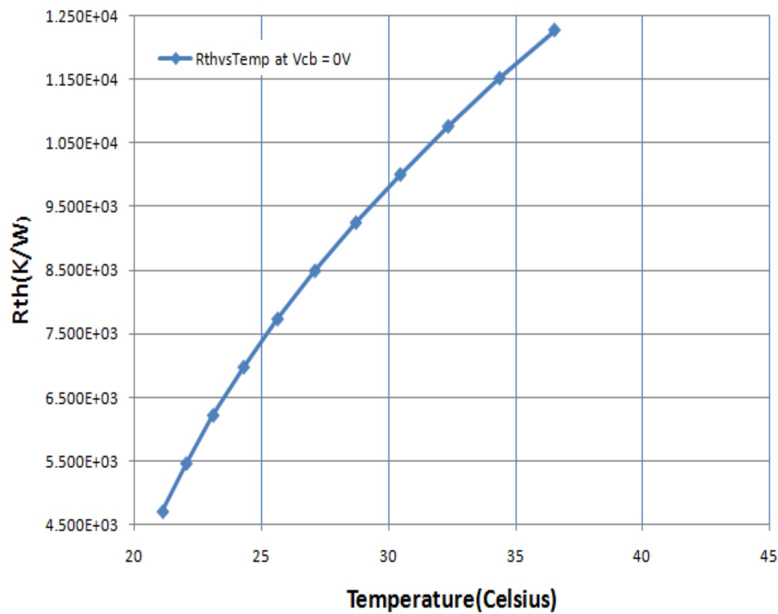

Figure 4.12 Plot of Rth versus temperature for V_{CB} = 0.125V.

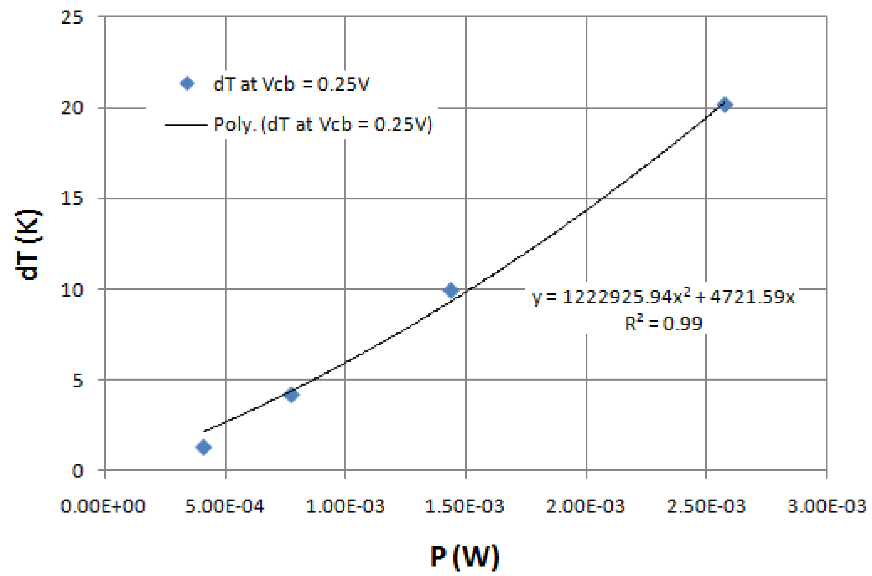

Figure 4.13 Polynomial curve fitting for dT versus P for V_{CB} = 0.25V.

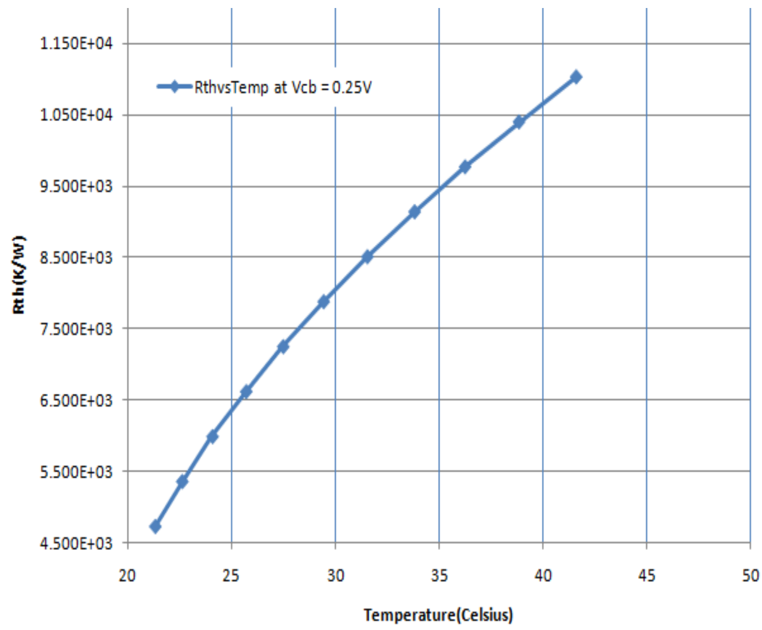

Figure 4.14 Plot of Rth versus temperature for V_{CB} = 0.25V.

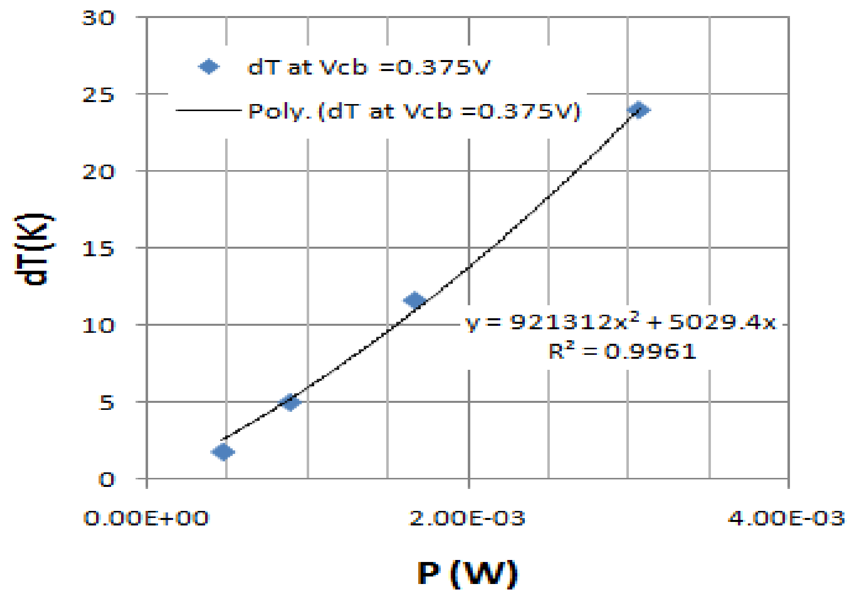

Figure 4.15 Polynomial curve fitting for dT versus P for V_{CB} = 0.375V.

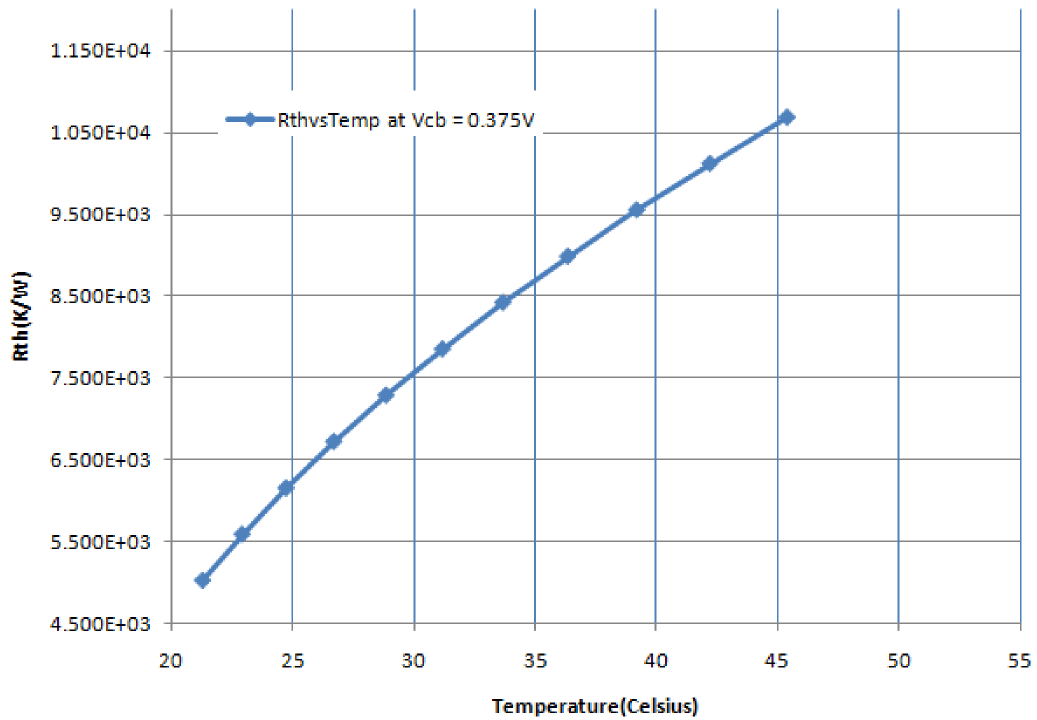

Figure 4.16 Plot of Rth versus temperature for V_{CB} = 0.375V.

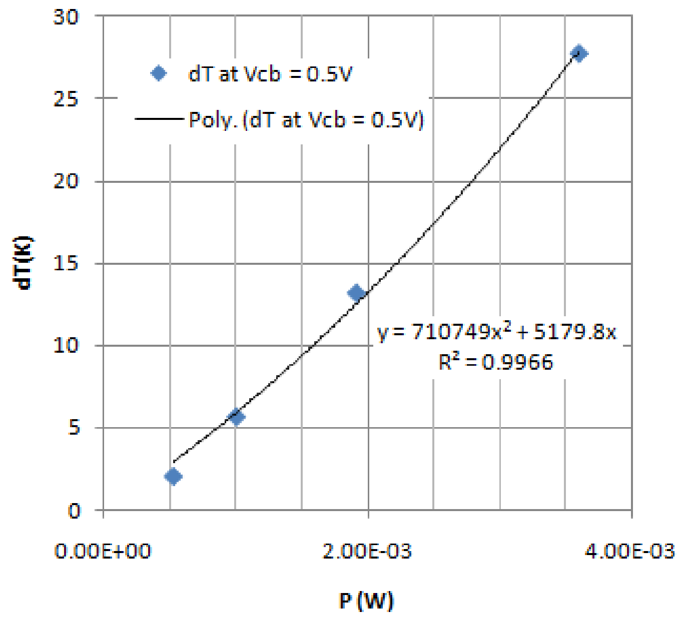

Figure 4.17 Polynomial curve fitting for dT versus P for V_{CB} = 0.5V.

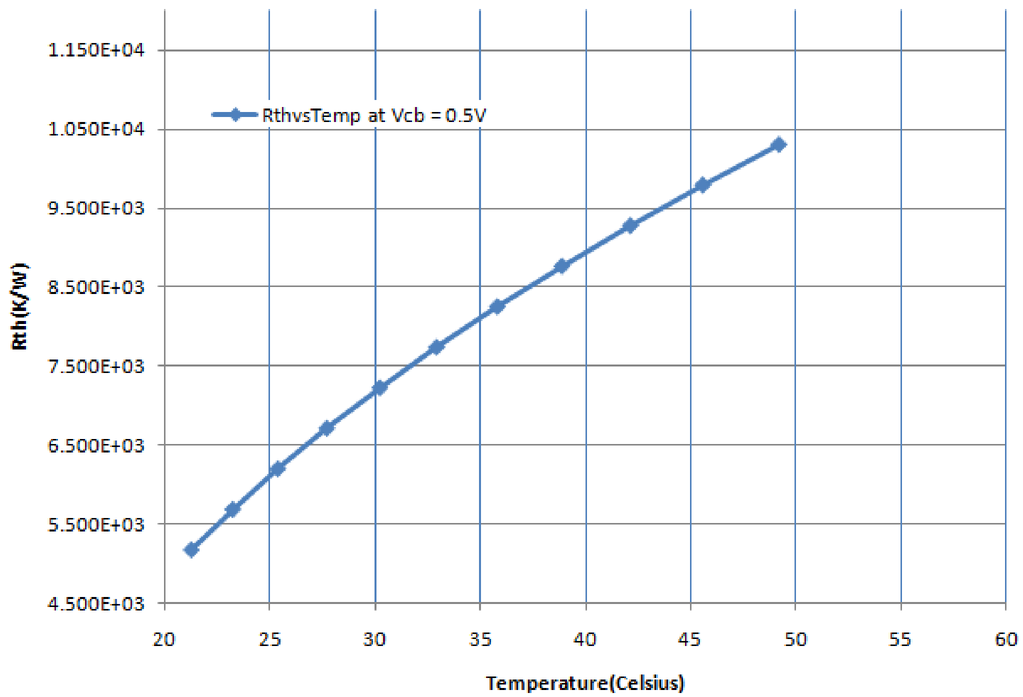

Figure 4.18 Plot of Rth versus temperature for V_{CB} = 0.5V.

4.3 Results and Discussion

From the trend line characteristics it can be observed that the total thermal resistance R_{TH} is 7510.635Ω at a dissipated power of 0.878mW. This value agrees with the theoretical total value of R_{TH} discussed in Chapter 2 with permissible amount of error. The Forward active common base setup is used to determine the total thermal resistance R_{TH} of the 5um HBT device. Here the powers dissipated at the junctions are varied by varying the collector-base voltage and base-emitter voltage. This in turn results in rise in the junction temperature from the ambient temperature. The dT versus P plots for each value of V_{CB} gives a mathematical model which shows rise in temperature as function of dissipated power. The slopes of these curves give the total thermal resistance calculated for a given dissipated power. The plots of R_{TH} versus Temperature for each value of V_{CB} show the variation of R_{TH} with temperature. The non linear dependence of R_{TH} on temperature is due to the change of thermal conductivities of Si and Si-oxide with change in temperature.

CHAPTER 5

FREQUENCY DOMAIN MEASUREMENTS OF CBC8 DEVICES

5.1 Circuit Setup

The frequency domain measurements on CBC8 device are performed to extract the value of thermal impedance parameters of the device. A common emitter setup is used for frequency domain measurements. The measurement setup used is as shown in figure 5.1

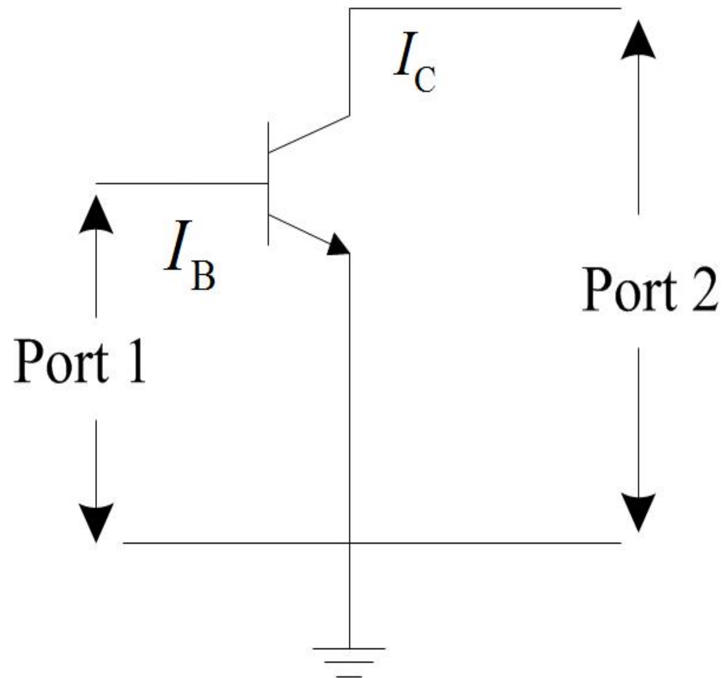

Figure 5.1 Measurement setup for frequency domain measurement.

The 8753ES network analyzer is used to get the frequency sweep from 30KHz to 3GHz.The port 1 is connected between the base and emitter and port 2 is connected between

the collector and base. 4142B DC source is used to give the required bias voltages to the device. The connections between the 4142B, 8753ES and probe station is as shown in figure 4.4. S parameter measurements are performed on a 5um low voltage NPN SiGe HBT. Transformations of S parameter to Y (Admittance) parameters using ICCAP transform. The Y11 plot is used to extract the value of total thermal resistance of the device. The foster network values derived in chapter 2 are used as initial values of the parameters for optimizations. The optimizations are performed only on the low frequency range from 30KHz to 600KHz. Therefore the total thermal resistance can be extracted from this range of data.

5.2 Frequency domain measurement plot

The plot of Y11 versus frequency obtained from measurements on a 5um low voltage NPN device is as shown in the figure 5.2.

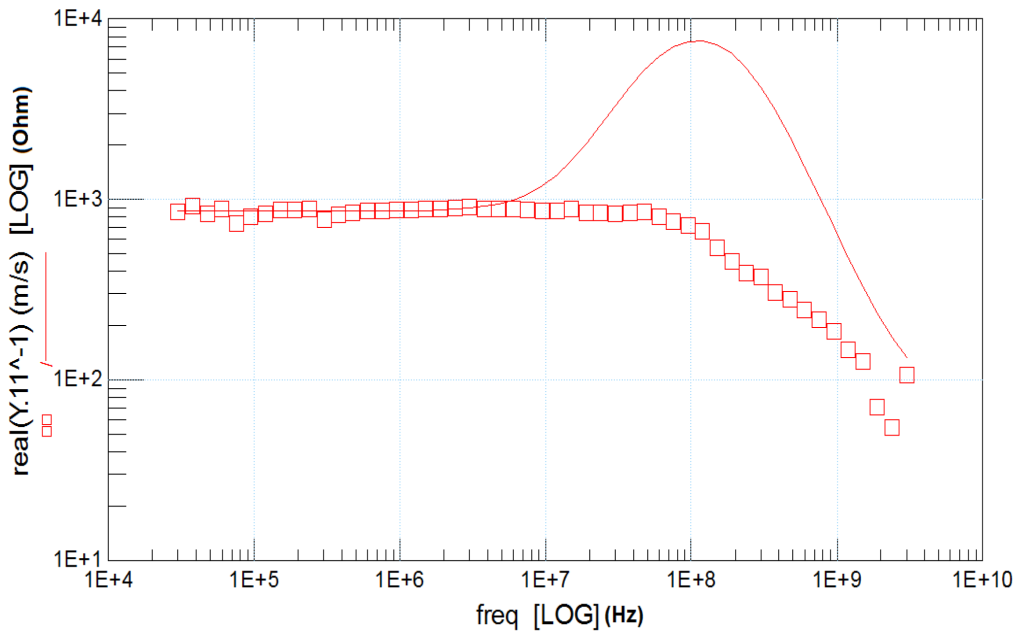

Figure 5.2 Optimized Plot of Real (Y.11^-1) versus frequency for V_{CE} = 3 V and V_{BE} = 820mV.

5.3 Results and Discussion

Table 5.1 The Foster network values before and after optimizations

	Rf1	Cf1	Rf2	Cf2	Rf3	Cf3
Initial Value	**503.3**	**29.37p**	**2.029K**	**76.8p**	**4.802K**	**68.88p**
Optimized Value	**1.151K**	**2.797p**	**3.914K**	**1.363p**	**3.480K**	**1.164p**

The frequency domain measurements were taken on the 5um low voltage NPN device and values of foster network components optimized are as shown in figure 5.3. Optimizations are performed in the low frequency range to extract the total thermal resistance (sum of the values of foster resistors). A table showing the initial and final values of foster network is shown in figure 5.3.It is observed from the final values of the foster network that optimized results is in close agreement with the theoretically estimated values.

CHAPTER 6

CONCLUSION AND RECOMMENDATIONS FOR FUTURE WORK

The important self heating parameters of the VBIC model of SiGe HBT are discussed. Various methods are used to estimate the thermal resistance and thermal capacitance of the HBT.

Theoretical calculations based on the thermal properties of the material and device dimensions were used to estimate the thermal resistance and thermal capacitance of each layer of the SiGe HBT. A 5um low voltage NPN SiGe HBT is chosen as sample device throughout this thesis.

The Masana's method is used for estimating the thermal impedance parameters of the Si-tub and oxide layers of the HBT. Joy and Schlig's method is used for estimation of thermal impedance parameters of Si-wafer layer. An appropriate Cauer thermal network is derived from these calculations.

After deriving the Cauer network, using Cauer to Foster network transformation method a Foster network is formed which is used as optimization network for time domain measurements. Time domain measurements are performed on the CBC8 5um low voltage NPN device sample and the thermal tails are used for optimizations with the Foster network as the optimization parameters. Frequency domain measurements are performed on the 5um low voltage NPN device to extract the value total thermal resistance which can optimize the low frequency range of Y parameter.

DC measurements are also performed to obtain the true value of I_S total value of R_{TH} .The Forward active common base circuit setup is used in this case. In this method the power dissipated at the junction is varied by varying the collector base voltage and base-emitter voltage. This in turn causes the rise in junction temperatures. From this setup the R_{TH} versus temperature plots are obtained for various collector-base voltages. The non-linear relationship between them suggests the non-linear dependence of thermal conductivity on temperature.

As the devices are thickly packed nowadays it is not only the self heating but also adjacent heating from neighboring devices also contribute to the rise in junction temperatures. This research work can be extended to study the effect of adjacent heating in SiGe HBTs. The DC measurements have shown that the thermal conductivities of Si and oxide are functions of the temperature. It would be worthwhile to study the effect of temperature on the thermal conductivities of each layer on the SiGe HBT and the subsequent dependence of R_{TH} on temperature.

APPENDIX A

CAUER TO FOSTER NETWORK TRANSFORMATION

The R_{TH} and C_{TH} values of the Si-tub and Oxide layers were obtained using the Masana Calculations [16].The Joy and Schlig method is used for estimation of R_{TH} and C_{TH} of wafer. The R_{TH} and C_{TH} values are distributed in the Cauer network as shown in Figure A.1

Here,

$$Cc1 = \frac{C_{tub}}{2} \tag{A.1}$$

$$Cc2 = \frac{C_{tub}}{2} + \frac{C_w}{2} \tag{A.2}$$

$$Cc3 = \frac{C_{ox}}{2} + \frac{C_w}{2} \tag{A.3}$$

$$Rc1 = R_{tub} \tag{A.4}$$

$$Rc2 = R_{ox} \tag{A.5}$$

$$Rc3 = R_w \tag{A.6}$$

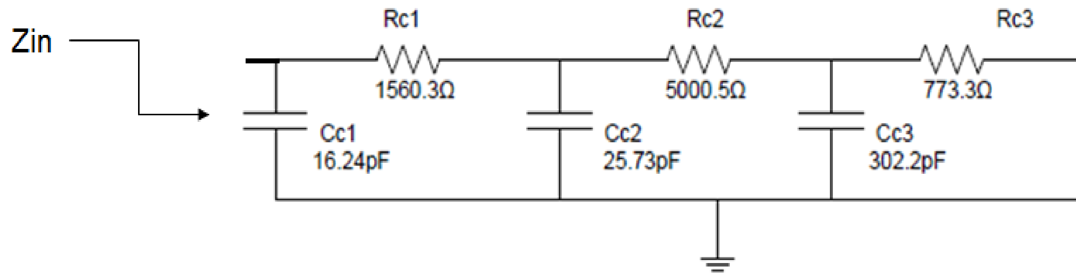

Figure A.1 Cauer network (Values of resistors and capacitors for a 5um device).

To convert the Cauer network to Foster network [23], first the input impedance at node 1 is calculated for the Cauer network given by,

$$Z_{in} = \frac{N_2 s^2 + N_1 s + N_0}{D_3 s^3 + D_2 s^2 + D_1 s + D_0} \tag{A.7}$$

Numerator coefficients are,

$$N_2 = Cc_2Cc_3Rc_1Rc_2Rc_3 \tag{A.8}$$

$$N_1 = Cc_2Rc_1Rc_2 + Cc_2Rc_1Rc_3 + Cc_3Rc_3Rc_1 + Cc_3Rc_3Rc_2 \tag{A.9}$$

$$N_0 = Rc_2 + Rc_1 + Rc_3 \tag{A.10}$$

Denominator coefficients are

$$D_3 = Cc_1Cc_2Cc_3Rc_1Rc_2Rc_3 \tag{A.11}$$

$$D_2 = Cc_1Cc_2Rc_1Rc_2 + Cc_1Cc_2Rc_1Rc_3 + Cc_1Cc_3Rc_1Rc_3 + Cc_1Cc_3Rc_2Rc_3 + Cc_2Cc_3Rc_2Rc_3 \tag{A.12}$$

$$D_1 = Cc_1Rc_1 + Cc_1Rc_2 + Cc_1Rc_3 + Cc_2Rc_2 + Cc_2Rc_3 + Cc_3Rc_3 \tag{A.13}$$

$$D_0 = 1$$

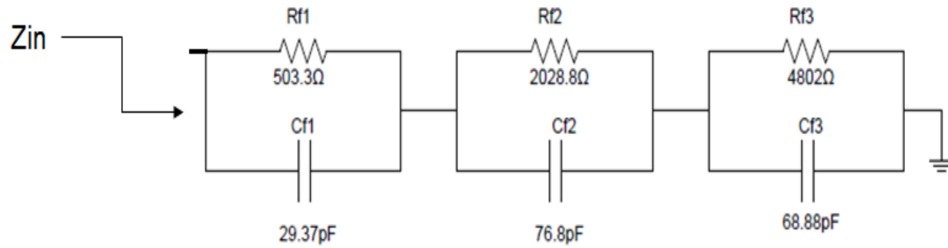

Figure A.2 Foster Network (Values of resistors and capacitors for a 5um device).

Equation (A.7) is converted to a partial fraction form as given below [23],

$$Z_{in} = \frac{A_1}{s-s_1} + \frac{A_2}{s-s_2} + \frac{A_3}{s-s_3} \tag{A.14}$$

$$Cf_1 = \frac{1}{A_1} \tag{A.15}$$

$$Cf_2 = \frac{1}{A_2} \tag{A.16}$$

$$Cf_3 = \frac{1}{A_3} \tag{A.17}$$

$$Rf_1 = \frac{1}{s_1A_1} \tag{A.18}$$

$$Rf_2 = \frac{1}{s_2 A_2} \tag{A.19}$$

$$Rf_3 = \frac{1}{s_3 A_3} \tag{A.20}$$

The values of Foster network were obtained using Matlab code. A impulse input was fed to the Cauer and Foster networks and the outputs observed proved the equivalence of the two networks. The simulations were done using pspice and the outputs are as shown below:

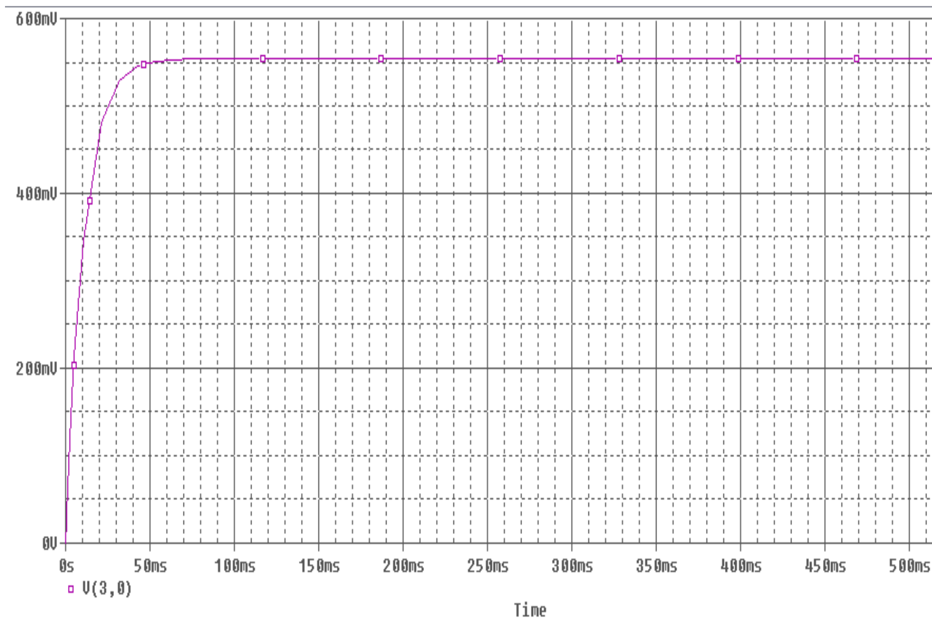

Figure A.3: Foster Response.

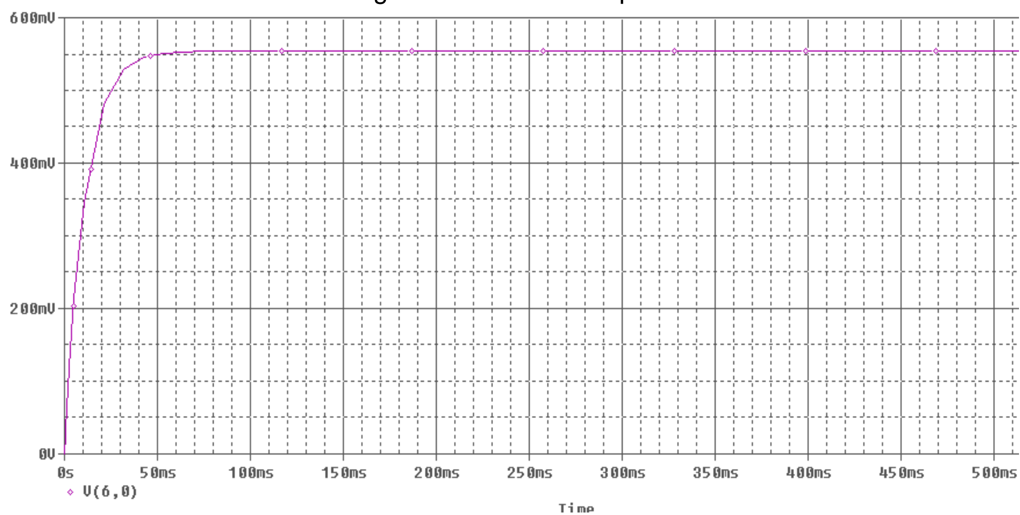

Figure A.4: Cauer Response.

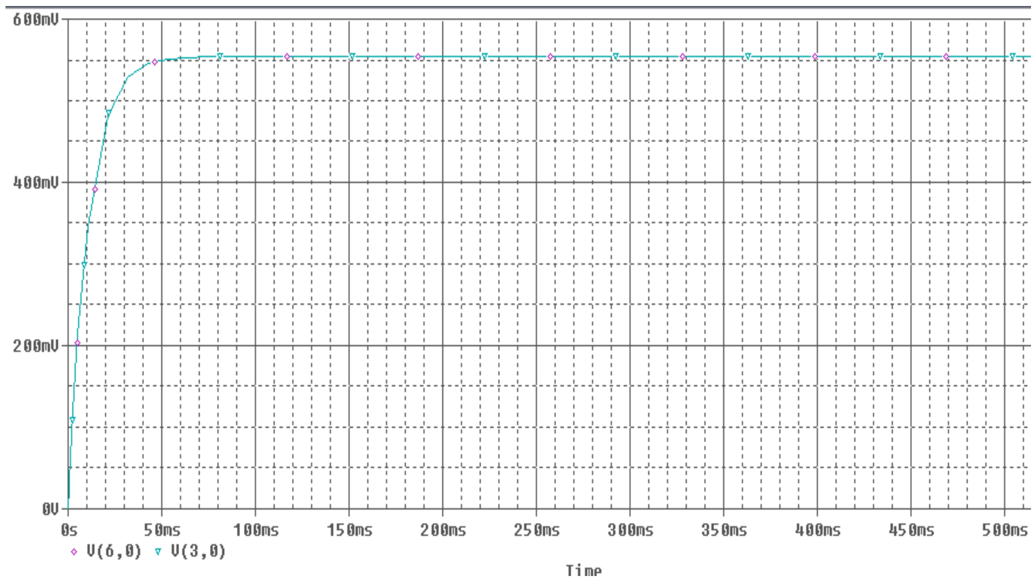

Figure A.5 Comparison-Cauer and Foster responses.

APPENDIX B

SPREADSHEET CALCULATOR USED FOR THEORETICAL ESTIMATIONS OF R_{TH} AND C_{TH}

The snapshot of the spreadsheet calculator used to derive the R_{TH} and C_{TH} of different layers of the SiGe HBT is as shown in the figure B.1.

Input Parameters	Value	Units
Length of Emitter(Le)	5.00E-06	m
Width of Emitter(We)	2.50E-07	m
Inner length of Si-tub(Lt)	6.60E-06	m
Inner Width of Si-tub(Wt)	3.03E-06	m
Thickness of wafer(tw)	7.00E-04	m
Thickness of tub(ttub)	1.65E-06	m
Thickness of Oxide(tox)	1.40E-07	m

Enter the dimensions in micrometers	
Length of Emitter(Le)	5
Width of Emitter(We)	0.25
Inner length of Si-tub(Lt)	6.6
Inner Width of Si-tub(Wt)	3.03
Thickness of wafer(tw)	700
Thickness of tub(ttub)	1.65
Thickness of Oxide(tox)	0.14

Note: Units
R -> K/W
C -> J/K

Directions:
1. Enter dimensions for the device in the yellow fields. (L>W)
2. Cauer and Foster network values are calculated automatically.
3. F2 through F8 are unprotected. The remaining cells are protected.

Masana and Joy & Schilg Estimations							
Input		Cauer Network		Foster Network		TAU_FOSTER (n-sec)	
Rtub	1560.3	R1	1560.3	Rf1	503.3	Tf1	14.78
Rox	5000.5	R2	5000.5	Rf2	2028.8	Tf2	155.82
Rw	773.3	R3	773.3	Rf3	4802.0	Tf3	330.74
Ctub	3.247E-11	C1	1.624E-11	Cf1	2.937E-11		
Cox	1.898E-11	C2	2.573E-11	Cf2	7.680E-11		
Cw	5.855E-10	C3	3.022E-10	Cf3	6.888E-11		

Figure B.1 Snapshot of the spreadsheet used for Theoretical Estimations.

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