POLYMER-BASED RF MEMS DEVICES

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ABSTRACT

The radio frequency micro-electro-mechanical system (RF MEMS) technology is rapidly transitioning from the research stage to commercial applications. Reducing material and fabrication costs, realizing IC compatibility, and improving the RF performance have been main focal points of many recent works. In this dissertation, we target at developing a RF MEMS methodology which realizes CMOS compatibility, cost effectiveness and high performance at the same time.

The current RF MEMS devices are mostly constructed on quartz and III-V compound materials to achieve low RF losses. These approaches proved to have excellent RF performance. However these materials are expensive and unable to be integrated into CMOS circuitry. In this work, we developed a CMOS-compatible approach to construct RF MEMS components where low-resistivity silicon and plastic were used as the substrate material and dielectric layer, respectively. This method is cost-effective and presents very high RF performance.

Coplanar waveguide (CPW) transmission lines were first realized using this approach. Devices were characterized from DC to 26 GHz, a low insertion loss of 3 dB/cm was achieved. Soft substrate of Kapton film was also used to build CPW lines to answer the increasing trend of flexible devices such as RFIDs, cell phone antennas and soft displays. A very low transmission loss of 1 dB/cm was obtained. Additionally, multiple devices with various dimensional emphases were fabricated to suit different dimensional situations.

A novel method of building CMOS-compatible distributed MEMS transmission line (DMTL) phase shifters was developed. A thick layer of Kapton film was bonded on a low-resistivity silicon substrate to prevent RF signal leakage. Design considerations, fabrication processes and measurement results were discussed in detail. For comparison purposes, DMTL phase shifters were constructed on glass substrates as well. In order to verify the design roles and fit for different space situations, various phase shifters were fabricated using this method. Our devices showed comparable results to those built on quartz and III-V compound substrates.

Tunable filters are essential elements for modern communication systems. Using the same polymer-silicon method, we built two types of tunable filters – partial-loaded short-ended filter and even-loaded open-ended filter. Design methodology, fabrication and measurements were discussed. Our tunable filter demonstrated a 2-GHz tunability and a 10-dB transmission loss. Failure mechanisms and possible improving methods were examined for possible improvements.

The fabrication process of the polymer-silicon approach developed for RF MEMS devices is simple, cost-effective and CMOS compatible. It virtually applies to any situation where quartz, III-V compound materials or other CMOS-incompatible materials have to be used for RF performance purposes. Thus, at the end of this dissertation, impedance tuners, digital controlled RF MEMS devices and a RF MEMS packaging technique using this polymer-silicon method were proposed for future works.

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CHAPTER 1

INTRODUCTION

1.1 Challenges and Motivation

The term "microwave" refers to frequency range from 300 MHz to 300 GHz. The microwave technology had been predominantly used in radar for military purposes since WWII. Since then, different frequency bands within the microwave spectrum have been intensively utilized for various applications extending from the radar technology. For example, the X band, 8-12 GHz, has been utilized for missile guidance; the Q band, 40-60 GHz, is the operational spectrum for the military communication [1.1]. In recent years, frequencies above 100 GHz and even terahertz are being investigated for concealed weapon detection [1.2][1.3].

Stemming from the military origin, both civilian and commercial applications have been growing in the last few decades in areas such as satellite communication, weather detection and air traffic control systems [1.1]. The immense success of personal communication systems, for example, cell phone and wireless handheld devices, further extends the microwave technology into every corner of people's daily life.

Microwave components have been predominantly based on active semiconductor technology, such as FET and pin diode, and waveguide devices. Time has proven these devices have good performance and reliability. However, their bulky

dimensions, large power consumptions, poor linearity and expensive building materials result in RF system complexity and high overall costs.

During the last decade, RF MEMS (radio frequency micro-electro-mechanical system) devices have achieved significant advancements and made great progress towards commercial successes. Basic RF MEMS blocks of capacitive switches [1.4]-[1.10], inductors [1.11]-[1.16], varactors [1.17]-[1.20], and micro-machined transmission lines [1.21]-[1.23] demonstrated impressive performances. Currently, many research and industry groups are focusing on further improving the reliability [1.24]-[1.28], power-handling ability [1.29], RF MEMS packaging [1.30][1.31] technique, and extending RF MEMS to wider applications. The MEMS approach has many attractive benefits such as less power consumption, lower signal attenuation, higher isolation level and smaller estate requirement, compared to most of its semiconductor counterparts [1.32][1.33]. Table 1.1 details the performance comparison between different technologies [1.32][1.33]

Table 1.1 Comparison between RF MEMS, PIN and FET technologies.

Parameter	RF MEMS	PIN	FET
Voltage (V)	20-80	± 3-5	3-5
Current (mA)	0	3-20	0
Power Consumption (mW)	0.05-0.1	5-100	0.05-0.1
Switching Time	1-300 µs	1-100 ns	1-100 ns
Isolation (1-40 GHz)	Very High	High-Medium	Medium-Low
Loss (1-100 GHz) (dB)	0.05-0.2	0.3-1.2	0.4-2.5
Size (mm^2)	<0.05	0.1	1-5

The successes of these fundamental components offer great opportunities to design and fabricate more complicated and extended RF devices using the MEMS

method. Built upon these elementary blocks, RF MEMS phase shifters [1.34]-[1.36], impedance tuners [1.37]-[1.39], and tunable filters [1.40][1.41] exhibited outstanding results. The great advancement of RF MEMS devices provides a possibility where the active semiconductor devices can be eventually replaced by passive RF MEMS counterparts. Table 1.2 lists some potential applications for RF MEMS to replace active devices in a wireless system [1.32].

Table 1.2 RF MEMS replacement strategies in a wireless system.

MEMS device	Subsystem	Replacement	Reasons
Switch (SPST*[1], SPST*[2]) filter banks	Receiver	Possible	Very low loss. High reliability for low-RF power. Must reduce cost of SPST and SPNT to about 1$.
Switch (SPST, SPST)	Transmitter	Possible	Use shunt design to ground. Do not handle high-RF power. Must reduce cost of SPST and SPNT to about 1$
Inductor	Oscillator	Possible	Eliminate off-chip inductor. Low cost implementation.
Inductor	Power Amplifier	Possible	Still need high-Q MEMS inductors for the matching network.
Varactor	Tunable filter	Possible	High-Q MEMS varactors results in low loss designs.
Varactor	Tunable matching network	Not soon/ Possible	Must be able to handle high-RF powers for antenna and power amplifier. Possible in receiver applications (low power).
FBAR*[3]	Filters	Possible	Eliminate off-chip filter. Still need thermal stability and low-cost packaging. Still need work on long term high-power handling (2-3w).
MEMS resonators	Oscillator	Possible	May replace crystal if thermal stability is solved. Requires vacuum packaging. Must reduce cost since crystals are 0.25$

*1: Single-pole N-throw. *2: Single-pole double-throw. *3: Film bulk acoustic resonator.

Fabrication of RF MEMS devices does not require especially dedicated equipment nor new materials outside IC processing scope. This fact presents a positive factor for RF MEMS mass production and provides a great convenience to improve existing and develop new RF MEMS devices.

Many RF MEMS devices have been successfully demonstrated on quartz, high-resistivity silicon (HRS), III-V compound and RF-grade glass substrates for their superb RF properties. The majority of existing integrated circuits use low-resistivity silicon (LRS). This is not suitable for microwave purposes due to its high attenuation to RF signals. Integrating RF MEMS devices into current integrated circuits remains a big challenge. Besides the IC incompatibility, the high material costs of the RF MEMS substrates further forbid its popularity.

1.2 Solutions: Organic Polymers

Many alternative methods have been examined to improve the poor RF performance of low-resistivity silicon substrate. Adopting a layer of silicon dioxide [1.42], silicon nitride or oxidized porous silicon as an isolation layer improves the RF performance significantly. However it suffers from the problem of thermal expansion mismatch between the silicon substrate and these dielectric materials [1.43]. The formation procedures of these dielectric layers could damage existing circuitry as well due to the high processing temperature. Using the unoxidized porous silicon as a dielectric layer avoids the problem of thermal expansion mismatch [1.43], yet it limits its own applications and is not suited to flexible processes due to the usage of hydrofluoric acid during the process of forming the unoxidized porous silicon. Furthermore, the thicknesses of these dielectric materials are limited to several micron meters, due to the formation methods, which may not be enough for many applications.

Polymers possess many appealing properties to MEMS devices. The benefits of low material and fabrication costs have been shown in many micro-fluidic devices

[1.44], micro-optical devices [1.45][1.46] and MEMS packaging [1.30][1.31]. The high resistivities, low dielectric constants and low dissipation factors of polymers provide potentials for high-performance RF applications. The ultra high resistivity (10^{19} Ω-cm or above) and low dielectric constant (2.65) of the benzocyclobutene (BCB) polymer [1.47] offer a very attractive option to the RF applications. Studies have shown a very low insertion loss [1.48] and high quality factor [1.49] up to the millimeterwave frequencies with BCB as a dielectric layer. BCB does not have the ion-drifting problem with copper as a conductive layer without nitride as an isolation layer [1.50]. The low processing temperature (250°C) is compatible with CMOS and post-CMOS processes. It is simple and cost-effective to deposit or vary BCB thickness through the spinning-curing process. Its resistance to some chemical agents, such as many acids, makes BCB compatible with most existing IC fabrication procedures. Its micromachining versatilities are especially attractive to MEMS fabrication processes. Be it as a structural layer or sacrificial [1.51] layer, the microstructures can be manufactured either using photolithography, plasma etching [1.52], RIE etching, or hot embossing techniques. Its non-outgassing property further eases the processing effort to achieve a good uniformity.

The polyimide resin has a resistivity of 10^{17} Ω-cm, dielectric constant of 3.4~3.5 and curing temperature of 350°C [1.53]. Though its RF properties are slightly inferior to those of BCB, polyimide does have its own outstanding merits. It does not need the surface promoter thanks to its excellent adhesive ability. Thus the deposition procedure is simplified. It also has the same micromachining versatilities as BCB. It resists most

known solvents currently used in semiconductor processing [1.53], hence processing polyimide can be of great convenience.

Kapton film is a factory-made polyimide sheet, and its electrical properties are identical to polyimide. Kapton films of various thicknesses are available for different purposes. Whenever a thickness is too high to be achieved by the spinning-curing process, multi-layer Kapton films can be easily bonded on a substrate surface using adhesive resins.

Kapton is firm enough to be self supportive without the need of a backing material, thus any losses associated with the substrate would be eliminated. Kapton film has adequate flexibility to be conformal to certain curvatures. This property is especially useful for non-planar applications, such as RFID, soft display and cell phone antenna. Kapton film maintains stable electrical and mechanical properties over a wide temperature range [1.54]. The robust properties of Kapton are very desirable to RF MEMS devices.

Due to their excellent mechanical and electrical properties, we proposed to use BCB, polyimide and Kapton to build 3-D RF MEMS devices. Table 1.3 summarized some of polymer properties [1.47][1.53][1.54].

Table 1.3 Properties of BCB, Polyimide and Kapton.

	BCB	Polyimide	Kapton
Dielectric constant	2.65	2.9~3.3	3.4~3.5
Dissipation factor	0.08%	0.18~0.25%	0.18~0.25%
Volume resistivity (Ω-cm)	1×10^{19}	$>1 \times 10^{17}$	$>1 \times 10^{17}$
Break-down voltage (V/cm)	3×10^{6}	$>1.54 \times 10^{6}$	$>1.54 \times 10^{6}$
Thermal conductivity (W/m°K)	0.29	NA	0.12
Curing temperature (°C)	250	350	N/A
Glass transition temperature (°C)	350	>350	up to 400
Photo patterning ability	Yes	Yes	No
DRIE* etching ability	Yes	Yes	Yes
Plasma etching ability	Yes	Yes	Yes
Out gassing	No	Yes	No

*: Deep reactive ion etching.

1.3 Chapter Description

In chapter 1, achievements and progresses of current RF MEMS devices are briefly introduced. The challenges facing RF MEMS development are also addressed. In searching for tactics to tackle these challenges and obstacles, a solution of using organic polymer layer is proposed.

Chapter 2 describes the development of coplanar waveguide transmission lines using various dielectric and substrate materials. Simulation and measurement results will be presented. Chapter 3 discusses the design approach, fabrication process, simulation and experiment results of RF MEMS phase shifters built on polymer and CMOS-grade silicon. Chapter 4 describes RF MEMS tunable filters using the polymer-silicon approach. Design methodology, manufacture procedure, simulation and characterization will be elaborated in detail. Methods of improving current design of tunable filters are also addressed.

Chapter 5 describes the possibility and plan for more RF MEMS devices using low-resistivity silicon and polymer approach. Also, a novel method of RF MEMS packaging method using hot embossing and polymer wafer bonding technique is proposed.

CHAPTER 2

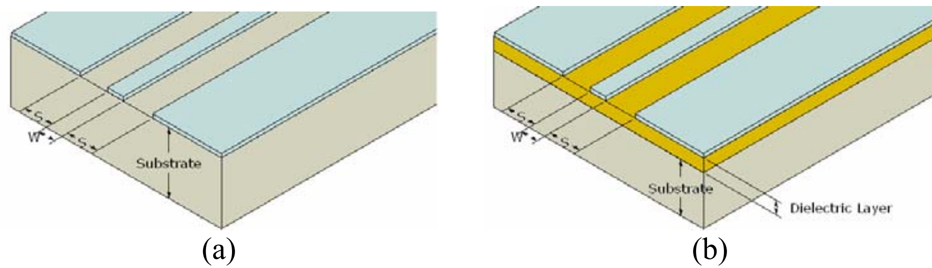
POLYMER-BASED HIGH-FREQUENCY TRANSMISSION LINES

The coplanar waveguide (CPW) transmission lines are foundation elements of many RF MEMS devices such as switches [2.1], phase shifters [2.2], filters [2.3] and impedance tuners [2.4]. The CPW lines have been widely used as interconnects in microwave integrated circuitries as well [2.5]. The low-resistivity silicon, used as the substrate material of the CMOS circuits, suffers from high attenuation as the frequency increases. To avoid this RF loss, conventionally, either CPW lines have to be built on low loss material, e.g. quartz and intrinsic silicon, or the high-conductivity silicon substrates have to be micro-machined to create a suspended structure [2.5]. However the material costs and fabrication expenses of such solutions are high.

2.1 Design Considerations

2.1.1 Using CMOS-Grade Silicon as Substrates

The reason that CMOS-grade silicon induces a high RF attenuation is due to the impurity dopants producing a high conductivity in which a RF signal vanishes. To minimize this effect, we apply organic polymers on the low-resistivity silicon to function as a dielectric medium in which a electromagnetic wave can travel through. When a polymer is thick enough, little or no electromagnetic wave will leak into the loss-inducing substrate. Fig. 2.1(a) shows a CPW line directly built on a substrate; (b) shows a CPW line built with a polymer intermediate layer on the substrate.



(a) (b)

Figure 2.1 (a) A CPW line without a polymer layer (b) a CPW line with a polymer dielectric layer.

2.1.2 Using Glass as Substrates

In the applications where quartz needs to be used, regular glass would be an alternative option for great cost deduction with the help of a polymer dielectric layer. Thus in this work, CPW lines were also constructed on glass substrates.

2.1.3 Flexible Polymer as Substrates

Flexible circuits can conveniently accommodate a nonplanar surface. Cell phone antenna, flexible display, and RFID [2.6][2.7] are among the forerunners of this growing trend. Hence, demands of CPW lines on flexible substrates are rising consequently. In this chapter, CPW lines on Kapton flexible substrates are also to be described.

2.1.4 Other Considerations

Besides the substrate attenuation, two other major sources contribute to RF signal loss as well: the reflection and dissipation loss. Wherever there is a mismatch between the characteristic impedance Z_o of the CPW line and that of the rest of the circuitry Z_r, there will be a reflection Γ, as shown in Fig. 2.2. To reduce the reflection, the characteristic impedances Z_o and Z_r need to be as close as possible. For most current

RF applications, Z_r is 50 Ω. The characteristic impedance, Z_o, of a CPW line is a function of its physical dimensions and its substrate dielectric properties. The design and optimization of CPW lines have been well documented by *Rainee* [2.5], thus the calculation procedure is not the major concern in this work.

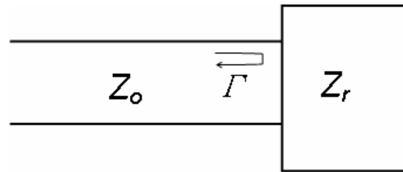


Figure 2.2 Reflection.

The dissipation loss is the signal loss in the form of heat. It primarily consists of three major mechanisms: 1) the skin effect; 2) the metal conduction loss; 3) and the material dielectric loss. The skin depth was calculated from Eq. 2.1, where f is the frequency, μ_0 is the free space permeability and σ is the conductivity loss. Using copper as the metal transmission lines, the skin depth is 0.66 μm at 10 GHz. The metal conduction loss is the result of the series resistance. The skin effect and metal conduction loss can be minimized by properly choosing a metal with a good conductivity and sufficient metal thickness. In this work, copper of 1.5 μm thickness is selected due to its excellent conductivity and affordable cost. The organic polymers have very small dissipation factors, e.g. 0.08% of BCB and 0.26% of polyimide, thus dielectric losses are low in these polymers.

$$\delta_s = \sqrt{\frac{1}{\pi f \mu_o \sigma}} \tag{2.1}$$

2.2 Fabrication Processes

2.2.1 Fabrication Process Using BCB or Polyimide as a Dielectric Layer

The low-resistivity silicon was cleaned with a RCA process and the glass substrate was cleaned with ultrasonic acetone bath to eliminate any contamination. A thin layer of surface promoter was applied to enhance the surface adhesion. The first BCB layer was spun on, followed by a soft-cure procedure at 210˚C in an inert gas chamber for 40 minutes. In order to obtain a thick BCB layer, multiple spinning-curing processes were performed. The device was hard-cured at 250˚C in the inert gas environment for 60 minutes. In our study, various thicknesses (13, 26, and 36 μm) of BCB were fabricated. A copper layer of 1.5-μm thickness was deposited on top of the BCB using a thermal evaporation process. The copper layer then was patterned with photolithography and wet etching processes.

The fabrication process using polyimide as a dielectric layer was similar to that of BCB except no surface promoter was needed and the final hard-cure temperature was 350°C.

2.2.2 Fabrication Process Using Kapton as a Supportive Layer

The manufacture process using Kapton is relatively simple. The Kapton film does not need a supporting substrate. The Kapton film was first cut into square shape of 1 inch to acquire a better strength before copper thermal evaporation. After the copper evaporation, the copper layer was patterned with photolithography and wet etching processes.

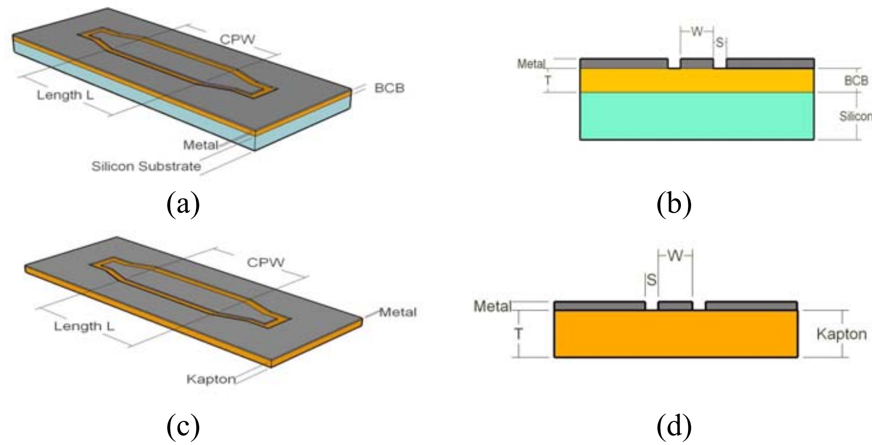


Figure 2.3 Coplanar waveguide transmission lines on polymer layers. (a) The conceptual structure of CPW lines with BCB as a dielectric layer and (b) the sideview. (c) The conceptual structure of CPW lines with Kapton as a substrate and (d) the sideview.

2.3 Measurement Results and Discussion

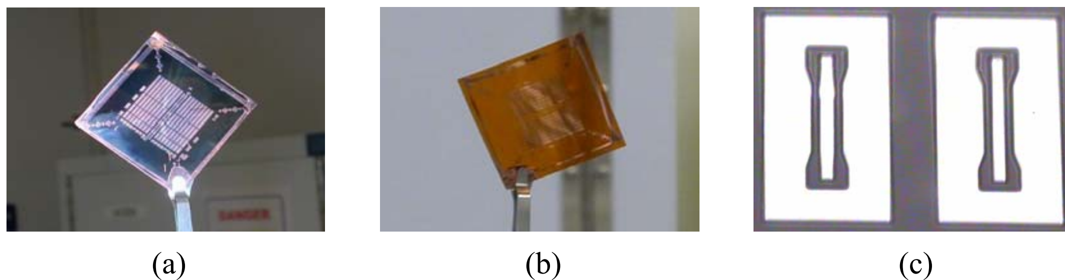
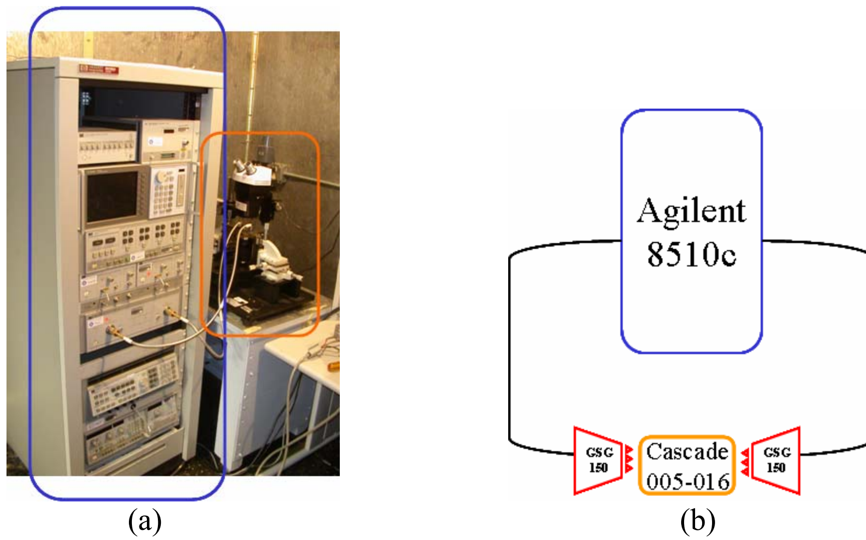


Figure 2.4 The fabricated coplanar waveguide transmission (CPW) lines. (a) The CPW lines with BCB as a dielectric layer and low-resistivity silicon as substrate. (b) The CPW lines built on a Kapton polymer. (c) The CPW lines under the microscope.

Fig 2.4 shows pictures of fabricated devices. The CPW-line devices were characterized with an *Agilent 8510c* network analyzer and *Cascade Microtech Infinity GSG-150* probes from DC to 26 GHz. The scattering parameter measurements were calibrated by the *Cascade Microtech ISS-005-016* calibration kits. In this section, the effects of different elements on performances will be discussed. Fig. 2.5 illustrates the testing setup.



(a) (b)

Figure 2.5 (a) *Agilent 8510c* network analyzer and the probe station. (b) Equipment connection demonstration.

2.3.1 The Performances of Different Substrates

Table 2.1 shows the device dimensions and their calculated characteristic impedances for different substrate materials with BCB (Benzocyclobutene) as a dielectric layer. Fig. 2.6 shows the measurement results of insertion loss and electric field simulations using finite element method (FEM).

Table 2.1 The CPW dimensions and characteristic impedances for different substrate materials.

Substrate	Dielectric layer	W(μm)	S(μm)	L(mm)	T(μm)	Z_o(Ω)
Glass	BCB	400	20	4	36	52
Low-resistivity silicon	BCB	70	20	4	36	54

Fig. 2.6(a) and (b) show that the insertion loss is below 1.5 dB/cm for the CPW lines built on BCB-glass and below 3.3 dB/cm for the one built on BCB-silicon substrates. The BCB-silicon has higher insertion loss because the level of conductive dopants in low-resistivity silicon is much higher than in glass. Thus when the

electromagnetic fields partially penetrate into the each substrate, as shown in the FEM field simulation in Fig. 2.6(c) and (d), the dopants in low-resistivity silicon generate a higher loss.

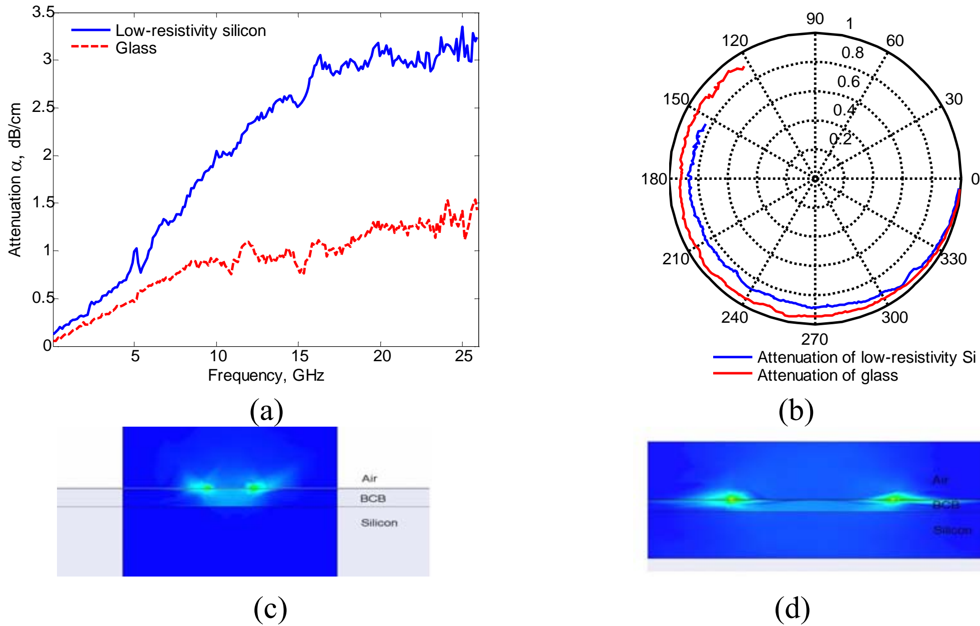


Figure 2.6. The performance comparison between silicon and glass substrates with BCB as a dielectric layer. (a) The magnitude comparison. (b) The Smith chart comparison. (c) The FEM field simulation of BCB-silicon. (d) The FEM field simulation of BCB-glass.

CPW transmission lines of the same dimensions were also directly built on low-resistivity silicon substrates without the polymer film. The insertion losses were greater than 40 dB. This result suggests most of RF signals were lost in the substrate without the help of a polymer dielectric layer.

2.3.2 Improvement by Etching Polymer

To reduce field coupling in the dielectric, one could reduce the dielectric losses. Using the reactive ion etching process (RIE), the polymer between the signal and ground metals were etched away. With the CPW line metal layer serving as a hard mask,

the air slots were achieved by a RIE process of 2:1 oxygen to tetrafluoromethane ratio. Table 2.2 shows the CPW line dimensions used in etching experiments. Fig. 2.7 shows the measurement and FEM field simulation results.

Table 2.2 The CPW dimensions for different substrate materials.

Polymer	Substrate	*W*(μm)	*S*(μm)	*L*(mm)	*T*(μm)
BCB	Low-resistivity silicon	60	20	2	36
BCB	Glass	400	20	4	36

After etching the BCB polymer and a 13-μm depth into the silicon substrate between the signal and ground metals, the insertion loss of CPW lines on BCB-silicon was improved by 2 dB/cm at the high frequency range (Fig. 2.7(a)). This is, firstly, due to the air between signal and ground metals presents less losses than silicon [2.8] and polymer. Secondly, after etching the BCB and silicon, fewer fields couple and penetrate into the silicon substrate, as shown in the field simulation in Fig. 2.7(c). Thus a lower attenuation was achieved. On the other hand, on the BCB-glass device the slot width (20 μm) is much smaller compared to the signal conductor width (400 μm) (Fig. 2.7(d)). Thus even the air is a lower-loss dielectric material, the improvement was insignificant (Fig. 2.7(b)) since the field concentration and penetration does not change significantly. Note that the RIE process only removed BCB and silicon, but not glass.

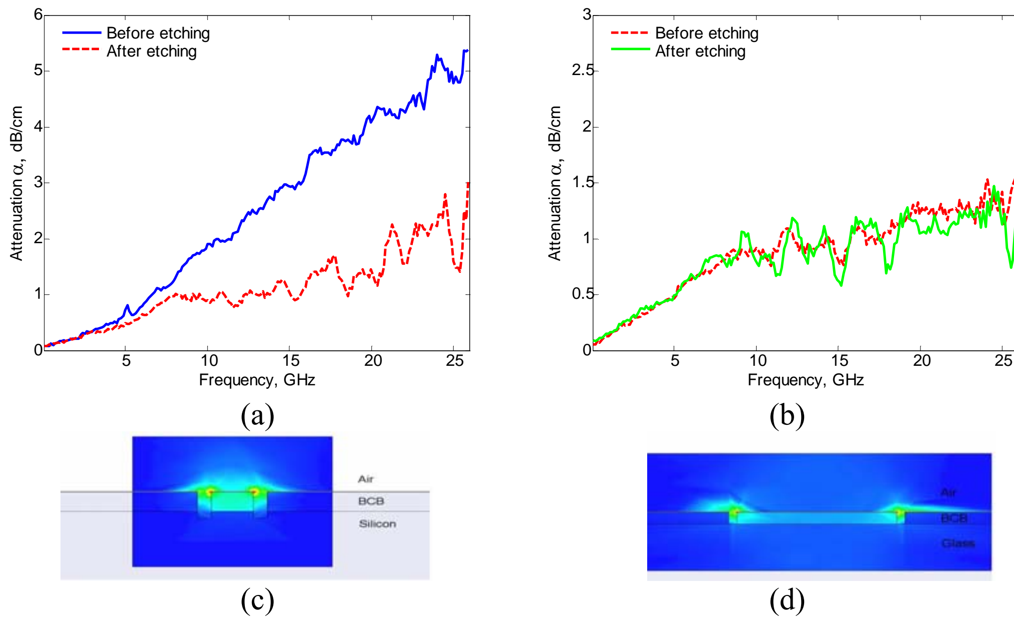


Figure 2.7 The performance comparison before and after etching. (a) The attenuation before and after etching BCB and a 13-μm depth into the silicon substrate. (b) The attenuation before and after etching BCB, but not into the glass substrate. (c) The FEM field simulation after etching BCB and the silicon substrate for a 13-μm depth. (d) The FEM field simulation after etching BCB, but not into the glass substrate.

2.3.3 The Performance of Different Polymers

2.3.3.1 Comparison between BCB and Kapton

The CPW lines built on Kapton do not need silicon or glass as substrates, thus a reduction of insertion losses is expected. The CPW lines were designed to have matched characteristic impedances. The dimensions are shown in Table 2.3. Fig. 2.8 shows the measurement results and electric field simulations.

Table 2.3 The CPW dimensions and characteristic impedances for different polymer materials.

Polymer	Substrate Material	W(μm)	S(μm)	L(mm)	T(μm)	Z_O (Ω)
BCB	Low-resistivity silicon	70	20	4	36	54
Kapton	No substrate	100	10	4	127	49

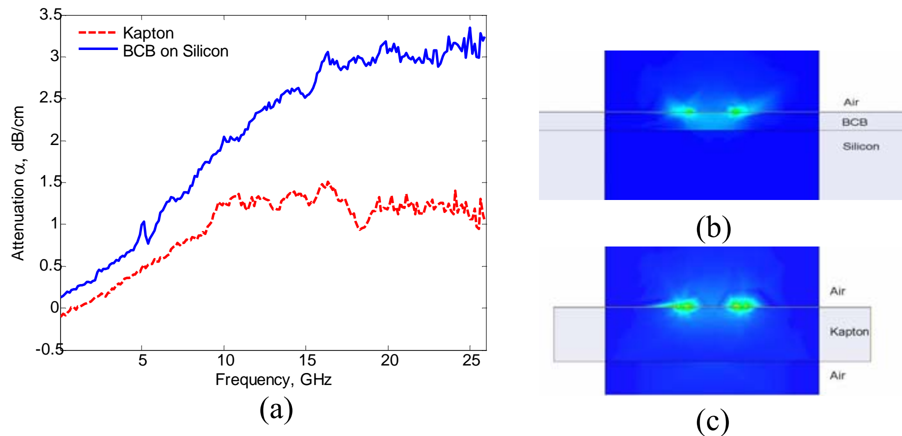


Figure 2.8 The performance comparison between BCB and Kapton. (a) The measurement results. (b) The field simulation of a CPW line on the BCB- silicon. (c) The field simulation of a CPW line on the Kapton.

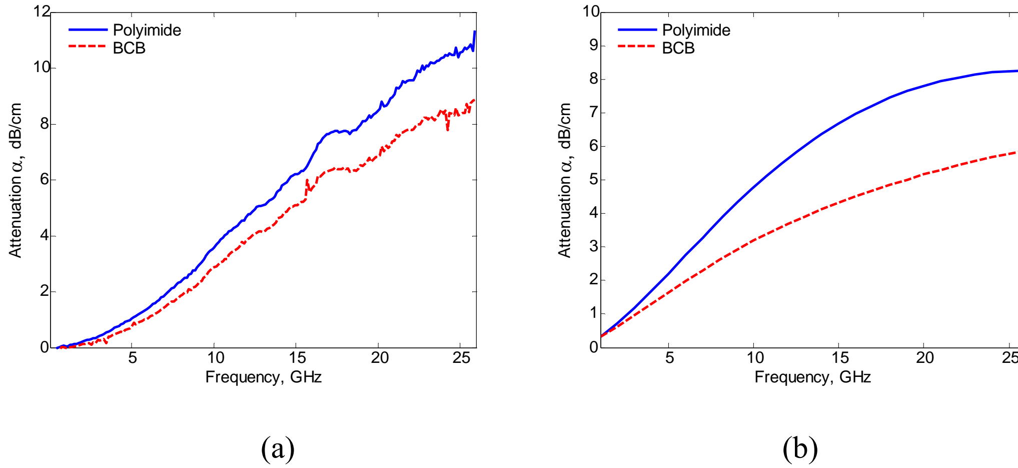
The Kapton presents an attenuation below 1.5 dB/cm up to 26 GHz, even with calibration noise included. The attenuation for a 36-µm BCB layer on silicon is below 3.3 dB/cm. The lower attenuation of the CPW line on Kapton is, primarily, due to the lower losses for the coupled fields into the substrate as shown in the field simulation in the Fig. 2.8(c). The CPW line on Kapton does not have a low-resistivity silicon as a substrate. Therefore, it eliminates any loss associated by the low-resistivity silicon. For CPW lines on BCB-silicon, as the electromagnetic fields penetrate through BCB into the substrate (Fig. 2.8(b)), the dopants induce a higher loss than polymers.

2.3.3.2 Comparison between BCB and Polyimide

Polyimide was also used as a dielectric layer to build CPW transmission lines to compare with the BCB polymer. Table 2.4 shows the device dimensions. Fig. 2.9 shows the measurement and FEM simulation results.

Table 2.4 The CPW dimensions for different polymer materials.

Polymer	Substrate	W(µm)	S(µm)	L(mm)	T(µm)
BCB	Low-resistivity silicon	60	20	2	13
Polyimide	Low-resistivity silicon	60	20	2	16



(a) (b)

Figure 2.9 The performance comparison between polyimide and BCB. (a) The measurement results. (b) The simulation results.

The thicker 16-µm polyimide layer suffers a slightly higher insertion loss than a thinner 13-µm BCB layer (Fig. 2.9(a)). This is due to the inherent electrical properties. The BCB has a lower dielectric constant (2.65), lower dissipation factor (0.08%) and a higher resistivity (10^{19}Ω-cm) while the polyimide has a dielectric constant of 3.4, a dissipation factor of 0.26% and a resistivity of 10^{17} Ω-cm. Thus the electromagnetic fields encounter less losses within the BCB polymer than polyimide. Simulation results in Fig. 2.9(b) confirm experimental results.

2.3.4 The Performance of Different Polymer Thicknesses

CPW lines on different-thickness polymers (13, 26 and 36 μm) were designed and fabricated. Table 2.5 shows the device dimensions. Fig. 2.10 shows the measurement results and FEM field simulation results.

Table 2.5 The CPW dimensions on different-thickness polymers.

Polymer	Substrate	*W*(μm)	*S*(μm)	*L*(mm)	*T*(μm)
BCB	Low resistivity silicon	60	20	1	13
BCB	Low resistivity silicon	60	20	1	26
BCB	Low resistivity silicon	60	20	1	36

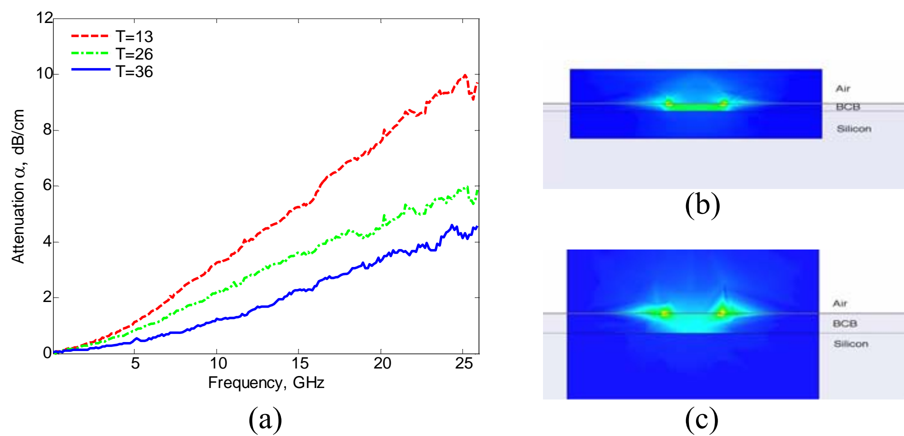


Figure 2.10 The performance comparison between different polymer thicknesses. (a) The measurement results. (b) The FEM field simulation of a 13-μm thick BCB layer. (c) The FEM field simulation of a 36-μm thick BCB layer.

A thicker polymer confines the electromagnetic fields better than a thin one does (Fig. 2.10(b) and (c)), hence less electromagnetic fields would be leaked into the loss-inducing silicon substrate. The measurement results (Fig. 2.10(a)) indicate that the thickest BCB polymer presents a lowest loss. At 10 GHz, the insertion loss of 36-μm thick BCB is below 1.5 dB/cm, meanwhile the insertion loss of 13-μm thick BCB is

below 3.5 dB/cm. It has been reported 4 dB/cm insertion loss for a 10-µm BCB polymer [2.9]. This is consistent with our experimental trends.

2.3.5 The Impacts of Device Dimensions

2.3.5.1 The Impacts of CPW Widths

To investigate the impacts of the center metal signal line, the signal-ground gap, *S*, was fixed, and the signal line widths, *W*, were varied, on fixed-length CPW lines. Table 2.6 shows the device dimensions and their characteristic impedances. Fig. 2.11 shows the measurement results and FEM field simulation results.

Table 2.6 The CPW dimensions and characteristic impedances.

Polymer	Substrate	*W*(µm)	*S*(µm)	*L*(mm)	*T*(µm)	Z_O (Ω)
BCB	Low-resistivity silicon	30	20	1	36	82
BCB	Low-resistivity silicon	70	20	1	36	54
BCB	Low-resistivity silicon	80	20	1	36	51
BCB	Low-resistitvity silicon	100	20	1	36	44

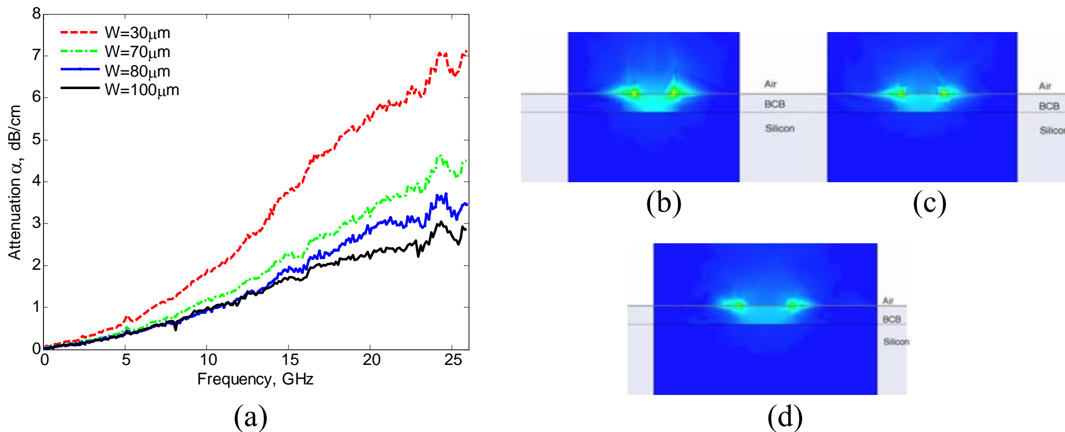


Figure 2.11 The performance comparison between different signal conductor widths. (a) The measurement results. (b) The FEM field simulation for a 70-µm width center conductor. (c) The FEM field simulation for a 80-µm width center conductor. (d) The FEM field simulation for a 100-µm width center conductor.

The CPW line with a 30-μm width presents the biggest attenuation due to its largely unmatched characteristic impedance. Intuitively, the matched CPW line with a 80-μm signal width is expected to have a lower loss than the 100-μm wide CPW line. The measurement results (Fig. 2.11(a)), however, indicated that a wider center conductor provides less insertion loss. The wider center conductor allows for a less concentrated field. Thus the skin-depth loss results in a lower attenuation. The field simulations in Fig. 2.11(b), (c) and (d) show a wider conductor has less field concentration.

2.3.5.2 The Impacts of CPW Lengths

CPW line lengths, L, were varied and signal width, W, and gap, S, were fixed to verify the effects of device lengths. Table 2.7 shows the dimensions and their characteristic impedances. Fig. 2.12 shows the measurement and simulation results for the total loss. The curves show a proportional trend with the length. This measurement is to establish the baseline for measurement accuracy. The measurement trends indicate the unit loss is about 0.6 dB/mm at 20 GHz.

Table 2.7 The CPW dimensions and characteristic impedances.

Polymer	Substrate material	L(mm)	W(μm)	S(μm)	T(μm)	Z_O (Ω)
BCB	Low-resistivity silicon	0.5	70	20	36	54
BCB	Low-resistivity silicon	1	70	20	36	54
BCB	Low-resistivity silicon	2	70	20	36	54

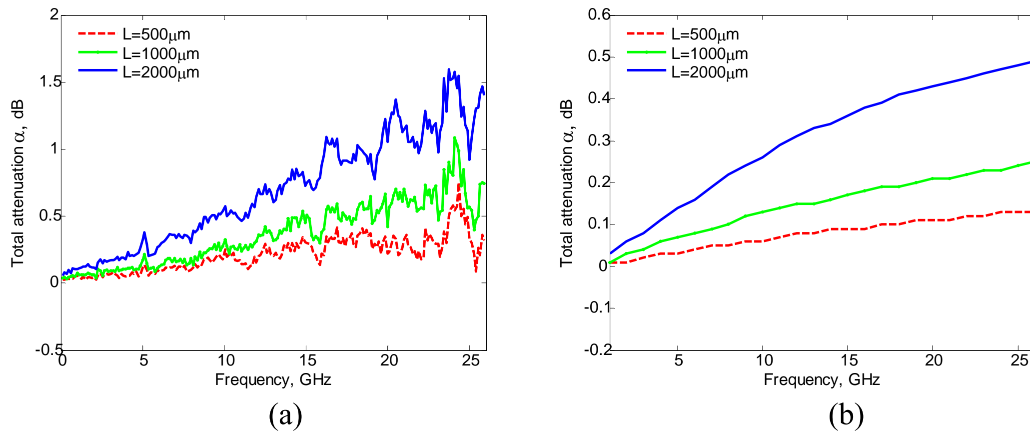


Figure 2.12 The insertion losses of CPW lines with different lengths. (a) The measurement results. (b) The FEM simulation results.

2.3.5.3 The Impacts of CPW Gap Sizes

To show the impacts of the gap size, the width, *W*, was fixed and gaps, *S*, were varied on fixed-length CPW lines. Table 2.8 shows the dimensions. Fig. 2.13 shows the measurement results and FEM field simulations.

Table 2.8 The CPW dimensions.

Polymer	Substrate material	*S*(μm)	*W*(μm)	*L* (mm)	*T*(μm)
BCB	Low-resistivity silicon	10	70	1	36
BCB	Low-resistivity silicon	20	70	1	36
BCB	Low-resistivity silicon	40	70	1	36

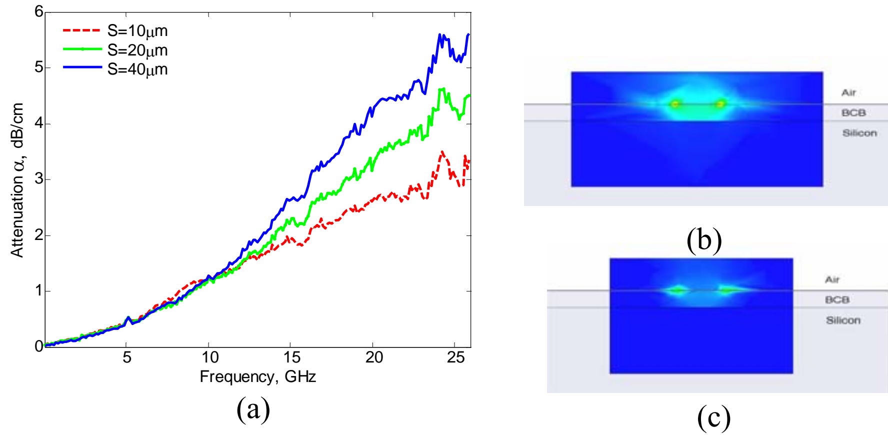


Figure 2.13 The insertion losses of CPW lines with different signal-ground gaps. (a) The measurement results. (b) The field simulation for a 40-μm gap. (c) The field simulation for a 10-μm gap.

The experimental results show (Fig. 2.13(a)) that the CPW line with widest gap suffers the highest loss. This is possibly because that a wider gap results in more coupled fields into the substrate, as indicated in the FEM field simulation in Fig. 2.13(b) and (c). Thus the attenuation induced by the dopants of substrates is higher [2.10].

2.3.6 The Impacts of Matching Circuits

The probes have CPW ground-signal-ground contacts with a spacing of 150 μm and width of 50 μm. Smooth impedance transitions were designed to accommodate different CPW line dimensions. Table 2.9 shows the matching circuit dimensions and their characteristic impedances. Fig. 2.14 shows the linear transitions of matching circuits between probe ends and the CPW lines. The insertion losses induced by such matching circuits are estimated to be smaller than 0.15 dB/cm [2.11].

Table 2.9 The taper dimensions and characteristic impedances.

Polymer	Substrate	W (μm)	L(μm)	S (μm)	T(μm)	Z_O (Ω)
BCB	Glass	140	100	10	30	50.1
BCB	Silicon	80	100	50	30	50.8

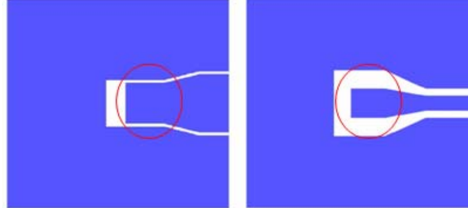


Figure 2.14 Taper matching circuits. (a) The matching circuits for CPW lines on BCB-glass. (b) The matching circuits for CPW lines on BCB-silicon.

2.4 Conclusions

In this chapter, we investigated the fabrication techniques and RF performances of CPW transmission lines on organic dielectric and substrate materials. The device built on polymer-silicon substrate presents an insertion loss of 3 dB/cm at 26 GHz. The device on polymer-glass substrate has an insertion loss of 1.5 dB/cm at the same frequency range. Whereas, the substrateless Kapton device only presents an insertion loss of 1 dB/cm. To our knowledge, it is the first flexible CPW lines ever developed.

The effects of device dimensions were studied as well. A short length, narrow gap, wide signal or thick polymer layer will induce a low insertion loss in general. The fabrication techniques are simple, low-cost and compatible with existing CMOS processes.

CHAPTER 3

A DMTL TUNABLE PHASE SHIFTER ON A LOW-RESISTIVITY SILICON

Phase shifters are key components of many communication and sensor systems. Most existing phase shifters are based on semiconductor or ferrites technologies. Heavy weights, expensive fabrication procedures, and high RF losses hinder their applications. The distributed MEMS transmission line (DMTL) phase shifter was first introduced by *Barker* [3.1] using a quartz substrate. A series of MEMS air-gap bridge varactors are placed over a coplanar waveguide (CPW) transmission line. Phase shifts are created by phase velocity changes induced by altering bridge parallel-plate capacitances. Due to the much lower series resistance [3.2], this approach provides a low attenuation. Its zero bias current and passive nature ensure a minimum power consumption and high linearity [3.1]. Like most current RF MEMS devices, the DMTL phase shifters and its related approaches have been fabricated using quartz [3.1], high-resistivity silicon [3.3], and III-V compounds [3.4] as substrates to achieve good RF performances.

In this chapter, the polymer-silicon approach discussed in the previous chapter is further explored and a novel solution to build RF MEMS phase shifters on CMOS-grade low-resistivity silicon is presented. Design considerations, fabrication processes and measurement results will be discussed in detail in this chapter.

3.1 Design Considerations

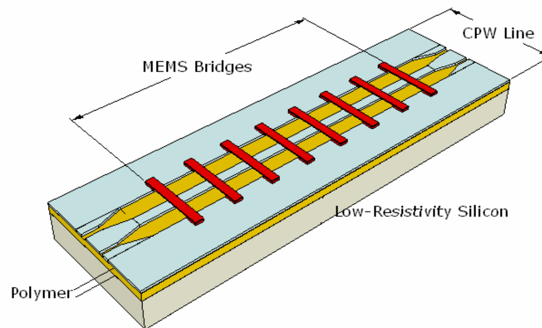


Figure 3.1 An overall sketch of a distributed MEMS phase shifter.

3.1.1 Silicon Substrate

Our DMTL phase shifter consists of four building blocks: a silicon substrate, a polymer dielectric layer, CPW transmission line and MEMS air-gap bridge varactors, as shown in Fig. 3.1. The CMOS-grade p-type <100> silicon was chosen as the substrate material. Measured by a *Veeco FPP-5000* four-point probe, it has a resistivity less than 10 Ω-cm.

3.1.2 Polymer Dielectric Layer

Facing the same problem as CPW lines, the CMOS-grade high-conductivity silicon substrate is not fitted for DMTL RF phase shifter due to its conductive nature. Thus an intermediate dielectric layer is required to prevent or minimize signal attenuations. The CPW line study indicated that polymers such as polyimide resin, BCB resin and Kapton film could serve for this purpose. With a BCB layer of 36 μm between the CPW line and the high-conductivity silicon wafer, the insertion loss could be controlled less than 3.3 dB/cm at 26 GHz. Micromachining the signal-ground gap will further reduce the insertion loss.

However, the gap dimensions (on the order of tens of microns) of CPW line research were much smaller than those of DMTL phase shifters (on the order of hundreds of microns). The RF signal losses, which are due to the electric fields penetrating through the polymer layer into the silicon substrate, are proportionally related to the CPW line gap dimensions as shown in the *Section 2.3.5.3*. Studies in the *Section 2.3.4* indicated that a thicker polymer layer results in a lower loss. Thus a thick polymer layer (e.g. above 100 μm) is needed for the DMTL phase shifters. However, obtaining a polymer thickness of 100 μm with good uniformity is a difficult and time-consuming task. This requires many spinning-curing cycles to deposit multiple layers to reach the required thickness, e.g. a 36-μm BCB layer requires at least 3 spinning-curing cycles. Multiple-curing process will also likely result in other unexpected complications such as degrading polymer properties and cross contaminations.

In this chapter, a novel solution to this problem is presented where Kapton films are bonded with a low-resistivity silicon substrate using BCB resin as the bonding material. A 250-μm polymer layer of Kapton film is thick enough to contain most of the traveling RF signals. Employing this method, only one curing cycle is needed, the deposition process is greatly simplified and the fabrication time is significantly reduced. Furthermore, the film quality is guaranteed.

3.1.3 Distributed MEMS Transmission Line

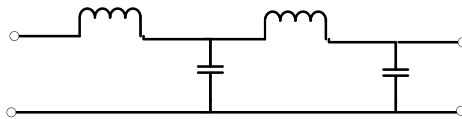


Figure 3.2 The unit-length equivalent circuit of an unloaded CPW line.

The unit-length equivalent circuit of the CPW line is shown in Fig. 3.2, where the L_t, and C_t are the unit-length inductance and capacitance, respectively. Eq. 3.1 reflects the relationship between the characteristic impedance, Z_o, the unit-length inductance, L_t, and capacitance, C_t,

$$Z_o = \sqrt{\frac{L_t}{C_t}} \text{ and } C_t = \frac{\sqrt{\varepsilon_{eff}}}{cZ_o} \qquad (3.1)$$

where the ε_{eff} is the effective dielectric constant, and c is the speed of light in free space. The phase velocity V_t of an unloaded CPW line is

$$V_t = \frac{1}{\sqrt{L_t C_t}} \qquad (3.2)$$

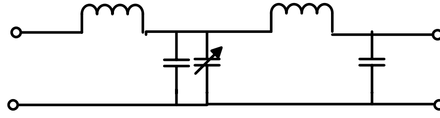


Figure 3.3 The unit-length equivalent circuit of a loaded CPW line.

Loading a CPW line with periodic MEMS bridges adds shunt capacitances C_b in parallel to the C_t. The unit-length equivalent circuit of a loaded CPW line is shown in Fig. 3.3. The total unit-length capacitance of the loaded CPW line thus becomes $C_l=C_b/s+C_t$, where s is the periodic spacing between two adjacent MEMS bridges. The loaded capacitances decrease the characteristic impedance. The modified characteristic impedance Z_l is given by *Barker* [3.1]. To obtain a minimum transmission loss, the dimensions of the unloaded CPW lines need to be properly designed so that the loaded characteristic impedance is close to 50 Ω.

$$Z_l = \sqrt{\frac{L_t}{C_t + C_b / s}} \qquad (3.3)$$

L_t

C_t

The fact that Kapton film has a dielectric constant of 3.5, close to that of the quartz (ε_r=3.78), provides the great convenience to take the advantage of existing designs based on quartz substrates. In this work, CPW line dimensions to have a signal-line width (W) of 100 μm and signal-ground spacing (S) of 100 μm were chosen, similar to *Barker's* design.

With a 250-μm thick polymer layer as the dielectric material, the low-resistivity silicon will not affect the characteristic impedance Z_o significantly. The *Agilent ADS* software is used to calculate the characteristic impedance of the unloaded CPW line. It found Z_o = 92 Ω, with a 250-μm Kapton dielectric layer and a perfect ground plane. Removing the ground plane, the characteristic impedance of such an unloaded CPW line is 98 Ω. The CMOS-grade silicon substrate has a resistivity less than 10 Ω-cm. Thus the characteristic impedance of the unloaded CPW line is expected to lie between 92 and 98 Ω.

3.1.4 MEMS Bridges

The MEMS bridge capacitances decrease the phase velocity and create phase shifting. The loaded CPW line phase velocity is shown in Eq. 3.4 [3.1]. Eq. 3.5 gives the MEMS bridge capacitances where ε_o is the free-space permittivity, w is the bridge width, and d is the bridge height.

$$V_l = \frac{1}{\sqrt{L_t(C_t + C_b / s)}} \qquad (3.4)$$

$$C_b = \varepsilon_o \frac{A}{d} \text{ and } A = W \times w \qquad (3.5)$$

Eq. 3.6 shows the relationship between the bias voltage and bridge height, where d_o is the zero-bias bridge height, and k is the spring constant of the bridge membrane as a function of its dimensions, material strength, and surface stress level [3.5]. Eq. 3.8 gives the spring constant formula where E is Young's modulus, υ is the Poisson ratio, σ is the stress level, and the L is bridge length. The pull-in condition happens at one third of the bridge height. The pull-in voltage is given in Eq. 3.7. A small original bridge height (d_o) will require a low actuation voltage; but a small bridge height presents a large fringe capacitance, thus the pull-in voltage is sensitive to small voltage variations, especially electrical noises. Taking this effect and fabrication convenience into account, a bridge height of 1.37 μm is selected.

$$V_{bias} = \sqrt{\frac{2k}{\varepsilon_o W w} d^2 (d_o - d)} \qquad (3.6)$$

$$V_p = \sqrt{\frac{8k}{27\varepsilon_o W w} d_o^3} \ (V) \qquad (3.7)$$

$$k = \frac{32Et^3 w}{L^3} + \frac{8\sigma(1-\upsilon)tw}{L} \qquad (3.8)$$

Eq. 3.9 shows that the phase shift value is a function of the device length (*l=n(s+w)+s)* and phase velocities of the original and biased states (V_o, V_b).

$$\delta\varphi = 2\pi f l (\frac{1}{V_o} - \frac{1}{V_b}) \qquad (3.9)$$

3.1.5 Other Considerations

The operational frequency of a periodic structure is limited by the *Bragg* frequency, beyond which the periodic structure becomes reactive and the return loss increases significantly [3.1][3.6].

$$f_{Bragg} = \frac{1}{\pi s \sqrt{L_t (C_t + C_b / s)}} \qquad (3.10)$$

Eq. 3.10 indicates, with MEMS bridges biased, the *Bragg* frequency is lower than that of the unbiased one.

The CPW transmission line has dimensions of 100-μm spacing and 100-μm width. The devices were measured with GSG (ground-signal-ground) probes which have dimensions of 150-μm spacing and 50-μm tip width. A taper-type matching circuit was designed, as shown in Fig. 3.4, to accommodate the dimensional difference and avoid an abrupt impedance change between the CPW line and the feeding pads [3.7][3.8].

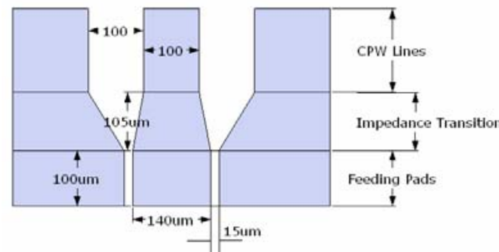


Figure 3.4 The taper impedance transition.

3.2 Fabrication Processes

3.2.1 Polymer Deposition

Low-resistivity substrates and Kapton films were cleaned with an acetone ultrasonic bath for 2 minutes to remove surface contaminations and followed by 1-minute hotplate baking at 100°C to dehydrate any residual liquid on the surfaces. BCB polymer was deposited on the low-resistivity silicon and two 125-μm Kapton films

using the deposition process described in the *Section 2.2.1*. The silicon and Kapton films were bonded together using the BCB as the adhesive material.

The hard curing step for BCB was conducted inside a nitrogen-purged environment oven ramping slowly from the room temperature to 250°C at which the curing process lasted for one hour. A pressure of 20 lb/inch^2 was evenly applied while curing. This pressure is necessary and critical to ensure a tight, bubble-free and planar bonding. Such a heating step cures more than 95% of the polymer [3.9]. Fig. 3.5(a) shows a polymer layer on a silicon substrate.

3.2.2 CPW Metal Formation

Samples were washed with acetone in an ultrasonic bath to remove any cross contaminations. *Futurrex* NR7-3000p negative photoresist was spun on top of the polymers at 3000 rpm for 40 seconds, followed by 150°C hotplate baking for 1 minute. Next, the CPW patterns were exposed through a soda lime photomask. Post exposure bake (PEB) was performed at 100°C for 1 minute. The samples were then developed in *Futurrex* RD6 developer with mild agitation for 25-30 seconds, followed by a de-ionized water rinse and nitrogen air drying.

A sandwich metal layer of chromium-aluminum-chromium was deposited using the thermal evaporation technique. The thickness of the Cr-Al-Cr layers is 500-8000-500Å, respectively. The two Cr layers functioned as adhesion materials. Experiments showed that without adhesion metals, the aluminum CPW layer neither firmly adhered on the polymer nor to the MEMS bridges in the later processing steps.

The samples were soaked in acetone solvent overnight for metal liftoff. Most of unexposed negative photoresist NR7-3000p together with the metals on top of it were lifted off by acetone soaking and a short time ultrasonic agitation (less than 2 minutes). However, due to the uncertainty of the photolithography and excessive thermal evaporation heating, the NR7-3000p may be partially overexposed and cured. Thus it was not easy to be lifted off by the acetone soak and ultrasonic bath completely. In this case, 10 minutes hot bath (~100°C) in RR2 photoresist stripper would be adequate to give a clean liftoff. Fig. 3.5(b) shows the cross section of a CPW transmission line on the polymer-silicon substrate.

3.2.3 Silicon Nitride Growth

The samples were cleaned with an acetone wash. Ultrasonic process was avoided in this step, because the metal layer formed in the last step was vulnerable to the ultrasonic waves. The patterns of the CPW center conductor insulating layer were defined by the same photolithography processes. A silicon nitride insulating layer of 6000 Å was grown using a RF sputtering technique. A lift-off process again was performed with the same conditions as in the previous step. Fig. 3.5(c) shows the silicon nitride on the CPW center conductor.

3.2.4 Sacrificial Layer Deposition

The samples were washed with acetone before the positive photoresist S1813 was used to form the sacrificial layer. The S1813 was spun on the samples at 3000 rpm for 30 seconds, followed by hotplate baking at 105°C for 70 seconds. The photoresist layer was patterned with the sacrificial photomask by the photolithography. The

samples were developed for 30 seconds in MF319 developer. The samples were then heated on a hotplate at 130˚C for 3.5 minutes. This post-developing bake was critical. It should give the sacrificial layer enough robustness, yet the photoresist should still be able to be dissolved later by the photoresist stripper. A different heating profile may either cure the photoresist or would not generate a firm sacrificial layer. Fig. 3.5(d) shows the sacrificial layer

3.2.5 Bridge Formation

A copper layer of 1.5-μm thickness was deposited using a thermal evaporation process. During the evaporation, samples were rotated at different angles to ensure an evenly grown copper layer. Bridges patterns were defined using a photoresist S1813 layer by the photolithography process. The photoresist served as a mask for copper etching. The etching process was performed in APS100 copper etchant at 50°C for 30 seconds. Fig. 3.5(e) illustrates this bridge formation process.

3.2.6 Device Release

The samples were soaked inside an PR1165 photoresist stripper overnight, followed by alcohol rinsing with mild agitation. To avoid the bridge stiction, the samples were baked at 110°C for 10 minutes to quickly evaporate the alcohol residues. Fig. 3.5(f) shows a bridge after releasing.

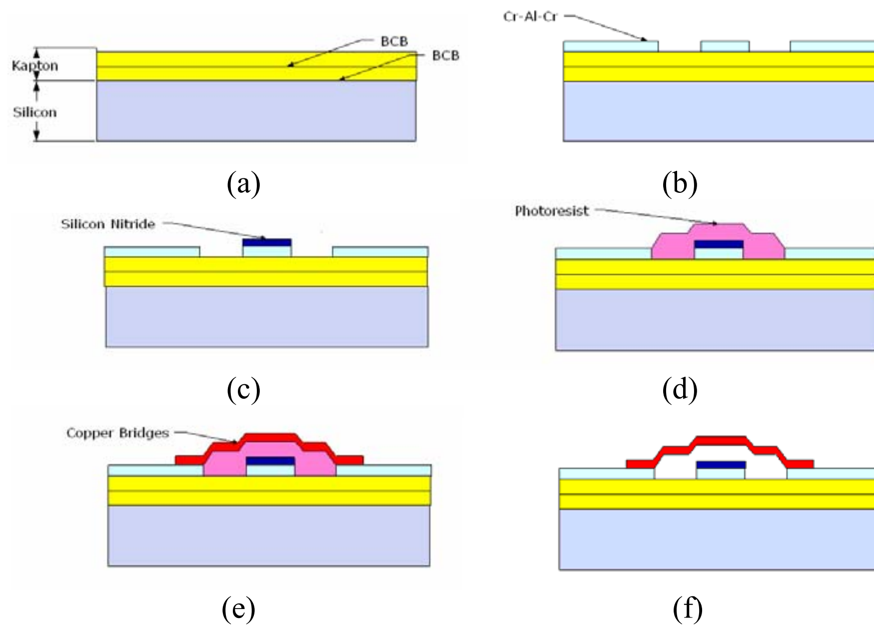


Figure 3.5 Fabrication processes. (a) Kapton-silicon bonding. (b) CPW transmission line formation. (c) Silicon nitride growth. (d) Sacrificial layer deposition. (e) Bridge formation. (f) Device release.

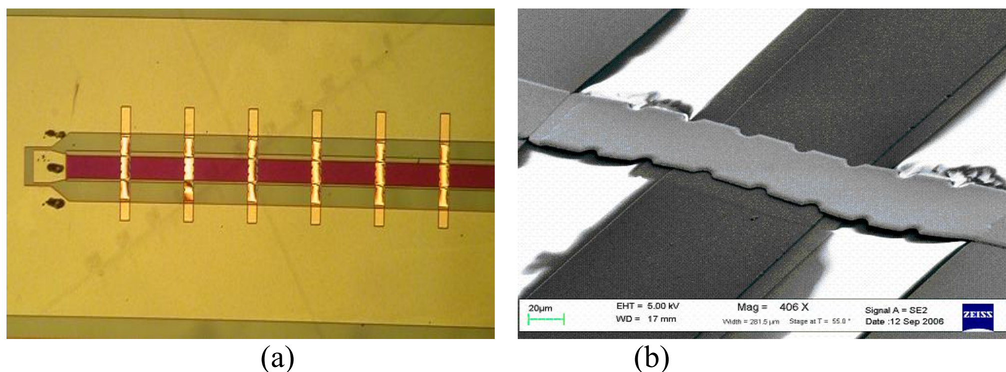


Figure 3.6 (a) A photo of the RF MEMS phase shifter. (b) A SEM photo of a MEMS bridge over a CPW center conductor line.

3.3 Measurement Results

Fig. 3.6(a) shows the RF MEMS phase shifter and Fig. 3.6(b) shows a SEM photo of a MEMS bridge over a CPW center conductor line. The bridges are 60-µm

wide and 300-μm long. The devices were characterized with two *Cascade Microtech Infinity GSG-150* probes connecting to an *Agilent 8510c* network analyzer. The measurement was performed from DC to 26 GHz. The scattering parameter measurements were calibrated by a *Cascade Microtech ISS-005-016* impedance standard substrate. The actuating voltages were applied by a *HP4142B* DC source and a *HP11612* biasing network.

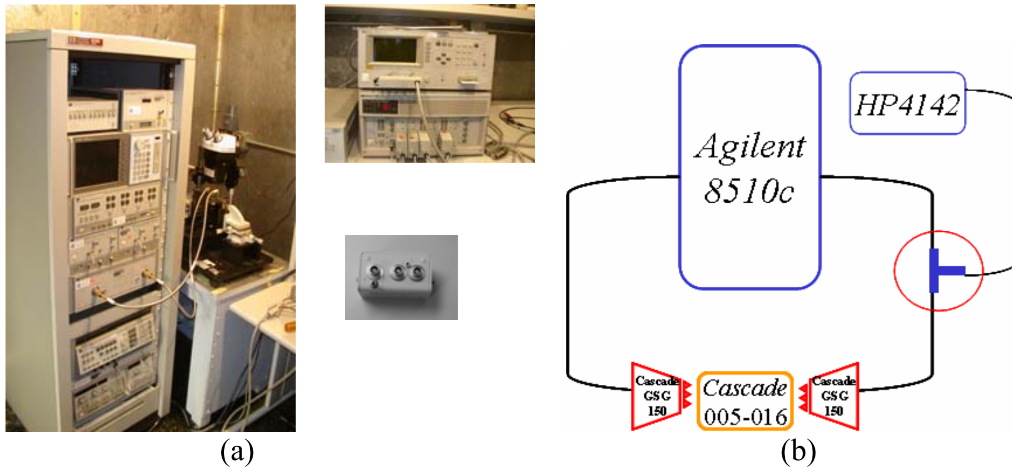


Figure 3.7 (a) *Agilent 8510c* network analyzer, *HP4142B* DC source and *HP11612* biasing network. (b) Equipment connection demonstration.

3.3.1 Phase Shifters on Kapton-Silicon Substrate

3.3.1.1 Phase Shifts versus Frequencies

The bridge height d is determined by the actuation voltage, as indicated by Eq. 3.6, where d_o is the bridge height under a zero biasing voltage, d is the bridge height under a nonzero biasing voltage, k is the spring constant, W is the CPW conductor width, w is the bridge width and ε_0 is the free-space permittivity. A higher biasing voltage results in a smaller bridge height d, thus a larger MEMS bridge capacitance C_b which creates a slower phase velocity and a larger phase shift.

The device configuration for the measurement of phase shifting values versus actuation voltages is shown in the Table 3.1, in micrometers, where t is the bridge thickness.

Table 3.1. Device dimension for phase shifting measurement. *: Low-resistivity silicon (LRS).

Substrate	d_o	n	s	w	t
Kapton-LRS*	1.37	8	400	60	2.1

Fig. 3.8 shows a phase shift of 43° with a 40-V bias voltage at 26 GHz is achieved, while the phase shifts are 22° and 8° under 30-V and 20-V bias voltages, respectively. The measurements display a linear relationship of phase shift values as a function of frequency under various bias voltages. This tendency suggests the phase shift values will continue to increase linearly beyond 26 GHz, which is the upper limit of our testing equipment, until it approaches the *Bragg* frequencies under each bias voltages.

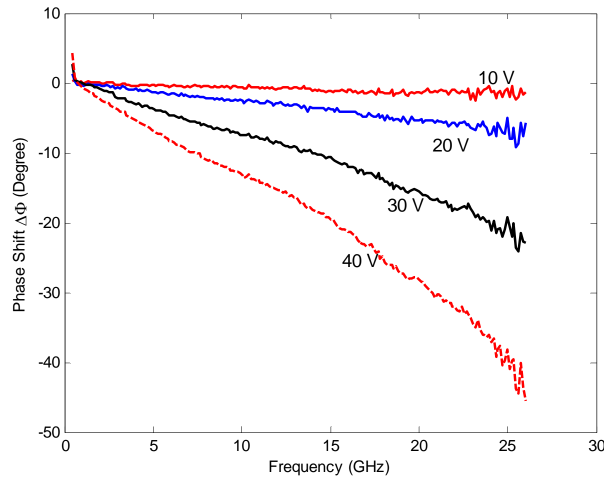


Figure 3.8 Experimental results of phase shifts with different bias voltages.

3.3.1.2 Insertion and Return Losses

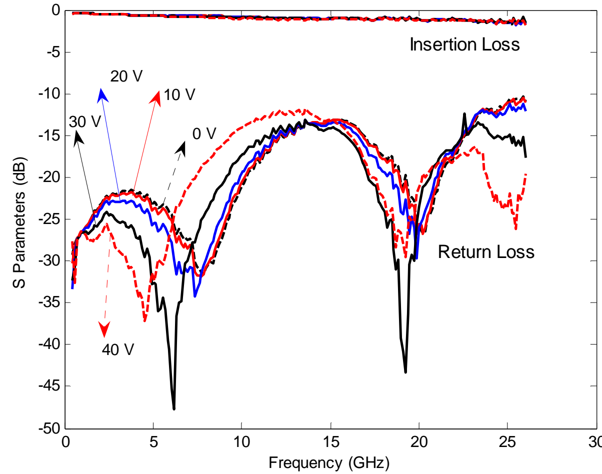


Figure 3.9 Insertion and return losses.

Fig. 3.9 shows the insertion losses are below 1.4 dB at 26 GHz regardless of the bias voltages. This result is comparable to the quartz-based phase shifter which has an insertion loss of 1.6 dB at 40 GHz [3.1]. The return losses are less than 10 dB at 26 GHz for all bias voltages.

Phase shifters were also directly built on CMOS-grade silicon substrates without the Kapton polymer film. The insertion losses were greater than 40 dB. This result implies most of RF signals vanished into the substrates when there were no polymer dielectric layer.

3.3.1.3 Phase Shifter Parameters

Fig. 3.9 shows the measured insertion and return losses. The loaded characteristic impedance Z_l can be extracted from the first peak of the return loss at which the device behaves as a quarter-wavelength transformer [3.1]. Using this Z_l value,

the MEMS bridge capacitance was calculated from Eq. 3.3, the *Bragg* frequency was extracted from Eq. 3.10, the effective dielectric constant was obtained using Eq. 3.11. With a zero bias voltage, the characteristic impedance Z_l is 54.3 Ω, MEMS capacitance C_b is 47.2 fF, effective dielectric constant ε_{eff} is 6.61, and the *Bragg* frequency f_{bragg} is 80.8 GHz.

$$\varepsilon_{eff} = c^2 \left[L_t \left(C_t + C_b / s \right) \right] \tag{3.11}$$

The theoretical calculation of C_b, with a zero bias voltage, is 38.8 fF from Eq. 3.5. Using this C_b value, the predicted Z_l, ε_{eff}, and f_{bragg} is 57.8 Ω, 5.85 and 85.9 GHz, respectively. The discrepancies between the measurement and theoretical prediction may be due to the contribution of the fringe capacitances at the edges of MEMS bridges. It significantly alters the phase shifter characteristics. With a 30- and 40-V bias voltage, the Z_l becomes 53.1 and 52.2 Ω, C_b is 50.7 and 53.1 fF, ε_{eff} is 6.93 and 7.15, and f_{bragg} is lowered to 78.9 and 77.6 GHz.

3.3.1.4 Pull-in Voltage

Using Eq. 3.7 and Eq. 3.8, the theoretical calculations of pull-in voltages are calculated as 34, 42 and 49 V assuming 0, 20 and 40-MPa stress, respectively. Knowing the MEMS bridge capacitance C_b from the measurement, the actual pull-in voltage was extracted using Eq. 3.5-3.8. It was calculated larger than 47 V. This pull-in voltage, as well as the Fig. 3.8, suggests that there exists a residual stress. The stress is most likely produced by the excessive heating during the thermal evaporation process. The variation of the bridge height and thickness owing to fabrication uncertainty may also

play a role to increase the pull-in voltage. Due to the limitation of the testing equipment, a bias voltage beyond 40 V is not achievable.

3.3.1.5 Simulated Insertion and Return Losses

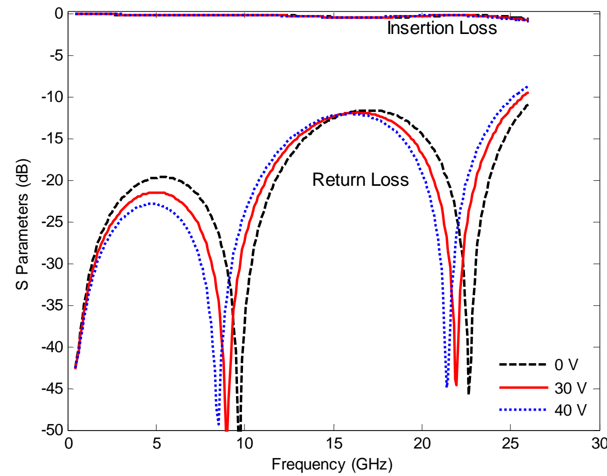


Figure 3.10 Simulated insertion and return losses.

Fig. 3.10 displays the simulated insertion and return losses for the same device with 0-, 30- and 40-V bias voltages using a lumped model. The DMTL phase shifter was modeled as 8 cascaded sections, each of which contains a CPW transmission line and a parallel shunt capacitance. In the simulation, the frequencies of two nulls are higher than those of measurement results in Fig. 3.9. This is likely because the simulation used a lumped-element model capacitance representing MEMS varactors C_b, as shown in Fig. 3.11(a); in reality, the MEMS bridge capacitance is distributed across the CPW center conductor line as indicated in Fig. 3.11(c). The MEMS bridge inductance L_b (Fig. 3.11(b)), in series with C_b, was not taken into consideration in the simulation. It produces counter-effect of the MEMS capacitance [3.1].

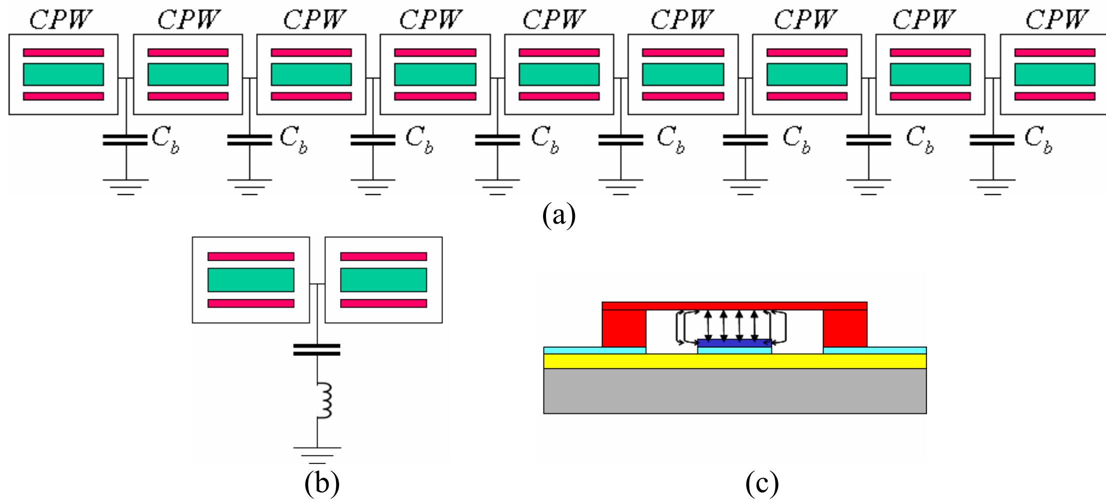


Figure 3.11 (a) The lumped model simulation. (b) Unit-bridge equivalent circuit. (c) Actual bridge capacitance distribution.

The simulation indicates a transmission loss of 0.8 dB at 26 GHz. It is 0.6 dB lower than the measurement result. The discrepancy is due to the mismatch losses at the contact pads, metal conduction losses and skin effect. In an ideal lossless network, the summation of the normalized power is unity [3.10] or 0 dB, as shown in Eq. 3.12.

$$\sum_{k=1}^{N} S_{ki} S_{ki}^{*} = 1 \qquad (3.12)$$

Fig. 3.12 displays the normalized power loss. It indicates that the loss contribution from the metal conduction loss and the skin effect is 1 dB at 26 GHz.

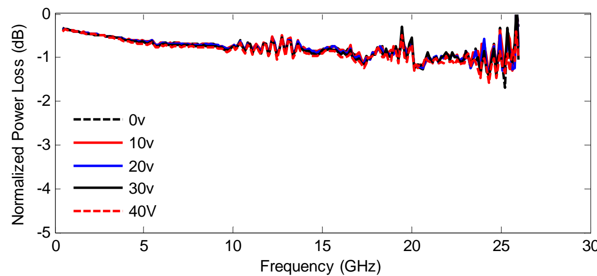


Figure 3.12 Experimental results of normalized power loss as function of frequency.

3.3.2 Phase Shifters on Polymer-Glass Substrate

Glass was also used as the substrate for the purpose of comparison. The glass substrate was coated with a thin layer of BCB polymer (10μm) to promote a strong adhesion and to increase the yield rate. The phase shifting values are compared for devices with similar dimensions. Table 3.2 gives the device dimensions, in micrometers, of the two compared devices, where t_p is the polymer layer thickness.

Table 3.2. Device dimensions for different polymers-substrates.

Substrate	t_p	n	s	w
Kapton-LRS	250	8	400	60
BCB*-Glass	10	8	400	60

Fig. 3.13 shows that with Kapton-LRS and BCB-glass as the polymer-substrate materials, 43˚ and 45˚ phase shifting values were achieved at 26 GHz, respectively. Fig. 3.13 illustrates the Kapton-LRS has the lower insertion loss (1.4 dB), while the BCB-glass has a loss of 1.9 dB, even the low-resistivity silicon presents a higher conductivity in the substrate compared to glass. This is due to the thickness of the Kapton layer (250 μm) on the low-resistivity silicon. Compared to the much thinner BCB, less electromagnetic fields are coupled into the silicon substrate. Should BCB have a same thickness (250 μm) on the glass substrate, the phase shifter of BCB-glass is expected to have a similar or lower insertion loss than that of Kapton-LRS. However, achieving such a thickness of BCB proved to be an exceedingly difficult task.

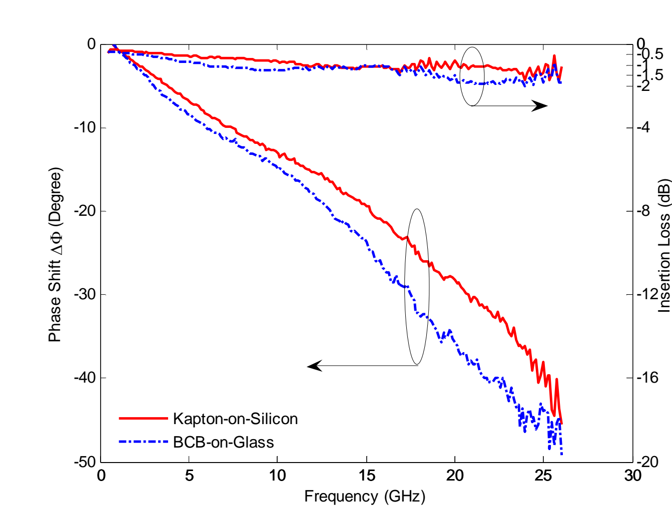


Figure 3.13 Experiment results of phase shifts and insertion losses of devices based on different substrate materials.

3.3.3 Device Dimensions

The effects of device dimensions are examined in the following discussions to verify the design rules. The fabrication consistency for comparison is crucial in order to achieve accurate conclusions. The devices to be compared were fabricated in the same batch and in the vicinity on the same wafer. All the devices discussed hereafter were fabricated on low-resistivity silicon with a Kapton dielectric layer.

3.3.3.1 Bridge Number

The phase velocity is determined by the unit-length bridge capacitance, as shown by Eq. 3.4. With same dimensions, the unit-bridge phase shift is same even if the total bridge numbers are different. To investigate the unit-bridge phase shifting value, bridge width (w) and spacing (s) are fixed, and the bridge numbers (n) were varied on two phase shifters. Table 3.3 shows the dimensions of these two circuits in micrometers.

Table 3.3. Device dimensions for different bridge numbers.

Substrate	*n*	*w*	*s*
Kapton-LRS	8	60	500
Kapton-LRS	16	60	500

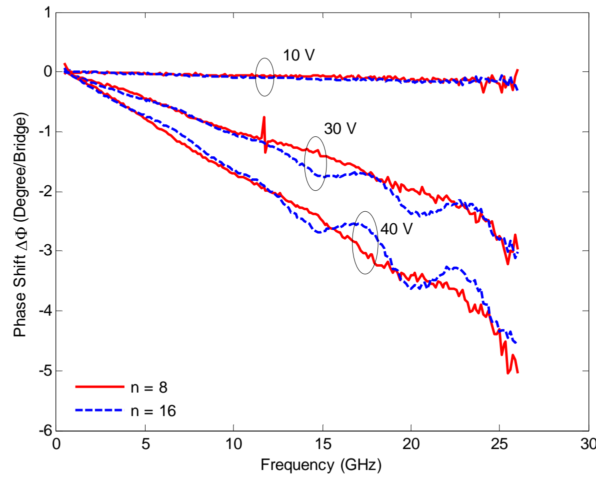


Figure 3.14 Effects of bridge numbers.

Comparing the performances of the two phase shifters in Fig. 3.14, with 8 and 16 bridges placed over CPW lines, the unit-bridge phase shifting values are very close. With a bias voltage of 30 V, the unit-bridge phase shift is 3˚ at 26 GHz; whereas the unit-bridge phase shift is 5˚ at 26 GHz with a bias voltage of 40 V, regardless of the bridge numbers. The ripples on the 16 bridge measurements are due to longer devices accumulating more standing waves.

3.3.3.2 Bridge Width

To investigate the impacts of the bridge width, the bridge number (*n*) and bridge spacing (*s*) were fixed, and the bridge widths (*w*) were varied, as shown in Table 3.4.

Table 3.4. Device dimensions for different bridge widths.

Substrate	*w*	*n*	*s*
Kapton-LRS	30	8	400
Kapton-LRS	60	8	400

According to Eq. 3.4, 3.5, 3.9, a wider bridge produces a larger MEMS capacitance C_b which creates a slower phase velocity. Thus a larger phase shift value $\Delta\Phi$ is achieved. Nonetheless, the dependency of phase shift on C_b is weaker than a first order linearity.

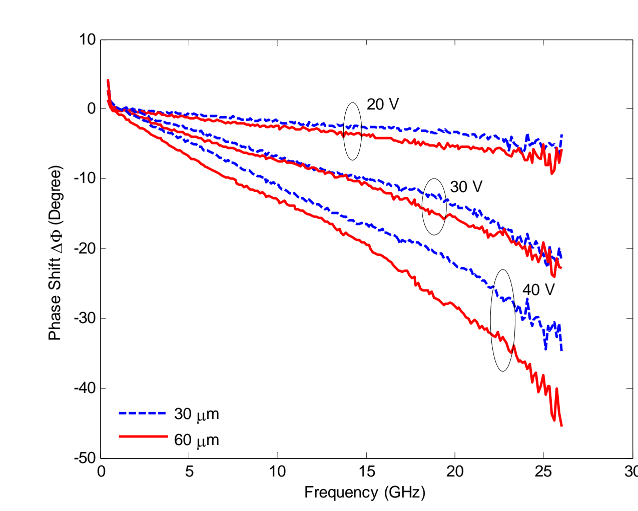


Figure 3.15 Effects of bridge widths.

Fig. 3.15 demonstrates that 60-μm bridges create larger phase shifts than 30-μm bridges regardless of bias voltages, e.g. at 26 GHz with a bias voltage of 40 V, the phase shifts are 43˚ and 31˚ for the 60- and 30-μm width bridges; with a bias voltage of 10 V, the phase shifts are 8˚ and 5˚ for the 60- and 30-μm width bridges, respectively.

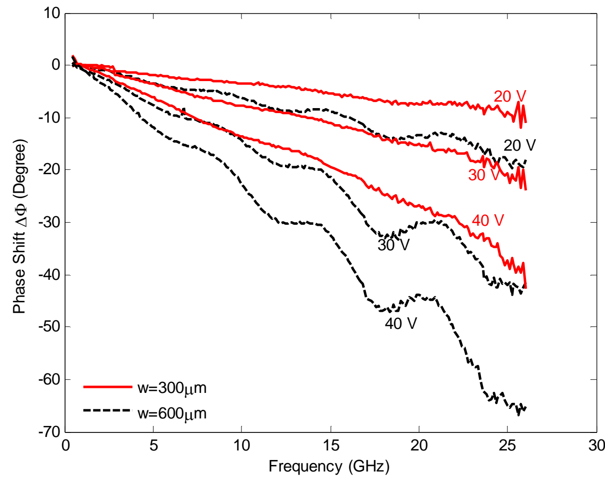
3.3.3.3 Bridge Spacing

The bridge spacing affects the phase shifting values in two opposite ways: 1) the device length is proportional to the bridge spacing s linearly, as shown in Eq. 3.12. A longer circuit delivers a larger phase shift, as indicated by Eq. 3.9; 2) the phase velocity is weakly proportional to $\sqrt{s}$, as suggested by Eq. 3.4. The result of these two conflicting factors is a less than linear phase shift increase versus spacing increase. Table 3.5 shows the dimensions of two compared devices.

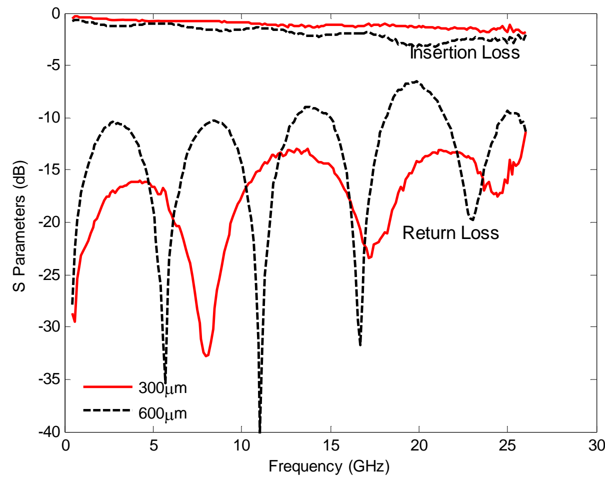
$$l = n(s + w) + s \qquad (3.12)$$

Table 3.5. Device dimensions for different bridge spacings.

Substrate	*s*	*w*	*n*
Kapton-LRS	300	30	16
Kapton-LRS	600	30	16



(a)



(b)

Figure 3.16 Effect of bridge spacing. (a) Phase shifts versus spacings. (b) Losses versus spacings.

As demonstrated in Fig. 3.16(a), a longer device clearly presents a larger phase shift for all bias voltages. However the larger phase shifting values come with penalties. Fig. 3.16(b) indicates the insertion loss, under a 40-V bias voltage, is nearly doubled when the spacing increased from 300 μm to 600 μm.

3.4 Conclusions

In this chapter, a novel method to build distributed MEMS transmission line phase shifter on CMOS-grade silicon was investigated. Kapton films were bonded with low-resistivity silicon to avoid the RF signal loss. Design approaches, fabrication techniques, simulation and RF performances were discussed in this chapter. A phase shift of 43° and a low insertion loss of 1.4 dB were achieved at 26 GHz. A good linearity implied that a higher phase shift value exists beyond 26 GHz. Glass substrate and benzocyclobutene were also used to construct RF MEMS phase shifters. A very close result to that of Kapton-silicon was achieved. Dimensional elements were inspected to investigate their impacts on RF performances and to verify the design rules. A longer device, larger bridge number or wider bridge will produce a larger phase shift. However, a longer devices will introduce more insertion loss. Utilizing the CMOS-grade low-resistivity silicon as substrates provides great opportunities for high-frequency IC applications.

CHAPTER 4

RF MEMS TUNABLE FILTERS

Microwave filters can be found in virtually all type of communication, radar, testing and measurement systems. Because the dynamic nature of these systems, there is a need to develop devices by which real-time functionalities can be reconfigured using software controls [4.1]. Tunable filters are essential parts for the success of such real-time systems.

Current tunable filters can be classified in three major catalogues according to their tuning mechanisms: mechanically, magnetically, and electrically tuned filters [4.2]. Mechanically tuned filters are generally built using coaxial or waveguide resonators. They have large power handling abilities and low insertion losses. The downsides are that they are heavy and the tuning speeds are very low. Magnetically tuned filters, such as Yttrium-Iron-Garnet (YIG) filters, have large tuning ranges, spurious-free responses, low insertion losses, high quality factors and good selectivities. However, they are bulky, expensive and require large quiescent currents [4.3]. The three dimensional structures make them unable to be integrated into an IC systems. Electrically tuned filters use FET or pin diodes as tuning elements. The semiconductor devices have fast tuning speeds, need low bias currents, require small areas and are IC compatible. Nonetheless, the active nature of this approach suffers from the nonlinearity, low quality factor and harmonics. Thus, electrically tuned filters are still unable to meet the

requirements of a high-performance RF transceiver system [4.2][4.3]. Table 4.1 shows a comparison of tunable filters based on different working principles [4.2].

Table 4.1 Comparison between different tunable filters.

Parameter	Mech.	YIG	PIN/FET	BST	RF MEMS
I.L.[dB]	$0.5-2.5$	$3-8$	$3-10$	$3-5$	$3-8$
Unloaded Q	>1000	>500	<50	<100	$<100-500$
Power Handling[W]	500	2	0.2	–	2
Bandwidth[%]	$0.3-3$	$0.2-3$	>4	>4	$1-10$
IIP_3[dBm]	very high	<30	<30	<30	>50
Tuning speed[GHz/ms]	very low	$0.5-2$	10^3	–	10^2
Tuning linearity[MHz]	±15	±10	±35	–	–
Miniaztrization capability	No	No	Yes	Yes	Yes
Millimeter – wave capability	No	Yes	No	No	Yes

The emergence of MEMS switches and varactors provides a new possibility to construct high-performance tunable filters. The inherent advantages of RF MEMS devices, such as low loss, high Q factor [4.3]-[4.7], high linearity, high isolation level and large bandwidth are ideally suited for tunable filter requirements. The high switching speeds [4.1][4.5] and long life spans [4.1] of MEMS devices are especially useful for a real-time system. The low power consumption [4.7] and miniaturized dimension of the MEMS approach are especially attractive to applications where a large number of filters are needed and the spaces are limited, e.g., phased-array antenna. Fabricating MEMS switches uses existing semiconductor manufacturing technologies and does not demand any new materials and equipment outside the current IC scope.

Thus the MEMS approach is very attractive for both commercial and military applications.

Some existing MEMS filters demonstrated benefits from different perspectives. *Liu'*s design presented a cost-effective approach [4.8], *Nordquist's* digital filter avoided thermal instability [4.9], *Garth*'s end-coupled filter displayed a stable bandwidth [4.10], *Rebeiz* demonstrated the finest tuning resolution, 16 states for a 6 GHz tuning range [4.11]. However, despite their individual advantages, neither of them was designed for low-resistivity silicon substrates. They all have difficulties to integrate with CMOS IC chips.

In this chapter, compact MEMS tunable filters designed and fabricated on CMOS-grade low-resistivity substrates are investigated.

4.1 Design Considerations

A band-pass filter is generally designed from its low-pass prototype and mapped to the band-pass counterpart using the filter transformation method. Such a filter, consisting of series resonators alternating with shunt resonators, is difficult to achieve by a microwave structure [4.12]. It is more realistic to utilize same type of resonators to form a microwave filter. Impedance inverters covert series resonators to parallel resonators and vice versa. Hence band-pass filters are normally designed as same type of resonators coupled by impedance inverters.

For a tunable filter, it is crucial that the tuning mechanism does not affect the coupling behavior. The filter formed by end-coupled resonators has a localized coupling form [4.2] which is insensitive to the tuning behavior. The end-coupling structure

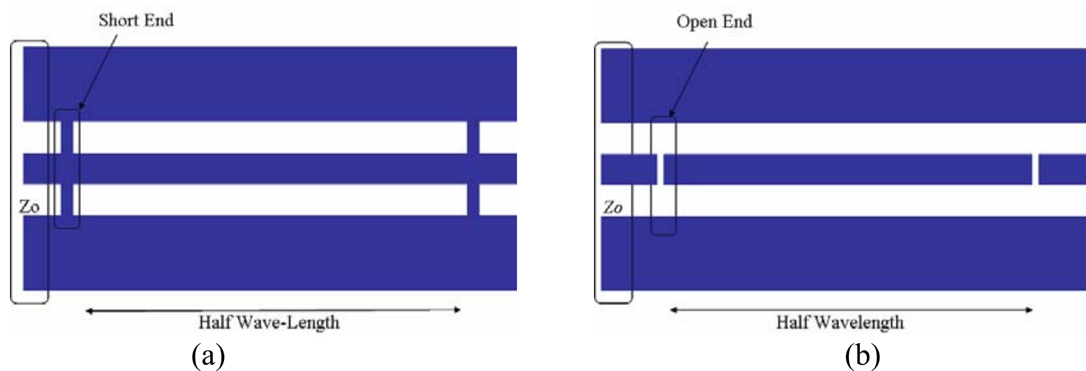
generally has a small space requirement. Thereby it leaves enough physical dimension for the tuning structure construction.

In order to be compatible with the CMOS circuitry, a dielectric layer is needed for utilizing the low-resistivity silicon. Benefited for the successes of the CPW lines and RF MEM phase shifters described in chapter 2 and 3, a similar polymer-silicon method will be employed where Kapton films are used as the dielectric material. Knowing the Kapton film has a dielectric constant of 3.5, which is close to that of quartz (3.78) and glass (3.8~5), design parameters based on quartz and glass [4.8][4.11][4.13] will be referenced for great convenience.

A band-pass filter consists of a number of coupled resonators, where a large number of resonators produce steep rising and falling slopes, but with the price of a large area requirement and a high transmission loss. After balancing these contradicting factors, the tunable filters discussed hereafter will focus on a 3-pole topology.

4.1.1 MEMS Tunable Resonator Design

Resonance happens when the resonator length (L) is equal to half or a multiple half the guided wavelength ($\lambda/2$). Resonators can be constructed using many waveguide structures, such as a CPW transmission line, strip transmission line, coaxial cable, etc. Due to the excellent microwave performance and simple fabrication process of MEMS-transmission lines, resonators will be designed based on half-wavelength coplanar waveguide transmission lines (CPW resonator).



(a) (b)

Figure 4.1 (a) Short-ended resonator. (b) Open-ended resonator.

Unlike transmission lines and phase shifters where the entire frequency of the signal source is fed in, filters need a feeding mechanism by which only the selected spectrum is able to pass through. There are two types of feeding mechanisms for the resonator input: short-ended feeding and open-ended feeding, as shown in Fig. 4.1. The open- and short-ended feeding mechanisms are dual to each other, and have identical frequency behaviors. Both mechanisms are mature and have been thoroughly investigated [4.14]-[4.16]. Hence, in this section, resonators using both feedings will be explored.

Loading a resonator with shunt capacitors slows down the wave velocity, and consequently, alters the resonant frequency. This controls the filter's tuning ability. So far, three types of loading structures have been investigated: partial-loaded distributed capacitors [4.2][4.17], even-loaded distributed capacitors [4.8] and tapped-loaded capacitors, as shown in Fig. 4.2. At the microwave frequency, the lumped capacitors and inductors are difficult to implement. The tapped capacitor has limited capacitive values due to the dimension restriction and displays inferior RF performance compared

with distributed capacitors [4.17]. For this reason, the tapped-loaded capacitors will not be further investigated from this point forward. On the contrary, distributed elements are more convenient to realize [4.12][4.18][4.19] and have larger capacitive values due to the dispensed nature. Furthermore, the well-controlled RF behaviors of distributed MEMS capacitors are ideal for the tuning purpose.

The maximum loading effect happens at the peak of the voltage distribution, likewise, the minimum loading effect happens when the voltage distribution is null. The short-ended resonator has the voltage peak in the middle of the device, whereas the open-ended resonator has the voltage peak at its ends [4.2][4.17]. For this reason, the shorted-ended resonator is partially loaded with MEMS capacitors in the middle section (Fig. 4.2(a)), the open-ended resonator is evenly loaded with MEMS capacitors across the resonator (Fig. 4.2(b)). In order to achieve a symmetrical voltage distribution, the MEMS bridges for both partial-loaded and even-loaded resonators are placed symmetrically to the circuit center line. In case of an odd number of bridges needed, the middle bridge is self-mirrored to the circuit center line.

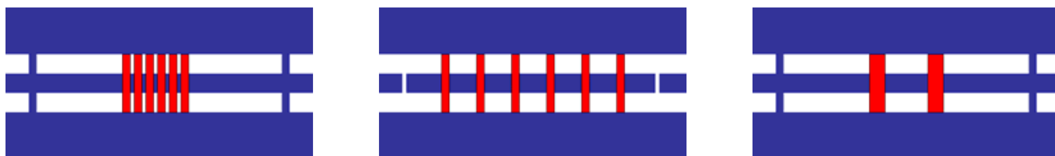


Figure 4.2 (a) Partial-loaded MEMS capacitors. (b) Even-loaded MEMS capacitors. (c) Tapped-loaded capacitors.

4.1.1.1 Partial-loaded Short-ended Resonator

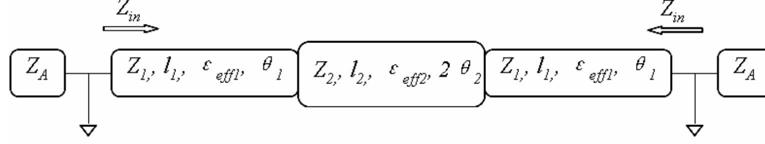


Figure 4.3 The equivalent circuit of a partial-loaded short-ended resonator.

The equivalent circuit of a partial-loaded short-ended resonator is shown in Fig. 4.3, where the Z_A is the characteristic impedance connected to the resonator, Z_1, l_1, ε_{eff1}, and θ_1, are the characteristic impedance, physical length, effective dielectric constant and half electrical length of the unloaded part of the resonator, respectively. Likewise, Z_2, l_2, ε_{eff2}, and θ_2 are those of the loaded part of the resonator, correspondingly [4.2][4.17][4.19].

Loading the CPW line with MEMS varactors results in a locally higher dielectric constant and lower impedance than the unloaded part. These uneven characteristics create a slow-wave structure and shift the resonant frequency towards a lower one. Biasing the MEMS capacitors further lowers the resonant frequency.

$$K = 1 + \frac{cZ_1 C_b}{(s + w + \Delta l)\sqrt{\varepsilon_{eff1}}} \tag{4.1}$$

$$\varepsilon_{eff2} = K\varepsilon_{eff1} \tag{4.2}$$

$$Z_2 = \frac{Z_1}{\sqrt{K}} \tag{4.3}$$

$$l_2 = n(s + w + \Delta l) \tag{4.4}$$

Eq. 4.1-4.4 [4.17][4.19] give the effective dielectric constant and characteristic impedance of the loaded part of a resonator, where c is the light speed in free space, s, n,

$w+\Delta l$ and C are the bridge spacing, number, effective bridge width and bridge capacitance. The Δl can be found using simulation tools such as the *Agilent ADS*. Knowing the physical dimensions of n, s, w, and Δl, the electrical length θ_2 is able to be determined by Eq. 4.5-4.6, where L_g is the guide wavelength and f is the resonant frequency.

$$\theta_2 = 0.5 l_2 \frac{2\pi}{L_g} \qquad (4.5)$$

$$L_g = \frac{c}{f\sqrt{\varepsilon_{eff2}}} \qquad (4.6)$$

Employing the same polymer-silicon method of building phase shifters, resonators were constructed on a 250-µm Kapton dielectric film with a low-resistivity silicon as the substrate. The CPW transmission line and bridge dimensions are shown in Table 4.2.

Table 4. 2 CPW line and MEMS bridge dimensions.

W (µm)	S(µm)	l_1(µm)	w (µm)	s (µm)	n
160	80	582	50	20	6

The dielectric constant of the Kapton film is 3.5, the effective dielectric constant is 2.32 acquired by the *Agilent ADS* simulation. Using Eq. 4.1-4.4, the resonator parameters are calculated and shown in Table 4.3.

Table 4.3 The resonator parameters.

ε_{eff1}	K	ε_{eff2}	Z_A (Ω)	Z_1(Ω)	Z_2(Ω)
2.32	22.4	51.9	50	73.4	15.5

The resonator input impedance seen from the feeding point is given as Eq. 4.7 [4.17], assuming a lossless network,

$$\overline{Z'_{in}} = j\overline{X'_{in}} = j\frac{\tan\theta_1 - \overline{Z_2}\cot\theta_2}{1+\overline{Z_2}\tan\theta_1\cot\theta_2} \quad (4.7)$$

where the bar sign and prime sign denote the half circuit and the normalization to the unloaded characteristic impedance, and the θ_1 is the half electrical length of the unloaded CPW line, θ_2 is the half electrical length of the loaded CPW line. Resonance happens when the reactance is equal to zero [4.18][4.19], as shown in Eq. 4.8. The electrical length θ_1 thus is able to be determined by manipulating Eq. 4.8.

$$\tan\theta_1 - \overline{Z_2}\cot\theta_2 = 0 \quad (4.8)$$

The reactance slope $\bar{x}$, which will be used later in the inverter design, is given by Eq. 4.9 [4.13] [4.17]. The electrical lengths θ_1, θ_2 and reactance slope $\bar{x}$ are listed in Table 4.4.

$$\bar{x} = \frac{\omega_o}{2}\frac{dX_{in}}{d\omega}\bigg|_{\omega_o} = \omega_o\frac{dX'_{in=}}{d\omega}\bigg|_{\omega_o} = \theta_1 + \overline{Z_2}\theta_2\cos^2\theta_1\csc^2\theta_2 \quad (4.9)$$

Table 4.4 The electrical lengths and reactance slope.

θ_1(deg)	θ_2(deg)	$\bar{x}$
22.3	27.2	0.8

4.1.1.2 Even-loaded Open-ended Resonator

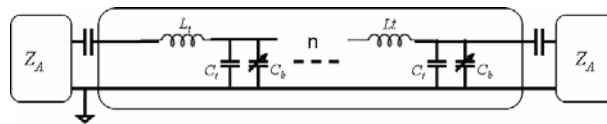


Figure 4.4 The equivalent circuit of an even-loaded open-loaded resonator.

Unlike the partial-loaded short-ended resonator, the even-loaded open-ended MEMS transmission line resonator has only one impedance level throughout the entire

device. The impedance level can be calculated as an open-ended transmission line [4.18].

$$\overline{Z_{in}} = \frac{1 + j\tan\beta l \tanh\alpha l}{\tanh\alpha l + j\tan\beta l} \quad (4.10)$$

Because the loaded CPW transmission line resonator has a very low loss, α, Eq. 4.10 is simplified as Eq. 4.11 and Eq. 4.12.

$$\overline{Z_{in}} \cong j\overline{X} \cong \frac{1}{j\tan\theta} \quad (4.11)$$

$$\theta = \beta l \quad (4.12)$$

The resonance occurs when θ is equal to $k\pi$, namely, the device length is half or a multiple half the guided wavelength. The resonant frequency ω_r is calculated from Eq. 4.13 to Eq. 4.15.

$$\omega_r = \frac{\pi V_{phase}}{l} \quad (4.13)$$

$$l = n(s + w) + s \quad (4.14)$$

$$V_{phase} = \frac{1}{\sqrt{L_t(C_t + C_b / s)}} \quad (4.15)$$

where l is the resonator's physical length and V_{phase} , described by Eq. 4.15, is the phase velocity of the RF signal traveling inside the resonator. The tuning range is given in Eq. 4.16 [4.8], where x is the loading factor equal to the ratio of maximum unit-length bridge capacitance C_b to unit-length CPW capacitance C_t (Eq. 4.17 [4.8]), and y is the tuning factor which is the ratio of C_{bmax} to C_{bmin} (Eq. 4.17).

$$\Delta = 1 - \sqrt{\frac{1+\frac{x}{y}}{1+x}} \qquad (4.16)$$

$$x = \frac{C_{b\max}/s}{C_t} \qquad (4.17)$$

$$y = \frac{C_{b\max}}{C_{b\min}} \qquad (4.18)$$

The resonator dimensions and parameters are given by Table 4.5 and Table 4.6, where *W, S, w* and *s* are CPW width, CPW signal-ground spacing, bridge width and adjacent bridge spacing.

Table 4.5 CPW transmission line and MEMS capacitor dimensions.

W (μm)	*S*(μm)	*w* (μm)	*s* (μm)
150	75	30	230

Table 4.6 The resonator parameters.

ω_o (GHz)	$Z_A(\Omega)$	$Z_o(\Omega)$	y	x	Δ
20	50	74	1.5	0.5	6%

For the purpose of convenience, in the later text, the partial-loaded short-ended resonator/filter and even-loaded open-ended resonator/filter will be stated as the partial-loaded resonator/filter and even-loaded resonator/filter, respectively.

4.1.2 Inverter Design

4.1.2.1 *K* Inverters for the Partial-loaded Resonator

The short-ended resonators are convenient for utilizing *K* type inverters as coupling devices. A *K* inverter has multiple forms of physical realizations [4.12]. Due to the simplest structure and compact dimension, inductor will be used in this work. Fig

4.5 shows an equivalent circuit of a 3-pole partial-loaded distributed transmission line tunable filter. Because of the symmetrical nature of the resonator filter, only half the circuit was shown in Fig. 4.5.

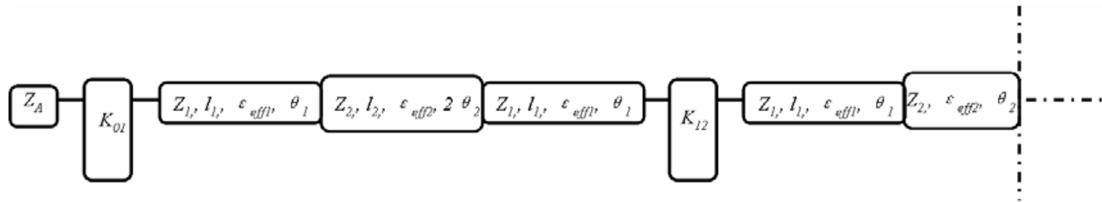


Figure 4.5 The half equivalent circuit of a 3-pole partial-loaded tunable filter.

The K inverter has negative electrical lengths at both sides of the inductor. Generally, these negative lengths do not introduce any problem since they will be absorbed by the adjacent transmission lines [4.12][4.18]. Fig. 4.6 shows the equivalent circuit of a K inverter, where subscripts L and R denote the left and right with the inductor as the reference plane, n represents the section number which is from 0 to 4 for a 3-pole tunable filter.

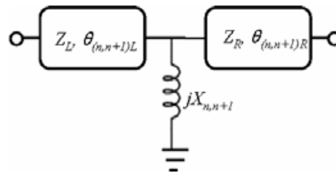


Figure 4.6 The equivalent circuit of a K inverter.

A *Chebyshev* filter with 3 poles and 0.05 dB pass-band ripple has element values given by the low-pass prototype filter shown in Table 4.7 [4.12][4.17]. The low-pass prototype filter is mapped to its corresponding band-pass filter using filter

transformation procedure [4.12][4.18]. The equation set from Eq. 4.19-4.29 describe the K inverter calculation procedure.[4.12][4.17]-[4.19].

Table 4.7 The element values of a *Chebyshev* low-pass filter of 3 poles with a 0.05-dB pass-band ripple.

g_0	g_1	g_2	g_3	g_4
1	0.879	1.113	0.879	1

$$\overline{K_{01}} = \overline{K_{34}} = \sqrt{\frac{\overline{wx}\overline{Z_A}}{g_0 g_1}} \tag{4.19}$$

$$\overline{X_{01}} = \overline{X_{34}} = \left[\left(\overline{K_{01}}^2 - 1\right)\overline{Z_A}^{-2} + \left(\overline{K_{01}}^{-2} - 1\right)\right]^{-0.5} \tag{4.20}$$

$$\theta_{01L} = \theta_{34R} = \left(\frac{p+q}{2}\right) \tag{4.21}$$

$$p = -\tan^{-1}\left[\left(\overline{Z_A}^{-1} + 1\right)\overline{X_{01}}\right] \tag{4.22}$$

$$p = -\tan^{-1}\left[\left(\overline{Z_A}^{-1} - 1\right)\overline{X_{01}}\right] \tag{4.23}$$

$$\overline{K_{12}} = \overline{K_{23}} = \frac{\overline{wx}}{g_2} \tag{4.24}$$

$$\overline{X_{12}} = \overline{X_{23}} = \frac{\overline{K_{12}}}{\sqrt{1 - \overline{K_{12}}^2}} \tag{4.25}$$

$$\theta_{01R} = \theta_{34L} = \left(\frac{p_{01}}{2}\right) \tag{4.26}$$

$$p_{01} = -\tan^{-1}\left[2\overline{X_{01}}\right] \tag{4.27}$$

$$\theta_{12L} = \theta_{12R} = \theta_{23L} = \theta_{23R} = \left(\frac{p_{12}}{2}\right) \tag{4.28}$$

$$p_{12} = -\tan^{-1}\left[2\overline{X_{12}}\right] \tag{4.29}$$

Designed to have the pass-band center frequency of 21 GHz, the K inverter electrical lengths and inductor values are shown in the Table 4.8.

Table 4.8 The K inverter parameters.

θ_{01L}(deg)	θ_{01R}(deg)	θ_{12L}(deg)	L_{01}(pH)	L_{12}(pH)
-18.6	-12.9	-3.3	134.4	32.1

Fabricating a 3-D structure of the inductive K inverter is complicated and time-consuming. It needs multiple-mask procedures and high-precision alignments. Fortunately, the inductive values required for tunable filters are small enough to be realized by ribbon straight line inductors [4.16] [4.20]. However, there is no closed-form formula to accurately calculate the inductive value given its dimension, or vice versa. In this work, both a simulation tool (*Sonnet*) and the classic formula of Eq. 4.30 [4.20] were employed for searching a precise value.

$$L = 2l\left\{\ln\left(\frac{2\pi l}{w}\right) - 1 + \frac{w}{\pi l}\right\} \ nH \qquad (4.30)$$

Eq. 4.30 is an empirical formula which reflects the relationship between the ribbon width w (cm), length l (cm) and the inductor value. The advantage is that it is independent of substrate material's dielectric properties. However report indicates Eq. 4.30 may have a 10% error margin [4.20]. The two methods, *Sonnet* simulation and empirical formula calculation, produced a large dimensional discrepancy for a given inductive value. In an effort of searching an accurate dimension, a compromised value between these two methods was also taken.

Table 4.9 shows the inductor dimensions of three different methods, *Sonnet* simulation, empirical formula calculation and a compromise of the two. Fig. 4.7 shows the sketch of a ribbon straight line inductor.

Table 4.9 K inverter dimensions calculated using three methods.

	$L_{01} = L_{34}$	$L_{12} = L_{23}$
Value (pH)	135	32
w (μm)	20	20
Simulated l (μm)	560	140
Calculated l (μm)	360	120
Compromised l (μm)	460	130

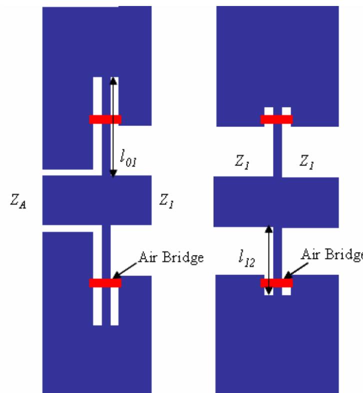


Figure 4.7 The sketches of (a) L_{01} and (b) L_{12}.

The lengths for both inductor values are longer than the spacing between CPW signal and ground. Therefore, the inductors have to extend into the CPW ground. Although, the inductor lengths could have been designed within the CPW signal-ground spacing by shrinking the inductor widths to submicron scales, our experiments indicated that such an effort introduced fabrication complexity and significantly increased the processing cost.

The asymmetrical impedances at the two sides of the inverter can support slot-line modes and cause radiation, thus the transmission loss will increase. To bypass this potential problem, the two halves of the grounds are shorted using an air bridge [4.2][4.17]. The air bridges will be formed in the same step with loaded MEM capacitors during the fabrication procedure.

4.1.2.2 *J* Inverters for the Even-loaded Resonator

The even-loaded open-ended resonator is naturally suited for the capacitive coupling mechanism. Fig. 4.8 shows the topology of a 3-pole tunable filter using *J* inverters.

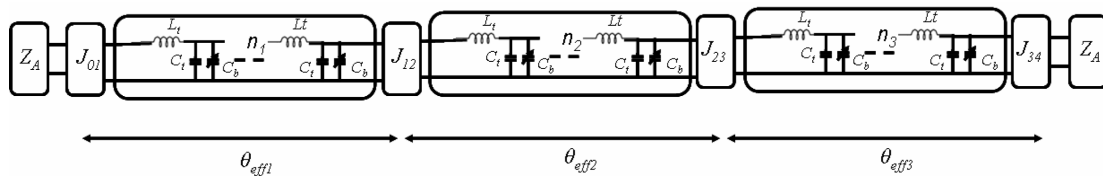


Figure 4.8 The equivalent circuit of a 3-pole even-loaded tunable filter.

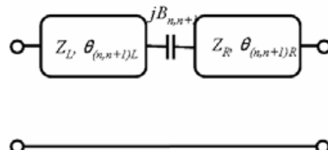


Figure 4.9 The equivalent circuit of a *J* inverter.

The parameter calculation process of the even-loaded tunable filter is identical to that of the capacitively coupled filter [4.18] except it has a higher dielectric constant and a lower phase velocity. The even-loaded tunable filter is designed to be a 0.5 dB

equal-ripple filter. The element values of the low-pass prototype filter are shown in Table 4.10 [4.18].

Table 4.10 The element value of a 3-pole 0.5dB equal-ripple filter.

g_0	g_1	g_2	g_3	g_3
1	1.5963	1.0967	1.5963	1

For a center pass-band frequency of 20 GHz, the electrical lengths and J inverter capacitive values were calculated as Table 4.11.

Table 4.11 The J inverter parameters

θ_{01L}(deg)	θ_{12L}(deg)	C_{01}(fF)	C_{12}(fF)
-13.35	-3.88	40	10.9

$$\begin{aligned} &\theta_{01L} = \theta_{01R} = \theta_{34L} = \theta_{34R} \\ &\theta_{12L} = \theta_{12R} = \theta_{23L} = \theta_{23R} \\ &C_{01} = C_{34} \\ &C_{12} = C_{23} \end{aligned} \tag{4.31}$$

The negative electrical lengths will be absorbed by the adjacent electrical lengths of CPW lines [4.12][4.18]. Thereby, the effective electrical lengths of each resonator, combining the resonator and inverter electrical lengths, were able to be calculated and listed in Table 4.12 .

Table 4.12 The electrical lengths of each resonator.

θ_{eff1}(deg)	θ_{eff2}(deg)	θ_{eff3}(deg)
162.8	172.2	162.8

Because of the difference of each resonator's electrical length, the bridge numbers were calculated using the Eq. 4.32 [4.8] as 11, 12, 11,

$$n = \frac{f_{bragg}}{f_o} \frac{l_{elec}\pi}{360} \tag{4.32}$$

where the *Bragg* frequency can be found using the same method discussed in chapter 3.

Three approaches were attempted to find an accurate capacitor value: air-gap capacitor, nitride-gap capacitor and interdigital capacitor. The dimensions of air-gap capacitor and nitride-gap capacitor can be easily calculated by Eq. 3.5. The dimensions of interdigital capacitor can be found either by mathematical calculation [4.21] or by simulations such as *Sonnet*. Fig. 4.10 shows the three different types of capacitors.

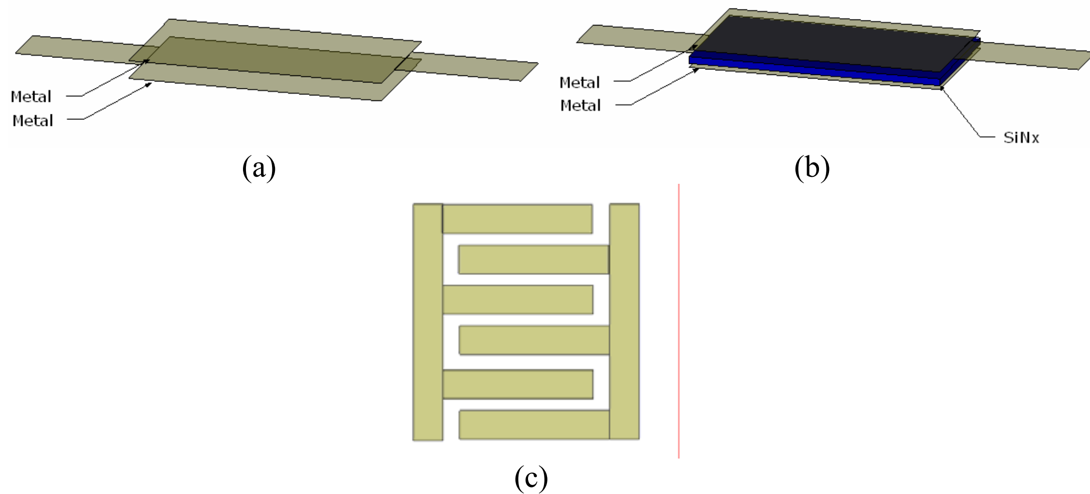


Figure 4.10 Coupling capacitors. (a) Air-gap capacitor. (b) Nitride-gap capacitor. (c) Interdigital capacitor.

4.2 Fabrication Process

4.2.1 Polymer Deposition

Low-resistivity substrates and Kapton films were bonded together using the bonding process described in *section 3.2.1* to form a 250-μm polymer layer on silicon. Fig. 4.11(a) shows this process.

4.2.2 CPW Metal Formation

CPW lines were defined on the polymer layer using the same process described in the *section 3.2.2*. Fig. 4.11(b) shows this CPW metal formation process.

4.2.3 Silicon Nitride Growth

The first silicon nitride layer was deposited on CPW center conductor lines using a same RF sputtering process detailed in the *section 3.2.3*.

This nitride layer functions as an insolating layer between the CPW signal lines and the silicon chrome bias lines. Fig. 4.11(c) shows the silicon nitride on the CPW center conductor.

4.2.4 Silicon Chrome Deposition

The samples were cleaned with an acetone wash. The patterns of bias lines were defined by the same photolithography processes. A silicon chrome (70/30 wt%) layer of 2000Å was grown using a RF sputtering technique. A lift-off process was performed with the same conditions as in the previous step. The high resistivity of the silicon chrome (>1000 Ω-cm) bias line will only allow DC voltage to pass through, and block RF signal from leaking out [4.2][4.8][4.18][4.23]. Fig. 4.11(d) shows the silicon chrome on the silicon nitride layer.

4.2.5 Silicon Nitride Growth

The identical silicon nitride growth process as in the step 2 was performed. This layer of silicon nitride will prevent the MEMS bridges from touching the CPW signal lines. Fig. 4.11(e) shows the silicon nitride on the silicon chrome layer.

4.2.6 Sacrificial Layer Deposition

The samples were washed with acetone before the positive photoresist S1808 was used to form the sacrificial layer. The S1808 was spun on the samples at 3000 rpm for 30 seconds, followed by hotplate baking at 90°C for 80 seconds. The photoresist layer was patterned with the sacrificial photomask by the photolithography. The samples were developed for 15 seconds in MF319 developer. The samples were then heated on a hotplate at 130˚C for 3.5 minutes.

4.2.7 Bridge Formation

Copper bridges of 1.2-μm thickness were defined using the same procedures explained in *section 3.2.5*. Fig. 4.11(g) illustrates this bridge formation process.

4.*2.8 Device Release*

The samples were soaked inside an PR1165 photoresist stripper overnight, followed by alcohol rinsing with agitation. The samples were baked at 110°C for 10 minutes to quickly evaporate the alcohol residues. Fig. 4.11(h) shows a bridge after releasing.

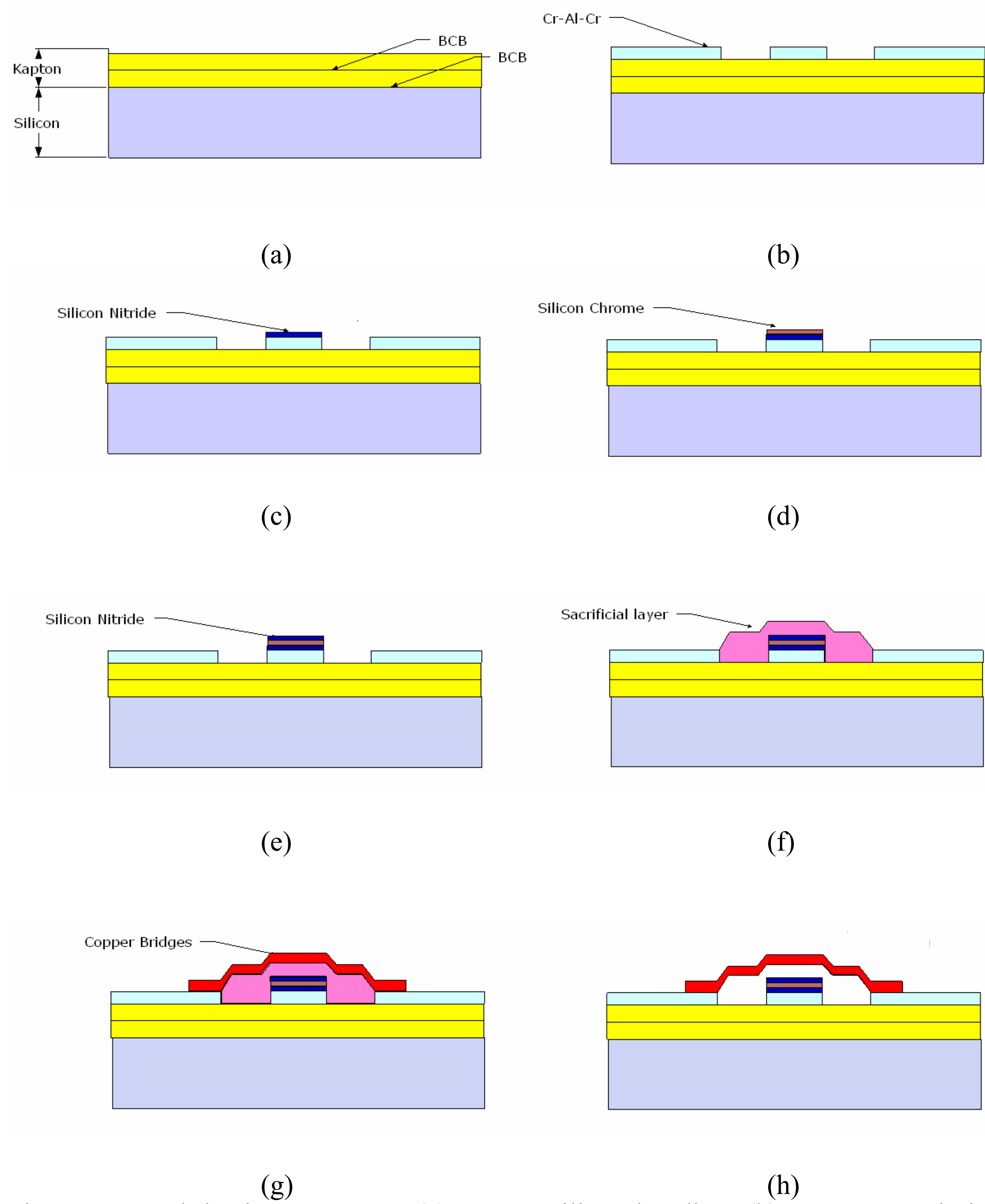


Figure 4.11 Fabrication processes. (a) Kapton-silicon bonding. (b) CPW transmission line formation. (c) Silicon nitride growth. (d) Silicon chrome deposition. (e) Silicon nitride growth. (f) Sacrificial layer deposition. (g) Bridge formation. (h) Device release.

4.3 Simulation Results

4.3.1 Partial-loaded Tunable Filter

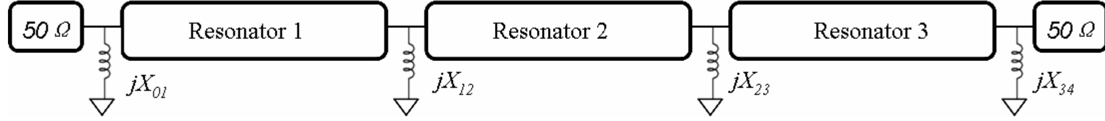


Fig. 4.12 The simulation topology of a 3-pole partial-loaded tunable filter.

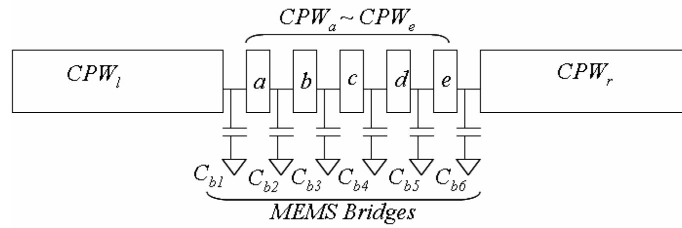


Figure 4.13 The simulation topology of a partial-loaded resonator.

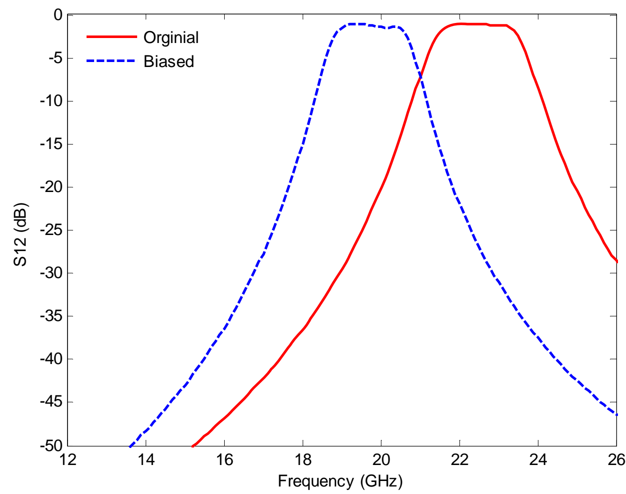
The inductively coupled MEMS tunable filter was simulated by *Agilent ADS* using a lumped-element circuit model, the simulation topology is shown Fig. 4.12. Fig. 4.13 shows that the MEMS resonator is modeled as a series of CPW lines loaded with shunt lumped capacitors to represent MEMS bridge varactors. The CPW line dimensions are identical to those of the actual filter and shown in the Table 4.13.

Table 4.13 The simulation parameters of 3-pole partial-loaded tunable filter.

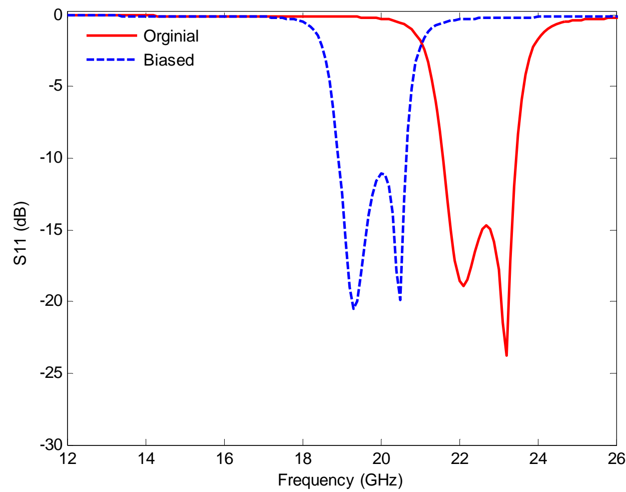
	Resonator 1~3		Resonator 1	Resonator 2	Resonator 3
	W (μm)	S (μm)	L (μm)	L (μm)	L (μm)
CPW_L	160	80	275	500	500
CPW_R			500	500	275
CPW_a~CPW_e			70		

Assuming a bridge height of 1.1 μm and using the bridge parameters given in Table 4.2, the calculated MEMS bridge capacitance is 64 fF using Eq. 3.5. The tuning

range is limited by the pull-in condition where the maximum tunable bridge height is one third. By applying this notion, the upper limit of the MEMS bridge capacitance is 85 fF. Therefore, the tuning range was simulated by setting the bridge capacitance minimum and maximum values to 64 fF and 85 fF, respectively.



(a)



(b)

Figure 4.14 Simulation results of a partial-loaded tunable filter. (a) $S_{12.}$ and (b) S_{11}.

The simulation indicates the center pass-band frequency is 22.5 GHz and 19.5GHz for the unbiased and near pull-in bias conditions. The 3 GHz tunable range accounts near 13% percent of the unbiased center frequency. The insertion losses for both pass bands are less than 1 dB. The 3-dB bandwidth is 11%.

4.3.2 Even-loaded Tunable Filter

The even-loaded tunable filter was also simulated using a lumped model by *Agilent ADS*, the simulation topology is shown as Fig. 4.15. Fig. 4.16 shows that the even-loaded resonator is modeled as a series of CPW lines loaded with evenly distributed shunt capacitors between two adjacent CPW lines. The dimensions of CPW lines are identical to the actual device and shown in the Table 4.14.

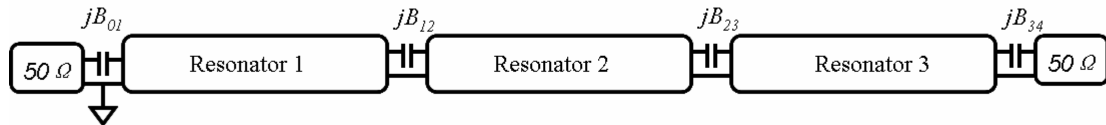


Figure 4.15 The simulation topology of a 3-pole even-loaded tunable filter.

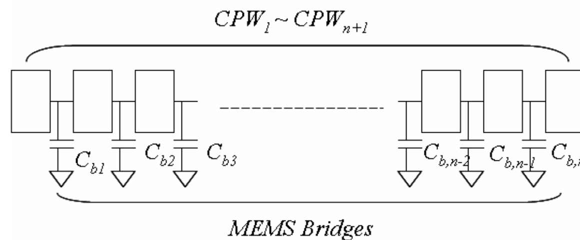
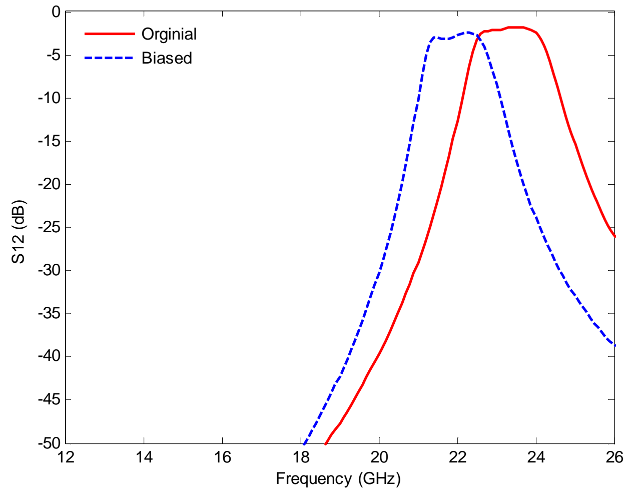


Figure 4.16 The simulation topology of an even-loaded resonator.

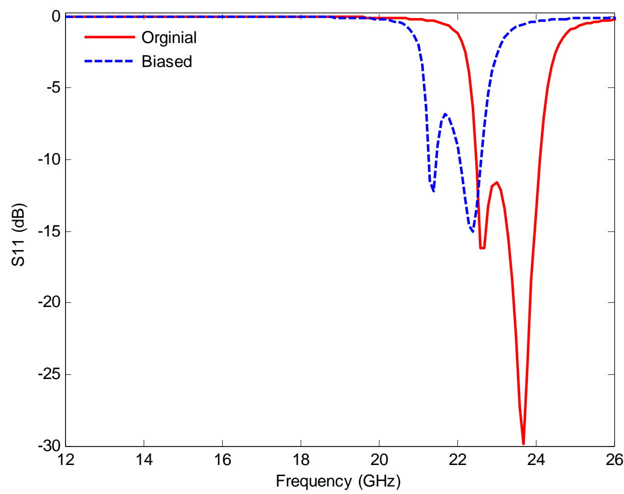
Table 4.14 The simulation parameters of 3-pole even-loaded tunable filter.

	Resonator 1~3			Resonator 1	Resonator 2	Resonator 3
	W (μm)	*S* (μm)	*L* (μm)	*Bridge # n*	*Bridge # n*	*Bridge # n*
$CPW_1 \sim CPW_{n+1}$	*150*	*75*	*230*	*11*	*12*	*11*

Table 4.14 shows that resonator 1, 2 and 3 has 11, 12, 11 MEMS bridge capacitors, respectively. Assuming a bridge height of 2.5μm and using the bridge parameters given in Table 4.5, the calculated value of an unbiased MEMS bridge capacitance is 13 fF using Eq. 3.5. The tuning range is limited by the pull-in condition where the maximum tunable bridge height is one third. By applying this notion, the upper limit of the MEMS bridge capacitance is 17 fF. The tuning arrange can be simulated by fixing the bridge capacitance minimum and maximum values to 13 fF and 17 fF, respectively.



(a)



(b)

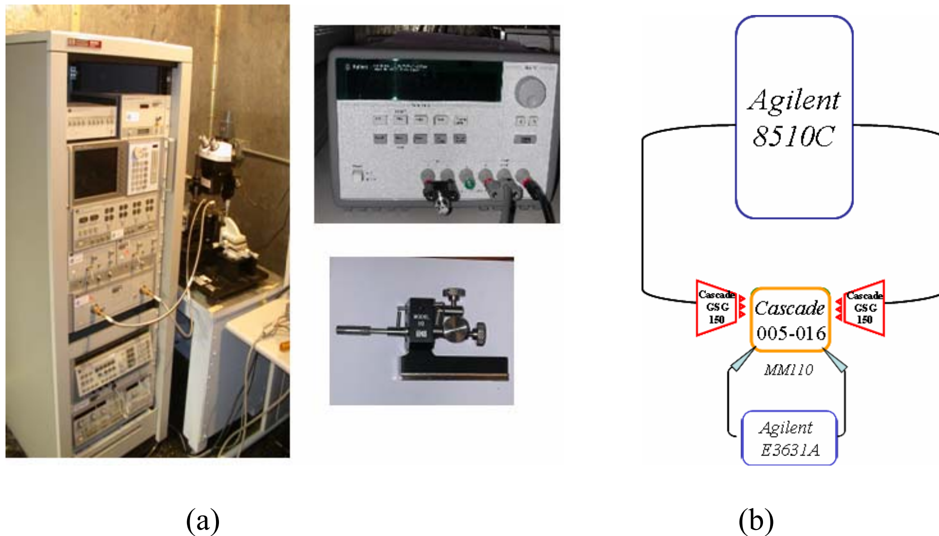
Figure 4.17 Simulation result of the even-loaded tunable filter. (a) S_{12} and (b) S_{11}.

The insertion loss at zero-bias voltage is less than 2.5 dB and the return loss is less than 10 dB for the pass band. Altering bridge capacitances gives a 9%, or 2 GHz, tuning range when biased with a near pull-in condition voltage. The biased return loss is greater than unbiased one. This is because the biased device introduced a larger unmatched impedance level. The 3-dB bandwidth is 9%. The bandwidth could be

improved by increasing the coupling capacitance. However, such an effort proved to be a difficult task due to the space limit and fabrication restraint. Thus, the capacitively coupled filters are primarily used for narrow-band applications [4.22].

4.4 Measurement Results

The devices were characterized from DC to 26 GHz with two *Cascade Microtech Infinity GSG-150* probes connecting to an *Agilent 8510c* network analyzer. The scattering parameter measurements were calibrated by a *Cascade Microtech ISS-005-016* impedance standard substrate. The actuating voltages were applied on the silicon chrome bias lines by an *Agilent E3831A* DC source through *MM110* micro-manipulators.



(a) (b)

Figure 4.18 (a) *Agilent* network analyzer, DC source and probe. (b) Testing setup.

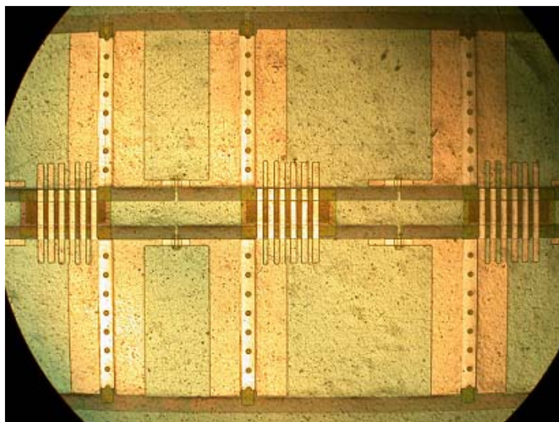
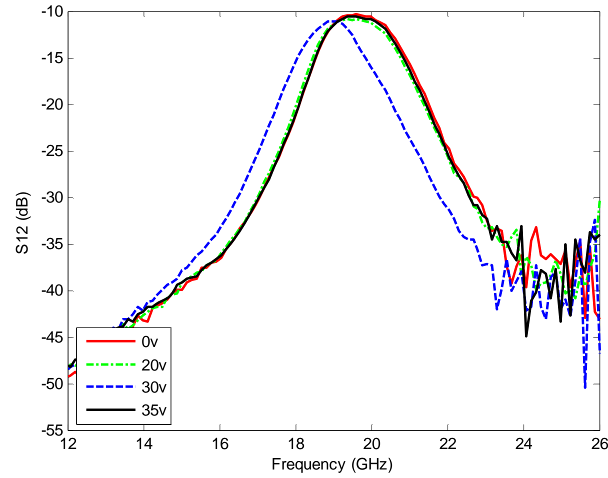
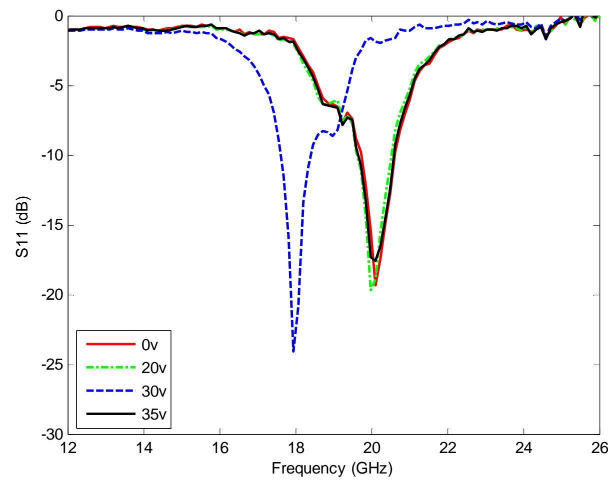


Figure 4.19 A 3-pole partial-loaded tunable filter.

4.4.1 Partial-loaded Tunable Filter



(a)



(b)

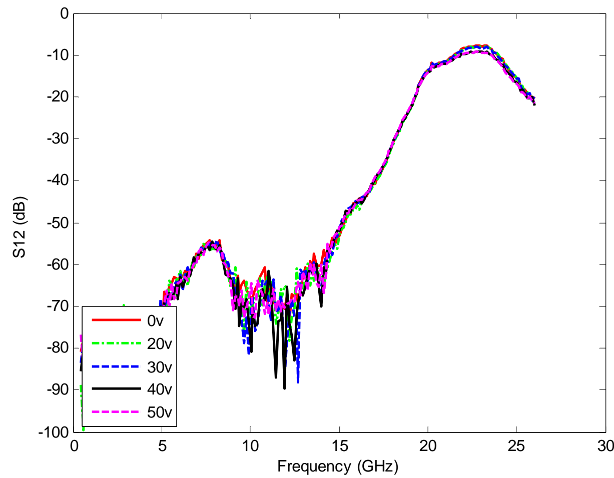
Figure 4.20 Measurement results of the partial-loaded tunable filter. (a) S_{12} and (b) S_{11}.

The Fig. 4.20 shows the S_{12} parameter and the S_{11} parameter of an partial-loaded tunable filter. The device dimensions are same as that of the *ADS* simulation. The *K* inverter dimension is the simulated value by *Sonnet*. From the S_{12} parameter plot (Fig. 4.20(a)), the tuning range is about 1 GHz, from 19 GHz to 20 GHz. However, the

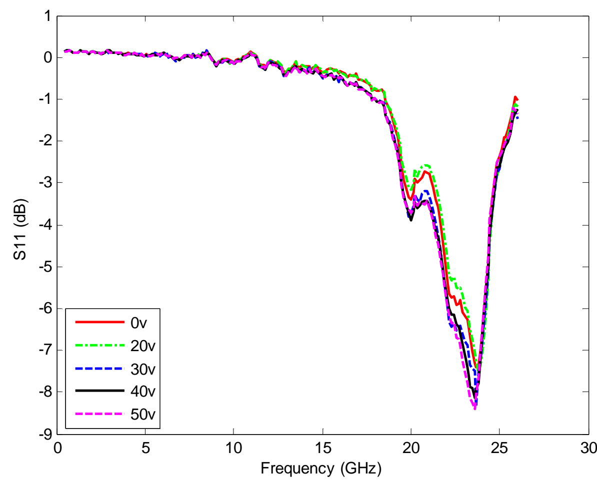
parameter S_{11}, Fig. 4.20(b), indicates a 2-GHz tuning range. The insertion loss is about 10 dB at the pass band.

Interestingly, at 20-V bias voltage, there is barely any frequency shift from the zero-biased state. Biased with a 30-V voltage, the filter shows a much larger shift towards the lower frequency. However, when further biased the filter with a 35-V voltage, the filter goes back to its unbiased shape. The reason will be explained in the next section.

4.4.2 Even-loaded Tunable Filter



(a)



(b)

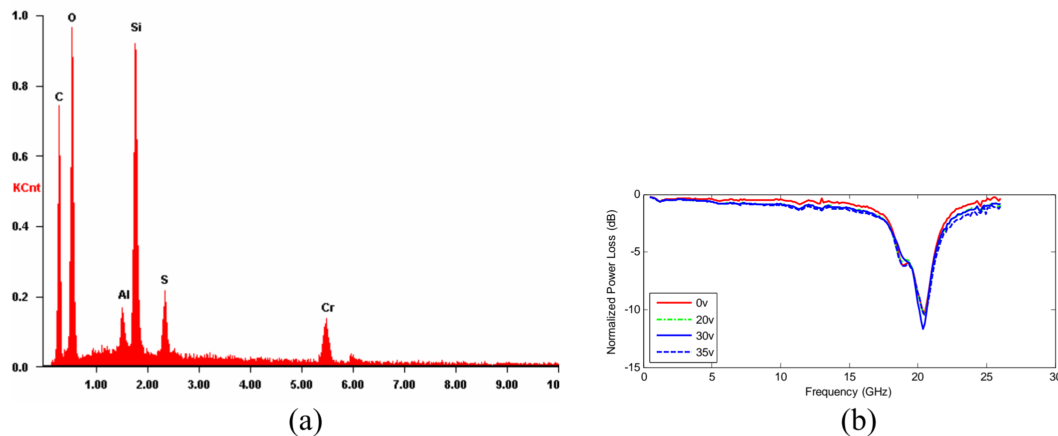
Figure 4.21 Measurement results of the even-loaded tunable filter. (a) S_{12} and (b) S_{11}.

The measurement of the even-loaded open-ended tunable filter fails to display any tunability and the insertion loss is about 10 dB. However, the insertion loss and return loss both display a bandpass filter characteristics.

4.5 Failure Mechanism

Though the partial-loaded filter displays a tunability, it still has a high return loss of 10 dB and the tuning range is much lower compared to the simulated result of 3 GHz. The mechanisms leading to these failure are due to:

1) The silicon chrome was deposited using the RF sputtering process. The *EDAX* element analysis indicated there were aluminum, oxygen and sulfur in the sputtered SrCr layer as shown in Fig. 4.22(a). Such unwanted elements, especially aluminum, introduced a signal leak which resulted in a high insertion loss at the passband (Fig. 20(a)). The signal leak was also confirmed by normalized power loss analysis. For a lossless network, the summation of the normalized power is 1 or 0 dB. Fig. 22(b) indicates that the power loss of the partial-loaded filter is 1 dB in vicinity of the passband.



(a) (b)

Figure 4.22 (a) The SiCr element analysis. (b)The normalized power.

2) There were other elements, aluminum, copper, ferrum, sulfur and oxygen, in the silicon nitride layer, as shown Fig.4.23(a). The aluminum, ferrum and oxygen were

contributed from the RF sputtering process. The copper residue was from the copper etching process. The sulfur was the leftover from the RR2 photoresist remover. These materials, especially the metal materials, degraded the Si_3N_4 insulating ability. Therefore, when the bias voltage was high enough, the Si_3N_4 layer would be broken through and formed a short circuit. It is evident that when the applied voltage reached 35 V, the filter's frequency behavior was identical to its 0-V biased behavior (Fig. 4.20(a) and (b)), which implies the Si_3N_4 was broken down.

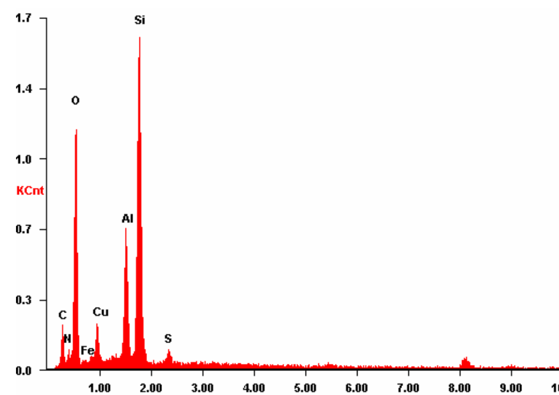


Figure 4.23 The Si_3N_4 element analysis.

The RF sputtering does not produce a uniform thickness of Si_3N_4 either. Fig. 4.24(a) and (b) displayed two silicon nitride samples which were deposited together by the same RF sputtering process and were in the vicinity on the same wafer. The left sample was nearly double the thickness of the right one (0.5 μm vs. 0.3 μm). The thickness difference also contributed the voltage break-through to some degree.

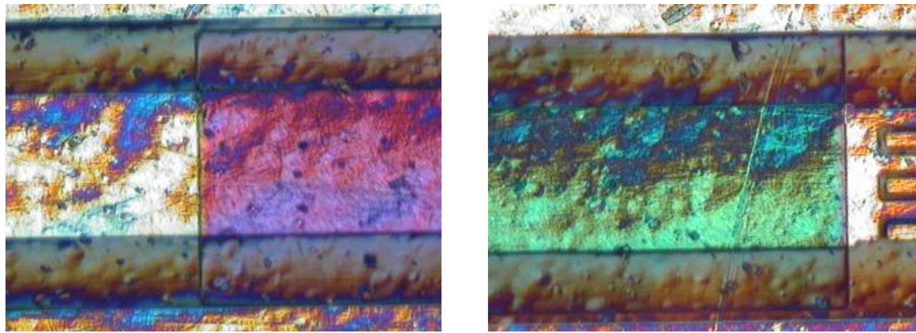


Figure 4.24 Nitride thickness variation. (a) A thick nitride and (b) a thin nitride.

3) Neither *Sonnet* simulation nor empirical computation gave an accurate dimension for a given inductance value. Hence, the *K* inverters did not have the precise coupling mechanism. To solve this problem, trial and error method needs to be employed for improvement of the filter design.

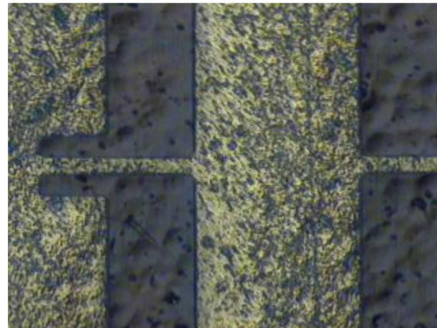


Figure 4.25 A ribbon straight inductor.

4) The MEMS bridge height differed from the desired values. Unlike the phase shifter, the requirement for the bridge height accuracy of tunable filters is much higher. The spinning variation, developing time, baking temperature difference and excess thermal evaporation heating all contributed to the bridge height variation. Thereby, the

characteristic impedance Z_2, electrical length θ_2, effective dielectric constant ε_{eff2} departed from the designed values and a high insertion loss was induced.

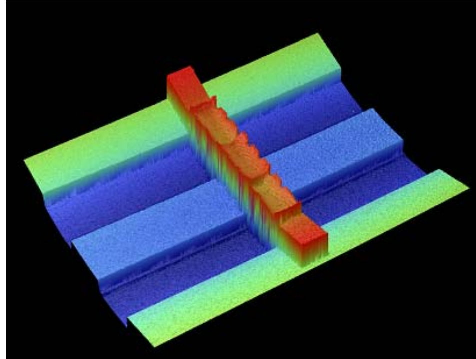


Figure 4.26 A 3-D optical image by a *Veeco* profiler.

5) The bridge width was smaller than 50 μm due to the over etching. The copper etching process is monitored by naked eyes. Thus, the human error and etching time variation between two processes were inevitable. An inadequate MEMS bridge width results in a high insertion loss.

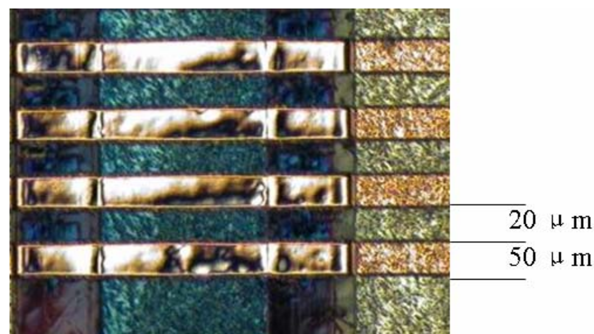


Figure 4.27 Over etched MEMS bridges.

6) The surface stress increased the bias voltage. Hence before the MEMS bridge reached the pull-in condition, the silicon nitride was broken down by a high bias voltage.

Therefore the tuning range was further limited. Fig. 4.28 shows that a tilted-up broken bridge which implies the existence of the surface stress. This tensile stress was also consistent with the report [4.5].

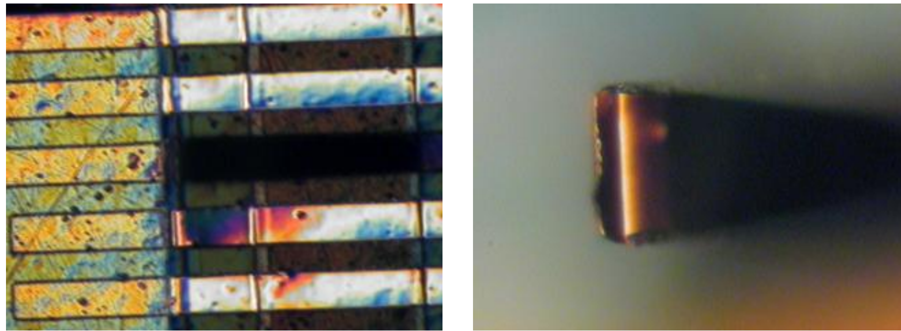


Figure 4.28 (a) A broken bridge within good bridges. (b) A close look of the broken bridge.

The even-loaded tunable filter suffered from the same problems of the partial-loaded tunable filter except the inductor inaccuracy. The coupling capacitors with accurate values are very difficult to fabricate. Though three approaches were attempted: air-gap capacitor, nitride-gap capacitor and interdigital capacitor, unfortunately, each of these approaches presents its own drawbacks

1) Air-gap capacitor was formed by the same process with the MEMS bridge, thus the air-gap height was not able to be precisely controlled for the same reasons of MEMS bridge height variation.

2) The silicon nitride, of the nitride-gap capacitor, does not have a uniform thickness and good quality due to the RF sputtering problem discussed early this section. It created a short circuit under a high voltage.

3) Interdigital capacitor has micron-scaled "fingers" due to capacitive values (40 and 10 fF). Hence the small structures presented a huge fabrication difficulty. Fig. 4.29(a) shows a partially broken interdigital capacitor; Fig. 4.29(b) shows an interdigital capacitor that was completely torn apart by the liftoff process.

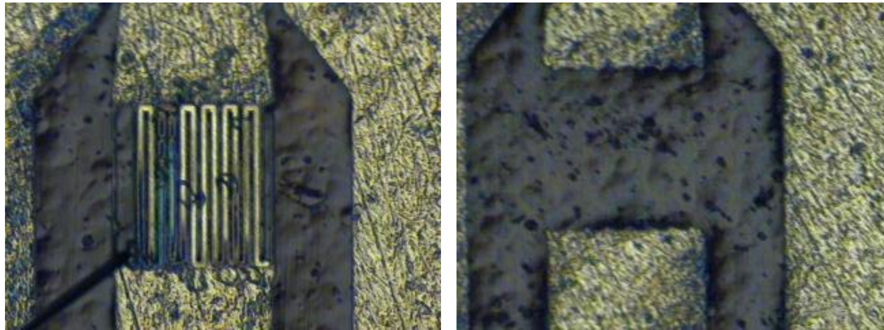


Figure 4.29 (a) A broken coupling capacitor. (b) A torn-away coupling capacitor

4.6 Conclusions

In this chapter, CMOS-compatible RF MEMS tunable filters were investigated. Two 125-μm Kapton films were bonded with silicon to prevent the RF signal loss and realize the CMOS compatibility. Two types of RF tunable filters were investigated – partial-loaded short-ended filter and even-loaded open-ended filter. Design methodology, fabrication process, simulation and measurement results were discussed in details. The measurement results of the partial-loaded short-ended tunable filter displayed a 2-GHz tuning range and a 10-dB insertion loss. The even-loaded open-ended tunable filter displayed a filtering ability, however, failed to demonstrate any tunability. Failure mechanisms were analyzed for the future improvements. The low tuning range and high insertion loss were largely contributed from the low quality

silicon chrome and silicon nitride where impurities degraded film qualities. Both tunable filters were also simulated using *Agilent ADS*. The simulation results demonstrated much more promising results for both tunability (3 GHz) and insertion loss (1 dB). Therefore, the simulation results will be used as a reference for the future improvement.

CHAPTER 5

FUTURE WORKS

5.1 RF MEMS Devices with Digital Control

Though polymer RF MEMS devices show great performance, electrical and thermal noise may introduce unwanted switching especially in the case of low-voltage bias applications. On the other hand, MEMS bridges with digital control only have two, up and down, states as shown in Fig. 5.1. If a sufficient voltage gap between the up and down states is designed, the MEMS devices will achieve a good immunity to electrical and thermal noise.

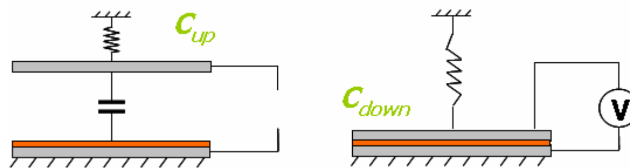


Figure 5.1 Two states of a MEMS capacitor.

Furthermore, each switch or varactor is controlled independently through digital biasing. It gives flexible control profiles. Thereby RF MEMS devices gain better precision and wider frequency range through digital controls [5.1][5.2]. Fig. 5.2 shows a tunable filter loaded with digitally controlled MEMS bridges.

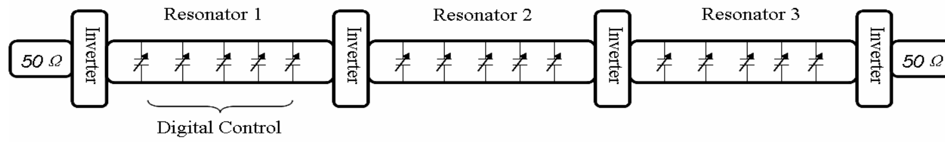


Figure 5.2 A digitally controlled tunable filter.

5.2 Impedance Tuner

An impedance tuner produces different impedance levels for the following purposes: maximizing the power delivery, improving the signal-to-noise ratio, and reducing amplitude and phase errors [5.3]. RF MEMS realization of an impedance tuner uses a distributed transmission line [5.4] or a stub structure loaded with MEMS switches [5.5]-[5.7]. Various impedance values are generated by independently biasing each MEMS switch. This method exhibits an easy tunability and superb Smith Chart coverage [5.4]-[5.9]. However, it faces the same IC incompatibility issue due to the requirement of quartz substrates.

The polymer-silicon approach developed in the previous chapters is virtually applicable to all situations where CMOS-grade silicon is not allowed to directly build RF MEMS circuitry. Via carefully selecting the polymer type and thickness, the electromagnetic field can be contained within the polymer film resulting in a very low transmission loss. Applying this polymer-silicon method to the impedance tuner, the impedance tuner will be accomplished with CMOS compatibility and cost effectiveness. Fig. 5.3(a) shows a distributed MEMS transmission line (DMTL) impedance tuner on a polymer-silicon substrate. Fig. 5.3(b) shows the simulation results using *Agilent ADS* software. Fig. 5.3(c) shows a measured result of a DMTL impedance tuner on glass

substrate [5.4]. Fig. 5.4(d-f) shows topologies of single-stub, double-stub and triple-stub MEMS impedance tuners [5.5][5.6].

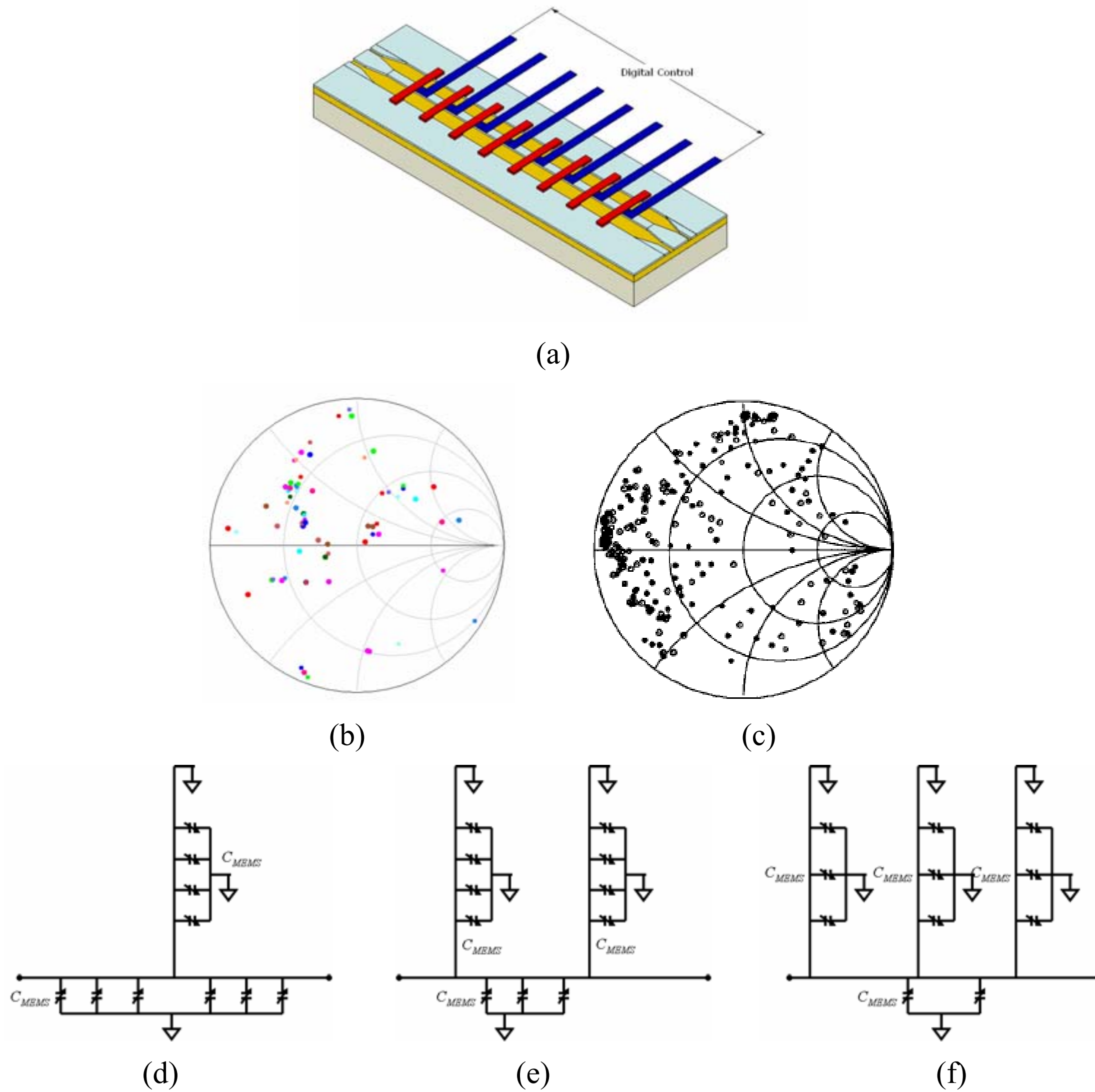


Figure 5.3 (a) A DMTL impedance tuner on polymer-silicon. (b) A simulation result at 26 GHz. (c) A measurement result at 26.2 GHz. (d) Single-stub impedance tuner topology. (e) Double-stub impedance tuner topology. (f) Triple-stub impedance tuner topology.

5.3 Plastic RF MEMS Packaging

Many RF MEMS devices need to be able to operate in full-weather conditions. The micro-scale devices are often susceptible to humidity which creates surface stress and alters MEMS bridge bias voltages. Eventually it may introduce false operations. Eq. 5.1-5.2 and Fig. 5.4 shows that a surface stress residue σ alters the spring constant, k, of a bridge and consequently changes the pull-in condition voltage, V_p. A special packaging method is necessary to avoid these issues. Unlike traditional packaging techniques, RF MEMS packaging has a unique requirement for low signal attenuation. Of course, commercial success is always contingent on the material and fabrication expense. Consequently, these special needs present a multitude of challenges for RF MEMS device packaging.

$$k = \frac{32Et^3w}{L^3} + \frac{8\sigma(1-\upsilon)tw}{L} \quad (5.1)$$

$$V_p = \sqrt{\frac{8k}{27\varepsilon_o Ww} d_o^3} \ (V) \quad (5.2)$$

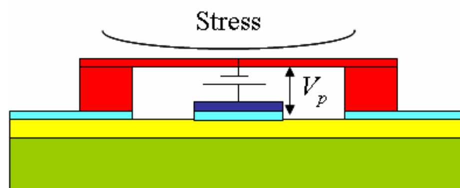


Figure 5.4 A surface stress changing the pull-in voltage.

Having known the benefits of the excellent RF performance, fabrication ease and low material cost, plastic will be the primary candidate for the packaging material. Creating a plastic hermetic chamber to enclose each RF MEMS component is the initial step of this research work. Hot embossing technique developed at UT Arlington and UC

Berkeley [5.10][5.11] will be used for this purpose. The plastic chamber and RF MEMS device then will be bonded together by a polymer bonding process [5.12]-[5.14]. Next, liquid glass will be applied on the device. The liquid glass is to seal the opening caused by the metal thickness. In the final step, a dry etching process is used to etch off the glass at two ends of the device. Thus metal pads are exposed for the connection purpose. Fig. 5.5 demonstrates this RF MEMS packaging technique. Fig. 5.6 illustrates a opening before and after liquid glass application.

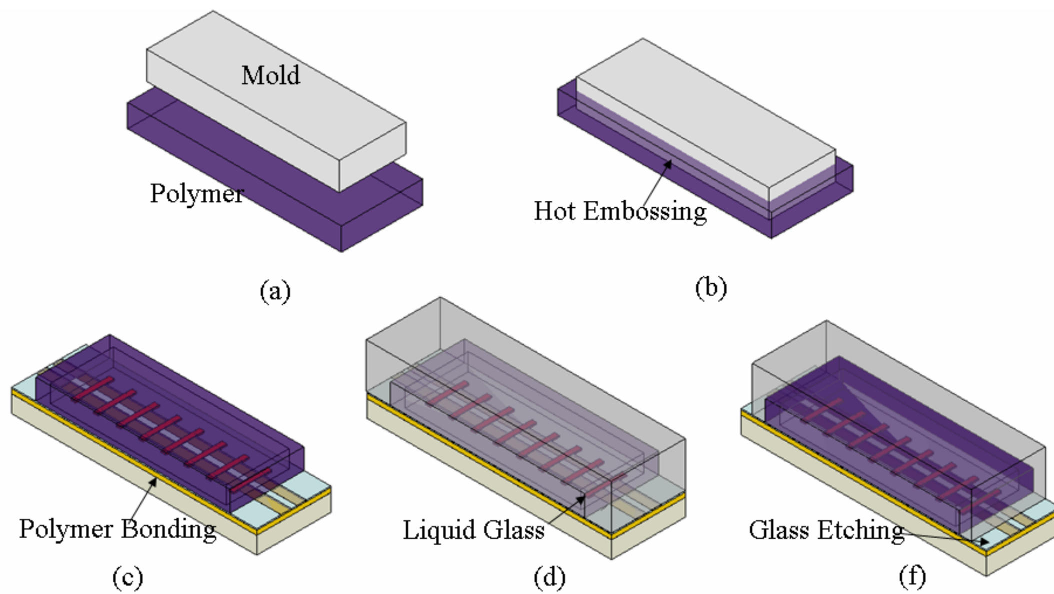
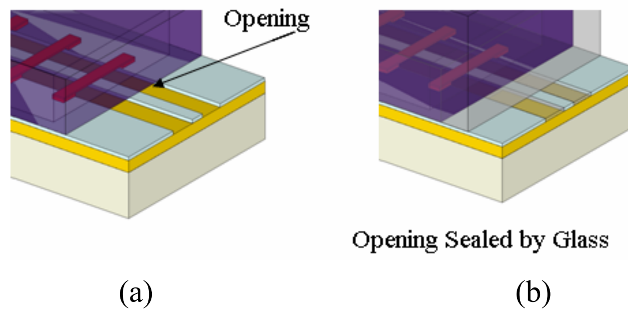


Figure 5.5 (a) A metal mold and polymer. (b) Hot embossing polymer. (c) Bolding polymer chamber with RF MEMS device. (d) Liquid glass application. (e) Glass etching process.



(a) (b)

Fig. 5.6 (a) An opening before liquid glass application. (b) An opening sealed after liquid glass application.

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