A HIGHLY LINEAR VOLTAGE CONTROLLED OSCILLATOR WITH LOW POWER DISSIPATION

by

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ABSTRACT

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A voltage-controlled oscillator using the 90 nm CMOS technology has been presented with the total power dissipation of 14 mW, which provides 1.7 mW of total output power. It has highly linear voltage to frequency transformation, with only 4.85% of maximum error. This VCO works in the long range from 5.1 to 9.099 GHz. The controlling voltage varies from 0 to 0.5 volts, The oscillator is powered by a 1 volt power supply.

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LIST OF ACRONYMS AND ABBREVIATIONS

CMOS – Complementary Metal Oxide Semiconductor

ASIC – Application Specific Integrated Circuit

MOSFET- Metal Oxide Semiconductor Field Effect Transistor

VCO- Voltage Controlled Oscillator

PLL- Phase Locked Loop

ADC- Analog to Digital Converter

CHAPTER 1

INTRODUCTION

1.1 Introduction

The invention of the first transistor in 1965 has brought the whole world an age of integrated circuits. People are now living in a world, which is surrounded by the all kinds of the integrated circuits. Radios, telephones, TVs, computers and other electronic devices all contain integrated circuits (ICs). The development of integrated circuits has been accelerated due to the great need of them in people's daily life. The Integrated Circuits have been gone through rapid transformations from the initial days of the triode tubes and the Bipolar Junction Transistors (BJTs) most of the integrated circuit chips now employ Complementary Metal Oxide Semiconductors (CMOS). The CMOS devices have low flicker noise (at high frequency) and consume low static power thereby giving it high efficiency. This becomes very crucial for battery-operated devices. The CMOS device also allows compact design of analog and digital chips. Since transistor's sizes are shrinking rapidly. This makes CMOS technology the most widely used technology in VLSI (Very-large-scale integration) chips.

The Voltage-Controlled Oscillators (VCOs) are fundamental to all the synchronous systems since they provide the reference signal. A steady reference signal is very important for Phase Locked Loops (PLLs) to synchronize career recovery in wired and wireless communication systems, both the analog and the digital. The VCOs are also used in microprocessors, where a system clock regulates the calculations and data transfers. The performance of an oscillator can be measured by several specifications, such as the oscillation frequency range, sensitivity, jitter noise, power dissipation, and circuit space.

The most common types of CMOS oscillators on the market are ring oscillators and LC oscillators. The ring oscillators have wide tuning range, low sensitivity to process variations and

compact size. Because they can be fully integrated, ring oscillators have been widely used in various applications such as semiconductor test structures, clock recovery, and data conversion. The LC oscillators, on the other hand, have less noise compared to the ring oscillators for the same power dissipation, and therefore have been dominant in synthesizers. However, as "Go Wireless" has become a trend for consumer electronics and caused a boom of demand for high performance, low cost, fully integrated transceivers, the interest in the VCOs based on the ring oscillators has grown significantly. The VCOs and synthesizers based on the ring oscillators are particularly attractive for the low-power communication systems with non-demanding phase noise requirements, such as Bluetooth and wireless sensor networks.

This work allows wide band frequency generation of 5.1 to 9.1 GHz which is 80% of the tuning range compared to circuit [15]. This latter work provides 4.5 GHz to 7.1 GHz thus giving about 45% tuning range. The circuit in [15] also dissipates 14 mW from a 1.6 V supply in the VCO core. The present work consumes only 1.65 mW of power in the VCO core. The work described in [16] uses artificial transmission lines, but the frequency range is small (3.1 – 4.85 GHz). Also the power consumption in [16] is higher (38 mW) as compared to the present work (22 mW) in the whole VCO design. Use of artificial transmission lines also increases the size, as compared to the ring oscillator and active filters as used in this work.

The work described in [17] uses the ring oscillator based on the 90 nm technology and consumes 6.3 mW power (in the VCO core) with a 1 volt power supply. The size of this VCO is also comparable with the present work, but power dissipation is higher in the VCO core.

A dual delay ring VCO [18] based on the 90 nm technology, generates 0.2 GHz to 6.2 GHz with 1.2 supply voltage, consumes 6.5 mW power at the VCO core, has good design but this well designed VCO still has a high tuning error as compared to this work which is only 4.85%.

In this work use of the inductors and capacitors have been avoided to match the input impedance of the load and the output impedance of the circuit. The size of the inductor is sometimes prohibitively large for a cheap but the high frequency requirement application.

A novel technique has been used in this work for impedance matching in this work. This technique uses a voltage to control the VCO frequency and the gain. With the help of this method 4 GHz range of frequency has been matched with a nominal power dissipation of 22 mW The VCO in this work uses the 90 nm CMOS technology and generates 5.1 to 9.099 GHz range of the frequency.

The frequency response with respect to the control voltage of 0 volts to 0.5 volts is exceptionally linear. The tuning error is only 4.85% (maximum). The VCO gain (K_{vco}) is 8.744 GHz/V and the average output power (AC power) delivered to the load is 1.4 mW. The output voltage swing is constant at 0.7 volts.

1.2 Thesis Outline

Chapter 2 explains a brief history of CMOS and the use of the voltage controlled oscillator for signal generation and clock generation. In chapter 3 ring oscillators have been discussed in detail with a closer look at the single ended and the differential ended topology. Chapter 4 focuses on design of a VCO differential delay cell, which is discussed in detail with the calculations of transistor measurements associated with this work. In chapter 5 simulation results and implication of those results have been discussed. Chapter 6 concludes work with a glimpse of future work which can be useful to make this VCO perform better.

CHAPTER 2

MOSFETS AND VCO

2.1 The MOSFET Devices

Use of the MOSFETs (Metal Oxide Semiconductor Silicon Field Effect Transistors) for circuit design has caused a revolution in the field of integrated circuits, enabling production of very small circuits with robust performance. [7]

2.1.1 The *CMOS Technology*

A CMOS (Complementary Metal Oxide Semiconductor) is a combination of NMOS (n-type Metal Oxide Semiconductor) and PMOS (p-type Metal Oxide Semiconductor) in the same chip. The digital CMOS circuits dissipate smaller power than digital Bipolar Junction Transistor (BJT) circuits. A CMOS digital circuit consumes very little power when off or on, and only consumes power during switching. Hence stand by power dissipation is very small. Due to the small size of CMOS ICs, a large number of transistors can be placed on a chip. This reduces costs considerably. A typical NMOS cross section is shown in figure 2.1.

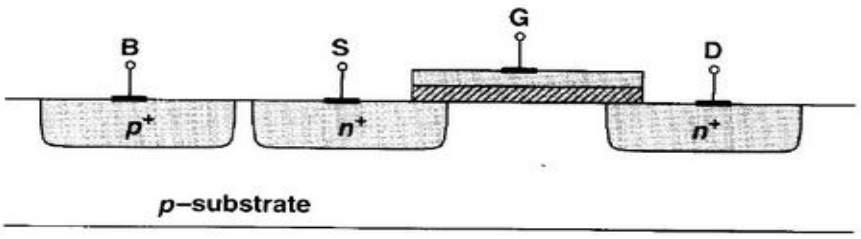

Figure 2.1 A MOSFET Device's Cross-section [7]

Figure 2.1 is the cross-section of a typical NMOS transistor, which is fabricated on a p-substrate. The source and the drain regions are heavily doped with n-type doping. A conductive polysilicon layer serves as the gate (shown as terminal "G"). The distance between the source (denoted by terminal "S") and the drain (denoted by terminal "D") is called the Length, usually

denoted by “L”. During the fabrication process, stray diffusion (side-diffusion) of the dopant causes a reduction in length between the source and the drain regions (described in figure2.2). If L_D is the amount of side diffusion, then the effective length (L_{eff}) would be [7]

$$L_{eff} = L - 2L_D \tag{2.1}$$

In succeeding chapters L_{eff} simply regarded as L.

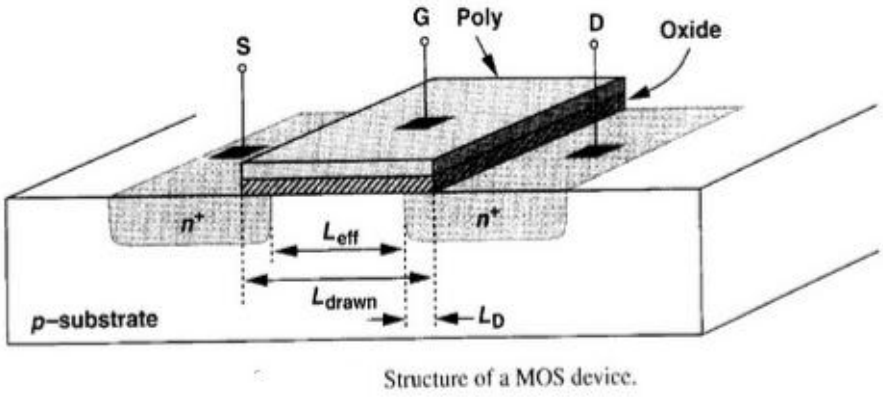

Figure 2.2 3-D view for a MOSFET Device cross-section [7]

The NMOS and the PMOS can be placed in the same chip. These type of chips are called Complementary MOSFETs (CMOS). A CMOS chip is shown in figure 2.3. The PMOS chip is an exact replica of the NMOS version with inverted regions, i.e. replacing heavily doped n-regions with heavily doped p-regions and substituting a p-substrate with an n-substrate. For PMOS the N-well serves as the substrate in the CMOS chip.

In the NMOS transistors current flows from drain to source, while in the PMOS transistors current flows from source to drain. For proper functioning of CMOS devices, it is necessary to avoid flow of current through drain to substrate or source to substrate. An n-type substrate is used for PMOS device, and an p-type substrate is used for NMOS device. It is possible to create a reverse biased connection between source and drain to substrate. Hence, in the NMOS

transistor, the substrate is connected to the lowest potential, while in the PMOS substrate it is connected to the highest potential. Figure 2.4 shows different symbols for an NMOS and a PMOS transistor. [7]

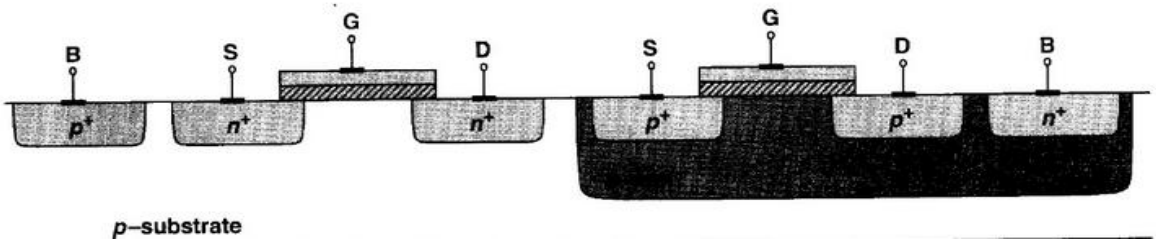

Figure 2.3 The Complementary MOSFET (PMOS and NMOS in same chip) [7]

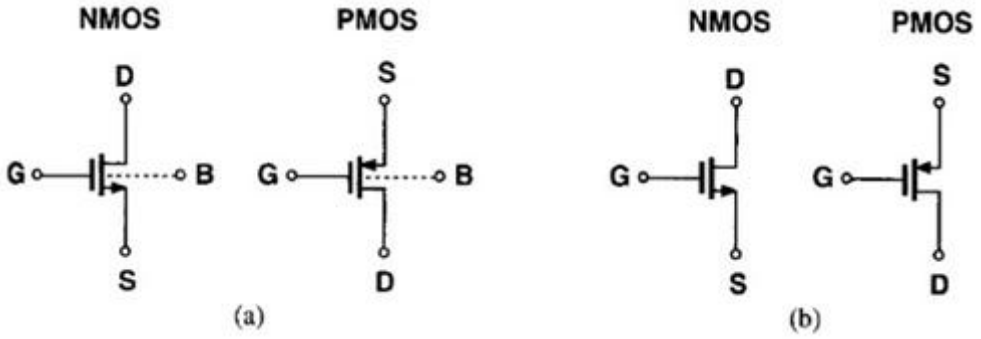

Figure 2.4 (a) A PMOS and an NMOS with bulk connections (b) without bulk connection [7]

2.1.2 *The V-I Characteristics of the CMOS Devices*

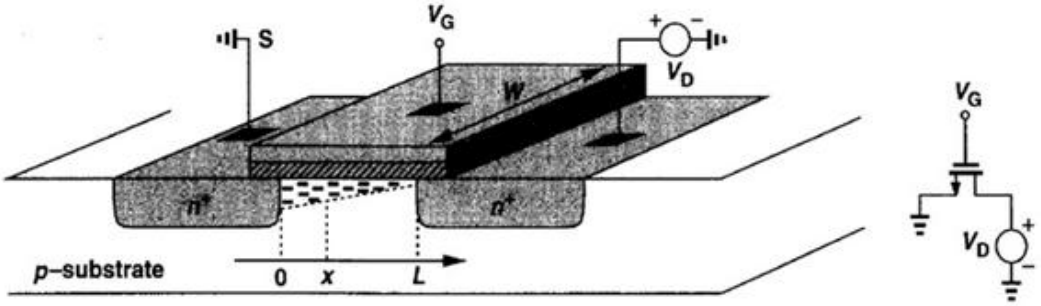

Figure 2.5 Biasing of a CMOS device [7]

Figure 2.5 shows a biased NMOS transistor, whose source is connected to ground and

drain voltage, V_{DS}. is varied for a fixed gate to source voltage (V_{GS}). Drain current (I_D) which flows through the channel from drain to source is given by equation (2.2). [7]

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{2.2}$$

This is the maximum current that can flow through the channel for a given V_{DS} and is called the saturation current. The NMOS device is in the saturation region when [7]

$$V_{DS} \geq V_{GS} - V_{TH} \quad \text{Saturation condition} \tag{2.3}$$

In equation (2.3), V_{TH} is the threshold voltage. If V_{GS} is smaller than the V_{TH} no conduction is possible through channel from drain to source. Channel conduction requires [7]

$$V_{GS} \geq V_{TH} \tag{2.4}$$

According to equations (2.3) and (2.4), the channel starts conducting when situation (2.4) is fulfilled and the channel reaches saturation if (2.3) is true. The difference between the gate voltage and the threshold voltage is called the over-drive voltage (V_{ov}). If the gate potential drops below the threshold voltage, the device is in the cut-off region. [7]

$$V_{GS} < V_{TH} \quad \text{Cut-off region condition} \tag{2.5}$$

For the triode region, drain current is given by equation (2.6). [7]

$$I_D = \mu_n C_{ox}\frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{\ 2}] \tag{2.6}$$

which occurs when $V_{DS} < V_{GS} - V_{TH}$.

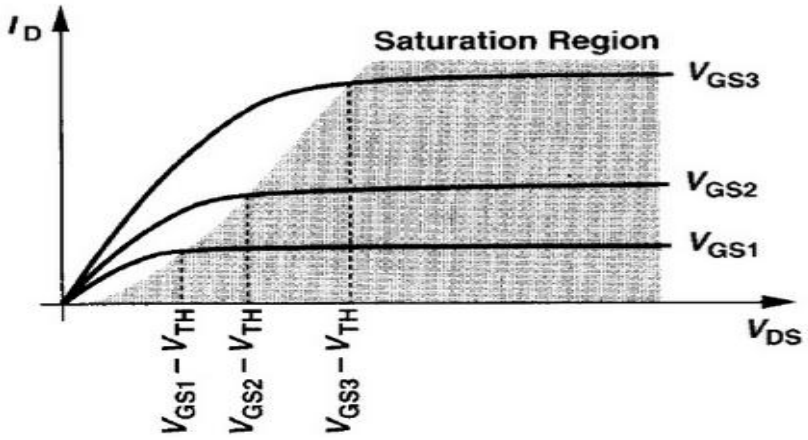

Figure 2.6 Voltage current characteristics [7]

2.1.3 The 90 nm CMOS Technology [1] [8]

A lot of effort been made to improve the CMOS technology, such as reduction in channel length L. Today channel length is reduced down to 22 nm. The small gate length CMOS devices are referred to as deep submicron technology ICs. The deep submicron CMOS designs follow different rules than the long channel CMOS circuits (with channel length above 1 micron). [8]

Previous equations from (2.1) to (2.6) are applicable only for the long channel devices, but for the deep submicron technologies, a different set of equations are required. In the short channel devices, the horizontal and the vertical fields start affecting the velocity of the carriers. The horizontal field increases the velocity of carriers, and when carrier speed reaches speed limit of the carrier in silicon, the saturation condition occurs. The horizontal field at which velocity of carriers saturate, is called the critical field E_c. [8]

For the electrons and the holes, the critical fields are the same and independent of doping level. Equation (2.7) shows critical fields for the NMOS and the PMOS device. [8]

$$E_{cn} = E_{cp} = 8 \cdot 10^6 \ V/m \tag{2.7}$$

If the horizontal field is given by E_y, and $V_{D_{sat}}$ is the drain voltage at which the horizontal field (E_y)

is greater then the critical field (E_c), then the saturation region current is given by the following equation. [8]

$$I_{DS} = W v_{sat} C_{OX} (V_{GS} - V_{TH})(1 + \lambda V_{D_{sat}}) \quad (2.8)$$

where [8]

$$V_{D_{sat}} = \frac{[(V_{GS} - V_{TH}) E_c L]}{[(V_{GS} - V_{TH}) + E_c L]} \quad (2.9)$$

Here W is the width of device, v_{sat} is the saturation velocity, C_{OX} is the oxide capacitance, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, λ is the channel length modulation coefficient, and V_{DS} is the drain to source voltage. Also the relationship between the critical field and the saturation velocity can be given by the following equation.

$$E_c = {}^{2v_{sat}}/_{\mu_e} \quad (2.10)$$

Here μ_e is the electron mobility in silicon.

2.1.4 The MOS Small Signal Model

The small signal models for the long channel device and the small channel device are the same.

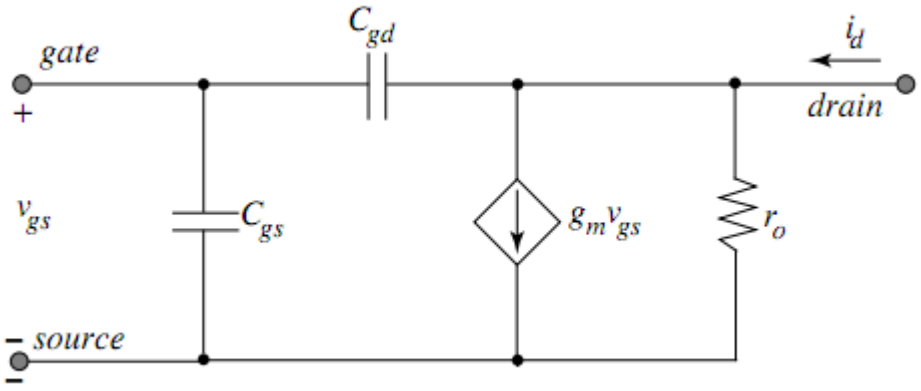

Figure 2.7 The small signal model for the CMOS device [7]

Figure (2.7) describes a small signal model for an NMOS device, which is biased with

gate to source voltage V_{GS}. The symbol g_m, denotes the transconductance of the transistor and r_o is the output resistance due to the channel length modulation.

Transconductance of a device is defined as the variation of the output current with respect to an input voltage.

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \qquad \text{with } V_{ds} \text{ constant} \tag{2.11}$$

The body transconductance g_{mb} is variation in I_D with respect to the V_{bs} (bulk to source voltage difference).

$$g_{mb} = \frac{\partial I_D}{\partial V_{bs}} \qquad \text{with } V_{gs} \text{ and } V_{ds} \text{ constant} \tag{2.12}$$

The input resistance is the variation in the input current with respect to the input voltage.

$$R_{in} = \left(\frac{\partial I_{GS}}{\partial V_{GS}}\right)^{-1} \quad \text{with } V_{DS} \text{ constant} \tag{2.13}$$

In a CMOS device R_{in} is very large, the output resistance given in figure (2.7) is variation in the output current with respect to the output voltage.

$$R_o = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1} \quad \text{with } V_{GS} \text{ constant} \tag{2.14}$$

2.2 Overview on VCO

A VCO (Voltage Controlled Oscillator) is an oscillator circuit whose frequency can be controlled by an externally provided control voltage. The VCO has a number of applications, mainly in communication systems such as in the Phase Locked Loop (PLL) or in the Analog to Digital Converter (ADC) for frequency modulation, phase modulation, or pulse width modulation. This chapter introduces oscillators and their major types of implementation.

2.2.1 The Clock Generation

Almost all digital circuits depend on clock sources. The clock signal which is generated by the VCO is used to synchronize digital operations in receivers. In the PLL the incoming communication signal is demodulated with the help of a synchronized VCO signal, A VCO output

frequency varies with respect to a reference frequency.

As shown in figure 2.8 a reference frequency is ‘compared’ with the VCO output frequency, which generates an ‘error signal’. This is the control voltage for the VCO. The VCO frequency is tuned such that it will shift to the reference frequency until the ‘error signal’ comes down to zero.

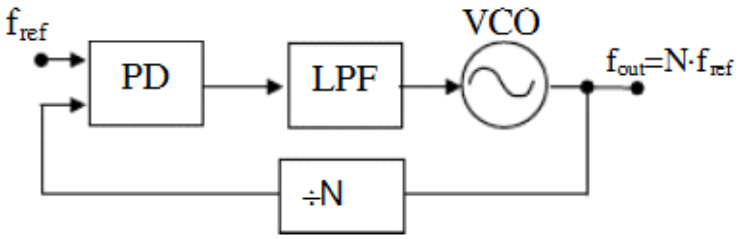

Figure 2.8 A VCO in the PLL [8]

2.2.2 The Oscillation

A oscillator produces a sinusoidal or square-wave signal. It is actually a feedback circuit which oscillates without any outside signal source. The feedback circuit’s transfer function is given by equation (2.15).

$$\frac{V_{out}}{V_{in}} = \frac{H(s)}{1+H(s)} \tag{2.15}$$

The above equation illustrate how a circuit can oscillate, If H(s) = -1, the gain of the feedback circuit will approach infinity. Even noise present in the circuit can be amplified and the amplified output would be fedback to the input again. This continues until the circuit generates an oscillatory signal in the loop.

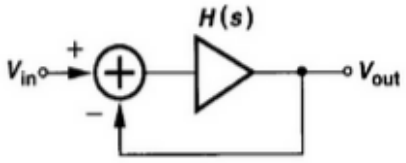

Figure 2.9 Feedback circuit[7]

The Barkhausen criteria for oscillation which govern condition for oscillators are given by

$|H(j\omega_0)| = 1$

$\angle[H(j\omega_0)] = 180^0$ (2.16)

It should be noted that these conditions are necessary but not sufficient. The simple circuit in figure 2.9 can be used to generate a single frequency but to generate a range of frequencies a VCO is required, A VCO is an oscillator whose open loop transfer function ($H(j\omega_0)$) can be varied by a control voltage.

2.2.3 Types of the CMOS oscillators

2.3.3.1 The LC Oscillator

Two major types of CMOS Voltage Controlled Oscillators (VCO) are available: LC oscillators and ring oscillators. An LC oscillator has a tank resonant circuit, which contains an inductor and a capacitor. In the tank circuit, energy keeps on transferring from one element to the other. However, inductors and capacitors not only have inductance and capacitance, but are lossy. The resistance in the LC circuits causes oscillation losses which must be compensated by an active circuit.

2.3.3.2 The Ring Oscillator

The common source (CS) amplifier provides a phase shift of 180^0. After any odd number of CS amplifiers or inverter stages, the phase shift would again be 180^0. If the feedback is applied from the output of the last stage to the first stage's input as shown in figure 2.10, and the gain of each stage is greater than a critical threshold, then the circuit fulfills the Barkhausen criteria. In figure 2.10 a three stage ring oscillator is shown.

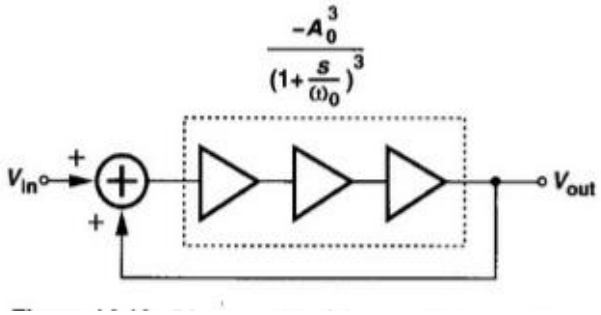

Figure 2.10 A 3 stage ring oscillator [7]

In figure 2.10 the open loop transfer function of the circuit can be given by the equation given below

$$H(s) = \frac{-A^3}{\left(1 + {}^{s}/_{\omega_0}\right)^3}$$

here s = $j\omega$

To find the frequency of oscillation, the Barkhausen criteria can be used

$$\left|\frac{-A^3}{\left(1+{}^{s}/_{\omega_0}\right)^3}\right| = 1 \qquad (2.17)$$

where A is the gain of each stage in figure 2.10. The phase response of this transfer function is given by the equation (2.18), since three stages are used so signal will face three phase shifts.

$$3(\tan^{-1} {}^{\omega_{osc}}/_{\omega_0}) = 180^0 \qquad (2.18)$$

Solving equation (2.17) and (2.18) for the oscillation frequency and for the gain, gives

$$\omega_{osc} = \sqrt{3}\,\omega_0$$

A =2 (2.19)

The oscillation frequency, ω_{osc}, is the oscillating frequency generated by the circuit in figure 2.10. The value ω_0 is the frequency at which the amplitude of the amplifier gain drops ${}^{1}/_{\sqrt{2}}$ times of its maximum value.

Considering each stage in figure 2.10 a single pole amplifier, transfer function of the

amplifier can be given by equation (2.20).

$$H_1(s) = {}^{-A_0}\!/_{(1 + sR_1C_1)} \tag{2.20}$$

$$H_1(\omega) = {}^{-A_0}\!/_{(1 + j\omega R_1C_1)} \tag{2.21}$$

According to the definition of ω_0, keeping ω_0 in place of ω in equation (2.21) gives the following equation.

$$\left| {}^{A_0}\!/_{(1 + j\omega_0 R_1C_1)} \right| = {}^{A_0}\!/_{\sqrt{2}}$$

$$\sqrt{2} = \sqrt{(1 + (\omega_0 R_1C_1)^2)}$$

$$\omega_0 = {}^{1}\!/_{R_1C_1} \tag{2.22}$$

Equation (2.22) shows that ω_0 depends on the product of a resistance and capacitance in a single stage amplifier. This product of resistance and capacitance is known as delay.

$$R_1C_1 = \tau_D \text{ seconds} \tag{2.23}$$

Putting the value of ω_0 in equation (2.20) gives the transfer function of the amplifier as

$$H_1(\omega) = {}^{-A_0}\!/_{(1 + {}^{s}\!/_{\omega_{01}})} \tag{2.24}$$

If more amplifiers are present then the transfer function will be the product of all the transfer functions of the amplifiers. In the case of N stages of amplifiers transfer function is given by

$$H_1(s)H_2(s)H_3(s) \dots\dots H_N(s)$$

$$= {}^{-A_{01}}\!/_{(1 + {}^{s}\!/_{\omega_{01}})} \cdot {}^{-A_{02}}\!/_{(1 + {}^{s}\!/_{\omega_{02}})} \cdot {}^{-A_{03}}\!/_{(1 + {}^{s}\!/_{\omega_{03}})} \dots\dots {}^{-A_{0N}}\!/_{(1 + {}^{s}\!/_{\omega_{0N}})}$$

If all the amplifiers are similar in size then the 3 dB frequencies and gains of all the amplifiers will be the same. So the transfer function for an N staged amplifier is given by equation (2.25).

$$H_1(s)H_2(s)H_3(s) \dots \dots H_N(s) = \left[{}^{-A_0}\Big/_{(1 + s/\omega_0)}\right]^N \quad (2.25)$$

The phase shift provided from the transfer function can be given by equation (2.26)

$$\angle\big(H_1(\omega)H_2(\omega)H_3(\omega) \dots \dots H_N(\omega)\big) = N \tan^{-1}\left(\frac{\omega}{\omega_0}\right) \quad (2.26)$$

CHAPTER 3

RING OSCILLATOR

This thesis deals with a differential ring oscillator, So that it is necessary to have some more understanding of ring oscillators.

3.1 General Purpose of the Ring Oscillator

The ring oscillator as discussed in section 2.3.3.2 is a ring of the three amplifiers. A common source (CS) amplifier produces a phase shift of 180^0 with some added phase change due to the delay (caused by capacitance and resistance) in the circuit.

3.1.1 Frequency Generated By the Ring Oscillator

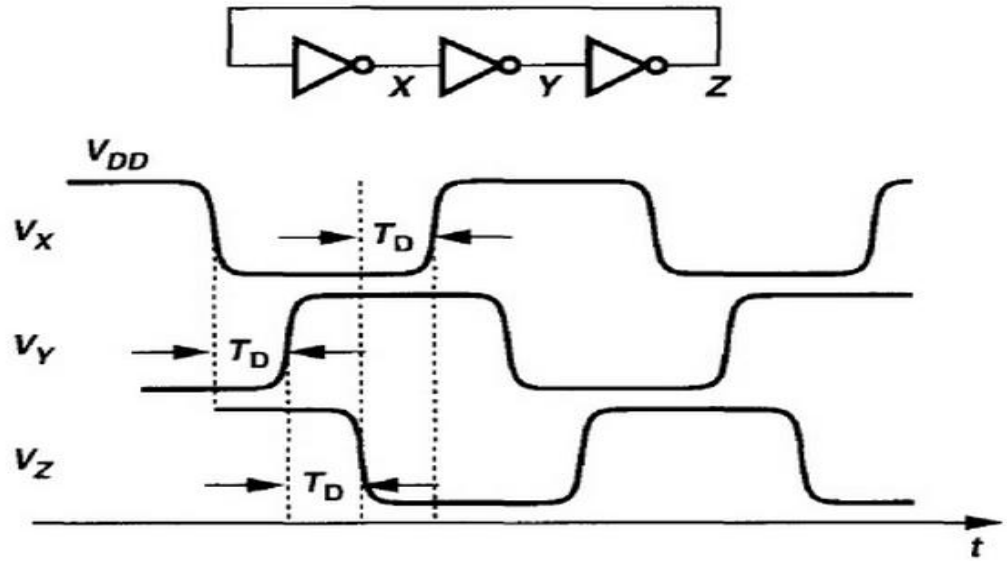

Figure 3.1 Oscillation due to the delay [7]

Figure 3.1 describes a ring oscillator and oscillation frequency waveform generated by this ring oscillator. If each node in this ring oscillator provides a delay of τ_D, it can be observed

from this figure that it will take $6\tau_D$ to complete one cycle. The oscillation frequency generated by the ring of the three amplifiers is given by the formula given below

$$f_{osc} = {}^{1}/_{6\tau_D}$$

If instead of the three amplifiers, the ring contains N stages then the oscillation frequency can be generalized in the form of equation (3.1).

$$f_{osc} = {}^{1}/_{2N\tau_D} \tag{3.1}$$

3.1.2 Fulfillment of the Barkhausen Criteria

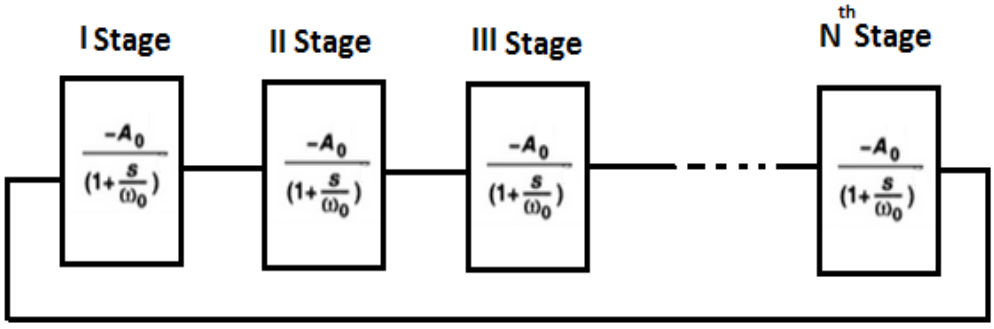

Figure 3.2 The N stage ring oscillator

For an N-staged ring oscillator, the open loop transfer function for figure 3.2 will be the product of the gain of the each stage given by equation (2.25).

$$H(s) = \frac{(-A_0)^N}{(1+\frac{s}{\omega_0})^N} \tag{3.2}$$

where s = $j\omega$. The phase shift provided by each stage is $\tan^{-1}({}^{\omega}/_{\omega_o})$, so the total phase shift, θ_{tot}, provided by the transfer function is given by equation (2.26)

$$\theta_{tot} = N\tan^{-1}({}^{\omega}/_{\omega_o})$$

According to the Barkhausen criteria the total phase shift (θ_{tot}) should be 180^0, hence

$N\tan^{-1}\left({}^{\omega}/_{\omega_o}\right) = 180^0$

Hence, the phase change for each stage is given by [7]

$$\tan^{-1}({}^{\omega}/_{\omega_o}) = {}^{180}/_{N} \quad (3.3)$$

In addition, the open loop gain should be more then unity to compensate for losses, these two criteria give the amount of gain and phase difference each stage should have.

$$\left|\frac{[-A_0]^N}{[\sqrt{(1+(\frac{\omega}{\omega_0})^2)}]^N}\right| = 1 \quad (3.4)$$

Simplifying the above equation would give equation (3.5)

$$\frac{A_0}{\sqrt{(1+(\frac{\omega}{\omega_0})^2)}} = 1 \quad (3.5)$$

The Frequency at which the circuit will start oscillating can be solved from equation (3.3).

$$\omega_{osc} = \omega = \omega_0 \tan({}^{180}/_{N})$$

3.2 Differential Ring Oscillator

A differential amplifier based ring oscillator is shown in figure 3.3. The differential amplifier based ring oscillators can employ even number of stages by making one of the input of differential amplifier cross connected.

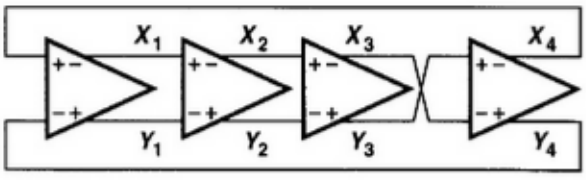

Figure 3.3 A differential even staged ring oscillator [7]

where τ_d is the delay, R is the resistance and C is the capacitance provided by each stage. The oscillation frequency can be made variable if R or C can be controlled. In present case the PMOS transistors serve this purpose of being variable resistors since their resistance changes with change in the gate voltage.

Figure 3.4 illustrates a PMOS transistor load differential amplifier. The NMOS transistors are used as an input transistors and the current source.

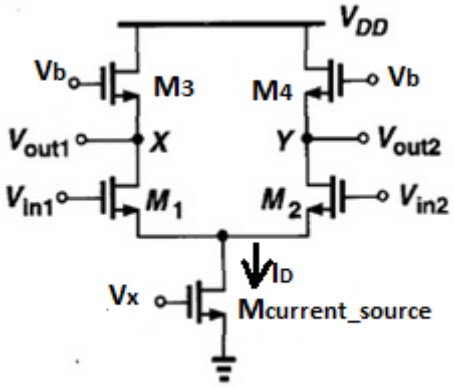

Figure 3.4 A Differential circuit [7]

The differential amplifier shown above uses an NMOS transistor as a current source. The NMOS transistor is not an ideal current source. Figure 3.5 shows a voltage current characteristics of an NMOS transistor. The dotted line shows characteristic of an ideal current source. Bold lines in figure 3.5 for the NMOS transistor demonstrate that current increases with increase in voltage, thus implying presence of the finite resistance in the NMOS transistor current source.

In figure 3.4 The PMOS loads and the NMOS current source transistor can be replaced by the equivalent output impedances to calculate the total output impedance. Replacing the transistors with resistances would not cause any difference in the value of output impedance.

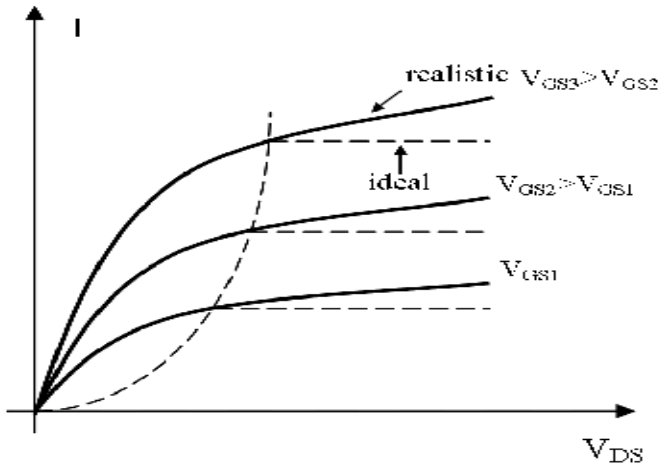

Figure 3.5 Current sources curves, ideal (dotted) and practical [7]

Figure 3.6 is the simplified diagram of figure 3.4 where all the impedances of the CMOS transistors are shown. In figure 3.6(a). The NMOS current source has been replaced with an equivalent resistance r_{oee}, M_1 and M_2 are shown with the equivalent output impedance r_{01}, R_{D1} R_{D2} are the PMOS loads' output impedances. In figure 3.6(b), branches of differential amplifier are divided with the doubling of the value of current source impedance to $2r_{oee}$, this impedance is the source degeneration resistance for M_1. Figure 3.6(c), shows total equivalent resistance where $2r'_{oee}$ is the equivalent output impedance of M_1, and R_{D1} is the PMOS load's output impedance. Value of r'_{oee} is solved in equation (3.5) [7]

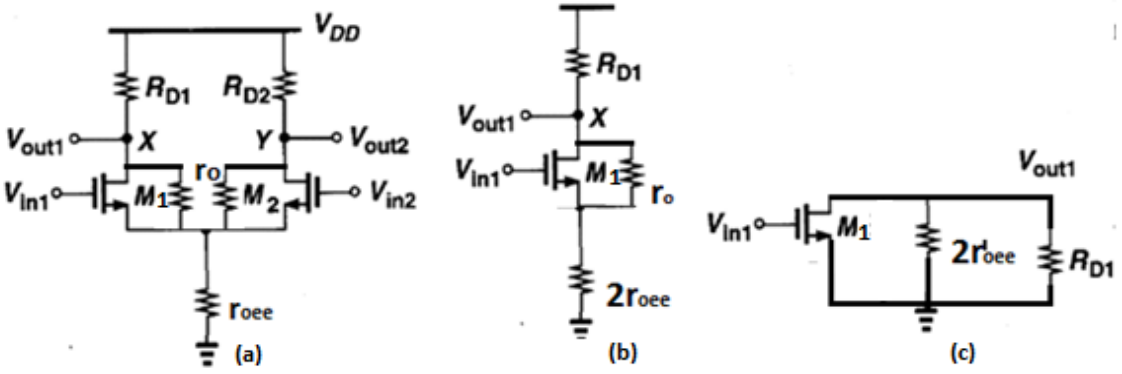

Figure 3.6 Effective resistances by output impedance of MOS and current source [7]

The differential amplifier based VCOs are less noisy than a single ended amplifier based VOCs. The single ended amplifier based VCOs can use only odd number of stages, but the differential amplifier based VCOs can use even number of stages. The differential amplifier based VCOs also generate two inverted output signals, which are helpful in some applications, e.g. amplitude demodulation.

3.2.1 Output impedance of the Differential Amplifier

A simplified symmetrical differential amplifier shown in figure 3.7, which is biased by an NMOS current source. This NMOS current source is providing current of I_D. The two branches of differential amplifier carry half of I_D. In the symmetrical differential amplifier load resistances are coupled with the capacitances C_{eq1} and C_{eq2}. C_{in1} and C_{in2} are the input capacitances of the next stage's input transistors of the figure 3.3. Node between current source and differential branch is a virtual ground whose potential remains constant, hence r_{oee} can be divided in to $2r_{oee}$.

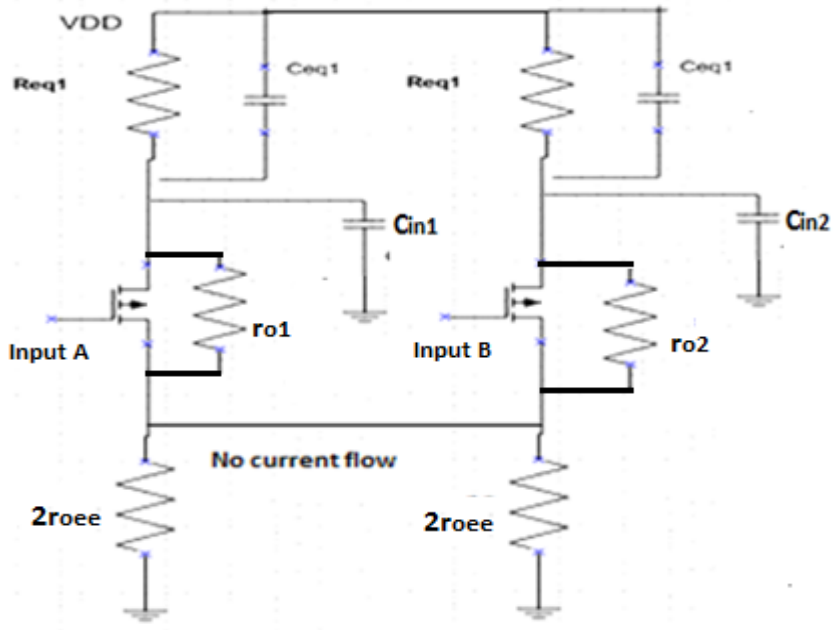

Figure 3.7 Effect of non-ideal current source on differential amplifier [7]

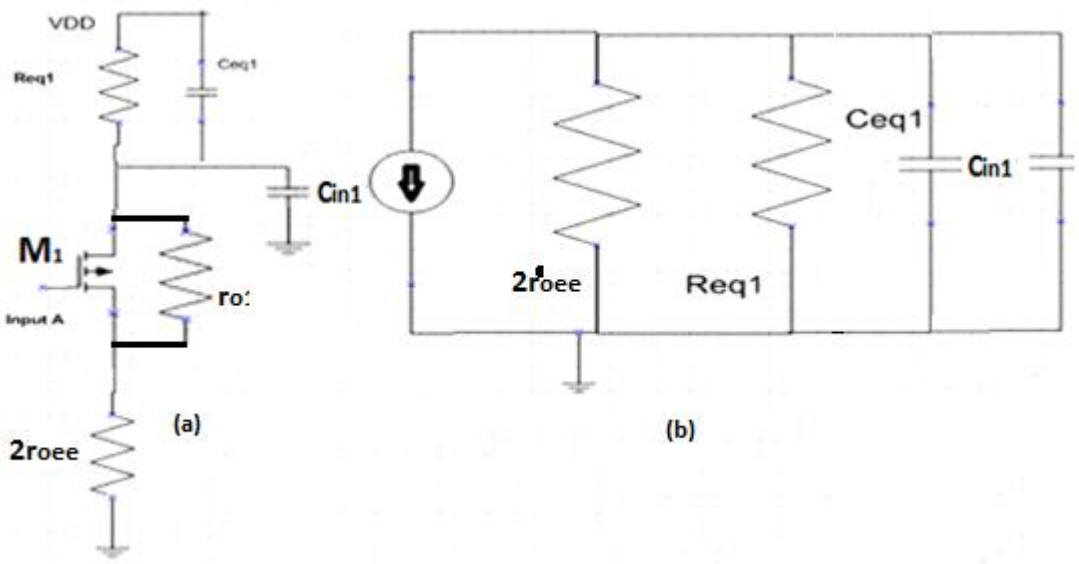

Figure 3.8 A differential amplifier simplified as a source degeneration common source amplifier and effective output impedance [7]

The circuit shown in figure 3.8(a) is a common source amplifier with $2r_{oee}$ as source degeneration resistor, using a small signal model to solve for the value of r'_{oee} gives a simpler circuit (figure 3.8(b)). [7]

$$r'_{oee} = [(1 + (g_{m1})2r_{oee})r_{01}] \quad (3.6)$$

where r'_{oee} is the effective output resistance of the MOS with source degeneration resistor, g_{m1} is transconductance of M_1, r_{01} is the output impedance of M_1, R_{eq1} and C_{eq1} are equivalent resistance and capacitance for active load.

$$R_{tot} = r'_{oee} || R_{eq1} \quad (3.7)$$

$$C_{tot} = C_{in1} + C_{eq1} \quad (3.8)$$

3.3 Voltage Swing Consideration

The total output impedance of each branch of the differential amplifier is a combination of the resistive loading caused by the active load (PMOS) and the output impedance of the NMOS. The current (I_D) ,and the total output impedance (R_{tot}) are decisive in determining the voltage

swing or vice versa. Voltage swing and current can decide value of resistance needed.

If the maximum current is I_D and voltage swing is given by V_{sw}, then the resistance R_{tot} is given by $\frac{V_{sw}}{I_D}$. [12]

$$R_{tot} = \frac{V_{sw}}{I_D} \tag{3.9}$$

Hence equation (3.9) becomes

$$\tau_d = \frac{V_{sw} C_{tot}}{I_D} \tag{3.10}$$

The voltage swing at the output of the VCO core can be fixed at 0.8 volts, Power dissipation, too, is a design parameter, and the value of I_D decides the amount of power dissipation, in the present case this is 1.0 mA. Putting both values in equation (3.9) gives the value of R_{tot} to 800 ohms.

$$R_{tot} = \frac{0.8}{0.001} = 800\ \Omega \tag{3.11}$$

The output impedance, R_{tot}, is the total output impedance of a differential amplifier. The frequency of the VCO is 10.0 GHz when the control voltage is 0.0 volts, τ_d is 12.5 psec. and the capacitance is 15.625 fF calculated from equation (3.1). These capacitances and resistances are inherent with a MOS transistor, Appendix A provides values of these capacitances. From equation (3.1)

$\tau_d = \frac{1}{2Nf_{osc}}$ = 12.5e^{-12} sec. for 10 GHz (3.12)

From equation (3.10) the value of C_{tot} can be calculated

$C_{tot} = \frac{\tau_d I_D}{V_{sw}}$

C_{tot}= 15.625 fF (3.13)

CHAPTER 4

DESIGN SUMMARY

The block diagram in figure 4.1 is the arrangement for the VCO. The oscillator core used in this circuit generates the oscillations between 5 and 10 GHz with a 0.8 voltage swing into the input of the buffer and gain control stage. The buffer and gain control stage serves as an impedance matching circuit and keeps the gain constant for the whole range of frequency. This last stage provides 0.7 volts peak-to-peak signal to the complex load of 50 ohms and 10 fF.

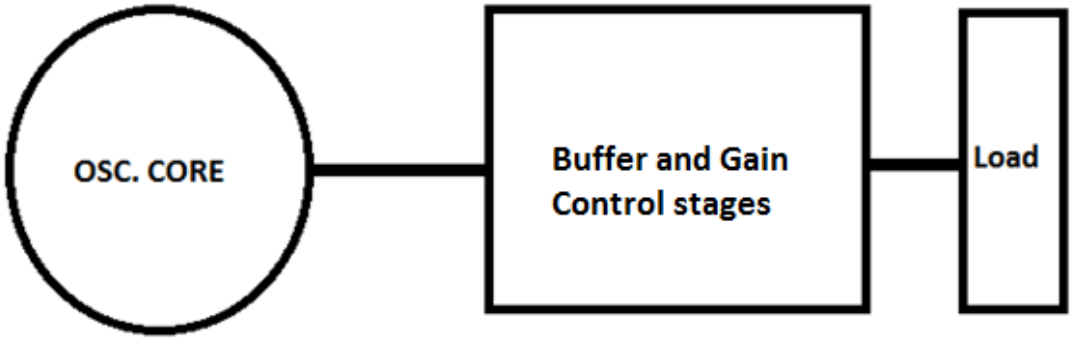

Figure 4.1 Architecture of VCO with buffer

4.1 VCO Core

The block diagram given below in figure (4.2) represents the VCO core circuit. A delay cell block follows the current mirror circuit block. The purpose of the current mirror circuit is to provide constant voltages to bias differential amplifiers.

The delay cells are identical and arranged in the form of a ring or of a cross-coupled loop (figure 4.2). Power supplies have not been shown. The arrow at the end of the ring structure shows the direction of the output signal.

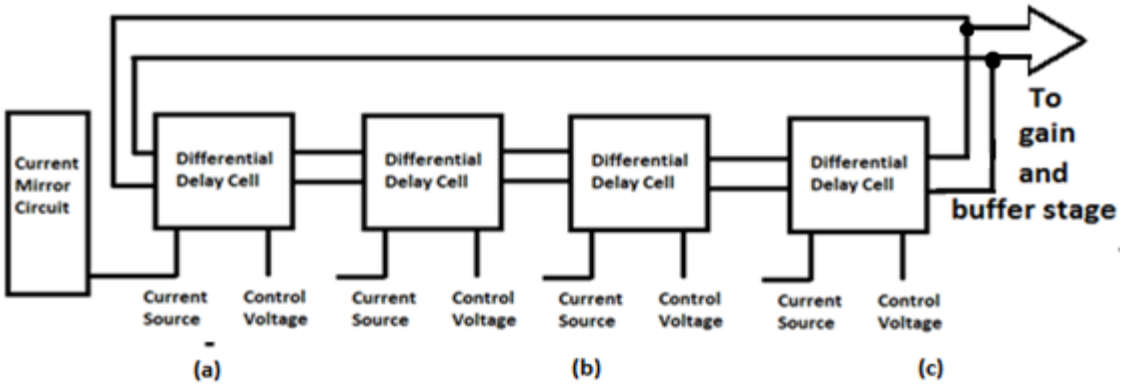

Figure 4.2 block diagram of the VCO core

4.1.1 The Delay Cell

The circuit shown in figure 4.3 is the delay cell used in the VCO. Here M_1 and M_2 are the input transistors.M_3 and M_4 are the controlled active loads whose gate voltage is controlled by a control voltage, and the gates of M_X 's and M_Y's are cross connected to output nodes.

In the VCO identical delay cells are connected back to back. The output of this cell will be fed to the next delay cell's input. This process of feeding the next delay cell continues until the last delay cell whose two differential outputs are then fedback to first delay cell's inputs, but in a cross-coupled way as shown in figure 4.2.

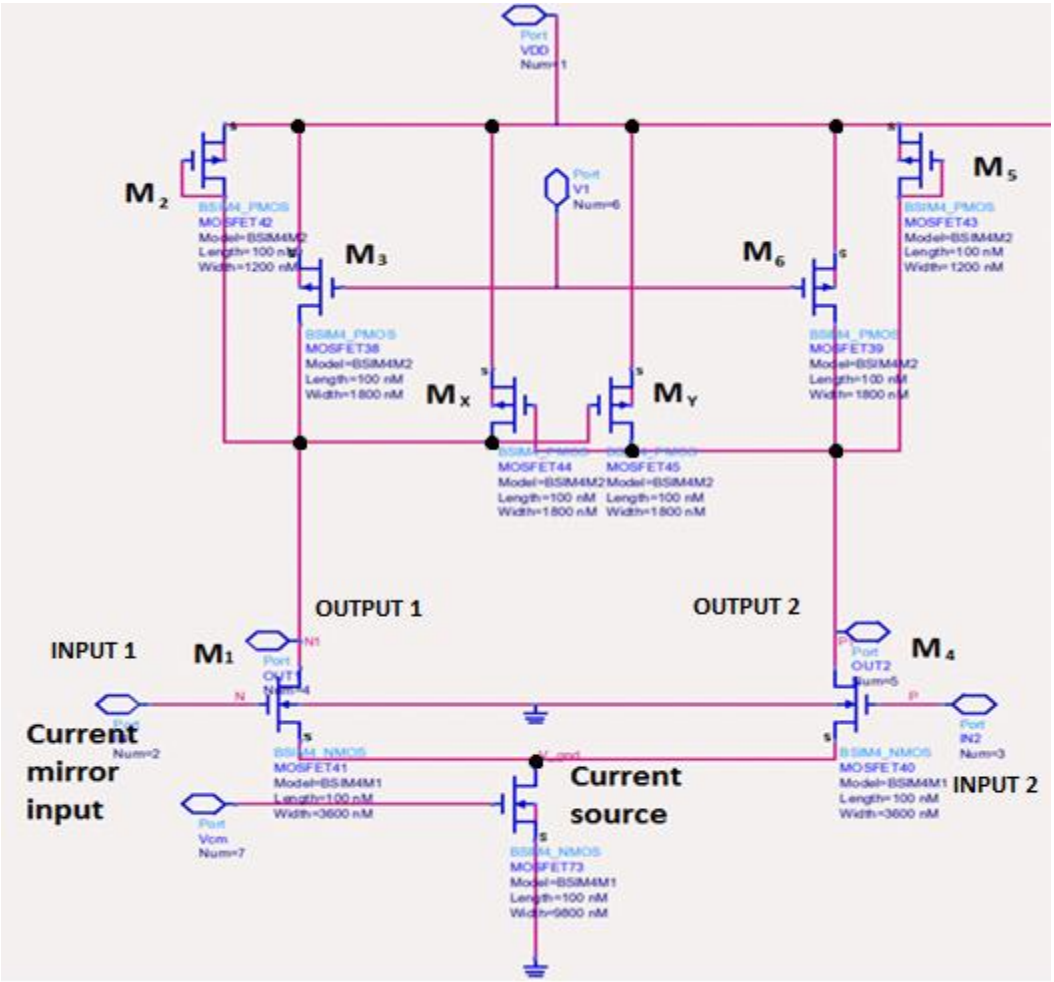

Figure 4.3 D/C (Delay Cell) as used in the present work

4.2 Frequency Calculation

From equations (3.4) and (3.5), the oscillation frequency for a ring oscillator is given by

$f_{osc} = {}^{1}/_{2N\tau_d}$; N=4 (Stages) since four delay cells have been used in the VCO.

where $\tau_d = R_{tot}C_{tot}$. From equation (3.5)

$\tau_d = {}^{V_{sw}C_{tot}}/_{I_D}$

When the control voltage is $0\,V$, the desired oscillation frequency is 10 GHz. The voltage swing (V_{sw}) is a design parameter. The value of I_D for each delay cell is 1 mA. From equation (2.8) current source's width (W) can be calculated which in the present case is 9.8 µm. Lengths of all the transistors used in this design are equal to the 100 nm. Values of R_{tot} and C_{tot} as solved in equation (3.10) are 0.8 kΩ and 15.625 fF respectively.

4.3 Small Signal Model Calculation

The small signal model for the MOS transistor is used to determine the value of resistances and capacitances. Figure 4.4 shows the small signal models of M_1, M'_1 and M_X , these three transistors affect the equivalent output capacitance "felt" by the out-going signal. M_1 and M'_1 have the same dimensions since M'_1 is the input transistor for the next stage's delay cell .

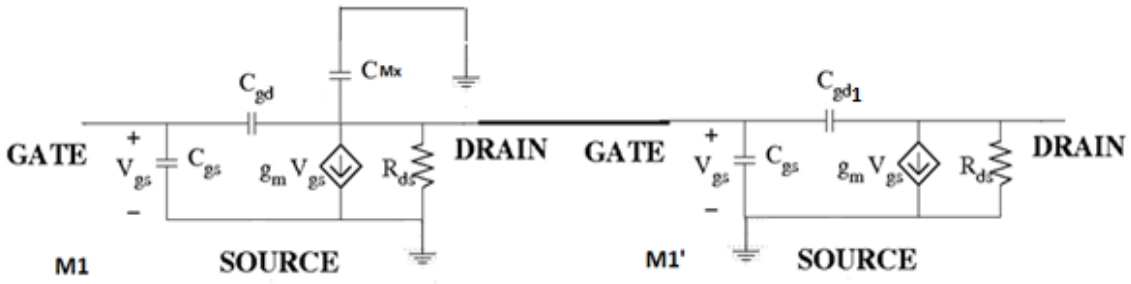

Figure 4.4 Use of small signal model to find equivalent output impedance

In figure 4.4 C_{gd} is connected between the gate and drain of M'_1. The effect of this capacitance has to be measured with the help of the Miller effect theorem, which is discussed in section 4.3.1.

The gain of M_1 is $g_m R_{tot}$, while from equation (3.11) the value of R_{tot} is 800Ω.

4.3.1 The Miller Effect

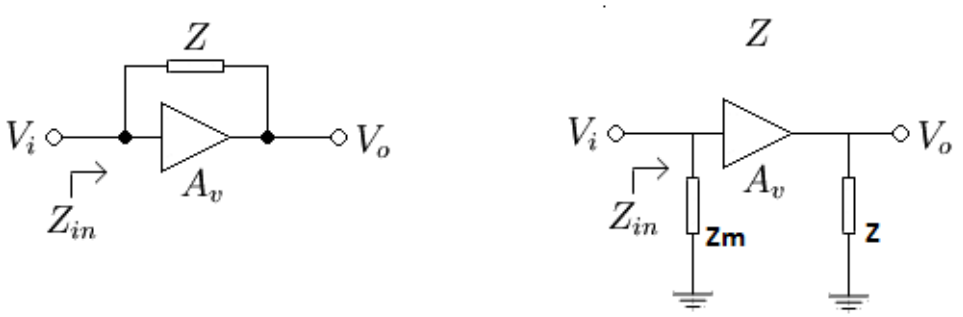

Figure 4.5 The Miller effect

The C_{GD1} is connected across transistor M'_1, The Miller effect helps to find the equivalent capacitance due to C_{GD1}. The Miller effect can be helpful to determine true value of C_{GDm1} (with respect to the ground).

In diagram 4.5 Z is the impedance between the input and output, and the gain is A_v. Solving for the value of the Miller impedance value of Z_m gives

$$Z_m = Z/(1 - A_v)$$

The gain A_v is negative, For circuit shown in figure 4.7 [7]

Z = $^1/_{j\omega C_{gd1}}$

$A_v = -g_{m1}R_{tot}$

Simplifying the figure 4.4 with the help of the Miller effect theorem [7]

$$C_{gdm} = C_{gd1}(1 + g_{m1}R_{tot}) \quad (4.2)$$

In equation (4.2) R_{tot} is the total resistive loading due to the active load, g'_{m1} is the transconductance of M'_1. C_{gd1} is $W'_1 C_{gdo}$ and the value of C_{gdo}(1.9e-10 F/m) is available in Appendix A.

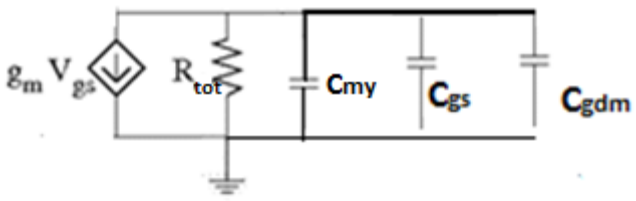

Figure 4.6 Effective output capacitance seen from M_1

According to the equation (3.8), the total output capacitance of the delay cell felt by outgoing signal would be

$C_{tot} = C_{in1} + C_{eq1}$

From figure 4.6 the input capacitance of next stage's input transistor would be

$C_{in1} = C_{gs1} + C_{gd1}(1 + g_{m1}R_{tot})$

The equivalent capacitance of differential cells branch is given by C_{eq1}

$C_{eq1} = C_{My}$

Hence value of C_{tot}

$C_{tot} = C_{My} + C_{gs1} + C_{gd1}(1 + g_{m1}R_{tot})$ (4.4)

4.4 Functioning Of M_Y

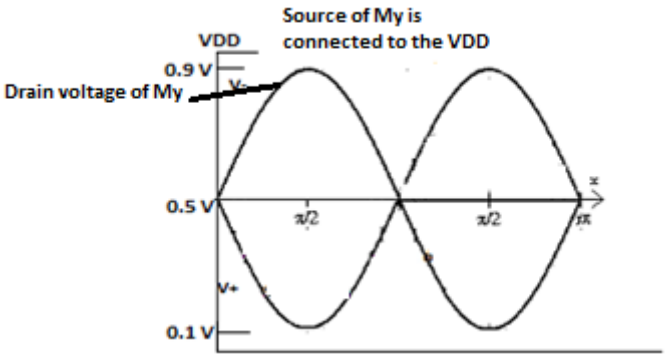

Figure 4.7 Operation of M_y

The transistor M_Y in the delay cell has the drain connected to the output node and source is connected to the VDD. The output node of the delay cell has voltage variation as shown in figure 4.7. It is assumed that the voltage swing at the delay cell output is 0.8 volts with the x-axis is at 0.5 volts of sinusoidal amplitude. The drain of M_Y is oscillating between 0.1 volts to 0.9 volts while the source terminal of M_y is always connected to the VDD.

V_{Drain} = 0.1 to 0.9 volts

V_{Source} = 1.0 Volts

The saturation voltage for the PMOS is V_{SDsat}. The required condition for the PMOS to saturate is given by

$V_{SD} \geq V_{SDsat}$ M_y is a P type CMOS

$$V_{SD} = V_{Source} - V_{Drain} \quad (4.5)$$

hence

$V_{SD_{min}}$ = 0.1 volts

The minimum V_{SD} for M_y is 0.1 volts, and the saturation voltage V_{SDsat} for M_y is 0.106 volts [with the help from Appendix A],

$$V_{SD_{min}} \cong V_{SDsat}$$

hence according to the saturation condition for the PMOS, M_y stays in the saturation region.

$$V_{SD} \gtrsim V_{SDsat}$$

Figure 4.8 shows variation of C_{GD} and C_{GS} capacitance of a CMOS transistor, in the saturation region, the total capacitance offered by M_y is given by equation (4.6)

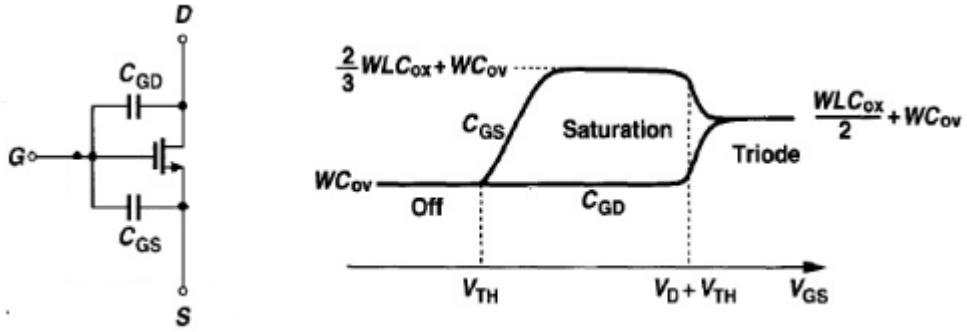

Figure 4.8 Variation of capacitances [7]

$C_{My} = C_{GD} + C_{GS}$

$C_{GD} = W_Y C_{ov}$

$C_{GS} = \frac{2}{3} W_Y L C_{ox} + W_Y C_{ov}$

hence

$$C_{My} = 2W_Y C_{ov} + \frac{2}{3} W_Y L C_{ox} \quad (4.6)$$

With all values of the capacitances' available, these can be placed in the previous equation of C_{tot} from equation (4.4)

$$C_{tot} = 2W_Y C_{ov} + \frac{2}{3} W_Y L C_{ox} + C_{gs1} + C'_{gd1}(1 + g_{m1} R_{tot}) \quad (4.7)$$

The value of C_{tot} is known from equation (3.13) which is 15.625 fF.

$$C_{gs1} = W_1.C_{gso} \tag{4.8}$$

$$C'_{gd1} = W'_1.C_{gdo} \tag{4.9}$$

Values of C_{gso} and C_{gdo} are available in Appendix A, W_1 and W'_1 are the gate width dimensions of M_1 and M'_1. M_1 and M'_1 are identical transistors, so their dimensions are equal.

4.5 Values of Transistor Widths

To calculate the oscillation frequency equations (3.4) and (3.5) are used. Replacing C_{tot} with equation 4.7 gives

$$f_{osc} = \frac{1}{[2NR_{tot}\{2W_YC_{ov} + \frac{2}{3}W_YLC_{ox} + W_1C_{gso} + W'_1C_{gdo}(1+g_{m1}R_{tot}))\}]} \tag{4.10}$$

All values of the capacitances are available in Appendix A. Values of R_{tot} and N are also known from equation (3.11). The transfer function for a four stage single ended oscillator is given by equation(4.11)

$$H(\omega) = \frac{A_0^4}{(1+(j\omega_{osc}/\omega_0))^4} \tag{4.11}$$

For a four stage ring oscillator's oscillation frequency, equation (3.3) becomes

$$\tan^{-1}(\omega_{osc}/\omega_0) = 45^0$$

giving

$$\omega_{osc}/\omega_0 = 1$$

Putting this value back into the transfer function equation given in (4.11), taking the magnitude of the transfer function, and applying the Barkhausen criteria gives

$$\frac{A_0^4}{[\sqrt{(1+(\omega_{osc}/\omega_0)^2})]^4} = 1 \tag{4.12}$$

Therefore the value of $A_0 = \sqrt{2}$

For the differential amplifier gain equation is given by [7]

$$g_m = \sqrt{\left[\mu_n C_{ox} \frac{W}{L} I_D\right]}$$

$$A_0 = g_m R_{tot}$$

$$A_0 = \left\{\sqrt{\left[\mu_n C_{ox} \frac{W}{L} I_D\right]}\right\} R_{tot}$$

So that

$$\frac{W}{L} = \frac{{A_0}^2}{{R_{tot}}^2 \mu_n C_{ox} I_D} \quad (4.13)$$

Values of $\mu_n, C_{ox}, R_{tot}\ and\ I_D$ are known, which gives

$$\frac{W}{L} = \frac{W}{L_1} = 35$$

The definition of the transconductance is:

$$g_{m1} = g'_{m1} = \frac{dI_{DS}}{dV_{DS}} = \frac{d\, W v_{sat} C_{OX} (V_{GS} - V_T)(1 + \lambda V_{DS})}{dV_{DS}} = W v_{sat} C_{OX} (V_{GS} - V_{TH}) \lambda \quad (4.14)$$

Values of v_{sat}, C_{OX} (C_{OX} is in F/m), V_{GS}, V_{TH} and L (100 nm for all the transistors) can be placed in equation (4.14) to find $g_{m1} (= g'_{m1})$.

From equation (4.10)

$$W_Y = \frac{1}{2NR_{tot} f_{osc} . (C_{ov} + \frac{2}{3} LC_{ox})} - \frac{W'_1 C_{gdo} (1 + g_{m1} R_{tot})}{(C_{ov} + \frac{2}{3} LC_{ox})} - \frac{W_1 C_{gso}}{(C_{ov} + \frac{2}{3} LC_{ox})}$$

equation above gives value of W_Y = 1.83 µm ≈ 1.8 µm. hence W_Y/L =18.

4.5.1 Calculation Of widths for M1 and $M_{current\ source}$

The output resistance R_{tot} is the resultant output resistance of the differential amplifier. This output resistance is the parallel combination of the source degeneration resistance (r'_{oee}), R_{M2} and R_{M3} , R_{M2} is the output resistance of M_2, R_{M3} is the output resistance of M_3 [7]

$$R_{tot} = r'_{oee}||R_{M2}||R_{M3} \tag{4.15}$$

$$r'_{oee} = [(1 + (g_{m1} + g_{mb1})2r_{oee})r_{01}]$$

The value of r'_{oee} can be calculated since the dimensions of M_1 are known, r_{01} and r_{oee} are the output resistances provided by M_1 and $M_{current\_source}$, g_{m1} is solved from the equation (4.14), and g_{mb1} is the body transconductance of M_1. From equation (3.11)

R_{tot} = 800 Ω

The value of r'_{oee} is known hence equation (4.15) reduces to the two unknown resistances R_{M2} and R_{M3}. The gate of transistor M_3 is connected to the control voltage and the control voltage changes the resistance of $M_3(R_{M3})$ to control the output frequency.

The variation in output frequency depends upon change in resistance of M_3. If R_{tot} is the output resistance at 10 GHz then assuming that $R_{tot@5GHz}$ is the output resistance for 5 GHz. From equation (3.5)

$f_{osc} = {}^{1}/_{2.N.R_{tot@5GHz}C_{tot}}$

With $f_{osc} = 5X10^9$ GHz and C_{tot} = 15.625 fF from equation (3.14) Gives

$R_{tot@5GHz}$ = 1600 Ω

The output resistance $R_{tot@5GHz}$ is the parallel combination of r'_{oee}, R_{M2} and R_{M3}. To vary the oscillation frequency from 5 to 10 GHz, the control voltage is varied from 0.5 volts to 0 volts. The output resistance $R_{tot@5GHz}$ is the resistance at the control voltage of 0.5 volts. The output resistance of M_3, R_{M3}, is the single parameter which changes with the control voltage. R_{M3} has to be chosen in such a way that the variation from 0 to 0.5 volts will cause a frequency variation of 5

to 10 GHz. The value of C_{tot} is known (from section 3.2), hence using the oscillation frequency at 5 GHz.

For 5 GHz, value of R_{tot} = $R_{tot@5GHz}$ from equation (3.5)

$$5X10^9 = {}^1/_{2.4.R_{tot@5GHz}C_{tot}} \quad (4.16)$$

$R_{tot@5GHz}$ = 1600 Ω

Equation (4.15) gives a new value of $R_{tot@5GHz}$

$$\frac{1}{800} - \frac{1}{1600} = \frac{1}{r'_{oee}} - \frac{1}{r'_{oee}} + \frac{1}{R_{m2}} - \frac{1}{R_{m2}} + \frac{1}{R_{m3}} - \frac{1}{R'_{m3}} \quad (4.17)$$

Here R'_{m3} is the resistance of M_3 at 5 GHz. After solving equation (4.17)

$$1/1600 = \frac{1}{R_{m3}} - \frac{1}{R'_{m3}} \quad (4.18)$$

where

$g_{ds3} = 1/R_{m3}$ and $g'_{ds3} = 1/R'_{m3}$

Equation (4.18) gives the change in conductance with variation in the control voltage. The conductance depends on the output current (I_D) with the output voltage (V_{DS}). The source of M_3 is connected to VDD, and the gate is connected to the control voltage. Hence V_{GS3} = 0.5 V for g'_{ds3} and V'_{GS3} = 1.0 V for g_{ds3}.

The differentiation of I_{DS} with respect to V_{DS} gives the transconductance of the transistor.

$$g_{ds} = \frac{dI_{DS}}{dV_{DS}} = \frac{d[W v_{sat} C_{OX}(V_{GS} - V_T)(1 + \lambda V_{DS})]}{dV_{DS}}$$

Equation (4.18) is the difference between two transconductance. From equation (4.17)

1/1600 = $v_{sat}W_3C_{OX}(1 - V_{TH})\lambda - v_{sat}W_3C_{OX}(0.5 - V_{TH})\lambda$ (4.19)

Solving equation (4.18) gives W_3= 1.76 μm, the value of W_3 in equation (4.16) provides a value of W_2 = 1.173 μm value L is same for all the transistors.

$L_1 = L_2 = L_3 = 100\ nm$

Hence

$\frac{W_3}{L_3} = 17.6 \approx 18$

$\frac{W_2}{L_2} = 11.73 \approx 12$

4.6 Capacitance Division

The discussion up to section 4.4 concludes the design for the VCO core. This VCO core produces a differential oscillatory signal, which needs to be transferred to a complex low impedance load. An opamp with the low output impedance can be used to convert a differential signal from the VCO core to a single ended low impedance load.

The VCO's frequency is based on the resistance and the capacitance of each node in the VCO core. During the calculation of frequency, the input capacitance of the next delay cell's input transistors were taken into account. A VCO, which generates a sinusoidal signal, must provide this sinusoidal signal to the next block i.e. the comparator and buffer stage.

From equation 3.10 oscillation frequency is given by

$$f_{osc} = \frac{1}{2NR_{tot}C_{tot}}$$

In above equation C_{tot} is the total output capacitance of each delay cell. The total capacitance depends on the device size and number of input transistors of the next stage. The first stage of the comparator and buffer stage (figure 4.1), the comparator, has the input transistors, which

provide capacitance to the incoming sinusoidal signal. This will cause extra loading on the VCO core's output. The extra loading would change the C_{tot} of the last delay cell, this in return will change the desired frequency range. In order to avoid this frequency shifting, capacitances in the comparator and the first stage of the VCO core have been divided into equal amounts so that the total capacitance (C_{tot}) at the last stage of the VCO core will remain same.

The capacitive loading has been described in figure 4.9. To avoid having different capacitive loading on the last delay cell, the first stage of the ring oscillator core and the first stage of the opamp (figure 4.10) have the same design and have half the widths of transistors of the delay cells shown in figure 4.3. [8]

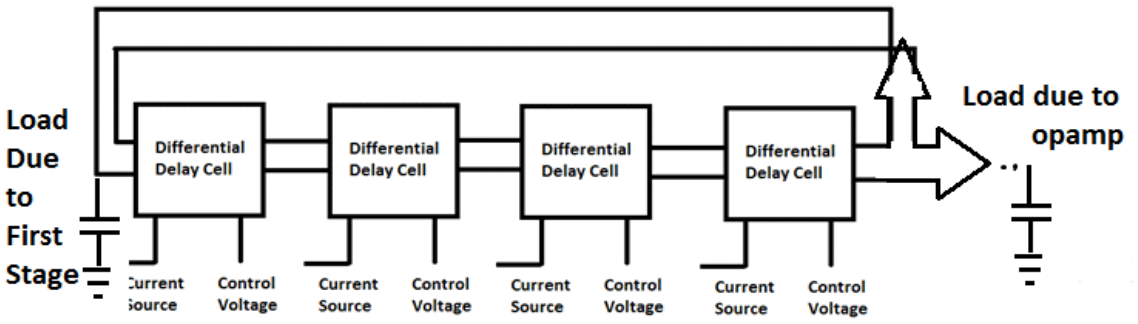

Figure 4.9 Capacitive load on the last stage

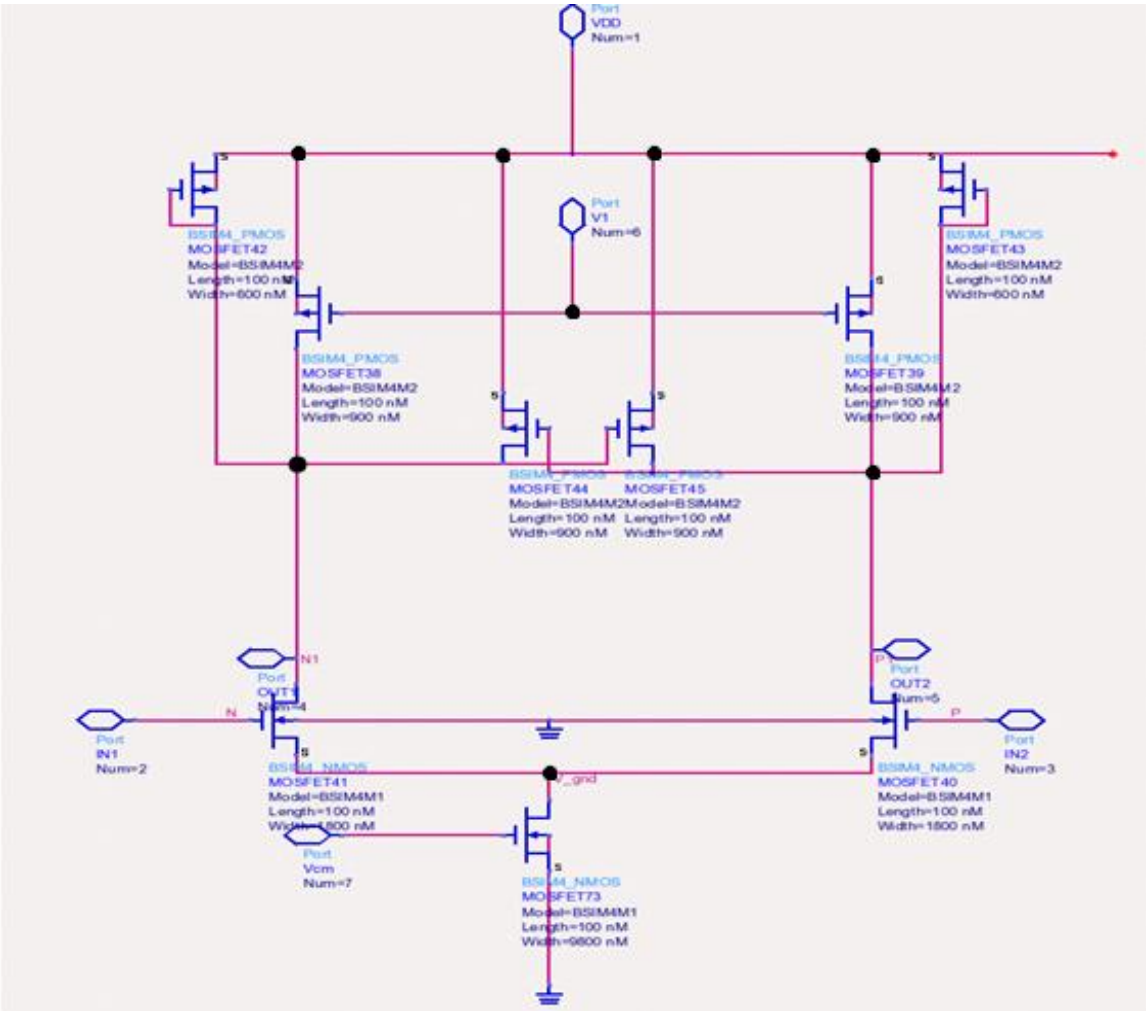

Figure 4.10 The half delay cell

Figure 4.10 shows a delay cell with half the values of width used in the VCO core. This half delay cell has been employed in figure 4.11 as a first stage. Figure 4.12 shows that the VCO core's last stage is connected to the first stage of the comparator and buffer stage.

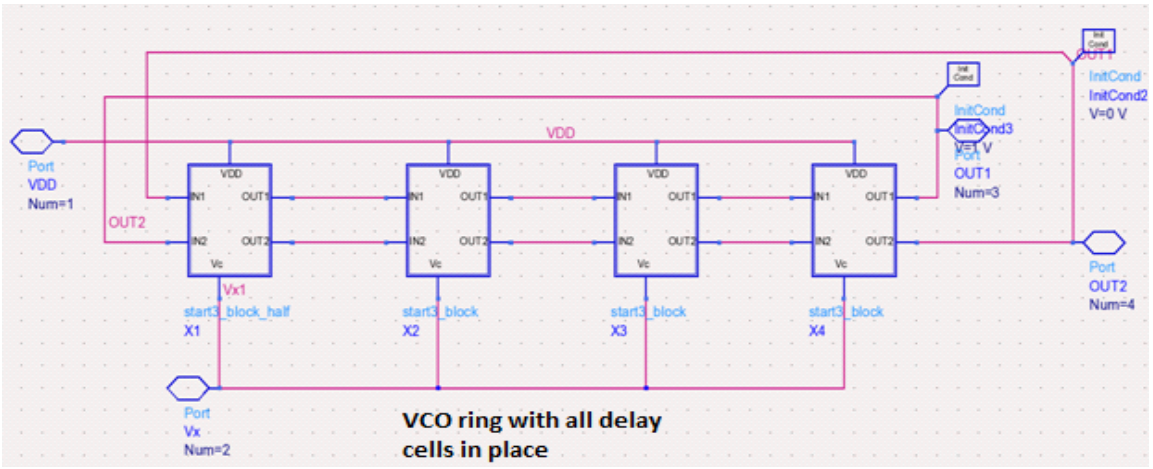

Figure 4.11 VCO core ring structure

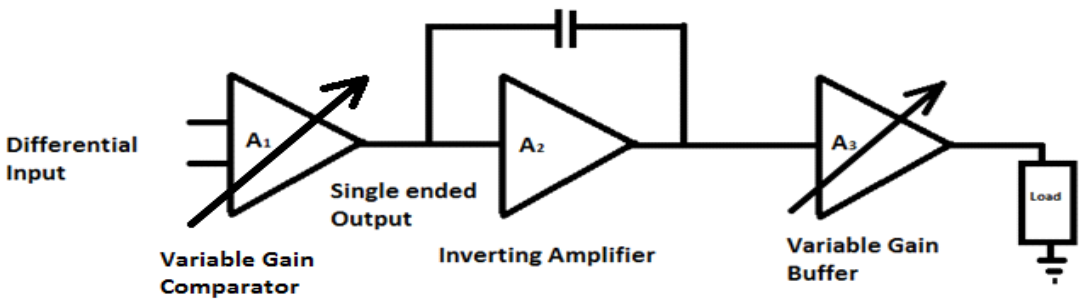

Figure 4.12 Comparator and buffer stage

Figure 4.12 shows the comparator and buffer stage with three stages. The first stage is the variable gain comparator in which the differential inputs are converted in to the single ended output signal. The single ended output from the comparator is supplied to an inverting buffer and then to the variable gain buffer stage.

The inverting amplifier stage works between the comparator and the buffer stage. The buffer stage maintains constant gain of output signal throughout the frequency range (i.e. 5 to 10 GHz).

4.7 Comparator

The comparator (figure 4.13) converts the differential input to the single ended output. The architecture of this comparator is based on a differential amplifier with a current mirror as the active load. The M_6 of the current mirror circuit is a diode connected device while the gate of M_8 is connected to the gate of M_6. Hence, any change on the drain and gate of M_6 replicates on the gate of M_8.

Suppose the input signal at M_4 is high and M_5 is low then M_6 would have a low gate-source voltage, which would replicate at the gate of M_8 hence equal current would flow through M_5M_8. On the other hand if input of M_4 is low (M_5 is high) then the gate of M_6 would be high and M_6 and M_8 would be off so that no current would flow through M_5M_8. In both the cases the output would be replicated at the input of the inverting amplifier. For the frequency range of 5–10 GHz, internal capacitances of the inverter (C_{GD}) would serve the purpose of capacitance across inverter as shown in figure 4.14 at the input node of the buffer.

The gain up to the inverting amplifier would be given by equation (4.21)

$$A_v = \frac{g_{m2}}{sC} \tag{4.21}$$

Figure 4.13 shows a current mirror with the comparator. The current mirror provides constant voltage bias to the buffer stage as shown in figure 4.14. The current mirror provides current in proportion to the transistor size. [7]

$$\frac{I_{req}}{I_{ref}} = \frac{(W/L)_{req}}{(W/L)_{ref}}$$

Here I_{ref} is the current in the current mirror circuit, $(W/L)_{ref}$ is the design ratio for the M_9 , I_{req} is current required in buffer stage's constant load (figure 4.14) and $(W/L)_{req}$ is the device size of the buffer's constant load as mentioned in figure 4.14.

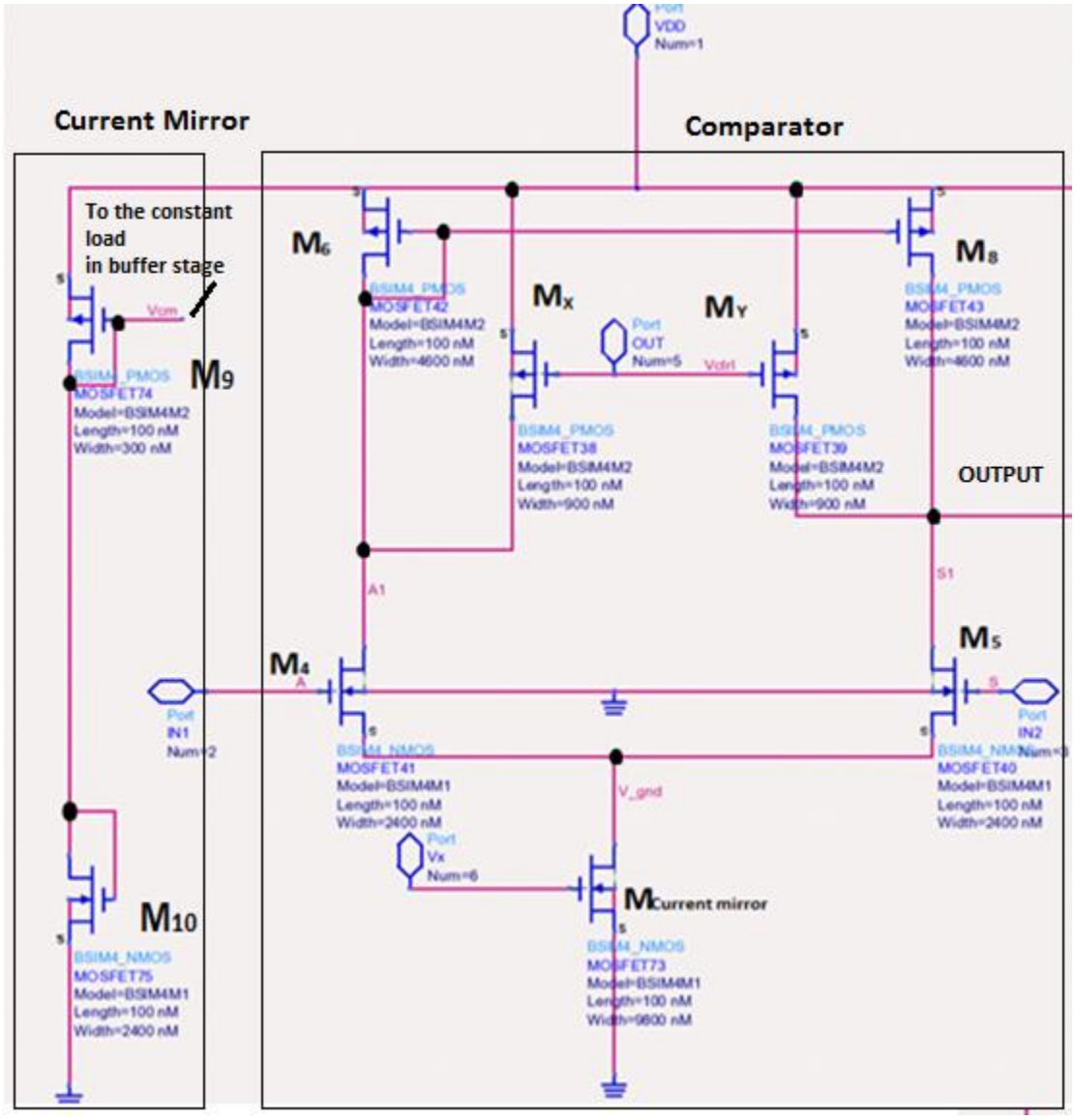

Figure 4.13 Opamp first stage

The gate voltages of the transistors M_x and M_y are controlled through the control voltage V_{ctrl}, which is also used as a control signal in the VCO for controlling frequency. Hence, it is appropriate to use it. An increase of frequency is associated with a decreasing control voltage, through M_4 and M_5. Thus by increasing transconductance and resistance of the comparator.

Three more stages of the buffers are used (figure 4.14) to further reduce gain variation during resistance transformation, which are described in section 4.6.2.

The VCO's output signal would be driving a complex load of 50 Ω and 10 fF, The voltage swing is required to be 0.7 volts. If a buffer loads this small impedance than the output impedance(R'_{77}) of the buffer would be calculated by the voltage division rule.

$$\frac{50}{R'_{77}+50} = 0.7$$

$$R_x = 21.4285\ \Omega$$

R_x is a small low impedance, so a large MOSFET is needed to drive this load. The amplifier's gain varies with the frequency, which can be understood with the formula given below

$$A(s) = {}^{A_0}/_{(1+R.C.s)};\ s = j\omega \tag{4.19}$$

where R and C are the output resistance and capacitance, it is easy to infer from equation (4.19) that the gain decreases with the increasing frequency

$$A_0 = g_m R_D \tag{4.20}$$

So a method to keep the gain constant throughout the range of 5 to 10 GHz is to increase g_m and R_D with frequency. This is easy in this case since the frequency itself is increasing with a decrease in control voltage this relationship can be exploited in the present case.

4.7.1 Sizing for the Comparator

The comparator is an approximate replica of a delay cell, which is used in the VCO ring. The delay cell used for the comparator has half the widths of the delay cell used in the VCO. Use of the half width delay cell in the comparator is important because it keeps the total capacitive loading on the last stage equal to the load shared by the other delay cells. In addition, the using of the delay cell as a comparator allows implementation of control voltage as a gain control mechanism.

4.7.2 Buffer Stage

The aim of this work is to drive a complex load of 50 Ohms and 10 fF, which requires having a final amplifier with an output impedance of 21.34 ohms that will provide 0.7 volts of voltage swing to the load.

A transistor with 21.34 Ω output impedance would be large one. A large transistor has small input impedance too, hence big transistors needed to run proportionally big amplifier. In a chain of the buffer amplifiers, stages of the amplifiers are used whose size increases in each stage as shown in figure 4.14. The process of the increasing the size to achieve a final low output resistance is called the buffer optimization. [10]

Three active load common source amplifiers are used to provide the constant gain. Each amplifier has two current source active loads. The first current source is driven by a constant gate voltage bias (from current mirror shown in figure 4.13) and the second current source is fed by V_{ctrl}.

The PMOS devices are suitable for this purpose, as shown in figure 4.14. The last stage has a constant current source and a variable current source. This stage provides a low output resistance for the output load for 0 and 0.5 volts. So putting these two conditions in the form of equation gives equation (4.21), the voltage swing delivered at the output has 0.7 volts.

$$A_{01}\Big/(1 + R_1C_1 \cdot 2\pi \cdot 10X10^{10}) = A_{02}\Big/(1 + R_2C_1 \cdot 2\pi \cdot 5X10^{10}) = 0.7 \qquad (4.21)$$

With the variation in the control voltage, the output resistance of the variable current source varies. R_1 is the parallel combinations of the variable load output resistance and the constant load output resistance(as shown in figure 4.14) for 0 volts and R_2 is the parallel combination at the 0.5 volts control voltage. For 0.5 volts, the variable load changes resistance such that the total output resistance is R_2. For 0 volts, the total output resistance is R_1. The capacitance C_1 will remain the

same in both cases. A_{01} and A_{02} are the gains for the control voltages of 0 volts and 0.5 volts.

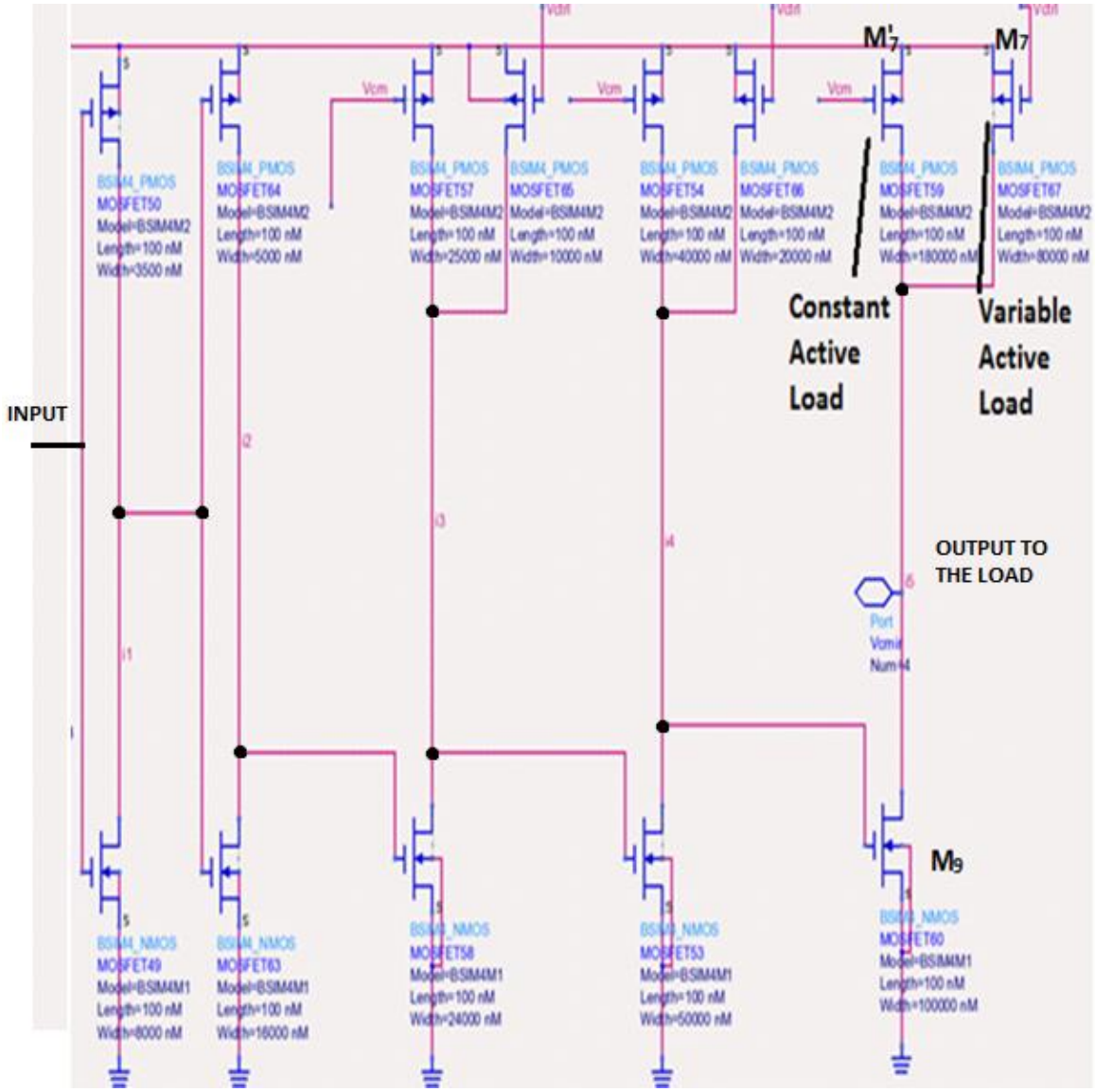

Figure 4.14 Opamp second and third stage

In the present case the number of unknowns are more than the number of equations present. Hence, the $\frac{W}{L}$ ratio of the NMOS is kept at $1/2.6$ times the width of the total PMOS active load (which is yet to be decided). [8]

To start the calculations dimensions of M_9 in figure 4.14 are assumed (which gives capacitance value of C_1), from here on it becomes easy with the help of equations above. Values of R_1 and R_2 help to decide the sizes of M_7 and M'_7.

As $A_{01} = g_{m9}R_1$ gives the solution for R_1 (g_{m1} known)

$$R_1 = R_{m9} \parallel R_{M_7} \parallel R_{M'_7} \quad (4.22)$$

$$R_2 = R_{m9} \parallel R'_{M_7} \parallel R_{M'_7} \quad (4.23)$$

$R_{M'_7}$ is the resistance for the constant active load and R_{M_7} is the resistance for the variable active load when control voltage is 0.5 volts, R_{M_7} is the resistance for the variable active load when the control voltage is 0 volts. Solving equation (4.22) and (4.23) provide solution for R_{M_7}, with this value of R_{M_7}, the W/L ratio of M_7, M'_7 and M_9 can be calculated. [8]

4.7.3 Behavior of Buffer Stage with Large Transistors

Figure 4.15 illustrates the flow of the signal and the impedance caused by M_9.The last transistor used for load driving is large and c_{gs} is directly proportional to the width of the transistor. However, due to the Miller effect the total capacitance faced by the signal would increase as shown by equation given below

$$c_{M\_tot} = c_{gs} + c_{gd}(1 + g_m R_{out})$$

$$c_{gso} = c_{gso} = 1.8\,X10^{-10}\ F/\mu m$$

$R_{out} = 25$, $g_m = 0.1$, W = $100\mu m$

$$c_{M_{tot}} = 8.1\ X\ 10^{-14}\ \text{F}$$

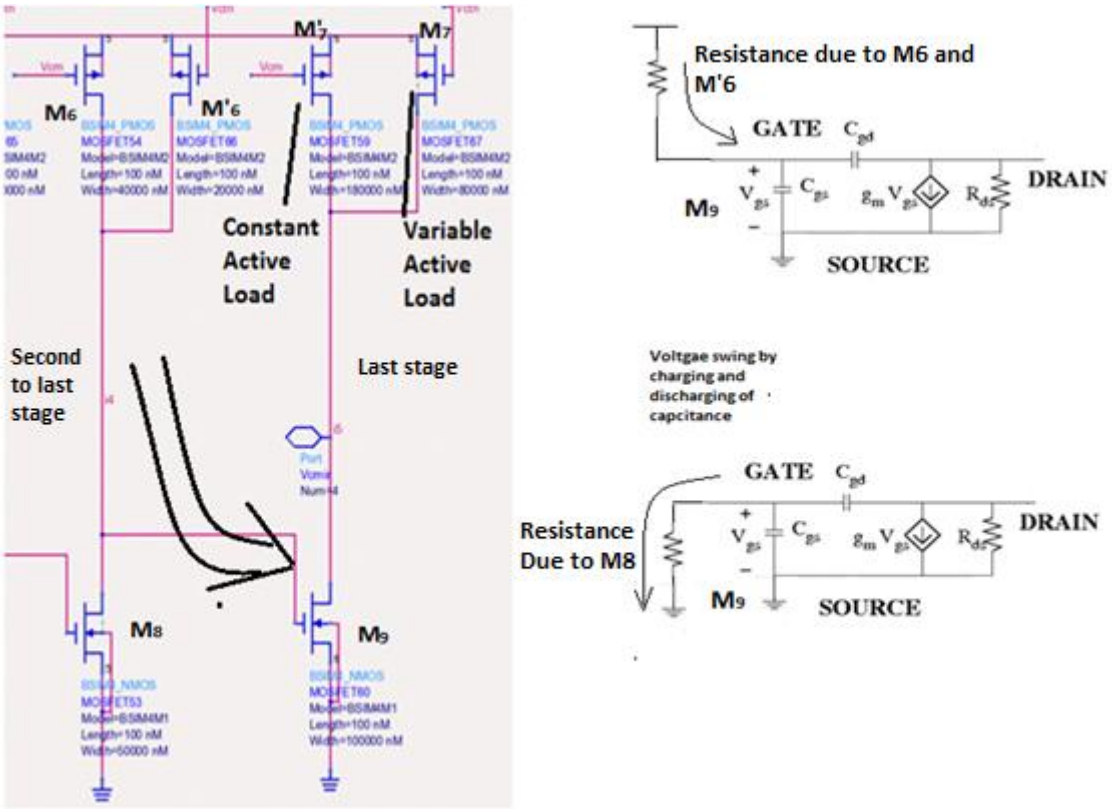

Figure 4.15 Signal movements in the buffer circuit

At the maximum frequency of 10 GHz the input impedance of M_9, which would act as a load impedance to the second to last stage is given by equation below.

$$Z_{in9} = {}^{1}/_{\omega C_{M_{tot}}}$$

$$Z_{in9} = 245.609\Omega$$

Measuring the input impedance of M_9 with a smaller frequency such as 1 MHz would give

$$Z_{in9_{1\,MHz}} = 2.456\ M\Omega$$

Z_{in9} is a small number as compared to $Z_{in9_{1\,MHz}}$, but still a large value relative to the low output impedance amplifier.

The largest transistor (M'_7) used in this work has width of 180 μm, which works as a current mirror. For this transistor, the input signal is a DC voltage hence high frequency does not interact with gate of this transistor. In absence of high frequency, the performance of this transistor does not deteriorate.

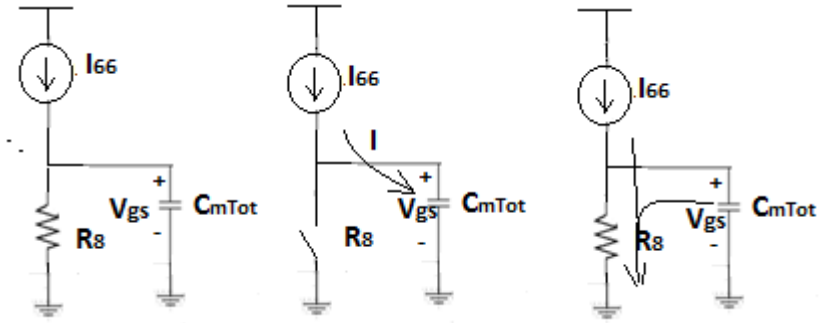

Figure 4.16 Working of the active load common source in presence of capacitive load

In figure 4.16 the active load works as a current source. The current output from the current source I_{66} is assumed to be constant, Due to this current charging and discharging of c_{M_tot} of M_9 are shown in figure 4.20. Charging and discharging of c_{M_tot} causes V_{GS} of M_9 to change, this V_{GS} is then amplified at the output of the last stage.

4.8 Jitter Calculation of the Circuit [11]

The jitter produced by the CMOS differential ring oscillator is given by equation (4.24)[11]

$$\sigma_t{}^2 = \frac{kT}{If_0}\left(\frac{2}{V_{DD}-V_{th}}\left(\gamma_n + \gamma_p\right) + \frac{2}{V_{DD}}\right) \quad (4.24)$$

Here $\sigma_t{}^2$ is the mean square value of the jitter, k is the constant for transistor, T is the temperature, I is the current in each delay cell used, f_0 is the natural frequency, V_{DD} is the supply voltage, V_{th} is the threshold voltage and γ_n and γ_p are the body bias coefficients for the NMOS

and the PMOS transistors respectively. The value of f_0 can be calculated with the help of equation (3.2), in equation (3.2) θ_{tot} is equal to 45^0.

According to the equation (3.2)

$$\tan^{-1}\frac{\omega_{osc}}{\omega_0} = 45^0$$

This gives

$$\omega_{osc} = \omega_0$$

Thus

$$f_{osc} = f_0$$

The value of γ_n from [12]

$$\gamma_n = \frac{\sqrt{(2q\varepsilon_{si}N_{substrate})}}{C_{oxe}} \quad (4.25)$$

$$C_{oxe} = \frac{EPSROX.\varepsilon_0}{TOXE}$$

$$\gamma_p = \frac{\sqrt{(2q\varepsilon_{si}N_{substrate})}}{C_{oxp}} \quad (4.26)$$

$$C_{oxp} = \frac{EPSROX \cdot \varepsilon_0}{TOXP}$$

$N_{substrate} = NSUB$ = NDEP

Here ε_{si} = 11.68 is a constant for silicon, TOXE, TOXP, EPSROX and NSUB are the transistors M_1 and M_2's parameters taken from Appendix A. q is the charge of an electron. Keeping all values in (4.25) and (4.26) gives the value of γ_n and γ_p.

$\gamma_n = 0.2488$, $\gamma_p = 0.205$

Putting values of γ_n and γ_p in equation (4.24) [11]

$$\sigma_t{}^2 = \frac{1.38\,X10^{-23}\cdot 300}{1X10^{-3}\cdot 8\cdot 10^9}\left(\frac{2}{1-\ 0.39}(0.2488+\ 0.205)+\frac{2}{1}\right)$$

Gives

$$\sigma_t{}^2 = 5.231X10^{-3} = -45.626\ dBc/Hz$$

The jitter noise in the time domain is

$$T_{jRMS} = \frac{10^{(\sigma_{tdb}{}^2/_{20})}}{\sqrt{2}.\pi.f_0} = 1.81 \text{ psec} \qquad (4.27)$$

The RMS jitter in the jitter histogram shown in figure 4.17 is the standard deviation of the jitter. Relationship between T_{jRMS} and T_{pp}(Peak to Peak Jitter)) given by equation (4.28).[12]

$$T_{jRMS} = \frac{Tpp}{\alpha} \qquad (4.28)$$

Here α is the scaling factor for the given BER (Bit Error Rate). For the BER of 10^{-5}, α is equal to 8.53 [12]. Hence equation (4.28) gives

$T_{pp} = \alpha \cdot T_{jRMS}$

$T_{pp} =$ 8.53$\cdot$ 1.28

$T_{pp} = 10.9184$ psec.

The peak-to-peak jitter is the measure of RMS jitter, which in circuit is 1.81 peco seconds. The peak-to-peak jitter noise determined from the simulation is 11 psec., which is close to the determined value of the peak-to-peak jitter from the simulation.

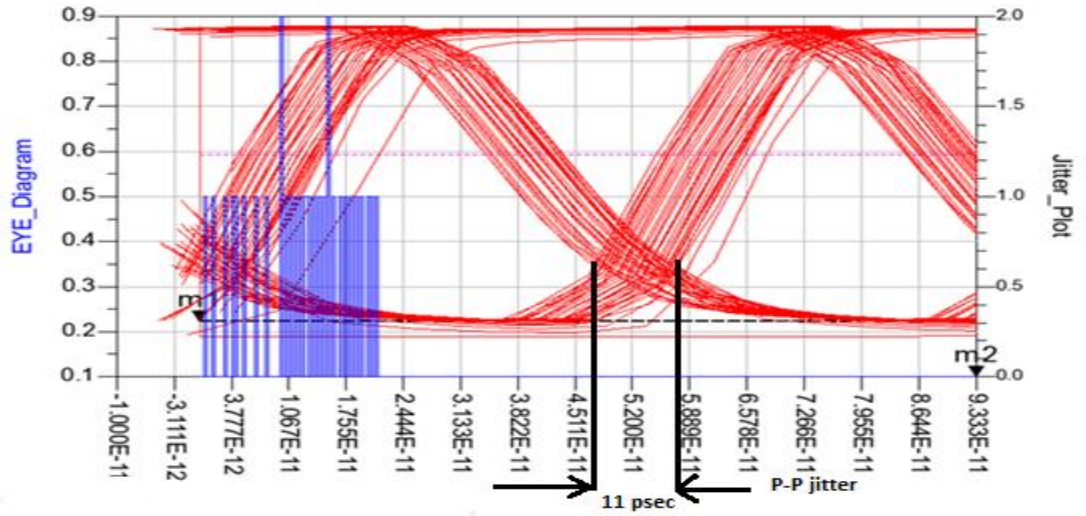

Figure 4.17 The eye-diagram and peak to peak jitter in the waveform

4.9 Combined Circuit

The combined circuit with the VCO core, the buffer, and the current mirror is shown in figure 4.18.

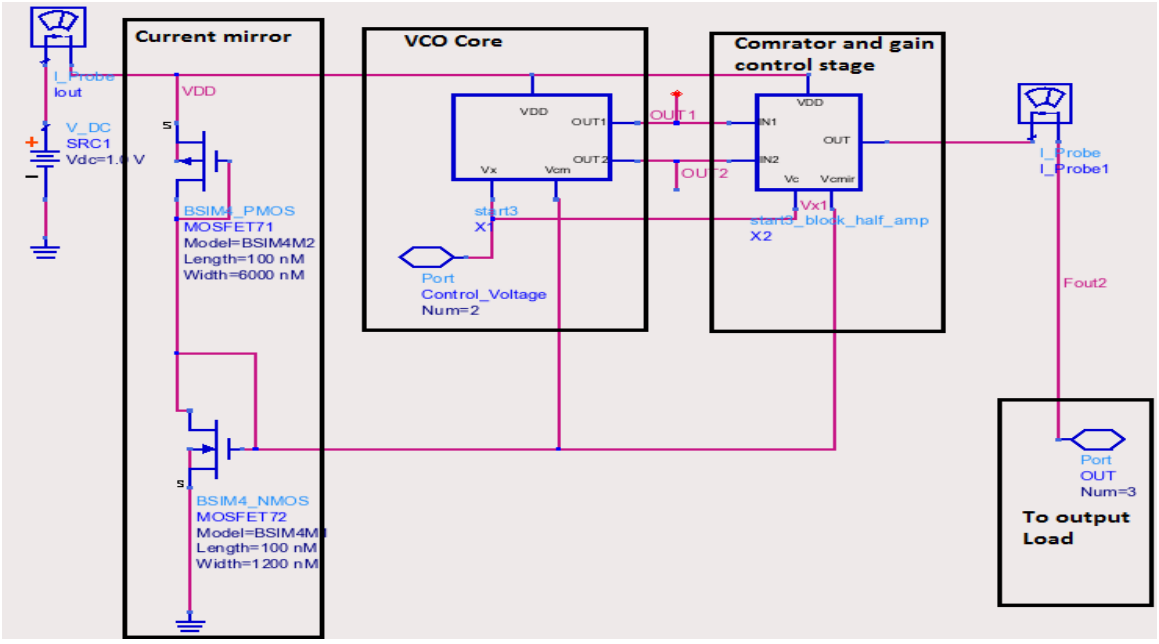

Figure 4.18 Combined circuit

A final circuit complete with output load is shown in figure 4.19

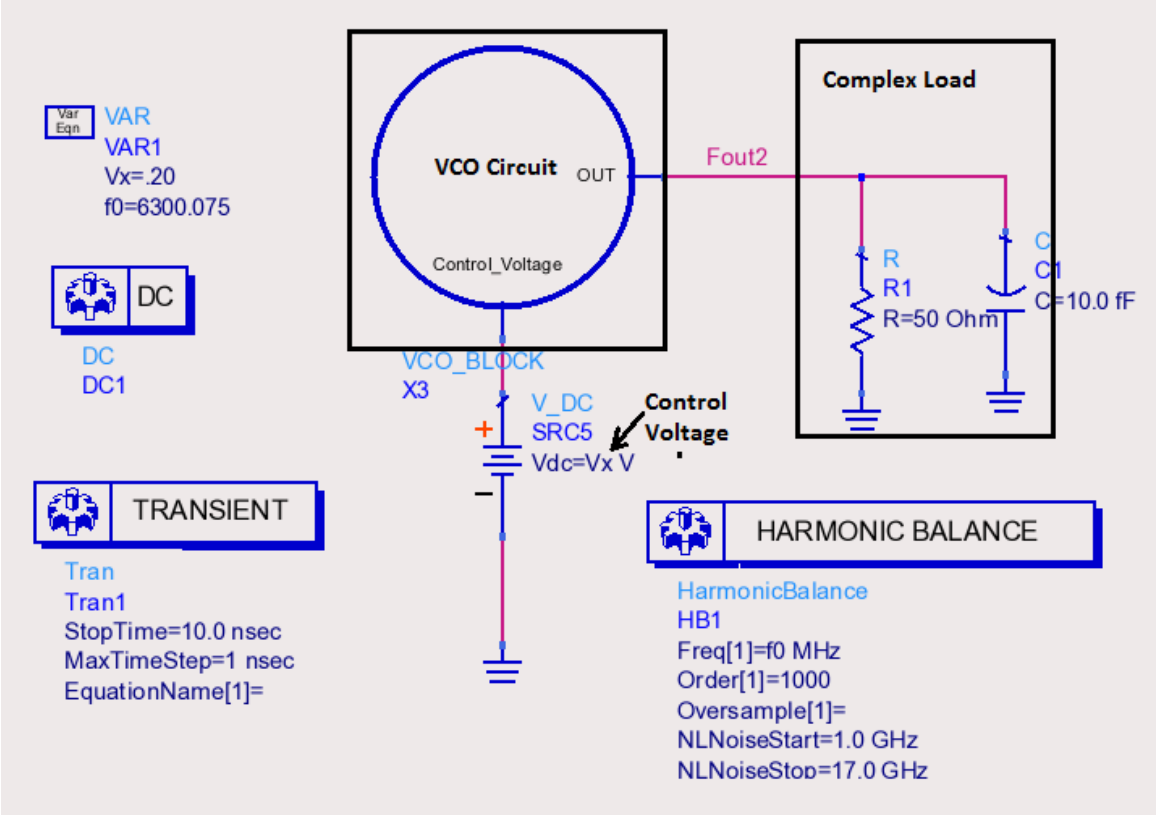

Figure 4.19 The final top level circuit

CHAPTER 5

SIMULATION RESULTS

5.1 Frequency Generation

The actual frequency range achieved in the simulation was 9.099 GHz for 0 volts and 5.100 GHz for 0.5 volts. However, the VCO was designed for 5 – 10 GHz. The error depends on many factors since many values, which were assumed constant, are actually not, such as the threshold voltage and the transconductance. Values of V_{th} and g_m vary with body bias and biasing voltage. Formulas that are more accurate are available too, but due to the complexities and large number of calculations present in this case, simpler but slightly less accurate formulas have been used.

Figure 5.1 shows range of frequencies between 5.1 to 9.099 GHz. The marker m3 marks the frequency of 5.1 GHz for the control voltage of 0.5 volts and the marker m20 marks 9.099 GHz frequency for the control voltage of 0 volts. The harmonic distortions are marked by the markers m15 and m16. The harmonic distortions are below -25 db and at least 5 GHz apart from the dominant harmonics.

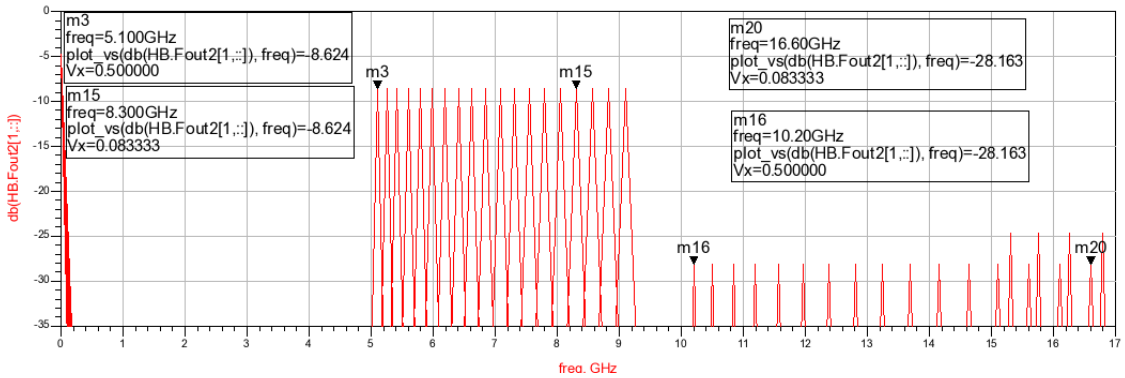

Figure 5.1 Output signals at the different control voltages

5.2 Effect of the Variable Gain Amplifying Stages or Buffers

Two figures 5.2 and 5.3 demonstrate the effect of the buffer and gain control stage in the circuit. Figure 5.3 shows the output harmonics before the use of the buffer stage and figure 5.2 shows the resultant harmonics after using the buffer stage.

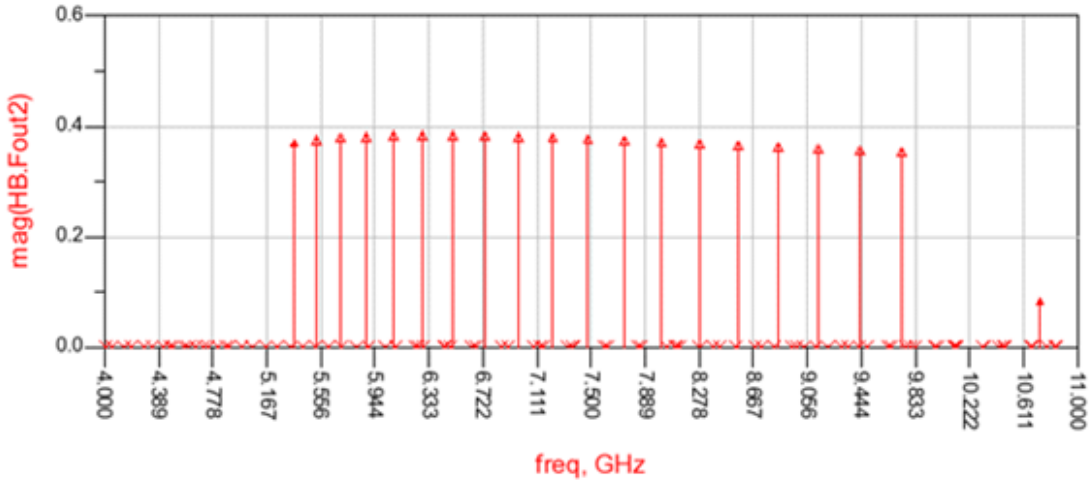

Figure 5.2 Effect of gain control at the output load

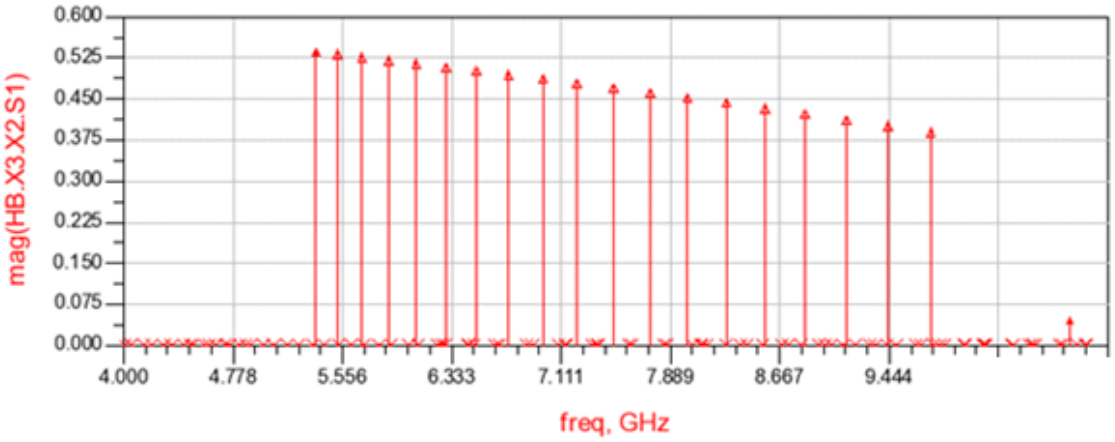

Figure 5.3 The gain variation before buffer mechanism

5.3 Power Dissipation in the VCO Core [Appendix C]

Figure 5.4 illustrates current dissipation with respect to the control voltage in the VCO while figure 5.5 is curve between total power dissipation and the control voltage in the VCO.

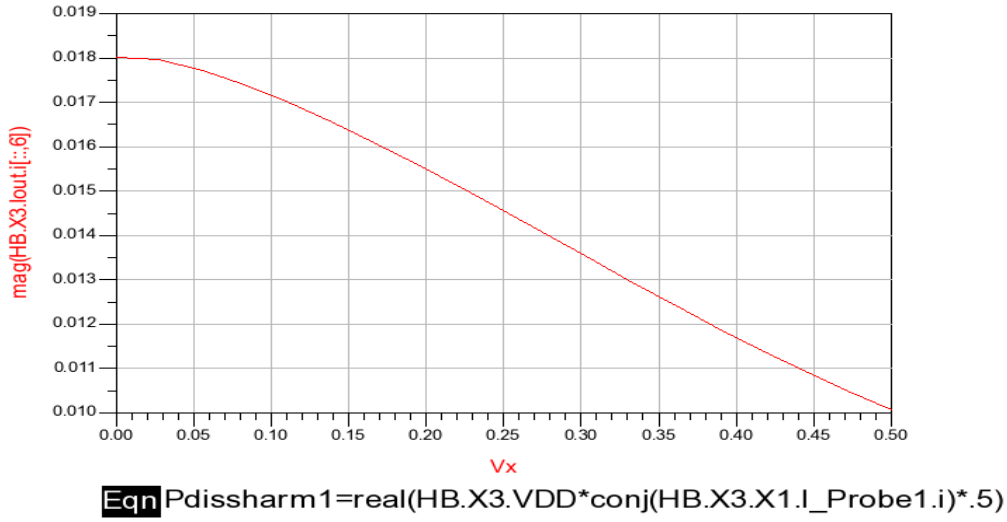

Figure 5.4 Total current dissipation in the VCO

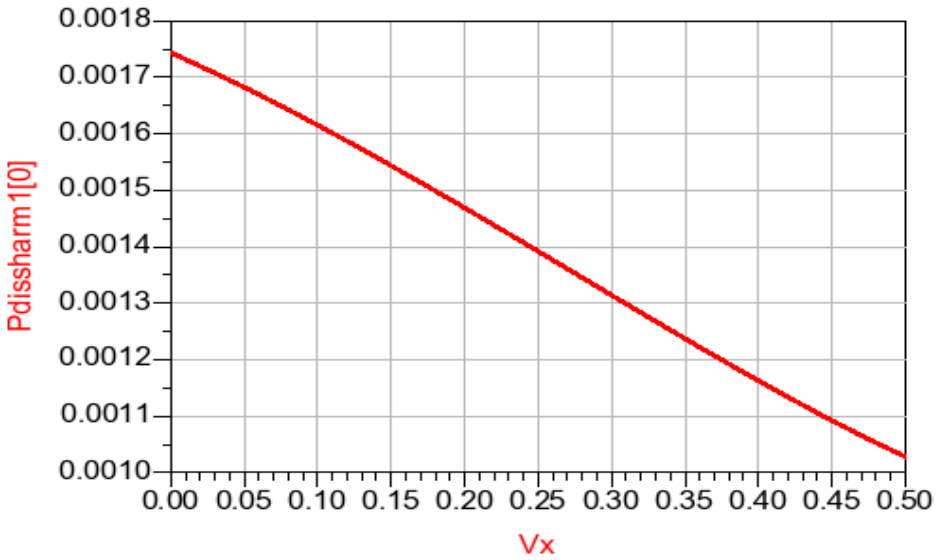

Figure 5.5 The power dissipation in the VCO

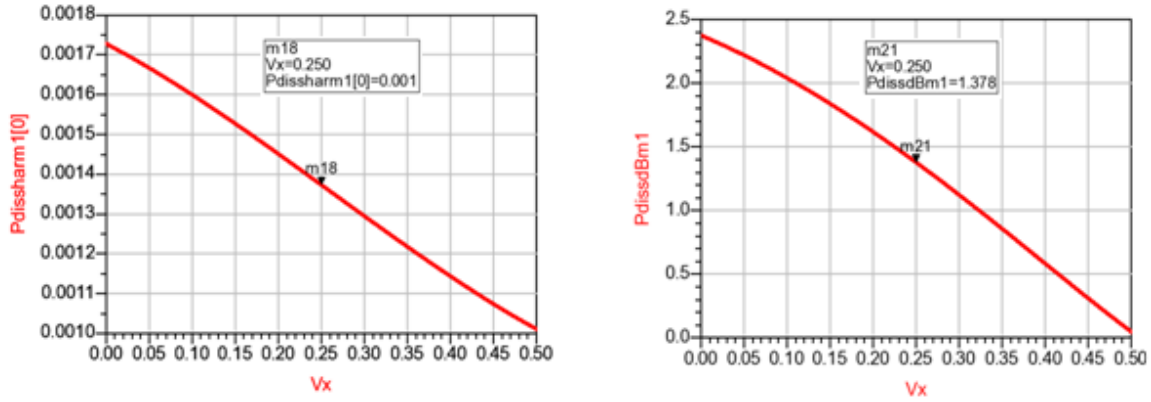

Figure 5.6 The power dissipation in the VCO core

Figure 5.6 shows the power dissipation in the VCO core with respect to the control voltage.

5.4 AC Power at the Output

The buffer provides 1.65 mw to the load , This value varies between 1.1 mw to 1.52 mw with respect to the control voltage as shown in figure 5.7

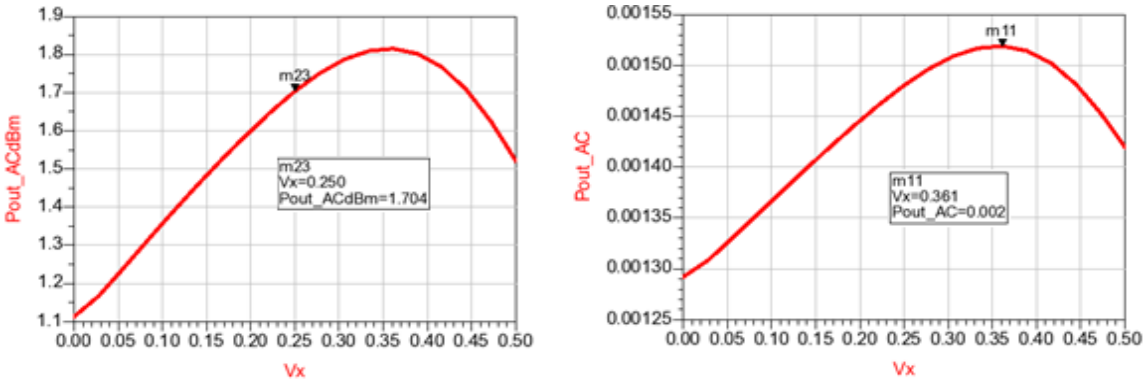

Figure 5.7 The power delivered to the load

5.5 Control Voltage Linearity

Figure 5.8 shows the variation of the frequency with respect to the control voltage, this curve is almost linear for the whole range of frequency. With further increase in the voltage towards 0.7 volts, the frequency still changes but errors increase since the PMOS device goes out of the saturation and starts to enter the linear region.

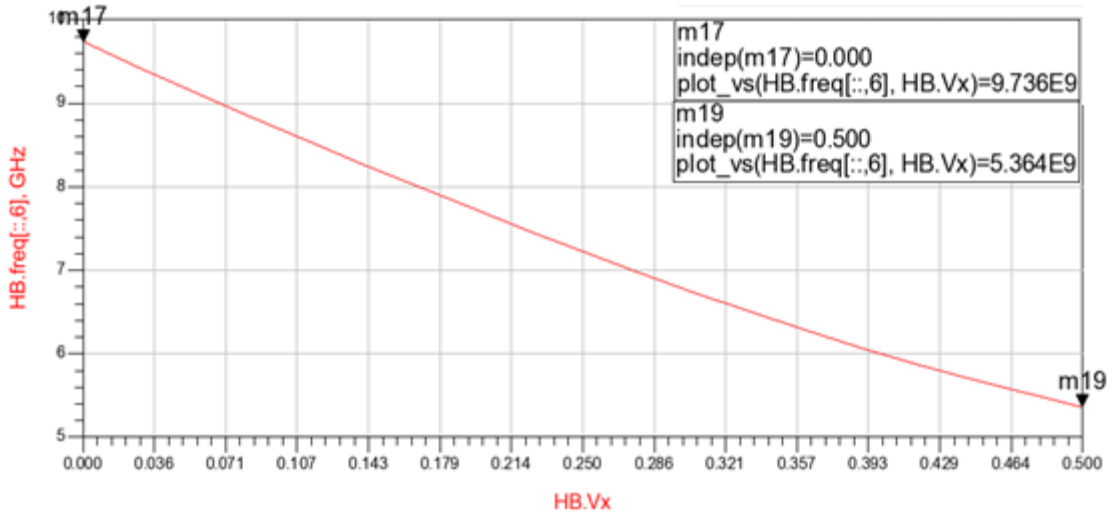

Figure 5.8 Frequency versus control voltage graph

5.6 Variation of Frequency With Respect To the Ideal Frequency

Figure 5.9 below shows the comparison between the ideal frequency with the achieved frequency. A plot between the error (in percentage) and the control voltage has been plotted in figure. [Appendix B]

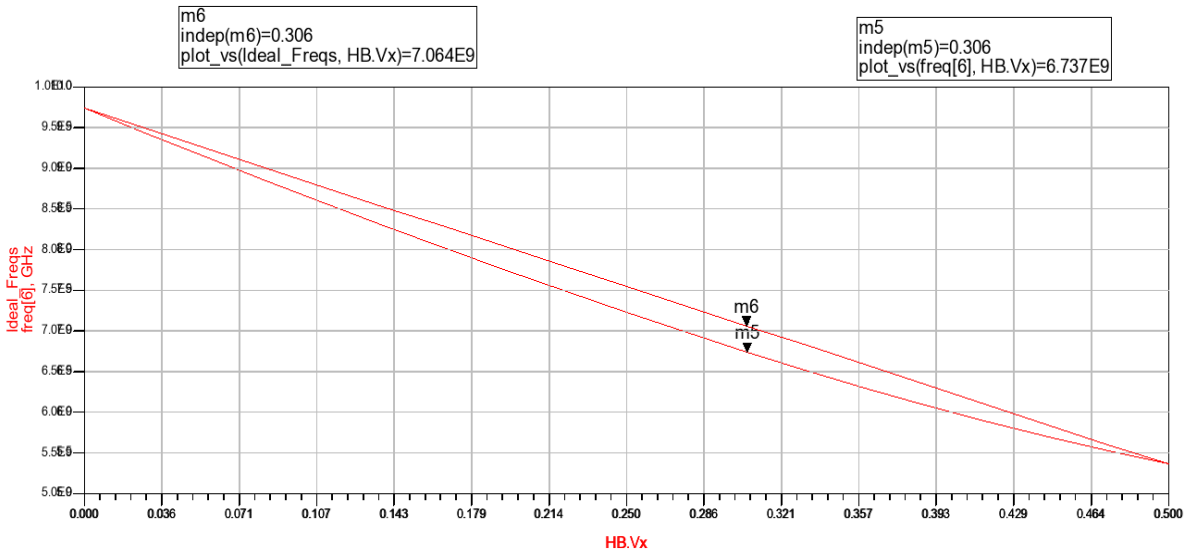

Figure 5.9 Ideal frequency versus achieved frequency

In figure 5.10 percentage error between the ideal frequency variation and the achieved frequency has been drawn with respect to the control voltage [Appendix A]. The figure 5.10 demonstrates that maximum error between ideal frequency and achieved frequency is -4.85% at the control voltage of 0.306.

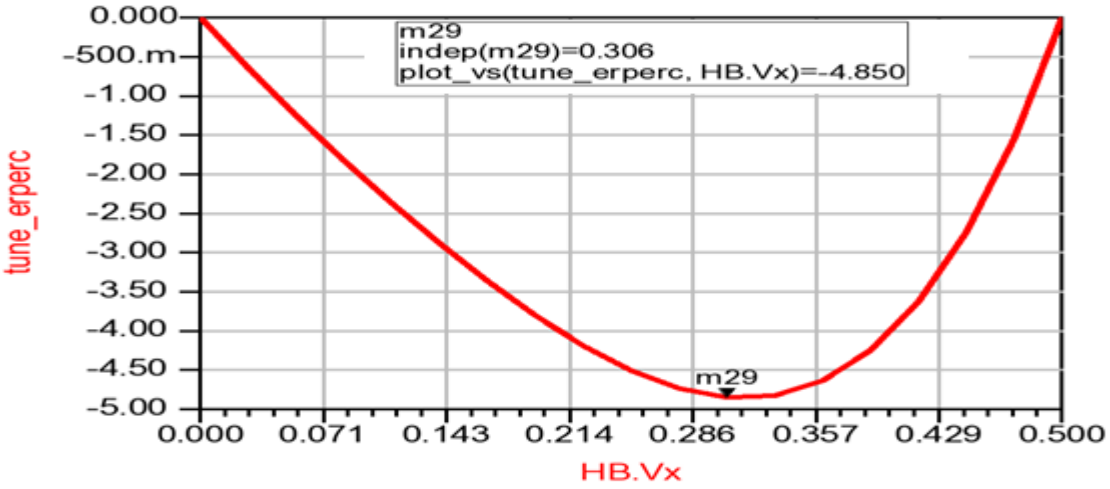

Figure 5.10 Frequency Error (in percentage) plot with respect to control voltage

5.7 Transient Response of the VCO

The transient responses from 0 volts, 0.2 volts and 0.5 volts has been plotted

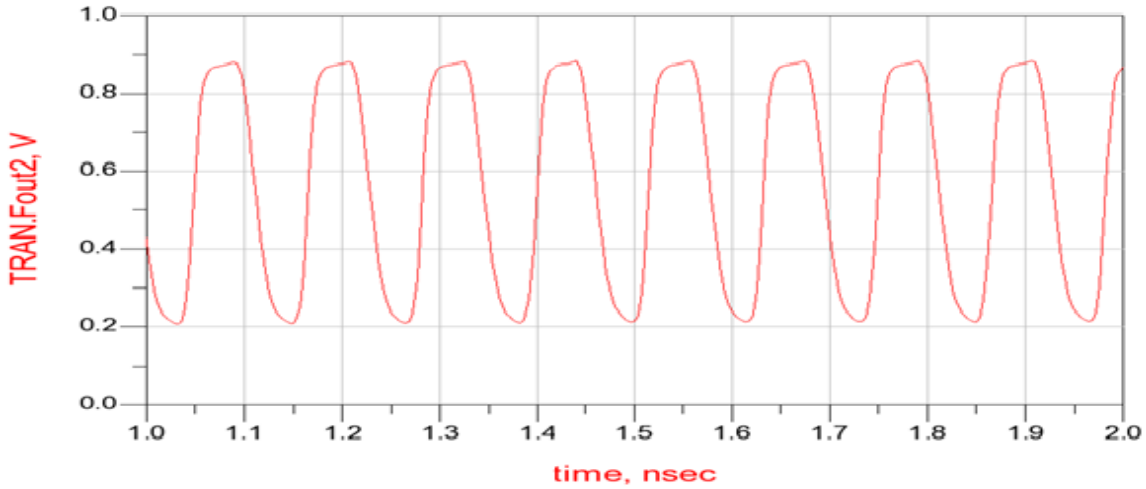

Figure 5.11 Transient frequency at 0 volts

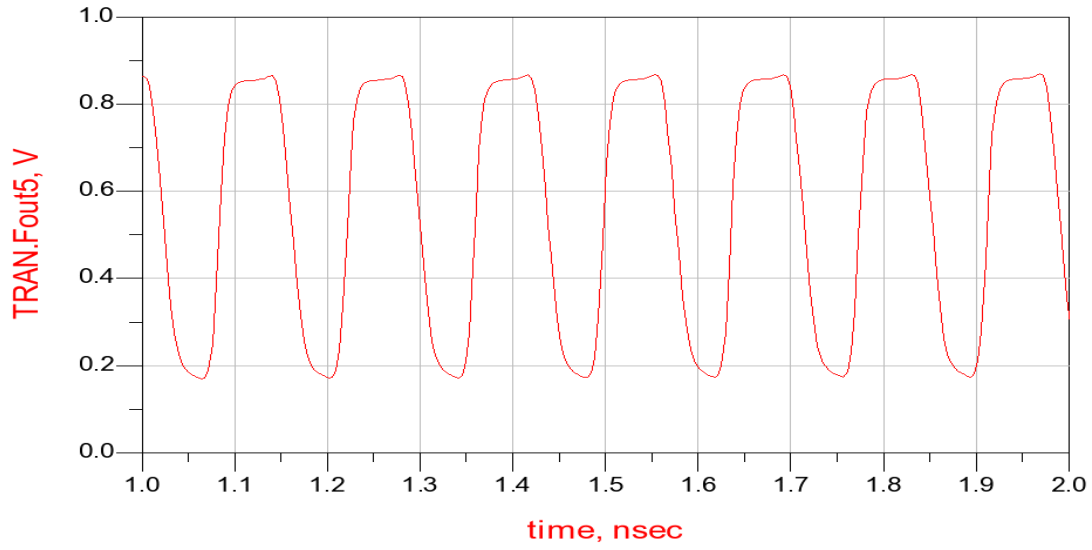

Figure 5.12 Transient frequency at 0.25 volts

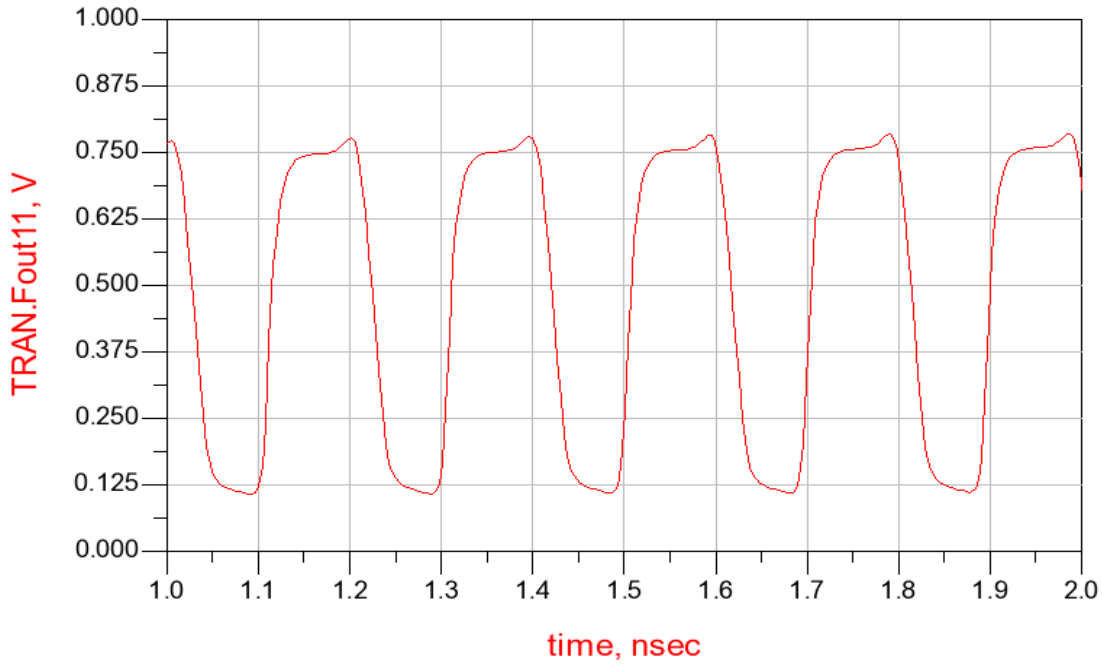

Figure 5.13 Transient frequency at 0.5 volts

5.8 Jitter Noise in the Oscillator

The eye diagram of the signal from the VCO has been drawn with the histogram of the jitter in figure 5.14

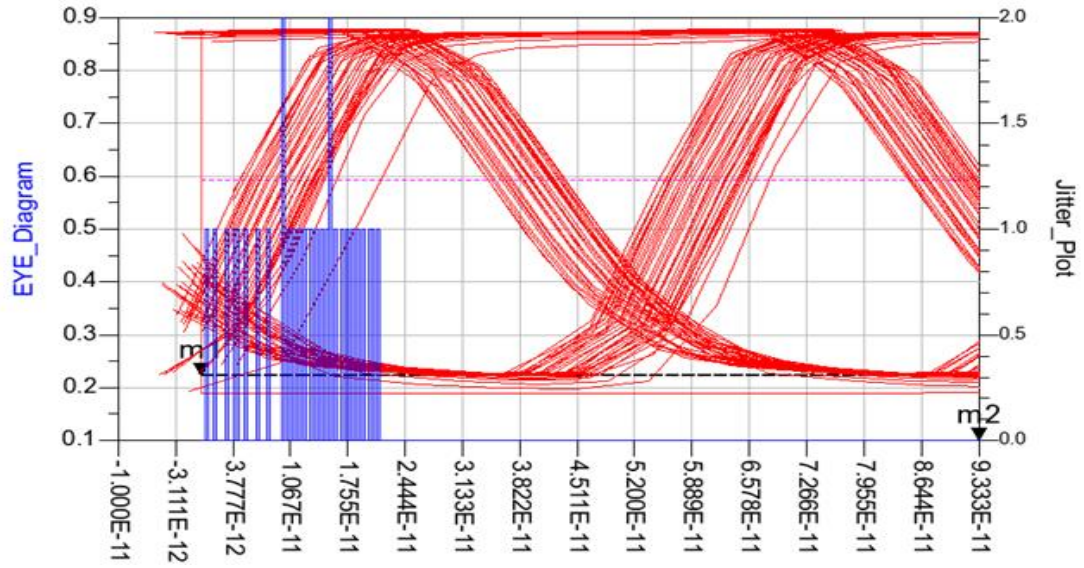

Figure 5.14 Jitter plot with eye diagram

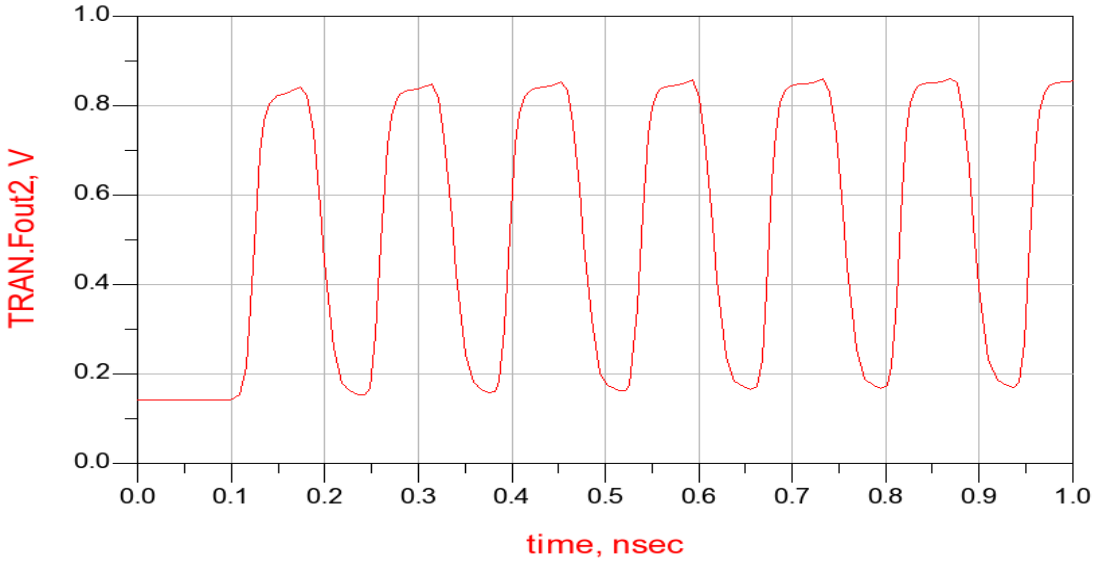

Figure 5.15 waveform used for jitter measurement

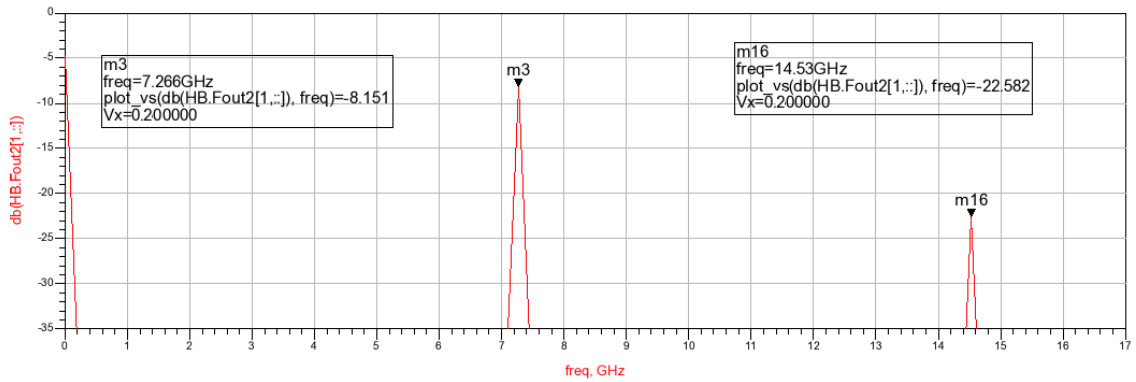

Figure 5.16 Frequency domain illustration for the signal used for jitter analysis

Figure 5.16 shows above the peak-to-peak jitter determined from the circuit, figure 5.11 is the time domain sinusoidal signal used for the jitter analysis and figure 5.12 shows the frequency domain illustration for the same frequency. The marker m3 in figure 5.12 marks the dominant harmonic of the signal, which is at 7.266 GHz, while the marker m16 marks the harmonic distortion signal at 14.53 GHz.

CHAPTER 6

CONCLUSION

6.1 Conclusion and the Future Work

The differential VCO designed here meets the design goal, but a number of compensations are required. The same control voltage is used for many purposes.

The buffer stage worked very well with the amplitude of output sinusoid remains constant for different frequencies, while sub-harmonics are below -25 db. Each sub-harmonic is at least 5 GHz away from the dominant harmonics as evident from figure 5.13. The frequency range of 5.1 to 9.1 GHz is wide, and matching this frequency to the low impedance load is achieved without the use of any passive elements such as inductor or capacitor. Inductors and capacitors take large area as compared to the CMOS transistors; hence this work will save chip area thereby reduce costs in productions.

The peak-to-peak jitter is 11 psec., which makes this VCO good for the timing signal generation. The frequency variation with the control voltage has been extremely linear and showed minor amount of error. The sinusoidal signal appeared at the output is fairly clean and constant. Increasing the number of stages and having cascaded current source can be helpful to achieve better performance.

APPENDIX A

MODEL FILE

Values of Design Parameters Used in the Circuit

* Beta Version			on 2/22/06								
* PTM 90nm		NMOS									
.model		nmos									
nmos		level	54								
						paramchk	=	1	mobmod	=	0
+version	=	4	binunit	=	1						
+capmod	=	2	igcmod	=	1	igbmod	=	1	geomod	=	1
+diomod	=	1	rdsmod	=	0	rbodymod	=	1	rgatemod	=	1
+permod	=	1	acnqsmod	=	0	trnqsmod	=	0			
+tnom	=	27	toxe	=	2.05E-09	toxp	=	1.40E-09	toxm	=	2.05E-09
+dtox	=	6.50E-10	epsrox	=	3.9	wint	=	5.00E-09	lint	=	7.50E-09
+ll	=	0	wl	=	0	lln	=	1	wln	=	1
+lw	=	0	ww	=	0	lwn	=	1	wwn	=	1
+lwl	=	0	wwl	=	0	xpart	=	0	toxref	=	2.05E-09
+xl	=	-4.00E-08									
+vth0	=	0.397	k1	=	0.4	k2	=	0.01	k3	=	0
+k3b	=	0	w0	=	2.50E-06	dvt0	=	1	dvt1	=	2
+dvt2	=	-0.032	dvt0w	=	0	dvt1w	=	0	dvt2w	=	0
+dsub	=	0.1	minv	=	0.05	voffl	=	0	dvtp0	=	1.20E-09
+dvtp1	=	0.1	lpe0	=	0	lpeb	=	0	xj	=	2.80E-08
+ngate	=	2.00E+20	ndep	=	1.94E+18	nsd	=	2.00E+20	phin	=	0
+cdsc	=	0.0002	cdscb	=	0	cdscd	=	0	cit	=	0
+voff	=	-0.13	nfactor	=	1.7	eta0	=	0.0074	etab	=	0
+vfb	=	-0.55	u0	=	0.0547	ua	=	6.00E-10	ub	=	1.20E-18
+uc	=	-3.00E-11	vsat	=	113760	a0	=	1	ags	=	1.00E-20
+a1	=	0	a2	=	1	b0	=	-1.00E-20	b1	=	0
+keta	=	0.04	dwg	=	0	dwb	=	0	pclm	=	0.06

+pdiblc1	=	0.001	pdiblc2	=	0.001	pdiblcb	=	-0.005	drout	=	0.5
+pvag	=	1.00E-20	delta	=	0.01	pscbe1	=	8.14E+08	pscbe2	=	1.00E-07
+fprout	=	0.2	pdits	=	0.08	pditsd	=	0.23	pditsl	=	2.30E+06
+rsh	=	5	rdsw	=	180	rsw	=	90	rdw	=	90
+rdswmin	=	0	rdwmin	=	0	rswmin	=	0	prwg	=	0
+prwb	=	6.80E-11	wr	=	1	alpha0	=	0.074	alpha1	=	0.005
+beta0	=	30	agidl	=	0.0002	bgidl	=	2.10E+09	cgidl	=	0.0002
+egidl	=	0.8									
+aigbacc	=	0.012	bigbacc	=	0.0028	cigbacc	=	0.002			
+nigbacc	=	1	aigbinv	=	0.014	bigbinv	=	0.004	cigbinv	=	0.004
+eigbinv	=	1.1	nigbinv	=	3	aigc	=	0.012	bigc	=	0.0028
+cigc	=	0.002	aigsd	=	0.012	bigsd	=	0.0028	cigsd	=	0.002
+nigc	=	1	poxedge	=	1	pigcd	=	1	ntox	=	1
+xrcrg1	=	12	xrcrg2	=	5						
+cgso	=	1.90E-10	cgdo	=	1.90E-10	cgbo	=	2.56E-11	cgdl	=	2.65E-10
+cgsl	=	2.65E-10	ckappas	=	0.03	ckappad	=	0.03	acde	=	1
+moin	=	15	noff	=	0.9	voffcv	=	0.02			
+kt1	=	-0.11	kt1l	=	0	kt2	=	0.022	ute	=	-1.5
+ua1	=	4.31E-09	ub1	=	7.61E-18	uc1	=	-5.60E-11	prt	=	0
+at	=	33000									
+fnoimod	=	1	tnoimod	=	0						
+jss	=	0.0001	jsws	=	1.00E-11	jswgs	=	1.00E-10	njs	=	1
+ijthsfwd	=	0.01	ijthsrev	=	0.001	bvs	=	10	xjbvs	=	1
+jsd	=	0.0001	jswd	=	1.00E-11	jswgd	=	1.00E-10	njd	=	1
+ijthdfwd	=	0.01	ijthdrev	=	0.001	bvd	=	10	xjbvd	=	1
+pbs	=	1	cjs	=	0.0005	mjs	=	0.5	pbsws	=	1
+cjsws	=	5.00E-10	mjsws	=	0.33	pbswgs	=	1	cjswgs	=	3.00E-10

+mjswgs	=	0.33	pbd	=	1	cjd	=	0.0005	mjd	=	0.5
+pbswd	=	1	cjswd	=	5.00E-10	mjswd	=	0.33	pbswgd	=	1
+cjswgd	=	5.00E-10	mjswgd	=	0.33	tpb	=	0.005	tcj	=	0.001
+tpbsw	=	0.005	tcjsw	=	0.001	tpbswg	=	0.005	tcjswg	=	0.001
+xtis	=	3	xtid	=	3						
+dmcg	=	0.00E+00	dmci	=	0.00E+00	dmdg	=	0.00E+00	dmcgt	=	0.00E+00
+dwj	=	0.00E+00	xgw	=	0.00E+00	xgl	=	0.00E+00			
+rshg	=	0.4	gbmin	=	1.00E-10	rbpb	=	5	rbpd	=	15
+rbps	=	15	rbdb	=	15	rbsb	=	15	ngcon	=	1

* PTM
90n m PMOS
.model pmos pmos level 54

+version	=	4	binunit	=	1	paramchk	=	1	mobmod	=	0
+capmod	=	2	igcmod	=	1	igbmod	=	1	geomod	=	1
+diomod	=	1	rdsmod	=	0	rbodymod	=	1	rgatemod	=	1
+permod	=	1	acnqsmod	=	0	trnqsmod	=	0			
+tnom	=	27	toxe	=	2.15E-09	toxp	=	1.40E-09	toxm	=	2.15E-09
+dtox	=	7.50E-10	epsrox	=	3.9	wint	=	5.00E-09	lint	=	7.50E-09
+ll	=	0	wl	=	0	lln	=	1	wln	=	1
+lw	=	0	ww	=	0	lwn	=	1	wwn	=	1
+lwl	=	0	wwl	=	0	xpart	=	0	toxref	=	2.15E-09
+xl	=	-4.00E-08									
+vth0	=	-0.339	k1	=	0.4	k2	=	-0.01	k3	=	0
+k3b	=	0	w0	=	2.50E-06	dvt0	=	1	dvt1	=	2

+dvt2	=	-0.032	dvt0w	=	0	dvt1w	=	0	dvt2w	=	0
+dsub	=	0.1	minv	=	0.05	voffl	=	0	dvtp0	=	1.00E-09
+dvtp1	=	0.05	lpe0	=	0	lpeb	=	0	xj	=	2.80E-08
+ngate	=	2.00E+2	ndep	=	1.43E+1	nsd	=	2.00E+2	phin	=	0
+cdsc	=	0.00026	cdscb	=	0	cdscd	=	6.10E-08	cit	=	0
+voff	=	-0.126	nfactor	=	1.7	eta0	=	0.0074	etab	=	0
+vfb	=	0.55	u0	=	0.00711	ua	=	2.00E-09	ub	=	5.00E-19
+uc	=	-3.00E-11	vsat	=	70000	a0	=	1	ags	=	1.00E-20
+a1	=	0	a2	=	1	b0	=	0	b1	=	0
+keta	=	-0.047	dwg	=	0	dwb	=	0	pclm	=	0.12
+pdiblc1	=	0.001	pdiblc2	=	0.001	pdiblcb	=	3.40E-08	drout	=	0.56
+pvag	=	1.00E-20	delta	=	0.01	pscbe1	=	8.14E+08	pscbe2	=	9.58E-07
+fprout	=	0.2	pdits	=	0.08	pditsd	=	0.23	pditsl	=	2.30E+06
+rsh	=	5	rdsw	=	200	rsw	=	100	rdw	=	100
+rdswmin	=	0	rdwmin	=	0	rswmin	=	0	prwg	=	3.22E-08
+prwb	=	6.80E-11	wr	=	1	alpha0	=	0.074	alpha1	=	0.005
+beta0	=	30	agidl	=	0.0002	bgidl	=	2.10E+09	cgidl	=	0.0002
+egidl	=	0.8									
+aigbacc	=	0.012	bigbacc	=	0.0028	cigbacc	=	0.002			
+nigbacc	=	1	aigbinv	=	0.014	bigbinv	=	0.004	cigbinv	=	0.004
+eigbinv	=	1.1	nigbinv	=	3	aigc	=	0.69	bigc	=	0.0012
+cigc	=	0.0008	aigsd	=	0.0087	bigsd	=	0.0012	cigsd	=	0.0008
+nigc	=	1	poxedge	=	1	pigcd	=	1	ntox	=	1
+xrcrg1	=	12	xrcrg2	=	5						
+cgso	=	1.80E-10	cgdo	=	1.80E-10	cgbo	=	2.56E-11	cgdl	=	2.65E-10
+cgsl	=	2.65E-10	ckappas	=	0.03	ckappad	=	0.03	acde	=	1

+moin	=	15	noff	=	0.9	voffcv	=	0.02		
+kt1	=	-0.11	kt1l	=	0	kt2	=	0.022	ute	=	-1.5
+ua1	=	4.31E-09	ub1	=	7.61E-18	uc1	=	-5.60E-11	prt	=	0
+at	=	33000	fnoimod	=	1	tnoimod	=	0			
+jss	=	0.0001	jsws	=	1.00E-11	jswgs	=	1.00E-10	njs	=	1
ijthsfwd	=	0.01	ijthsrev	=	0.001	bvs	=	10	xjbvs	=	1
+jsd	=	0.0001	jswd	=	1.00E-11	jswgd	=	1.00E-10	njd	=	1
ijthdfwd	=	0.01	ijthdrev	=	0.001	bvd	=	10	xjbvd	=	1
+pbs	=	1	cjs	=	0.0005	mjs	=	0.5	pbsws	=	1
+cjsws	=	5.00E-10	mjsws	=	0.33	pbswgs	=	1	cjswgs	=	3.00E-10
+mjswgs	=	0.33	pbd	=	1	cjd	=	0.0005	mjd	=	0.5
+pbswd	=	1	cjswd	=	5.00E-10	mjswd	=	0.33	pbswgd	=	1
+cjswgd	=	5.00E-10	mjswgd	=	0.33	tpb	=	0.005	tcj	=	0.001
+tpbsw	=	0.005	tcjsw	=	0.001	tpbswg	=	0.005	tcjswg	=	0.001
+xtis	=	3	xtid	=	3						
+dmcg	=	0.00E+00	dmci	=	0.00E+00	dmdg	=	0.00E+00	dmcgt	=	0.00E+00
+dwj	=	0.00E+00	xgw	=	0.00E+00	xgl	=	0.00E+00			
+rshg	=	0.4	gbmin	=	1.00E-10	rbpb	=	5	rbpd	=	15
+rbps	=	15	rbdb	=	15	rbsb	=	15	ngcon	=	1

APPENDIX B

FORMULAS USED FOR SIMULATIONS

Calculations for tuning error

Eqn MaxVxIndex=sweep_size(HB.Vx)

Eqn Avg_slope=(freq[MaxVxIndex-1,6] -freq[0,6])/(HB.Vx[MaxVxIndex-1] -HB.Vx[0])

Eqn Freq0=freq[0,6]

Eqn Vbdc_step=HB.Vx[1]-HB.Vx[0]

Eqn Ideal_Freqs=Freq0 +[0::MaxVxIndex-1]*Vbdc_step*Avg_slope

Eqn Tuning_error=freq[6]-Ideal_Freqs

Eqn tune_erperc=((freq[6]-Ideal_Freqs)/freq[6])*100

APPENDIX C

FORMULAS USED FOR THE OUTPUT POWER

Total power dissipated

Eqn Pdissharm=real(HB.X3.VDD*conj(HB.X3.SRC1.i)*.5)

Power dissipation in dBm

Eqn PdissdBm=10*log(Pdissharm[0])+30

DC power dissipation

Eqn Pout_DC=Poutharm[0]

DC power in dBm

Eqn Pout_DCdBm=10*log(Poutharm[0])+30

Harmonic power delivered to load

Eqn Poutharm=real(HB.Fout2*conj(HB.X3.I_Probe1.i)*.5)

Desired harmonic power to load

Eqn Pout_AC=Poutharm[6]

total harmonic power disspation in VCO core

Eqn Pdissharm1=real(HB.X3.VDD*conj(HB.X3.X1.I_Probe1.i)*.5)

Power dissipation in VCO Core in dBm

Eqn PdissdBm1=10*log(Pdissharm1[0])+30

Desired AC power output in dBm

Eqn Pout_ACdBm=10*log(Poutharm[6])+30

total power at load in dBm

Eqn Pout_totaldBm=10*log(Poutharm[6]+Poutharm[0])+30

APPENDIX D

FORMULAS USED FOR THE JITTER MEASUREMENT

```
Eqn eye_diagram=eye(Time_waveform,sym)
Eqn eye_jitter=cross_hist(Time_waveform,time1,time2,m1,m2,nbin,sym,n,delay1,steps)
Eqn delay1=0
Eqn nbin=300
Eqn n=1
Eqn Time_waveform=TRAN.Fout2
Eqn a8=(a7-a6)/200
Eqn sym=9.90 Ghz
Eqn steps=20
Eqn a6=min(Time_waveform)
Eqn a7=max(Time_waveform)
Eqn a4=vs(m2,[time1::a3::time2])
Eqn a5=vs(m1,[time1::a3::time2])

Eqn time1=0
Eqn time2=n/sym
Eqn a3=(time2-time1)/400
Eqn a10=vs(a9,0)
Eqn a11=vs(a9,time2)
Eqn a9=[a6::a8::a7]
```

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BIOGRAPHICAL INFORMATION

Sourabh Sharma received his Bachelor of Engineering degree in Electronics and Telecommunication Engineering from Bhilai Institute of Technology (Pt. Ravishankar Shukla University) Durg Chhattisgarh, India, in June 2005. After completion of his studies he joined Qualcore Logic Inc. (Hyderabad) as an ASIC engineer. He left his job at October 2008 for further studies, pursued his master's studies at the University of Texas at Arlington from January 2009, and received his M.S. degree in Electrical Engineering in May 2011.