SIMULATION AND E-BEAM PATTERNING OF SINGLE ELECTRON TRANSISTOR

by

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ABSTRACT

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Electron beam lithography is gaining widespread use as semiconductor industry. Current optical lithography techniques are limited to resolution of few hundreds of nanometers and suffer from diffraction problems.

The focus of this thesis is to pattern single electron transistors (SET) using electron beam lithography on silicon and silicon on insulator (SOI) substrate which can be further processed to form working SET device. We used different types of e-beam resists like UVN 30, PMMA and HSQ to define source, drain and island for SET. We demonstrated the use of RIE and Deep RIE to etch silicon by using resist as etch mask.

Single electron transistor is simulated using a MATLAB program. This program calculates the current through SET as a function of drain-source voltage, V_{DS}, for a given values of gate voltage Vg, which is predefined in the program. Simulations are performed at various temperatures from 4.2K and 77K.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS.. iii

ABSTRACT iv

LIST OF ILLUSTRATIONS.. x

LIST OF TABLES.. xiii

Chapter Page

1. INTRODUCTION 1

1.1 Single Electronics…… 1

1.2 Single Electron BOX ……… 5

1.2.1 Problems with Single Electron BOX ……… 6

1.3 Single Electron Transistor…………… 6

1.3.1 Operation of SET………… 7

1.4 Issues with SET………………………………………………………… 9

1.4.1 Limitations of SET………….. 9

1.4.2 Solution ……….. 11

1.5 Applications of SET…………………………………………………. 11

1.5.1 Electrometer ……….. 11

1.5.2 Single Electron Memory……… 12

2. PHOTOLITHOGRAPHY…………... 14

2.1 Types of Photoresists 15

2.1.1 Positive Photoresists………………….................................. 15

2.1.2 Negative Photoresists.. 15

2.2 Types of Lithography…………… 16

2.2.1 Optical Lithography……………... 16

2.2.2 E-beam Lithography…………… 17

2.2.2.1 Applications of e-beam Lithography…………….... 18

2.2.2.2 Problems with e-beam Lithography……………....... 18

2.2.3 X-Ray Lithography…………… 19

2.2.4 Nanoimprint Lithography…………… 19

2.3 Projection Schemes in e-beam Lithography …………….................... 20

2.3.1 Projection Printing …………….. 20

2.3.2 Direct Writing……………... 23

2.4 E-beam Resist Systems…………….. 24

2.4.1 PMMA…………… 25

2.4.2 HSQ…………… 26

2.4.3 UVN 30……………... 27

3. NPGS, SEM and AFM …………….. 28

3.1 Nanometer Pattern Generation System 28

3.1.1 Working…………… 29

3.2 Scanning Electron Microscope 30

3.3 Atomic Force Microscope…………… 32

4. FABRICATION AND PATTERNING OF SET 35
4.1 Patterning of SET 35
4.1.1 CAD Pattern........ 36
4.2 Fabrication Process Flow........ 37
4.3 E-beam Patterns........ 40
4.3.1 PMMA Patterns 40
4.3.2 UVN 30 Patterns........ 47
4.3.3 HSQ Patterns........ 49
4.3.4 Etching Silicon using HSQ as Mask........ 50
5. SIMULATIONS OF SET 56
5.1 Simulation Methods for Single Electronics........ 56
5.1.1 Monte Carlo........ 56
5.1.2 Spice macro-modeling........ 58
5.1.3 Master Equation........ 58
5.2 Simulation Software 59
5.2.1 SIMON 59
5.2.2 MATLAB........ 60
5.3 Simulation Results........ 60
6. SUMMARY AND FUTURE WORK 64
Appendix
A. FABRICATION RECIPIES 66

B. SEM AND E-BEAM WRITER SPECIFICATIONS 75

REFERENCES 78

BIOGRAPHICAL INFORMATION... 84

LIST OF ILLUSTRATIONS

Figure Page

1.1 a) An electron feeling a strong attractive force as it approaches a sphere. b) Once a sphere gets charged by an electron; other electrons feel strong repelling force 2

1.2 Charge flow in good conductor 3

1.3 Tunnel Junction 3

1.4 Current biased tunnel junction and Coulomb oscillation a) Circuit diagram. b) Dripping tap. c) Tunneling oscillations 4

1.5 Single electron box. a) Construction. b) Circuit. c) Coulomb staircase 6

1.6 Single Electron Transistor……………………………………………………… 7

1.7 Energy level diagrams of Coulomb blockade. a) Zero current-Coulomb blockade condition. b) Charging energy barrier being overcome by drain-source bias Vds. This is onset of conduction 8

1.8 Voltage gain of SET as a function of gate capacitance 10

1.9 SET integrated with FET to resolve problems related to SET 11

2.1 Basic steps involved in photolithography 14

2.2 Positive and negative photolithography 16

2.3 Schematic of Nanoimprint lithography process 20

2.4 SCALPEL: principle of operation 21

2.5 Schematic of PREVAIL 22

2.6 Schematic of direct writing system 24

2.7 Conversion of MMA to PMMA 25

2.8 Chemical structure of HSQ a) Cage form b) Network form. 26

3.1 NPGS block diagram 30

3.2 Schematic diagram of SEM 32

3.3 AFM principle of operation in contact mode 34

4.1 SET design pattern 36

4.2 Six SET patterns at different exposure doses.
Designed using DesignCAD LT 36

4.3 Schematic after spin coating of resist.. 37

4.4 SET image patterning on resist using e-beam lithography 38

4.5 Resist image after development 39

4.6 SOI wafer after dry etching... 39

4.7 SET device pattern on SOI substrate... 40

4.8 All six SET patterns at variable exposure dose... 41

4.9 SEM Image for pattern exposed at 48nC/cm 42

4.10 SEM Image for pattern exposed at 56nC/cm 42

4.11 SEM Image for pattern exposed at 64nC/cm 43

4.12 SEM Image for pattern exposed at 72nC/cm 43

4.13 SEM Image for pattern exposed at 80nC/cm 44

4.14 SEM image for wheel pattern... 44

4.15 SEM image of wheel at 651.51 KX zoom 45

4.16 SEM Image of 50μm pad at 60° tilt with Al on top 46

4.17 EDAX after silicon RIE and before removal of aluminum............................ 46

4.18 EDAX after aluminum removal from pad... 47

4.19 SEM image of all six SETs at different exposure dose................................. 48

4.20 SEM image at 60° tilt showing island 48

4.21 SET pattern after developing wafer in 300 MIF 49

4.22 High resolution SEM image of SET pattern 50

4.23 AFM image of SET structure after developing in 300 MIF........................... 51

4.24 AFM image of island of SET 51

4.25 AFM image after RIE of silicon... 52

4.26 AFM image of SET pattern after DRIE 53

4.27 Three-dimensional AFM image of SET after DRIE 53

4.28 Thickness measurement after removing HSQ in CF_4 plasma 54

4.29 SEM Image of island after DRIE 55

4.30 SEM Image showing 5µm pad at 45° tilt 55

5.1 SET I-V characteristics at T= 4.2K 62

5.2 SET I-V characteristics at T= 77K.. 63

LIST OF TABLES

Table Page

5.1 SET simulation parameters for T= 4.2K 61

5.2 SET simulation parameters for T= 77K 62

CHAPTER 1

INTRODUCTION

1.1 Single Electronics

Single electronics comes into picture when we try to control movement of single electron or very small number of electrons. Robert Millikan demonstrated manipulation of single electrons during early 1920's by performing his oil drop experiment, but it was not implemented in solid state circuits until late 1980's despite some earlier background work. The reason behind this delay is that the manipulation of single electrons requires very small conducting particles and precise positioning with respect to external electrodes. The nanofabrication techniques that are available today were not present in those early days [1].

The fundamental concept behind single electronic devices can be explained by considering the small metal sphere, figure1, which is initially elecroneutral i.e. it has same number of electrons and protons. So we can say the net charge is zero. Assume that a single electron is positioned close to the sphere. Now it gets attracted by the sphere and joins the sphere leaving a negative charge of –e on it. This creates an electric field around the sphere so that if any other electron comes nearby, it will encounter a repulsive force. The theory behind the single electron phenomenon shows that the more adequate measure of strength of this tunneling effect is charging energy, $E_C = e^2/2C$.

From equation we can see that if the capacitance is small enough charging energies can be dominating.

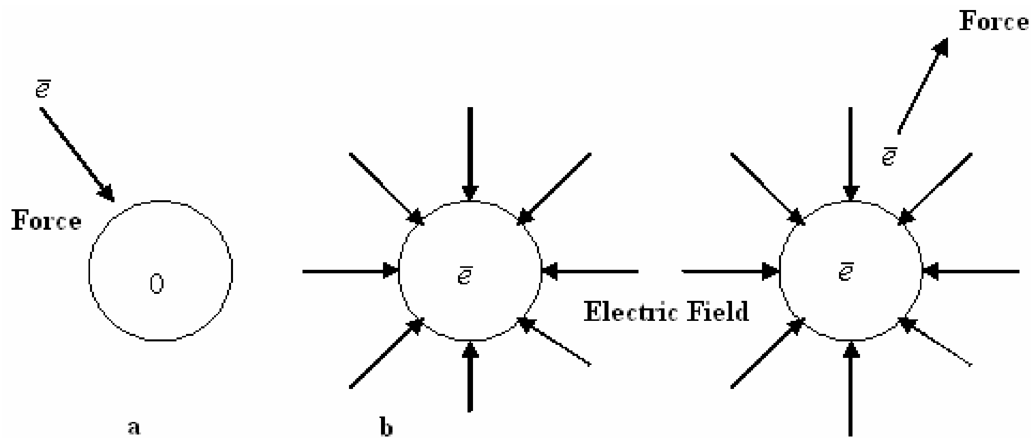


Figure1.1 a) An electron feeling a small attractive force as it approaches a sphere. b) Once sphere gets charge by a single electron; other electrons will feel a strong repelling force [2].

In order to understand single-electron transfer one must have concept about movement of electronic charge through a conductor. Due to availability of free electrons in a conductor current flows through it in a continuous manner. In order to determine current we need to calculate the charge transferred through the conductor per time interval. Now this charge can have any value. Hence, it is not quantized. Since electron cloud shift against the lattice of the atoms is not quantized in a conductor, the transfer of charge through a conductor is a continuous quantity. This is shown in figure 1.2.

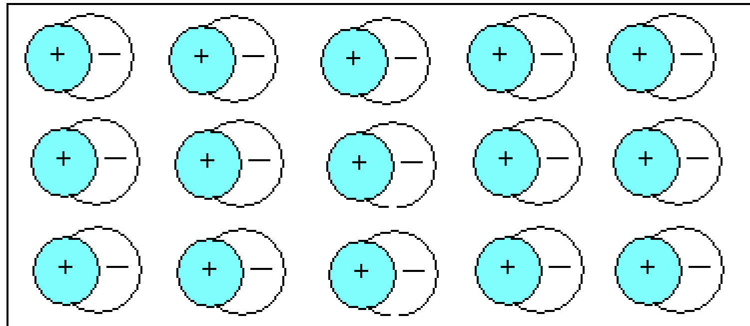


Figure 1.2 Charge flow in a good conductor [2].

If we place a tunnel junction in an ordinary conductor, as shown in figure 1.3, it will restrict the flow of electrons penetrating the barrier. Thus we can say current through tunnel junction is quantized. Due to introduction of the tunnel junction as a barrier in ordinary conductor, electric charge will now move by both discrete and continuous process. Now the charge will get accumulated at the tunnel junction due to the fact that only discrete electrons can tunnel through junctions. When a high enough bias gets built up across the junction, one electron gets transferred [2].

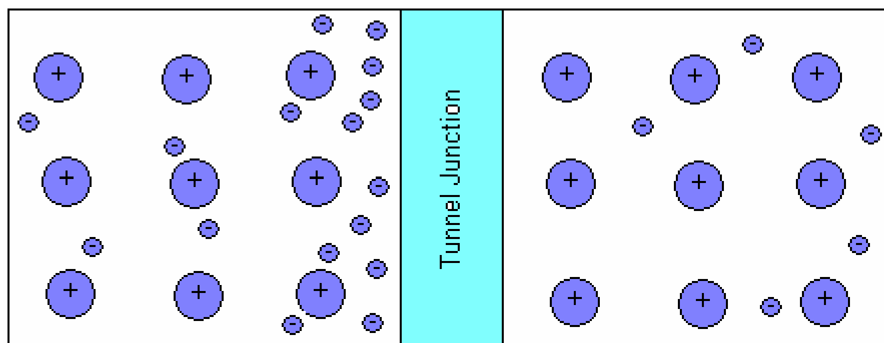


Figure 1.3 Tunnel Junctions [2]

Single electron tunneling phenomenon has been described analogous to dripping tap by K.K. Likharev [3]. In other words single-electron tunneling oscillations will

appear with frequency f = I/e, if single tunnel junction is biased with constant current I. This analogy is demonstrated in figure 1.4.

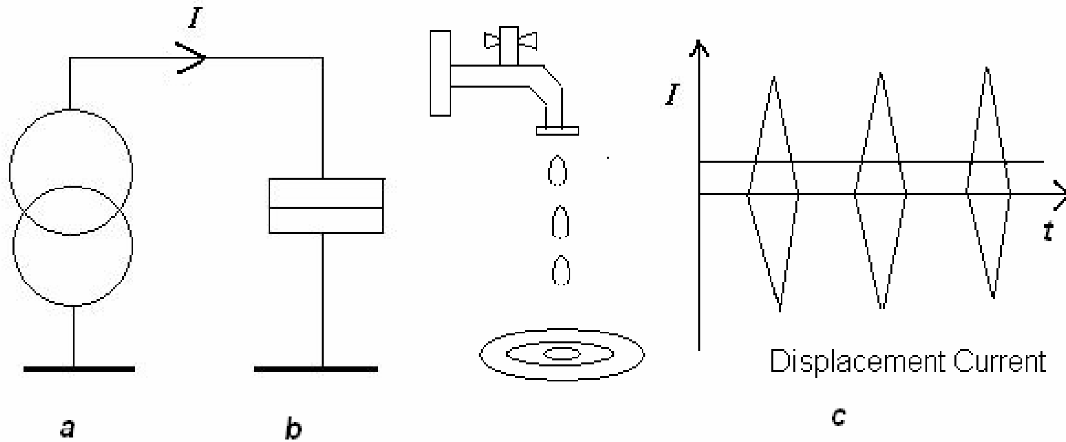


Figure 1.4 Current biased tunnel junction and Coulomb oscillation. a) Circuit diagram. b) Dripping tap. c) Tunneling oscillations [2].

There is always a close contest between charging and discharging of tunnel junction and thermal fluctuations. It is always required to have Coulomb energy greater than thermal fluctuations. Otherwise thermal fluctuations will disturb motion of electrons and will suppress quantization effects. The necessary condition to observe single electron phenomenon is

$$E_C= e^2/2C> k_BT,$$

Where k_B is boltzmann's constant and T is temperature in Kelvin.

In order to observe charging effects at room temperature capacitance C must be smaller than 3 af and this limits grain size to 5nm. A second fundamental condition to observe charging effects is that quantum fluctuations of the number of electrons must be negligible. In other words electrons should be localized on the island and all tunnel

junctions should be opaque for electrons to confine them to islands [2]. This opacity can be maintained if tunnel resistance R_T larger than resistance quantum i.e

$R_T > h/e^2 = 25.813\ K\Omega$

Where h is plank's constant and e is electronic charge.

1.2 Single Electron Box

A single electron box is one of the simplest circuits which demonstrates single electron charging effects. It consists of a small island separated from large electrode by a tunnel barrier (usually oxide).Consider a metal particle which is surrounded by oxide layer as shown in figure 1.5 and biased by a voltage source Vb. Top oxide layer is made thinner for electrons to tunnel through. For an electron to hop into the particle, the coulomb energy $E_C = e^2/2C$ is required. Just considering bias voltage Vb and neglecting thermal or any other energy, as long as bias voltage is less than threshold voltage Vth=e/C, no tunneling can be observed because not enough energy is available to charge the metal grain. This current suppression at low bias voltages, caused by charging effects is called coulomb blockade. If the bias voltage is raised further, this will populate particle with one, two, three and so on electrons and thus it forms a staircase like pattern. This staircase like pattern is termed as Coulomb Staircase as shown in figure 1.5 b. The physics of Coulomb Staircase is very simple: as bias voltage is increased the grain attracts more and more electrons.

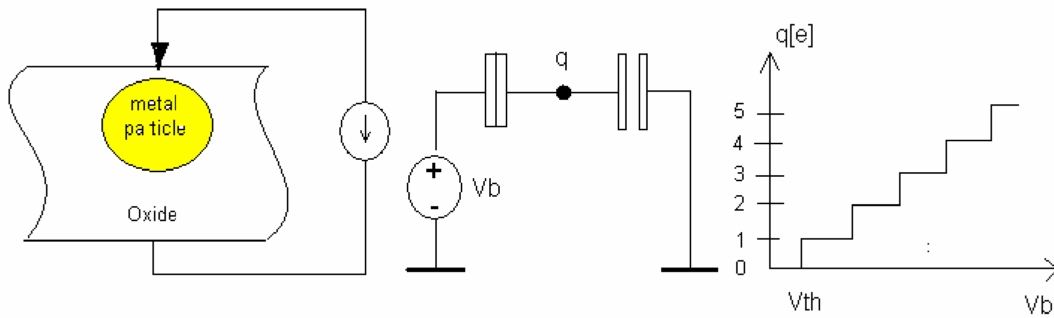


Figure 1.5 Single Electron Box. a) Construction. b) Circuit. c) Coulomb staircase [2]

1.2.1 Problems with Single Electron Box

This structure cannot be used to store information in any form as it lacks internal memory. The number of electrons is a function of applied bias voltage. The second problem is that, the ultrasensitive electrometer is required to measure its charge state as it does not have any capability to carry dc current [1].

1.3 Single Electron Transistor

Single electron transistor consists of a small island coupled to three electrodes as shown in figure 1.6. Source and drain leads are coupled to the island by a high resistance tunnel junction and the gate is capacitively coupled to the island.

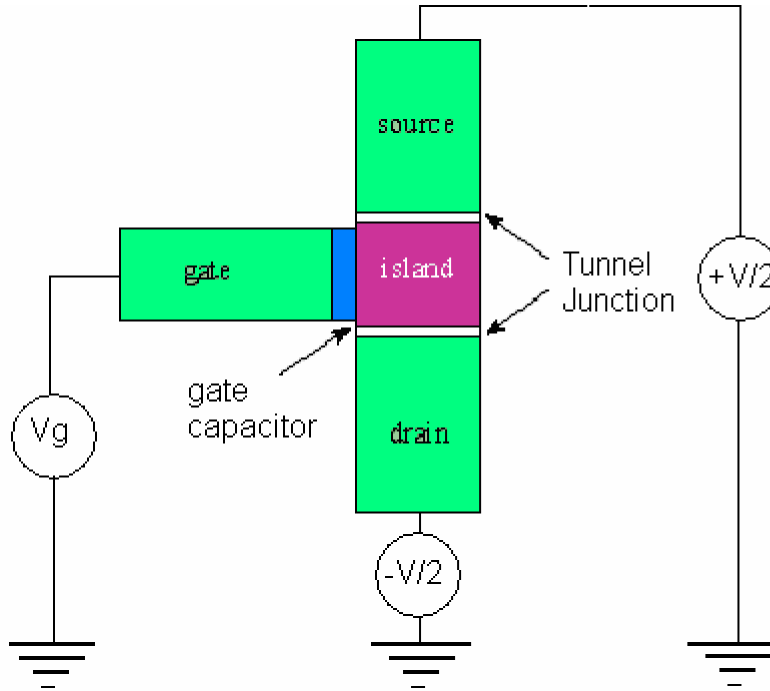


Figure 1.6 Single Electron Transistor

The SET can be viewed as a single electron box that has two junctions for entry and exit of electrons. This is analogous to a conventional MOSFET which has channels replaced by tunnel junctions i.e. source and drain regions are connected to island by tunnel junctions. Gate electrode can be used to control number of electrons on the island.

1.3.1 Operation of SET

In a single electron transistor charge passes through the island in quantized units. For an electron to shift into the island its energy should be $e^2/2C$.When gate and bias voltage is set to 0volts the electron does not have sufficient energy to hop into island and therefore current does not flow. Upon increasing bias between source and drain, electron can enter and leave island once the system has energy equal to E_C i.e.

coulomb energy. This effect is coulomb blockade and the critical voltage needed to transfer electron is e/C, is called coulomb gap voltage.

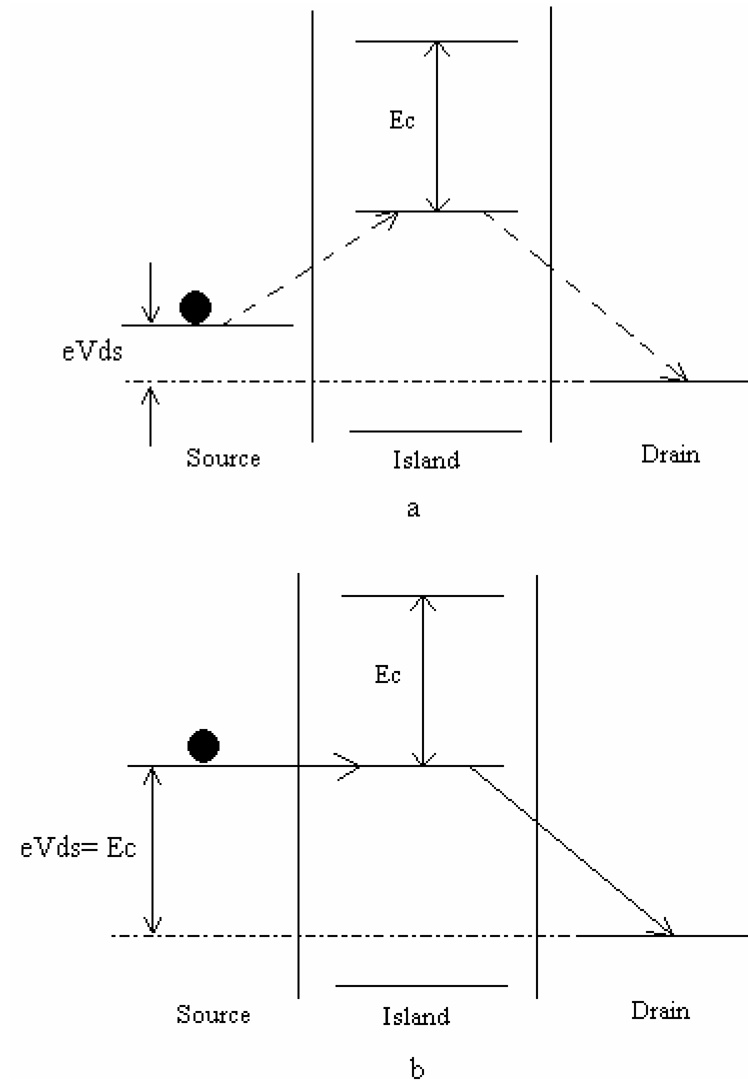


Figure 1.7 Energy level diagrams of Coulomb blockade. a) Zero current-Coulomb blockade condition. b) Charging energy barrier being overcome by drain-source bias Vds . This is onset of conduction.

The Coulomb blockade condition can be further illustrated by using energy level diagrams as shown in figure 1.7. Figure 1.7a shows that electrons cannot

overcome the energy barrier, resulting in zero current. This happens due to small value of drain-source voltage, V_{ds}. In order for current to flow we need to adjust gate bias, V_g so as to align energy level on central island to the Fermi levels in the leads. Figure 1.7b shows the situation in which $eV_{ds}=E_C$. This condition depicts the drain-source conduction threshold , given a “maximally blockade” SET with $Q_g=ne$, where n is an integer. Thus for larger Vds biases, current through device is only limited due to tunnel resistances [37].

1.4 Issues with SET

1.4.1 Limitations of SET

Voltage gain of SET decreases as the dimensions of device shrink to few nanometers. This is due to fact that voltage gain is directly proportional to gate capacitance, so as gate capacitance decreases, voltage gain drops. To modulate output by tens of millivolts, an input signal of the order of tens of volts needs to be applied. The voltage gain of SET is can be defined as ratio of gate to junction capacitance. As seen from the figure 1.7, where junction capacitance is fixed and gate capacitance is varied, the voltage gain first increases and then decreases. The voltage gain increases with increasing gate capacitance until charging energy of the order k_BT is reached and then there is sudden drop in voltage gain. Sometimes we do consider charge gain for a transistor to be useful. The charge gain is the modulation of the charge that passes through the SET divided by change in the charge on the gate i.e.

$$g_{charge} = (dI/dV_{g1})/(2\prod fC_g)= 1/ (2\prod f RC_{\sum})$$

It can be seen from the above equation that charge gain is a frequency dependent quantity. Charge gain greater than unity can be easily achieved at room temperature. The charge gain comes into picture in situations where charge needs to be measured, for instance to readout a memory cell or charge coupled device. Another problem with SET is the large output impedance of at least 100KΩ.This diminishes the performance of SET by making it a slow device [4].

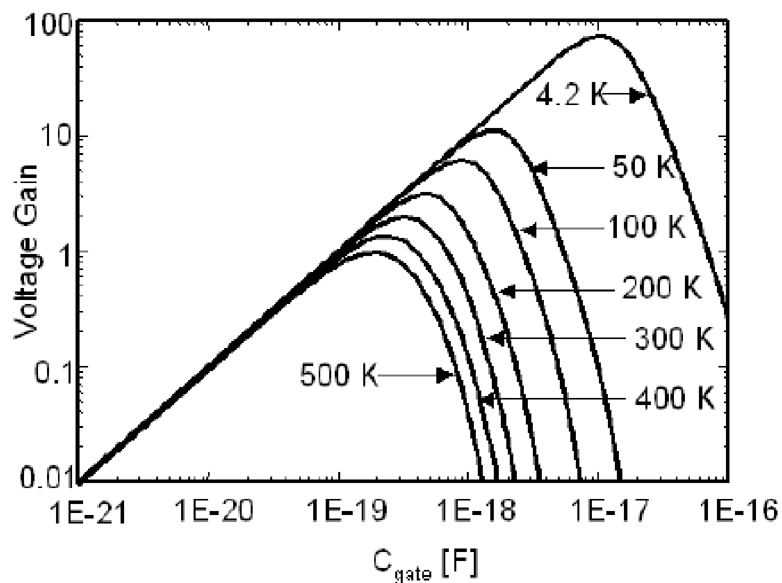


Figure 1.8 Voltage gain of SET as a function of gate capacitance [4].

The background charge problem is another important issue that inhibits widespread use of SET. It originates due to extreme charge sensitivities of SETs. A single charged vacancy or interstitial ion in the oxide is sufficient enough to change state of SET from conducting to non-conducting. Although there are same charge problems with field effect transistor but, it is not as sensitive as SET [4].

1.4.2 Solution

All three problems of low voltage gain, high output impedance and background charge problem can be solved by integrating SET with FET. Such a hybrid circuit was suggested by Peter Hadley [4] and shown in figure 1.8. In this circuit SET provide charge sensitivity while the FET provides desired voltage gain and low output impedance.

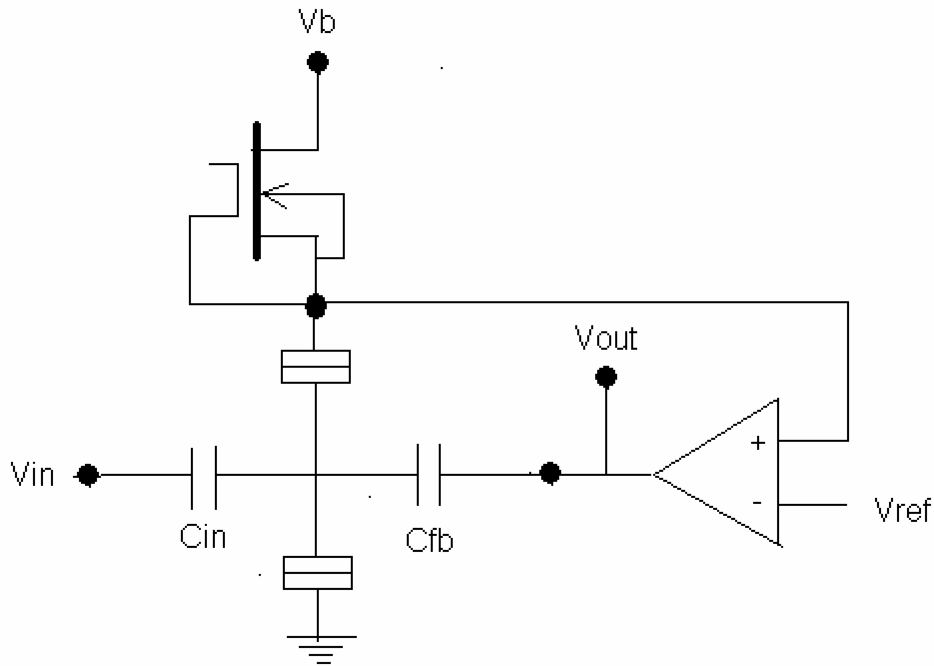


Figure 1.9 SET integrated with FET to resolve problems related to SET [4]

1.5 Applications of SET

1.5.1 Electrometer

When a single electron transistor is operated above coulomb blockade threshold it forms an electrometer. As we know that, random background charge problem is associated with SET. Even small amount of background charge can change the coulomb

blockade and thus alter working of the SET device. The advantage of this problem is that we can build the high sensitive electrometers. This change in charge is detected by an island of SET. The SET electrometer can be operated by capacitively coupling external charge source to the gate of SET. For very small changes in the gate voltage there is a large change in source and drain current. This happens due large amplification coefficient. Likharev, Krotkov and Averin have predicted the achievable sensitivity of 10^{-5} e/ sqrt Hz [5]. This sensitivity is much better than many common electrometers made by MOSFET. With such good sensitivity we can measure very small amounts of charge. High sensitivity can be achieved by increasing gate capacitance but, this can reduce coulomb energy [2].

1.5.2 Single Electron Memory

It is perhaps one of the interesting applications of SET. It stores information by predicting presence and absence of an electron on an island. Chan and Chou independently demonstrated single electron memory which stores information in the form of one electron in two different publications [6], [7].

They used gate electrode to inject single electron to island and this can modulate source-drain current. They fabricated memory element by having one or several nanoparticles embedded in thin layer of silicon dioxide insulator. Finally, source, drain and gate electrodes are fabricated around nanoparticles. Chan's structure demonstrated read write time of 20ns with lifetime of more than 10^{9} cycles and can retain information ranging from few days to several weeks [8].

Another way to construct a memory element is by considering 1 bit = 1 electron, then an array of 4-7 SETs can be used and positions of single electrons in an array will define different memory states. The practical limitation of such a memory is fabrication. If this type of memory is realized it will be very much advantageous over CMOS. This can be proved to be advantages when time comes for integration of SET to form logic gates. This can be considered as a threshold of quantum computing [8].

CHAPTER 2

PHOTOLITHOGRAPHY

Photolithography is a process of transferring geometric pattern on the mask on to wafer surface. Once pattern is transferred on the substrate we can perform further processing steps such as film deposition, implantation or etching. The basic steps involved in the photolithography process are explained in figure 2.1.

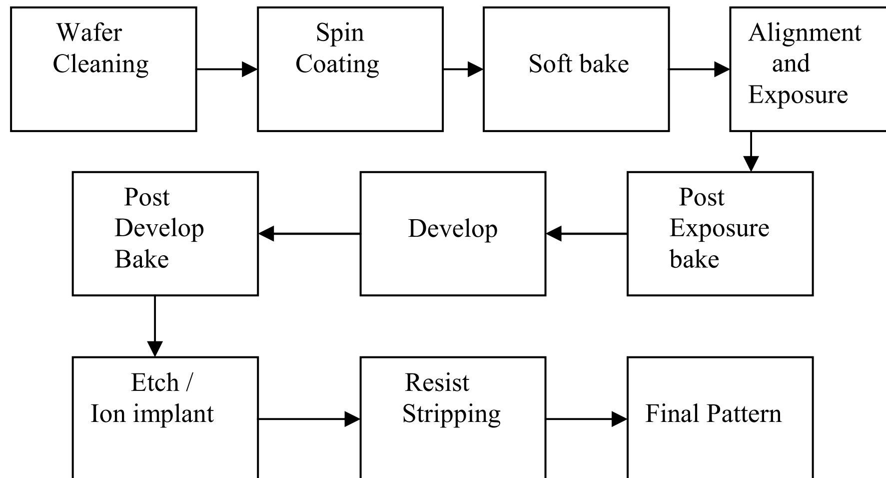


Figure 2.1 Basic steps involved in photolithography

Initially wafers are cleaned by using various chemicals so as to remove contaminants. Sometimes we have to use adhesion promoter to increase photoresist adhesion to the substrate. Then a layer of photoresist which is sensitive to a particular radiation is deposited by spin coating .Then wafers are transferred to a hot plate to reduce the concentration of solvent in the film and to increase adhesion further. Then

wafers are sent to the next stage called alignment, to expose wafer using a mask. Once the image is printed, the wafer is baked again and this is called post exposure bake. This stage initiates further chemical reactions. Then wafers are developed in a developer. This solution removes the exposed or unexposed resist depending on type of resist used .We can develop using Batch method, spray or puddle. Resist is baked again after development to use it as a mask in some process. Resist can be stripped using plasma or some wet chemical. We finally get our pattern on the wafer substrate.

2.1 Types of Photoresists

Photoresists can be classified as negative and positive. Figure 2.2 shows the schematic of positive and negative photoresist action.

2.1.1 Positive Photoresists

The positive resist when exposed to UV light, e-beam, X-rays etc., the exposed part of the resist gets removed when rinsed in developer solution. Therefore we can say area uncovered by the mask goes off in developer, so we get positive mask image.

2.1.2 Negative Photoresists

Negative resist behaves exactly opposite to positive resist. The part of resist that gets exposed becomes cross linked and hence insoluble in developer solution. So we get the negative pattern on wafer i.e. opposite to what we have on our reticle**.**

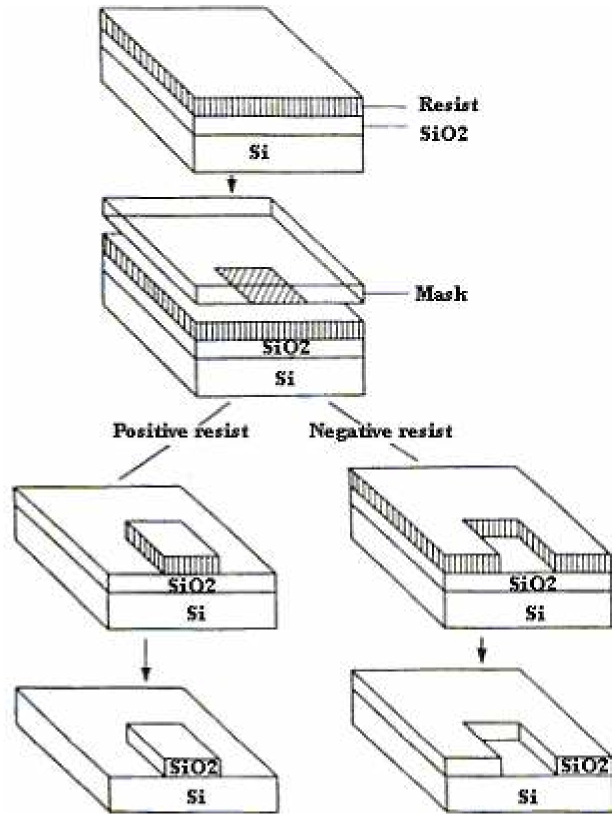


Figure 2.2 Positive and negative photolithography

2.2 Types of lithography

2.2.1 Optical Lithography

It can be further classified into UV and DUV. Ultraviolet lithography operates in the range of 365 to 405 nm (I-line 365nm, G-line-436 nm and H-line 405nm). Most of the resists when exposed to UV radiation in this range becomes crosslinked, insoluble or soluble in the developer solution, depending on the resist type. These resists came out to be very good till resolution required was 2μm to 0.5 μm. As the structure size began to shrink and chips became denser i.e. when resolution went below 0.25 μm i-line and g-line could no longer print these structures so, Deep-UV

lithography in the range of 193nm to 248 nm wavelength came into existence. These resists utilized the principle of chemical amplification. These new chemically amplified resists offers increased photo speed, higher resolution and improved contrast [9]. J.M Shaw et al. from IBM explained the entire chemistry of negative, positive and Deep UV resist system [10]. Optical lithography is still being used in fabrication due to higher yields and throughput .Critical dimension can be further reduced by using step aligners.

2.2.2 Electron Beam Lithography

Electron beam lithography plays a major role in development of nanostructures. Due to diffraction limits of optical lithography, it is becoming quite inadequate to define features in nanometer size range. It is anticipated that refractive optical lithography will reach is limits at 157nm range. If we want to go beyond this range there are significant issues about masks, light sources and new photoresists systems. Electron beam lithography is used to generate extremely fine patterns which are invisible with naked eye. This is possible due to extremely small spot size of e-beam. The e-beam has wavelength so small that diffraction no longer defines lithographic resolution. Derived from earlier scanning electron microscopes, the technique involves exposure of electrons on the surface that is covered with e-beam resist, thus depositing energy in the desired pattern on resist film. This process is very much analogous to process of forming beam of electrons and scanning it across the surface of a CRT display. The advantages include very high resolution, versatile pattern formation, ability to work with variety of materials due to its flexibility, high precision. On the downside, it is expensive and much slower than optical lithography.

2.2.2.1 Applications of e-beam Lithography

Currently e-beam lithography finds applications in mask making. It is preferred due to flexibility in providing rapid turn around of a finished part described by CAD file. We can attain tight linewidth control and high resolution.

Second application involves direct writing of patterns on the resist which can further be used to manufacture integrated circuits consisting of silicon and gallium arsenide [11]. This can be further extended in manufacturing of nanoscale devices such as single electron transistors, quantum dots, etc.

2.2.2.2 Problems with e-beam Lithography

When electrons penetrate resist they undergo many small angle scatterings called forward scattering and they also undergo large angle scattering called back scattering and this causes proximity effect [12].

Due to forward scattering the beam diameter broadens as e-beam penetrates through resist. This can result is broader beam profile at the bottom than on top. The increase in beam diameter can be given by the formula $d_f = 0.9(R_t/V_b)^{1.5}$, where R_t is the resist thickness in nanometers and V_b is voltage in kilovolts [13]. Thus we can minimize forward scattering using thin resist layers and high acceleration voltage. Forward scattering can also be minimized by using bilayer resist process in which top resist is sensitive to electrons and pattern can be transferred to bottom resist layer by using dry etching. This can be done at the cost of increased process complexity.

As electrons penetrate through resist to substrate, some experience large angle scattering and many of them return back to resist causing additional resist exposure.

This is called proximity effect. During this process electrons are continuously slowing down as a result producing secondary electrons. This leads to the problem that exposed features after development might turn out to be more than the required size. Proximity effect can be reduced by using lower beam energies. Another approach to correct proximity effect is to use variable dose according to the pattern size [13].

2.2.3 X –ray Lithography

X-rays were discovered in 1895 by W.H. Roentgen, while he was conducting experiment with cathode rays [14]. As X-rays operate at very short wavelength in range of 0.01 to 1 nm [13], which provides better resolution. X-rays can penetrate deep into resist with negligible scattering and this allows fabrication of microstructures of high aspect ratio. H.I. smith was the first person to propose use of X-ray lithography to define patterns on semiconductor substrates [14]. The mask is a low atomic number material such as diamond, polyimide or beryllium or a thin membrane of high atomic number material such as silicon or silicon carbide. PMMA is most widely used resist for X–ray lithography. Other chemically amplified resists include Sal-605, APEX-E, AZ-PF 514 and ZEP. X-ray lithography is generally used in LIGA (Lithography, electroplating, molding) process to create a mold in PMMA resist.

2.2.4 Nanoimprint Lithography

This technique involves the use of mold which has nanostructures on its surface. This mold is pressed into the resist on the substrate and we can get the duplicate image in the resist film. This creates thick contrast in the resist. This type of process was refined by S.Y Chou and his coworkers [15]. They were able to demonstrate 25 nm

feature sizes and they also mentioned that they can achieve resolution in sub 10 nm using this technique. After defining pattern using a mold the complete pattern is transferred using RIE to remove resist in the mold area. The resist used is a thermoplastic material which can be deformed by using a mold by heating resist above glass transition temperature and once pattern is formed the resist is cooled down and mold is removed. As this technique does not use any masks or energy source to define patterns so, resolution is not limited by scattering, proximity effect and diffraction. One can use the same mold many times which makes this process cost effective with high throughput. Silicon dioxide can be used as mold on PMMA resist. Figure 2.3 shows the schematic of nanoimprint technique.

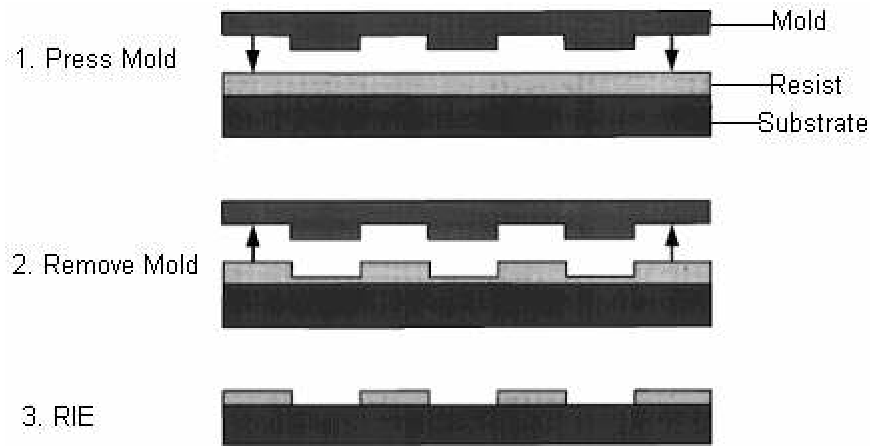


Figure 2.3 Schematic of nanoimprint lithography process [15]

2.3 Projection Schemes in e-beam Lithography

2.3.1 Projection Printing

In this scheme a mask is used to project a large size electron beam on a resist coated wafer by using high precision lens system. Several versions of projection e-beam

lithography are there, but I am going to discuss just two of these, SCALPEL (Scattering with angular limitation in projection e-beam lithography) and PREVAIL (Projection reduction exposure with variable axis immersion lenses). These are developed by IBM [16], [17]. As shown in figure 2.4 SCALPEL uses a scattering mask [18]. Mask is made up of thin nitride as base material and tungsten is used to define structure on top of it. Thus we have low atomic number membrane on which high atomic number material like tungsten is patterned. When electrons pass through low atomic number material they scatter at lower angles than those passing through high atomic number material. Now aperture located at back focal plane of the projection lens blocks electrons with high scattering and passes the one with less scattering. As a result these electrons with small scattering define high contrast image on wafer coated with e-beam resist. To avoid distortion electron beam size projected on wafer is kept small, of the order of $1mm^2$. This limits the throughput of the process as we have large diameter wafer. Then lucent technologies [19] came with a new state of art system which uses step and scan writing instead of step and speed used in earlier systems.

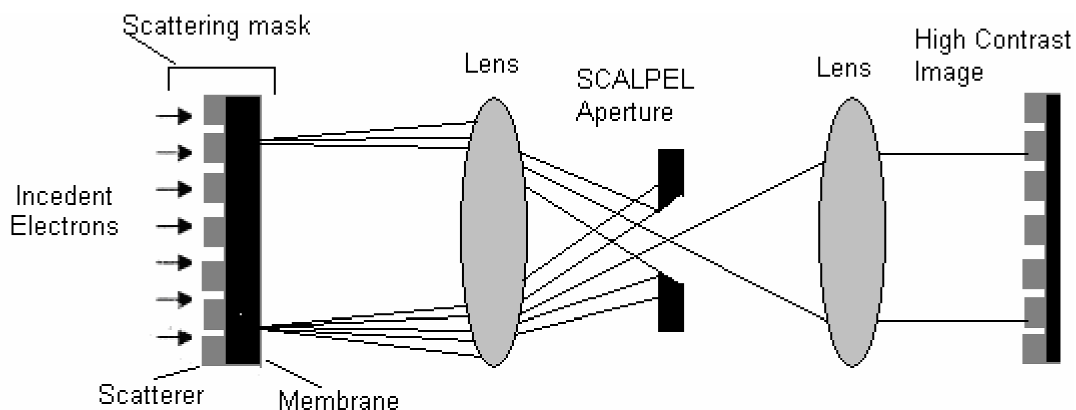


Figure 2.4 SCALPEL: principle of operation [18]

PREVAIL approach involves the combination of e-beam scanning and moderate speed mechanical scanning. It uses system of variable-axis lenses. This allows shifting electron optical axis along predefined curvature and simultaneous deflection of e-beam to curvilinear variable axis thus eliminating any off axis aberrations. Figure 2.5 shows the basic PREVAIL system consisting of illuminator to provide illumination of each field pattern by imaging 1 X 1 mm shaped beam into reticle. Recently people from IBM [17] have demonstrated e-beam pattering using PREVAIL on 10 X 10 MM substrate.

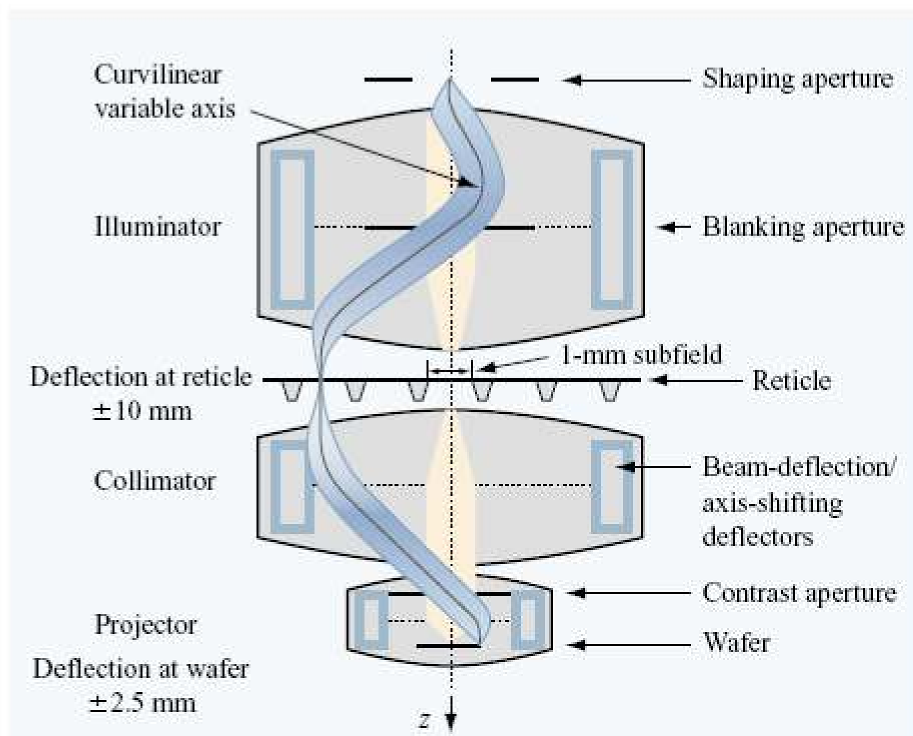


Figure 2.5 Schematic of PREVAIL [17]

2.3.2 Direct Writing

Direct writing involves a small finely focused Gaussian electron beam exposure directly on a resist coated substrate.

In direct writing we can eliminate mask making process. This uses the early scanning electron microscopes. These types of system generally expose one pixel at a time and work in vector scan mode. It consists of e-beam source blanker, stage for substrate, deflection system and focusing optics. As this process saves lot of money and time by eliminating mask and provides high resolution, so it is used at research laboratories. This is a time consuming process as system exposes one pixel at a time. We can attain very small beam diameters. Figure 2.6 shows schematic of direct writing system.

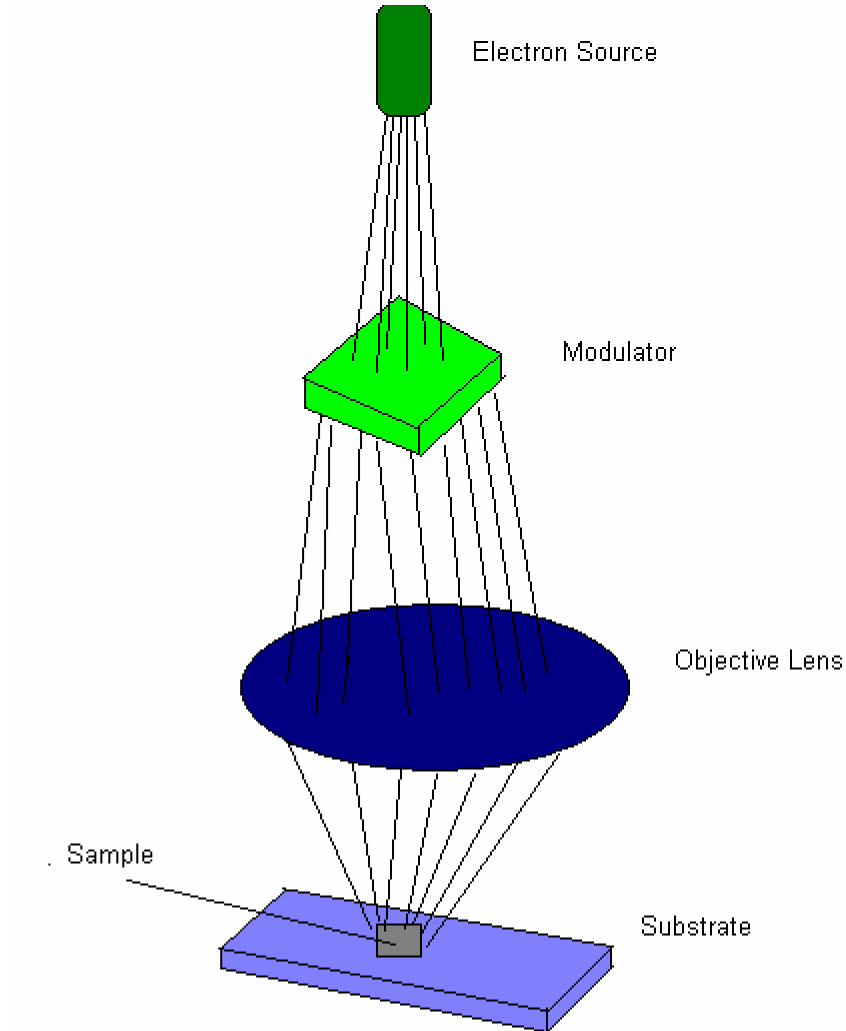


Figure 2.6 Schematic of direct writing system [18]

2.4 E- beam Resists Systems

Electron beam resists are polymers dissolved in liquid solvents. Resists change their structure when exposed to electrons. They are classified as positive and negative tone resists. Positive resists when exposed to e-beam, the exposed part becomes soluble in developer and gets removed in the developer solution. For negative resist systems

opposite happens i.e. exposed part gets crosslinked and thus becomes insoluble in developer solution.

2.4.1 PMMA

One of the most widely resist used for e-beam lithography is PMMA (poly methyl methacrylate). It can be used as a positive as well as negative photoresist. It is the first resist developed for e-beam lithography. It has a glass transition temp of 114 ^{o} C. It is available in powder form and can be dissolved in anisole and chlorobenzene according to the desired concentration. It can be easily deposited by spin coating. PMMA is a vinyl polymer made by free radical vinyl polymerization of monomer, methyl methacrylate (MMA). Figure 2.7 demonstrates the reaction involved.

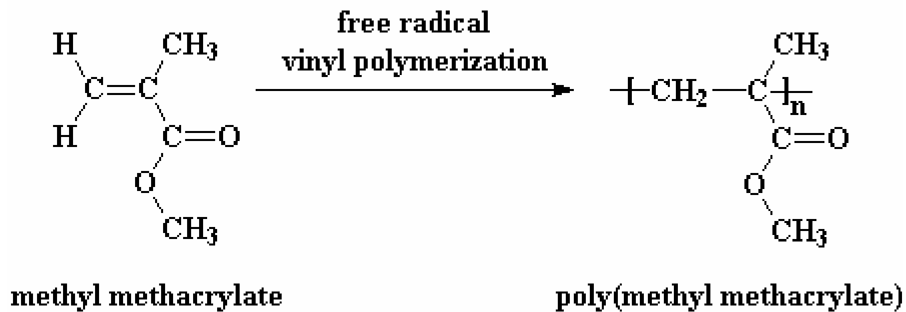


Figure 2.7 Conversion of MMA to PMMA

PMMA products cover wide range of film thickness and are formulated with 495K and 950K molecular weight. The dose values for electron beam exposure lies between 50 to 500μC/ cm^2. Exposure energy varies between 20-50 KV. PMMA is developed in a mixture of MIBK (methyl isobutyl ketone) and IPA (isopropanol). PMMA has very high resolution and can resolve feature sizes down to 10 nm range [20]. The major problem is poor dry etch resistance and poor sensitivity [18].

When PMMA is exposed to moderate doses the scission process dominates and lower molecular fragments of resist are formed. Thus exposed part of the resist gets removed in the developer solution and PMMA acts like positive resist. However, when exposed to high irradiation doses of the order of 50-70 C/cm^2, the PMMA molecules gets crosslinked and thus exposed part becomes resistant to most developers. The unexposed part can be easily removed in acetone [21].We have used 2% of 950K PMMA in anisole as a solvent for our research purpose.

2.4.2 HSQ

HSQ is a low k dielectric, another negative e-beam resist. It is an inorganic resist being utilized to pattern nanostructures since past half decade. It has a cage structure before curing which gets transformed to network structure after curing. Properties of HSQ depend upon curing process [22].

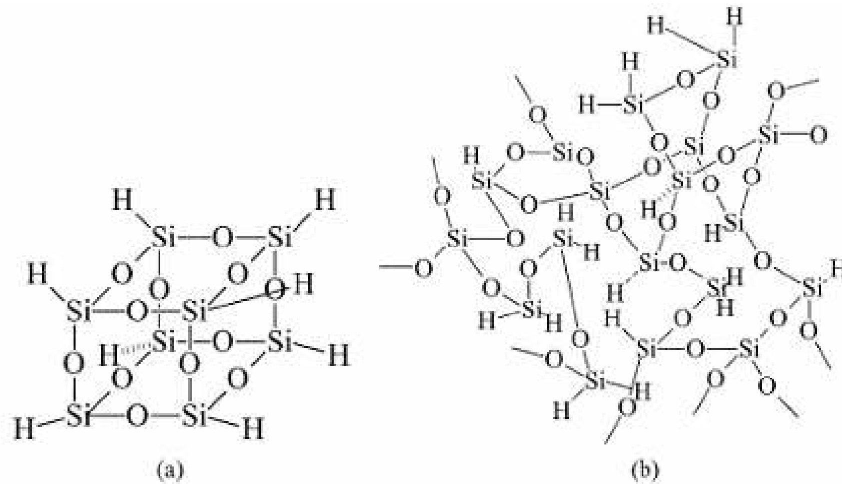


Figure 2.8 Chemical structure of HSQ a). Cage form b). Network form [22]

HSQ can be used for a single layer or bilayer process depending on the requirement. It has exhibited resolution better than 20 nm in e-beam lithography. It can

be easily deposited by spin coating to get uniform film in variety of ranges depending upon concentration and spin speed. Pattern can be developed in any TMAH (tetra methyl ammonium hydroxide) based developer. We used MIF 300 to develop our patterns. The major drawback of HSQ is that, it needs high electron beam dose in order to break down the caged pattern. Another major drawback of HSQ is very small shelf life of just 6 months. HSQ is commercially available with different solid concentrations with MIBK (methyl isobutyl ketone) as the base solvent. For our research purpose we used XR 1541 which is equivalent of Fox 12.

2.4.3 UVN 30

UVN 30 is another negative tone chemically amplified photoresist for DUV, X-ray and e-beam applications. We utilized UVN 30 to pattern SET structures using e-beam lithography. It has low post exposure bake sensitivity of less than 1 mm/^{o}C. It is very stable and has high dry etch resistance. It can be develop in MF 702 developer. UVN 30 needs HMDS prime for better adhesion to substrate. We noticed that resolution became poor as our structure size reduced to 100nm.

As a part of this thesis PMMA, HSQ (XR 1541) and UVN 30 is used to pattern single electron transistors with island size of about 100nm. This is explained further in Chapter 4.

CHAPTER 3

NPGS, SEM and AFM

3.1 Nanometer Pattern Generation System

Nanometer Pattern Generation System is abbreviated as NPGS. It has been developed by J.C. Nabity. NPGS uses a SEM being converted to electron beam writer by using necessary hardware and software. The pattern generator developed by them uses computer aided design CAD program to interpret data and controls SEM for performing e-beam lithography [23].

There are three basic steps to the pattern generation process: pattern design, parameter run file creation, and pattern writing with optional auto or semi-automatic alignment for multilevel lithography.

Pattern design can be accomplished using DesignCAD. This is very powerful program which simplifies all design aspects. Pattern elements with different exposure parameters can be designed in different colors or different drawing layers. So we get unlimited number of exposure conditions within a single pattern. It is also capable of importing patterns from DWG, DXF, GDSII, CIF and IGES.

Once the pattern is designed, the run file editor records the different exposure conditions for drawing elements in pattern. In this way it keeps a separation between details of exposure and pattern design, therefore to vary exposure conditions only run file needs to be changed. File editor accepts doses as area dose ($\mu C/cm^2$), a line dose (nC/cm) or a point dose (fC). It calculates the point exposure times automatically.

NPGS version 9 supports up to 5000 parameters in single run file ands their sequence of operation.

Once the run file is created, the pattern described by it may be written using NPGS.exe. NPGS uses PG.exe for writing and AL.exe for alignment. PG writes a pattern by controlling X-Y scanning coil and beam blanker of microscope. Scan coils are stepped with 16 bit resolution. Exposure times of 0.2 μs to several hours can be achieved.

3.1.1 Working

Figure 3.1 shows block diagram of NPGS. The image signal, XY DAC s, and blanking control are all handled by high speed NPGS PC1516 board. The I/O can be serial, Ethernet, USB, GPIB, etc and depend upon the hardware. SEM working is explained in section 3.2. Once the software has been initialized with necessary SEM settings, it reads the pattern data file and writes pattern by controlling X-Y beam positioning and beam blanker. A picoammeter is required to read the beam current hitting the sample.

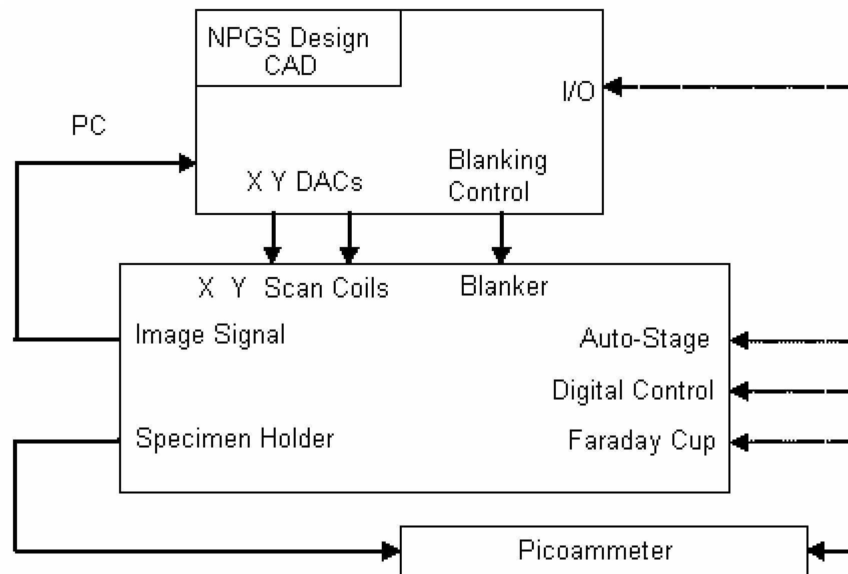


Figure 3.1 NPGS Block Diagram

3.2 Scanning Electron Microscope

Scanning Electron Microscopy (SEM) uses a focused electron beam to scan small areas of solid samples. Secondary electrons are emitted from the sample and are collected to create an area map of the secondary emissions. Since the intensity of secondary emission is very dependent on local morphology, the area map is a magnified image of the sample. Spatial resolution is as high as 1 nanometer for some instruments, but 4 nm is typical for most.

Optical microscopes have the limited magnification and lower resolution of 1000X maximum and 0.2 μm respectively. SEM can provide resolution in the range of 15X to 200,000 X. The SEM has a large depth of field, which allows a large amount of the sample to be in focus at one time. The SEM also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. Preparation of the sample is relatively easy since SEM only requires the

sample to be conductive. The combination of higher magnification, larger depth of focus, greater resolution, and ease of sample observation makes the SEM one of the most heavily used instruments in research areas today.

Figure 3.2 shows the schematic of SEM. The electron gun with tungsten filament acts as a source of electrons. The electrons are accelerated by applying a voltage between grid coils and anode, which changes energy of the beam. Most common acceleration voltages used are between 20 KV to 50 KV. Condenser lens is used to reduce the diameter of the beam generated by electron gun. Then beam is focused by a lens called objective lens so as to form very small spot of few nanometers diameter. This spot is scanned across the sample surface in the form of raster by scanning coils housed inside the final lens. As electrons interact with sample surface, different types of signals are generated and are used to modulate the brightness of cathode ray tube. Normally the beam is scanned at TV rates making the effects of magnification, focusing and repositioning instantaneous [24].

At UTA we have ZEISS SUPRA 55 VP SEM. It can be used to perform EDAX also. It can handle wafer sizes up to 8 inch and has maximum resolution 1 nm. All technical specifications are given in appendix B.

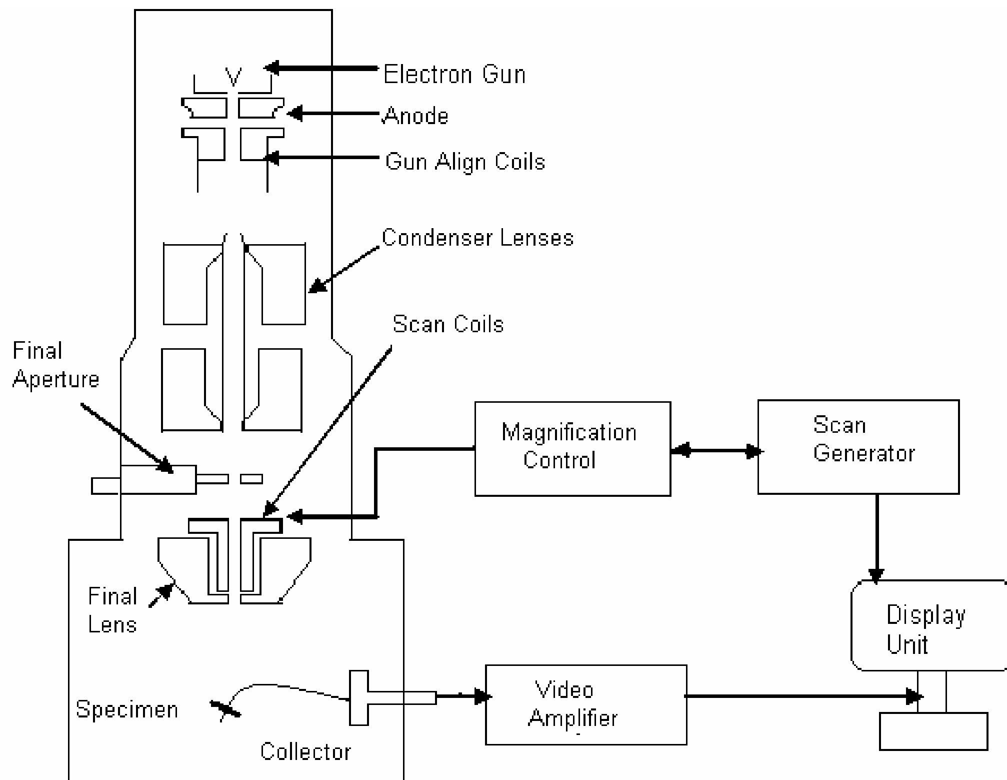


Figure 3.2 Schematic diagram of SEM [24]

3.3 Atomic Force Microscope

AFM is a powerful instrument for imaging and nanomanipulation of surfaces at the atomic level. The atomic force microscope (AFM) was invented in 1986 by Binnig, Quate and Gerber. The AFM utilizes a sharp probe moving over the surface of a sample in a raster scan. In the case of the AFM, the probe is a tip on the end of a cantilever which bends in response to the force between the tip and the sample. AFM can perform three-dimensional measurements in x, y and z direction. This helps in producing three-dimensional images of a sample. One can easily achieve resolution of 0.1 to 1 nm. AFM require neither any special sample preparation like other analysis techniques nor it

needs any vacuum on stage to hold sample and can be operated in any cleanroom. AFM finds applications in semiconductors, physics, material science etc.

AFM can be operated in contact and tapping mode. One of the most used AFM modes is contact mode and in this mode it operates by rastering a sharp tip made of silicon or silicon nitride attached to a cantilever across a sample. As AFM tip scans either a repulsive force between sample and tip or actual tip deflection is recorded and converted into image. Figure 3.3 illustrates the basic principle of operation in contact mode. The user gets the AFM tip closer to the sample surface. The tip now scans across the sample under the action of piezoelectric actuator, either by moving the sample or tip relative to the other. A laser beam on top of the scanner, aimed at back of cantilever tip reflects off the cantilever surface to a photodiode detector, which records deflection in cantilever. The purpose of the feedback loop is to keep constant tip-sample separation and this can be achieved by moving the sample in Z-direction. If this feedback loop would have been absent, tip might bang into the sample. By maintaining constant tip-sample separation and by using hooks law, force between tip and sample is calculated. Finally the distance moved by scanner in Z direction is stored in a computer relative to X-Y plane to generate image of the feature on the sample [25].

Tapping mode is used in case of sample surfaces which are prone to damage. Tapping mode overcomes problems associated with friction, adhesion, electrostatic forces, and other difficulties that an plague conventional AFM scanning methods by alternately placing the tip in contact with the surface to provide high resolution and then lifting the tip off the surface to avoid dragging the tip across the surface. Tapping mode

imaging is implemented in ambient air by oscillating the cantilever assembly at or near the cantilever's resonant frequency using a piezoelectric crystal. The piezo motion causes the cantilever to oscillate with a high amplitude (typically greater than 20nm) when the tip is not in contact with the surface. The oscillating tip is then moved toward the surface until it begins to lightly touch, or tap the surface. During scanning, the vertically oscillating tip alternately contacts the surface and lifts off, generally at a frequency of 50,000 to 500,000 cycles per second. As the oscillating cantilever begins to intermittently contact the surface, the cantilever oscillation is necessarily reduced due to energy loss caused by the tip contacting the surface. The reduction in oscillation amplitude is used to identify and measure surface features.

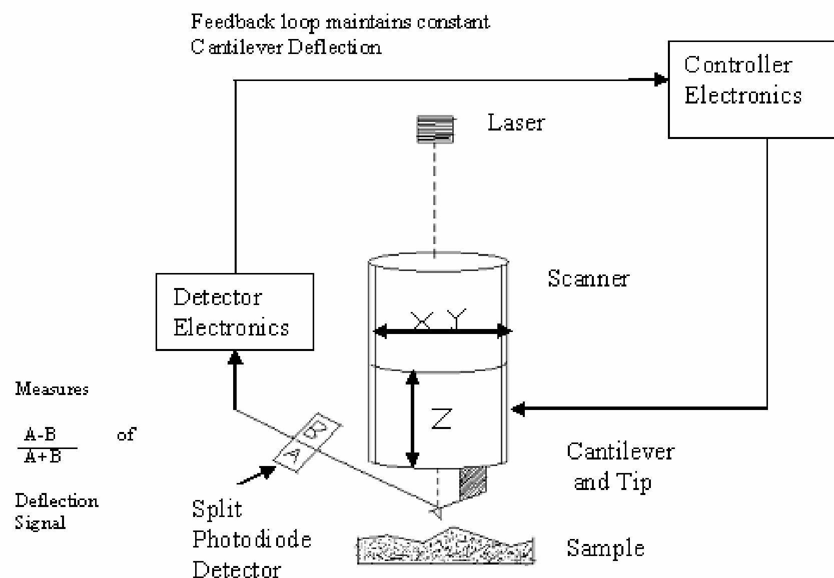


Figure 3.3 AFM Principle of Operation in Contact Mode [25]

CHAPTER 4

FABRICATION AND PATTERNING OF SET

As of now we have gone through physics governing single electronics, types of lithography along with their limitations. One of the main requirements to fabricate single electronics is to achieve capacitance in attofarad or less, which can be achieved by making structure less than 100nm. Optical lithography is being used in industries for mass fabrication of semiconductors is limited to feature sizes greater than 100nm if we use very sophisticated aligners.

Christoph Wasshuber [2] mentioned two approaches as top down and bottom up. In former, one starts with wafer, define structures using lithography, etch, deposit layers if required. This is the conventional approach used in semiconductor industry and we process complete wafer at one time. Most widely used approach is top down. Bottom up approach involves building of small molecules and then assembling them on top of the substrate. These molecules include nanoparticles of gold or quantum dots. This is a slow step but we can achieve high precision.

4.1 Patterning of SET

Single electron transistors are patterned using NPGS (Nanometer Pattern Generation System). Pattern is finally observed using AFM (Atomic Force Microscope) and SEM (Scanning Electron Microscope). SEM used is ZEISS SUPRA 55 VP. It can be used to perform EDAX also.

4.1.1 CAD Pattern

Program for SET pattern is written in DesignCAD LT 2000. This is windows based CAD program. Desired dimension of source and drain pads are 5μm X 5μm and for island is 100nm, diameter. The desired distance between source, drain electrode and the dot is 10nm. Figure 4.1 shows the pattern design. Refer appendix A for more details.

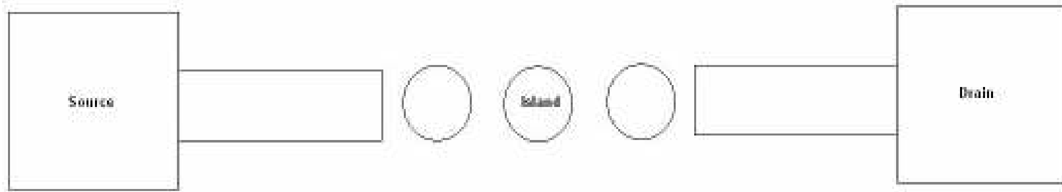


Figure 4.1 SET Design pattern

CAD file was written in such a manner so that we can expose six SET patterns as shown in figure 4.2, with different exposure doses. We also made one 50μm pad so as to locate our patterned devices.

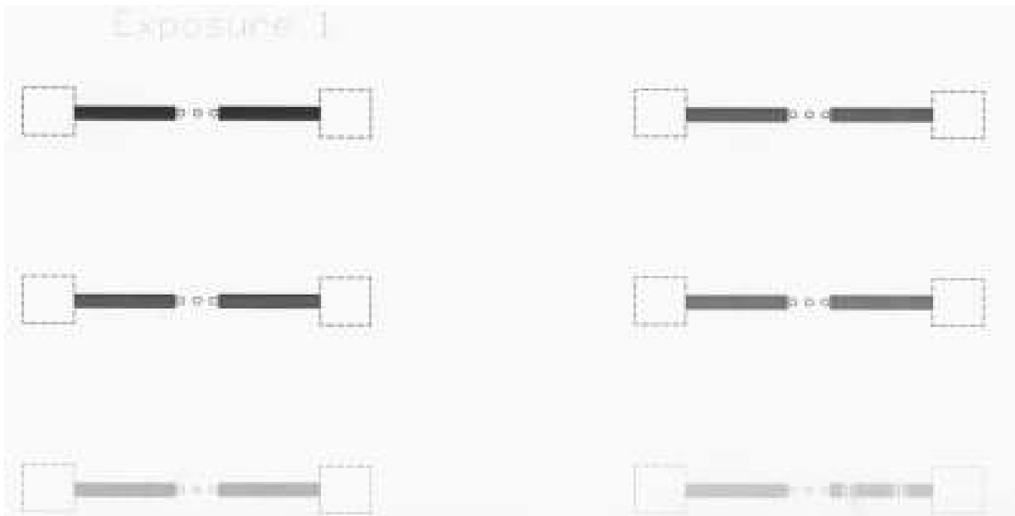


Figure 4.2 Six SET patterns at different exposure doses. Designed using Design CAD LT

4.2 Fabrication Process Flow

We used top down approach using silicon on insulator (SOI) wafers as a starting material to pattern our devices. SOI wafers with p-type doping, of size 1cm X 1cm with <100> crystal orientation. Buried oxide thickness is 140 nm with device thickness layer as 55nm. I explained the fabrication recipe in appendix A. Patterning steps are common as mentioned below:

First step is to clean SOI wafers using RCA and HF cleaning to get rid of contaminants and native oxide layer. Cleaning recipe is mentioned in appendix A. Then wafers went through dehydration bake on hot plate, if required.

Negative e-beam photoresist was applied by spin coating so as to get uniform resist layer on substrate. Resist is softbaked so as to improve adhesion. This is shown in figure 4.3

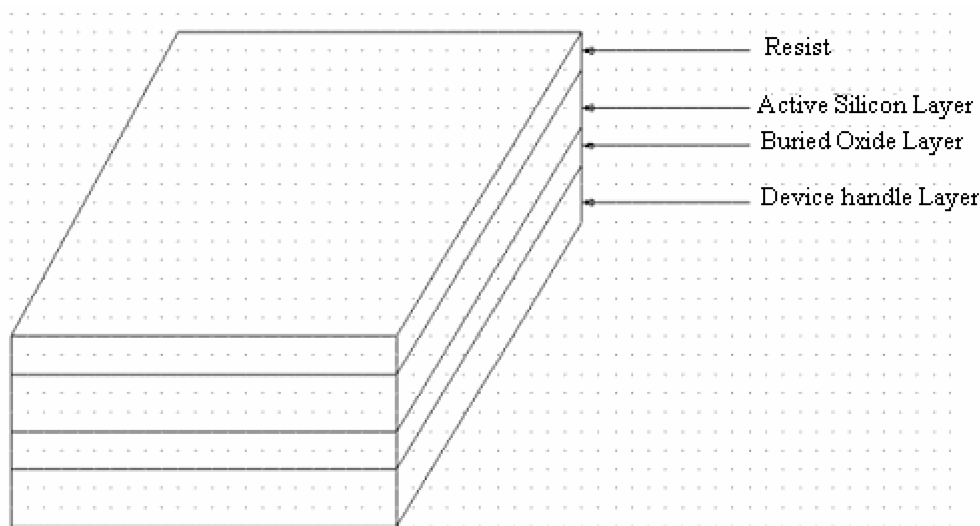


Figure 4.3 Schematic after spin coating of resist

Wafers are exposed at the desired e-beam dose for specific time. This step prints SET image on resist and we defined drain and source pads as shown in figure 4.4. Post exposure bake is also performed after this step.

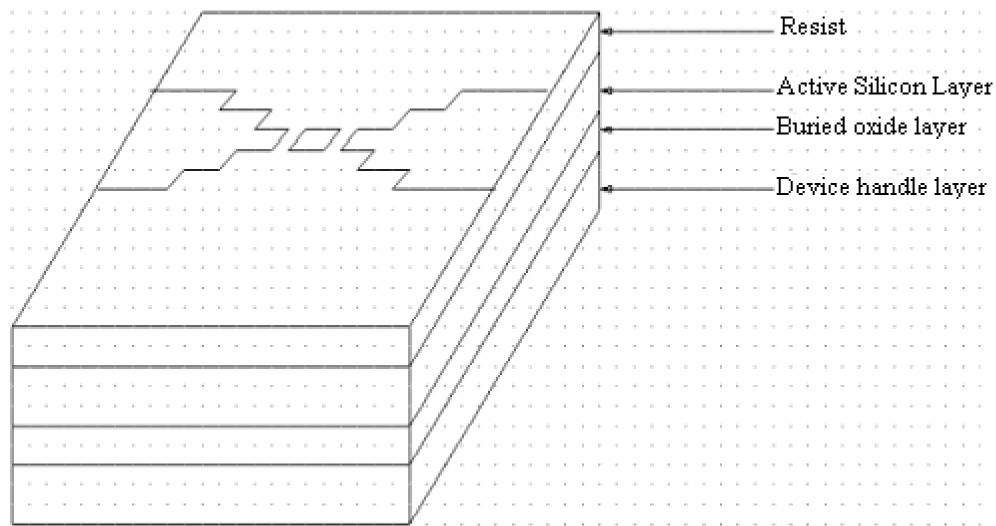


Figure 4.4 SET Image printing on resist by e-beam lithography.

Next step is to develop our wafers using a developer such as acetone for PMMA, MF 702 for UVN 30 and MIF 300 for HSQ. This step removes unexposed resist and we get our pattern on the substrate. The resist is then cured, if required so as to improve dry etch resistance .Figure 4.5 shows the substrate after developing our wafers.

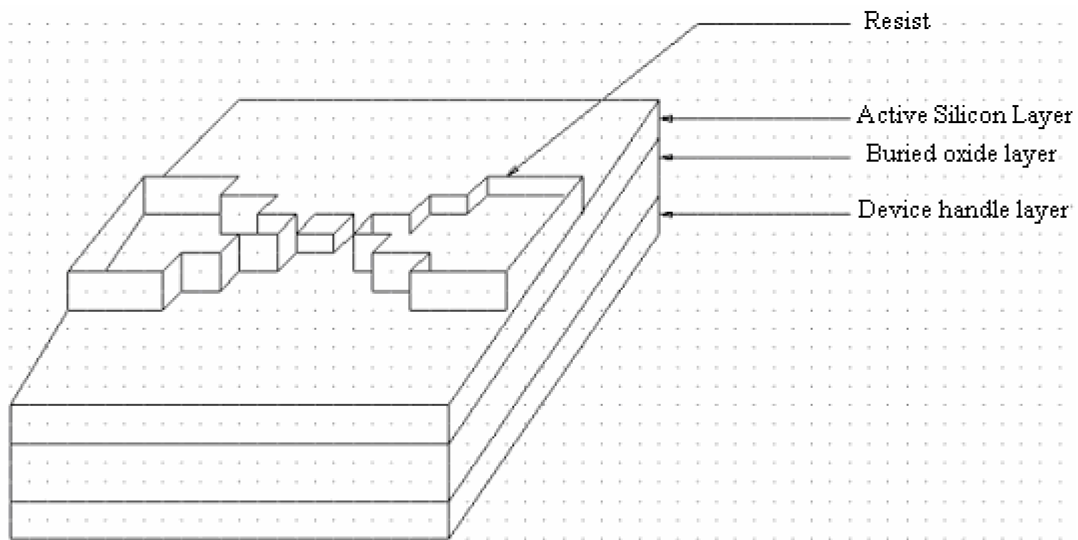


Figure 4.5 Resist image after development

Resist image is printed on silicon device layer using RIE and deep RIE. This is demonstrated in figure 4.6.

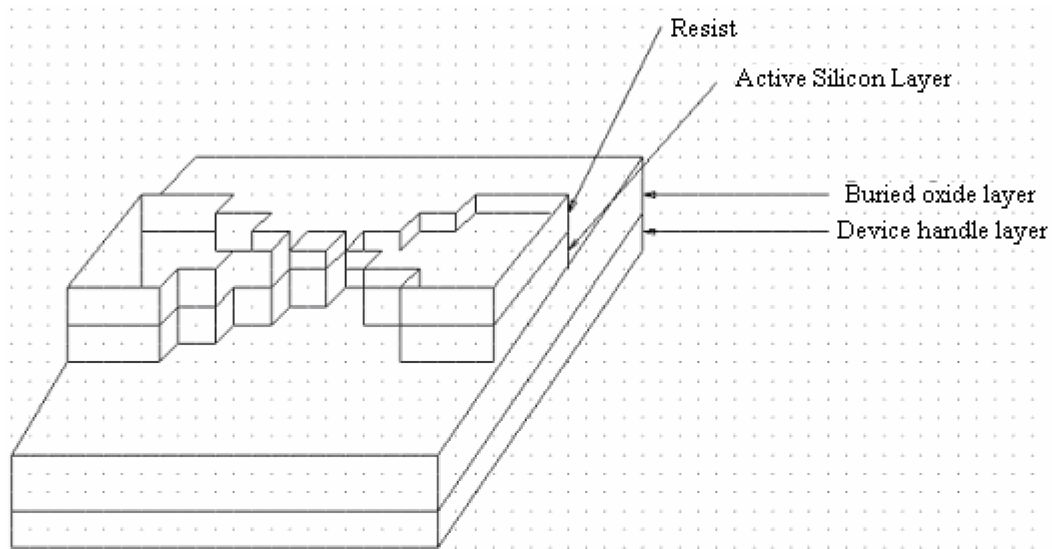


Figure 4.6 SOI wafer after dry etching

Finally resist is removed using dry etching and chemicals such as HF and H_2SO_4 . Figure 4.7 shows the SET pattern on SOI substrate.

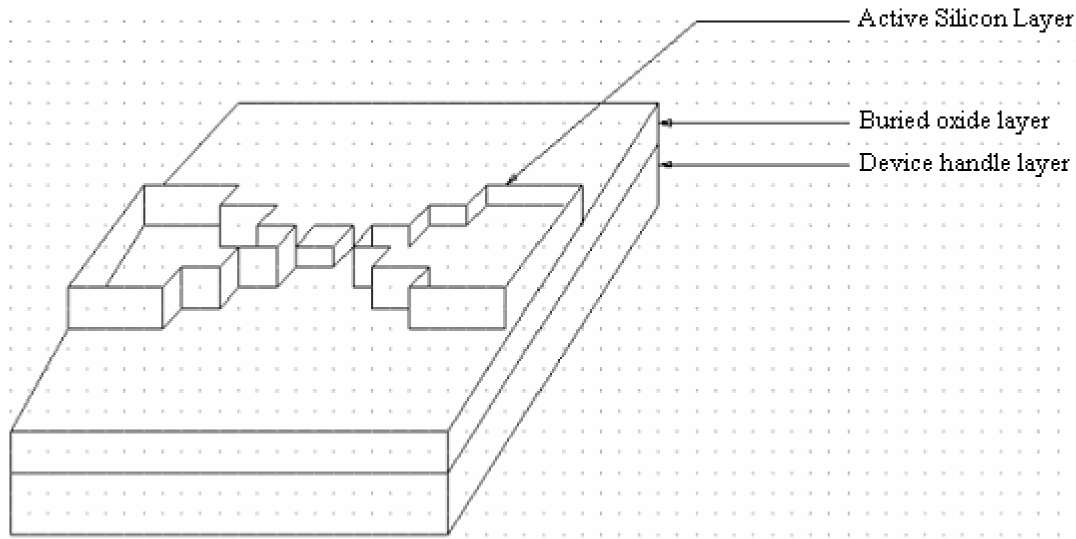


Figure 4.7 SET Device pattern on SOI substrate

4.3 E-beam Patterns

We defined six SET structures and nine wheels measuring 10μm in diameter using electron beam lithography. We used SEM and AFM to analyze our samples that were patterned using PMMA, UVN 30 AND HSQ. SEM is used to analyze devices patterned by all three resists. AFM is used to analyze patterns fabricated by using HSQ as resist.

4.3.1 PMMA Patterns

PMMA is spin coated on substrate using the recipe mentioned in appendix A. We exposed six SET patterns and nine wheels at different exposure energies ranging from 40nC to 80nC and finally developed. At such high doses the exposed PMMA gets crosslinked and acts as a negative resist. SEM was performed on the wafer to analyze sample and find the pattern dimension left after developing wafer in acetone. Figure 4.8 shows all the six SET structures at various doses. Figures 4.9 to 4.13 shows SET

structures at various doses. It can be observed that the width of tunnel junction i.e. distance between island and source or drain increases, as the dose is varied from 40nC to 80nC. These patterns define island, source and drain for SET. Figures 4.14 and 4.15 shows the wheel pattern after developing our wafer in acetone with ultimate resolution of 27 nm.

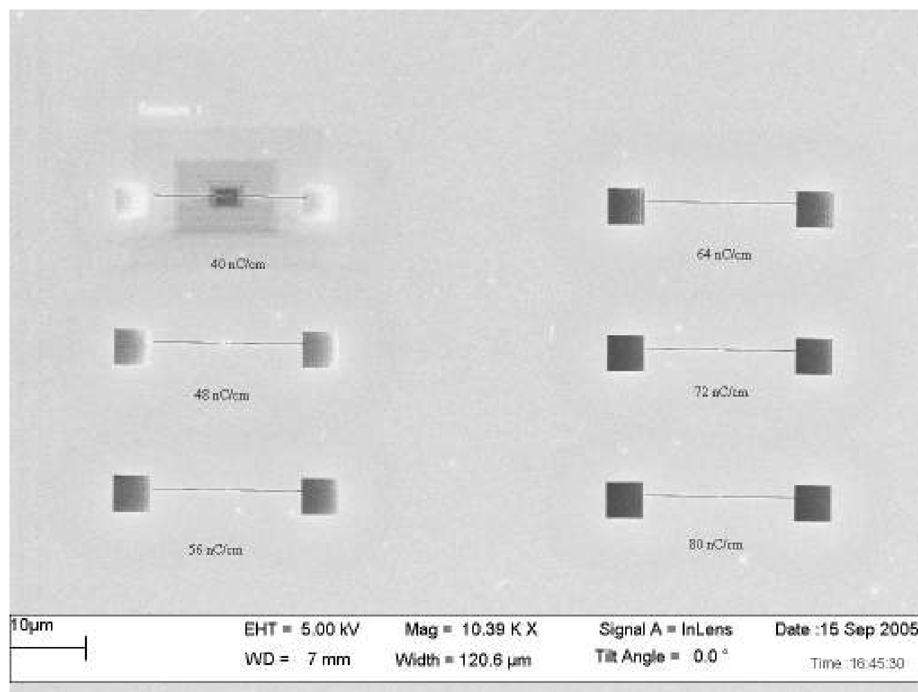


Figure 4.8 All six SET patterns at variable exposure dose

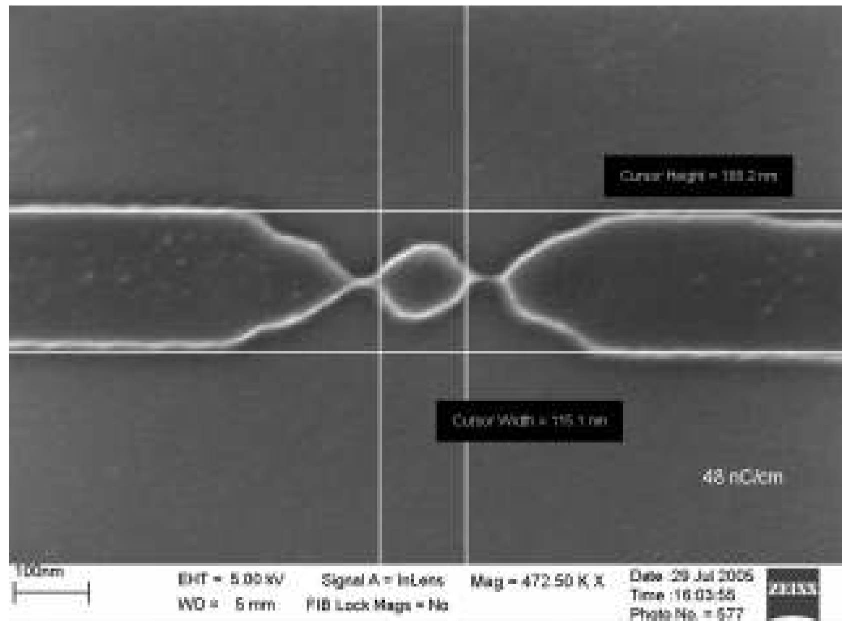


Figure 4.9 SEM Image for pattern exposed at 48nC/cm

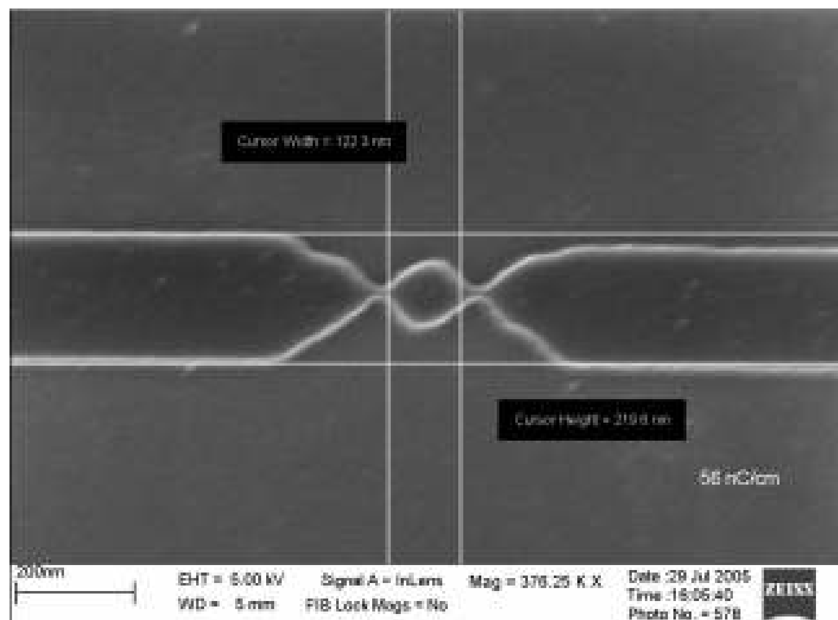


Figure 4.10.SEM Image for pattern exposed at 56nC/cm

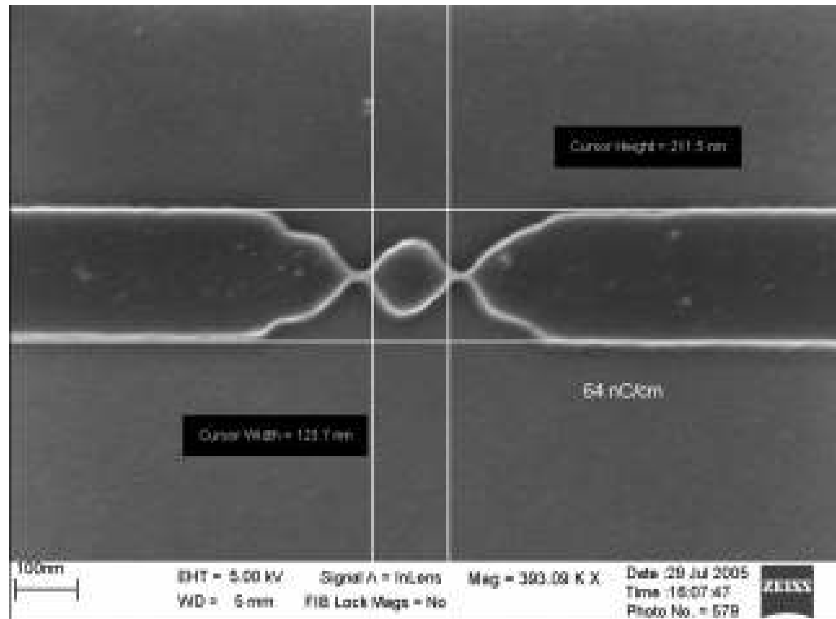


Figure 4.11 SEM Image for pattern exposed at 64nC/cm

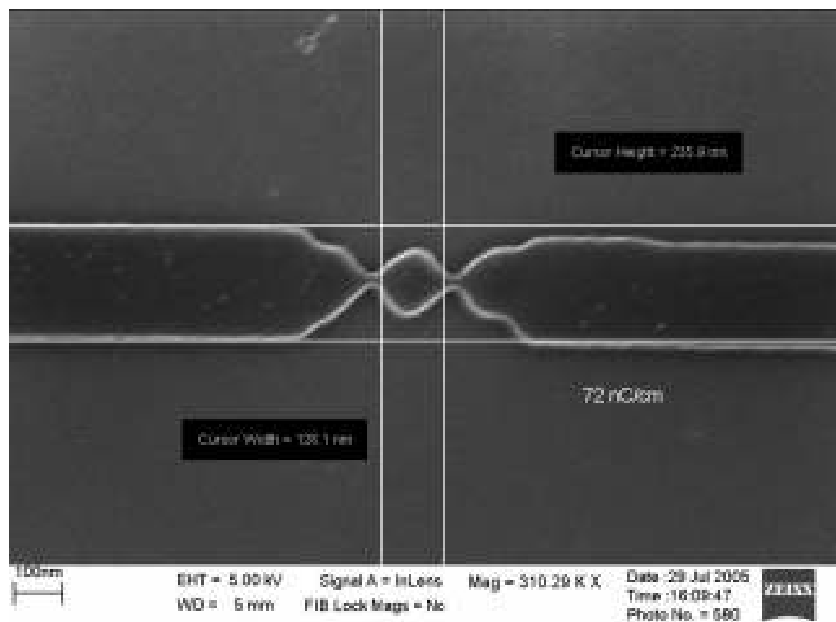


Figure 4.12 SEM Image for pattern exposed at 72nC/cm

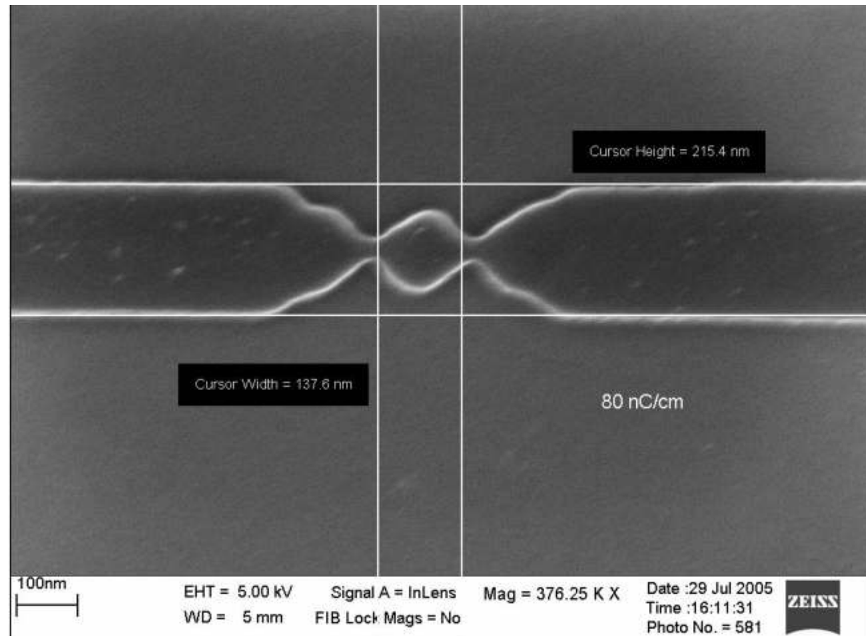


Figure 4.13 SEM Image for pattern exposed at 80nC/cm

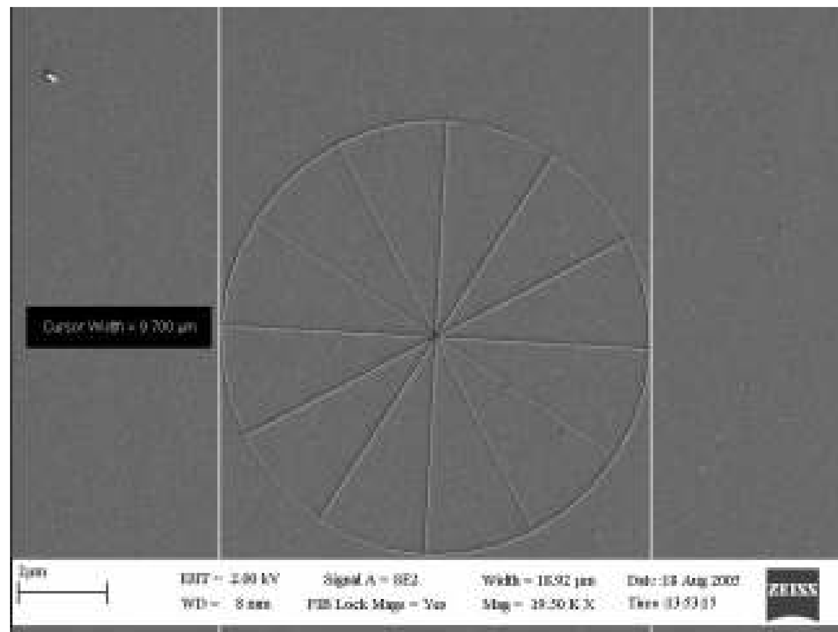


Figure 4.14 SEM image for wheel pattern

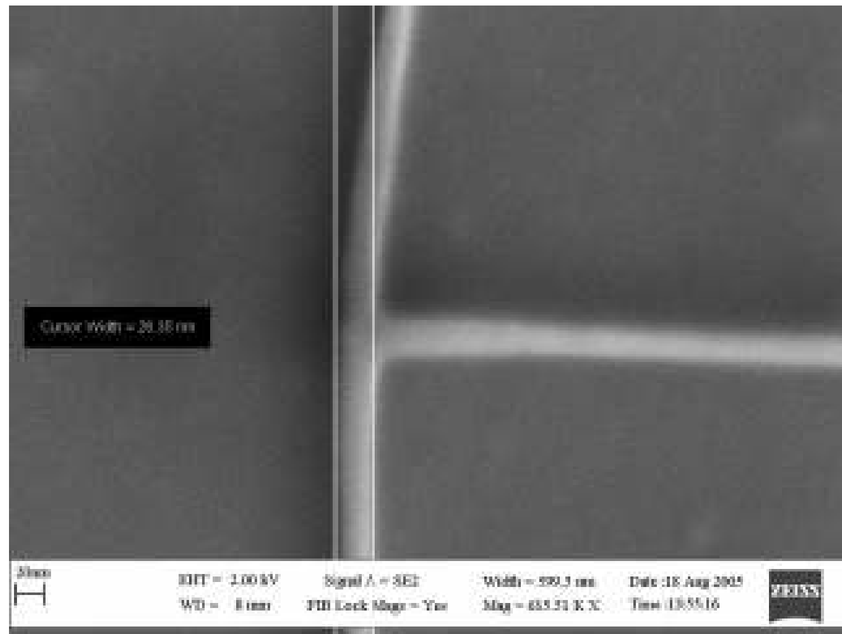


Figure 4.15 SEM image of wheel at 651.51 KX zoom

Next step is to etch the silicon on SOI that is not covered by PMMA. We tried etching silicon using a wide combination of gases such as O_2 and CF_4 and power levels ranging from 75 to 100 watts in Technics RIE, but PMMA was not able to with stand any of these gases and was getting ashed off after RIE. So we tried another process in which we deposited thin aluminum film (500À) by evaporation on substrate before e-beam resist coating and exposure. In this process aluminum was to be used as hard mask to etch silicon not covered by a layer of aluminum. This involves two extra steps i.e. evaporation of aluminum before resist application and etching of aluminum using wet etching after we develop our pattern, so as to remove aluminum which is not covered by e-beam resist. This exposes silicon on SOI wafer. We used CF4 only to etch silicon by using aluminum as hard mask and this also removes PMMA on the structure. Refer appendix A for recipe. Once we were able to etch silicon we removed remaining

aluminum in aluminum etchant. SEM is performed to look for pattern dimensions along with 50µm pad, figure 4.16 shows that etch depth is found to be 1.3µm. EDAX is also performed to find the concentration of various elements at specific point on wafer. Figures 4.17 and 4.18 shows EDAX results.

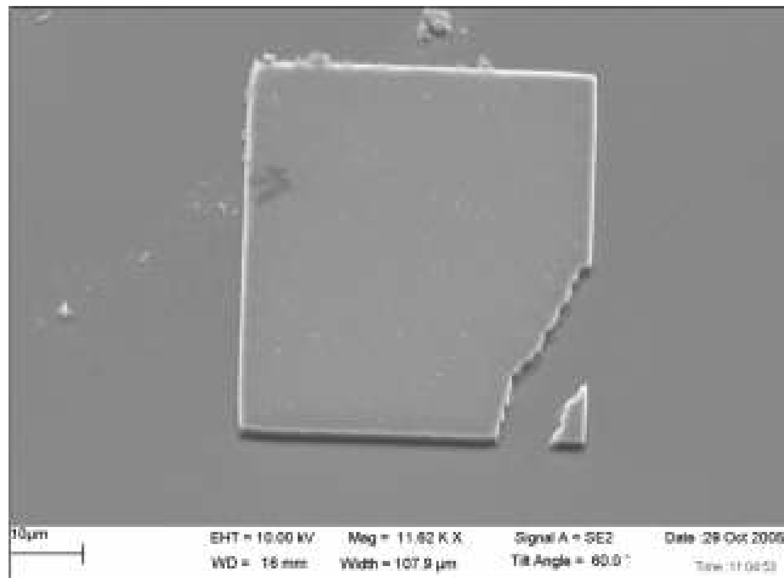


Figure 4.16 SEM image of 50 microns pad at 60° tilt angle with Al on Top

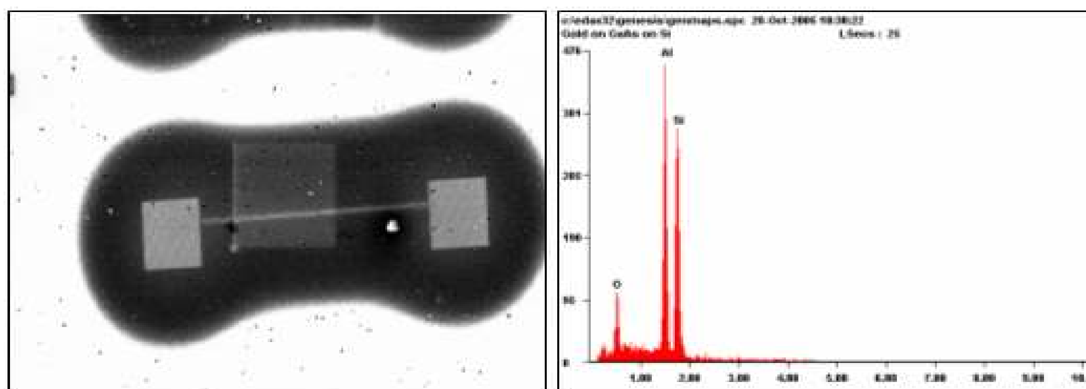


Figure 4.17 EDAX after silicon RIE and before removal of aluminum

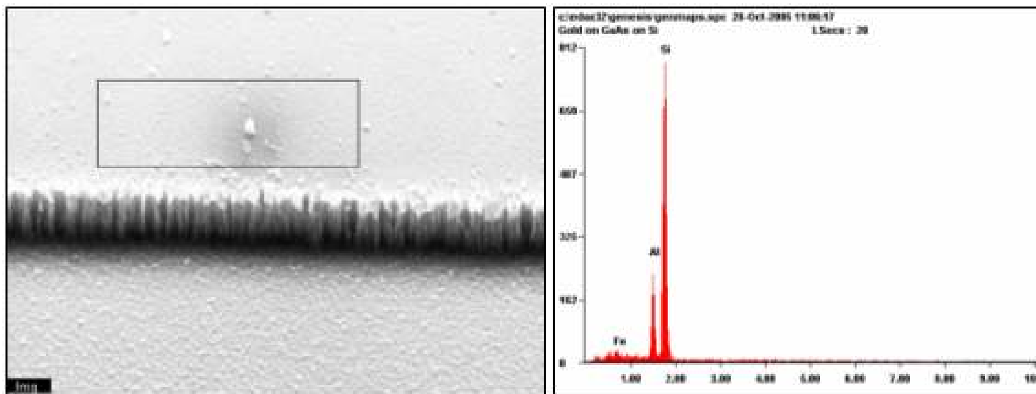


Figure 4.18 EDAX after aluminum removal from pad

We encountered lots of problems with this process also as there was an undercut due to aluminum wet etching. The resolution was also poor. So this process was discontinued.

4.3.2 UVN 30 Patterns

Six SET patterns are exposed using recipe mentioned in appendix A. Figure 4.19 shows the SEM image of six SET structures after developing in MF 702 developer. The dose is varied from $2.365 \mu C/cm^2$ to $20 \mu C/cm^2$.

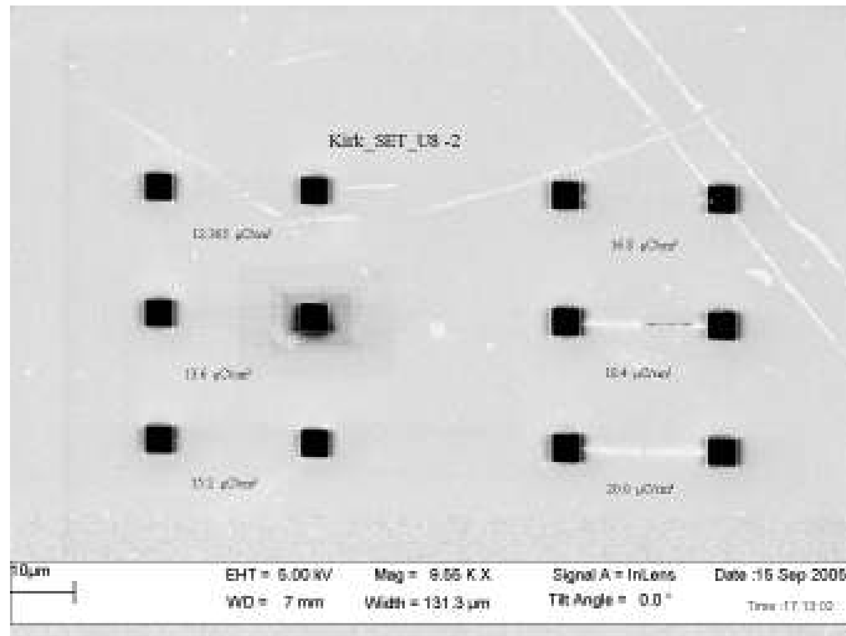


Figure 4.19 SEM image of all six SETs at different exposure dose.

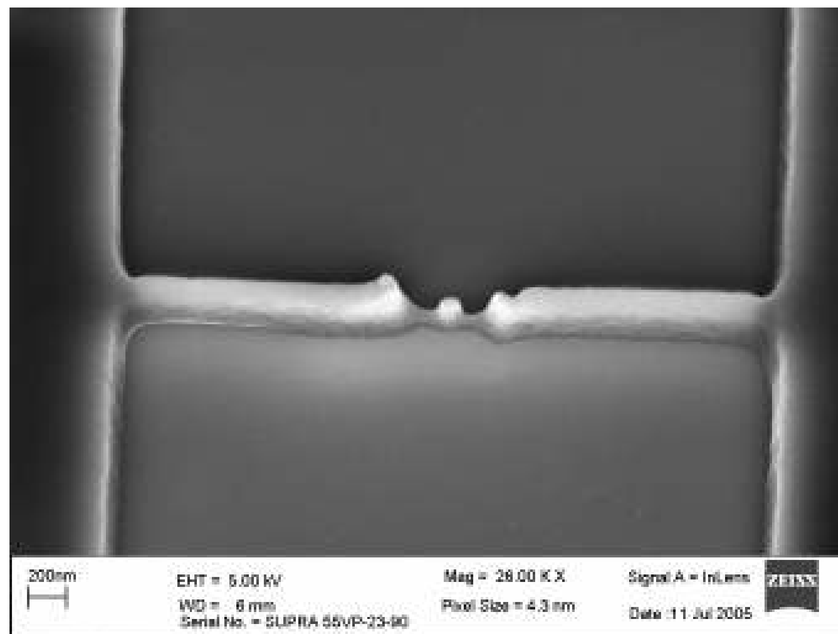


Figure 4.20 SEM Image at 60° tilt showing island

Although UVN 30 provides good dry etch resistance but its use was discontinued due to non uniform resist profile and poor resolution as seen from figure 4.20.

4.3.3 HSQ Patterns

Now hydrogen silsesquioxane (XR 1541) is evaluated as the next candidate. HSQ chemistry is explained in chapter 2. Recipe is mentioned in appendix A. Figure 4.21 shows all six SET patterns after exposure and develop step.

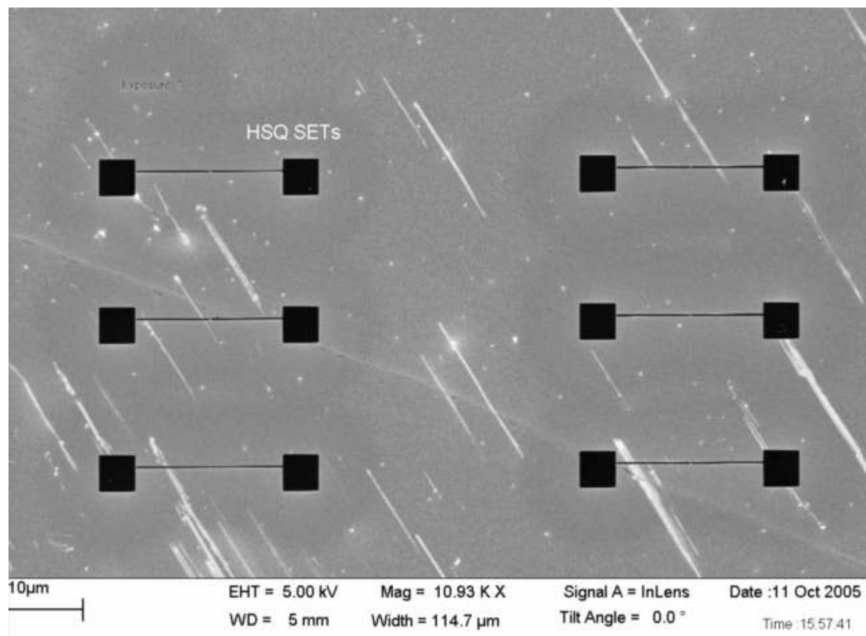


Figure 4.21 SET patterns after developing wafer in 300 MIF.

After spin coating and soft baking HSQ, wafer is exposed for six SET patterns using e-beam writer at different doses. Figure 4.22 shows SEM image for one of the patterns. This image shows that HSQ has high contrast as compared to previously evaluated e-beam resist like PMMA and UVN 30 and clearly shows a thin line of resist connecting the island to source and drain finger electrode on each side. This can be used

for the formation of tunnel junction of SET once we etch silicon on SOI using resist as mask.

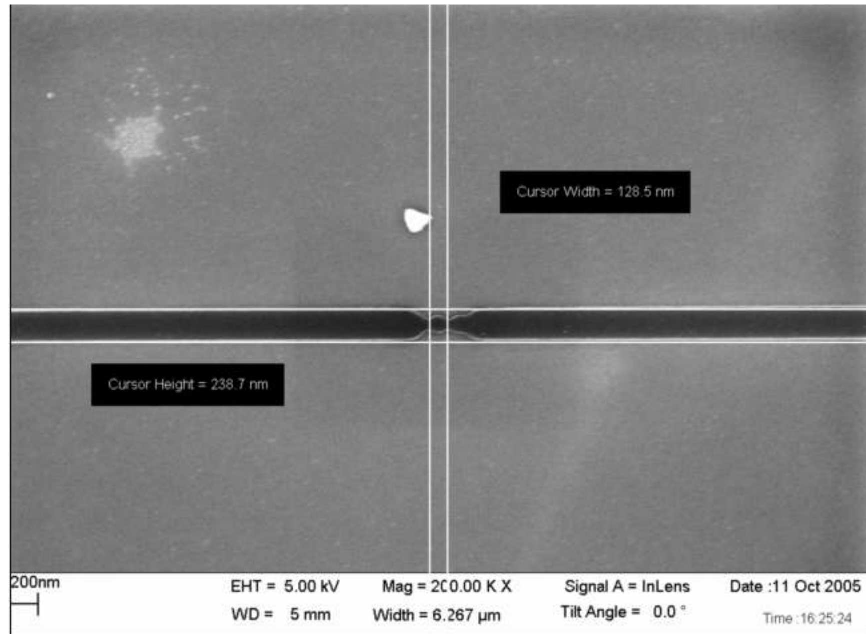


Figure 4.22 High resolution SEM image of SET pattern

4.3.4 Etching Silicon Using HSQ as Mask

Next step is to etch silicon not covered by HSQ, after developing our pattern. Details about the process are given in appendix A. We performed RIE using CF_4 and O_2 as the process gas without curing HSQ and all resist was getting removed after etching for 1 min. HSQ is cured at 400° C for 30 min in blue oven once the pattern is developed. This step improves the adhesion of HSQ to the substrate. Figure 4.23 and 4.24 shows image of the pattern after expose, develop and post develop bake step (hard bake) and figure 4.25 shows the pattern after etching silicon using RIE. It is clearly visible form figure 4.24 that there is no separation between island and finger electrodes, hence it can form tunnel junction once we etch silicon, remove resist and oxidize.

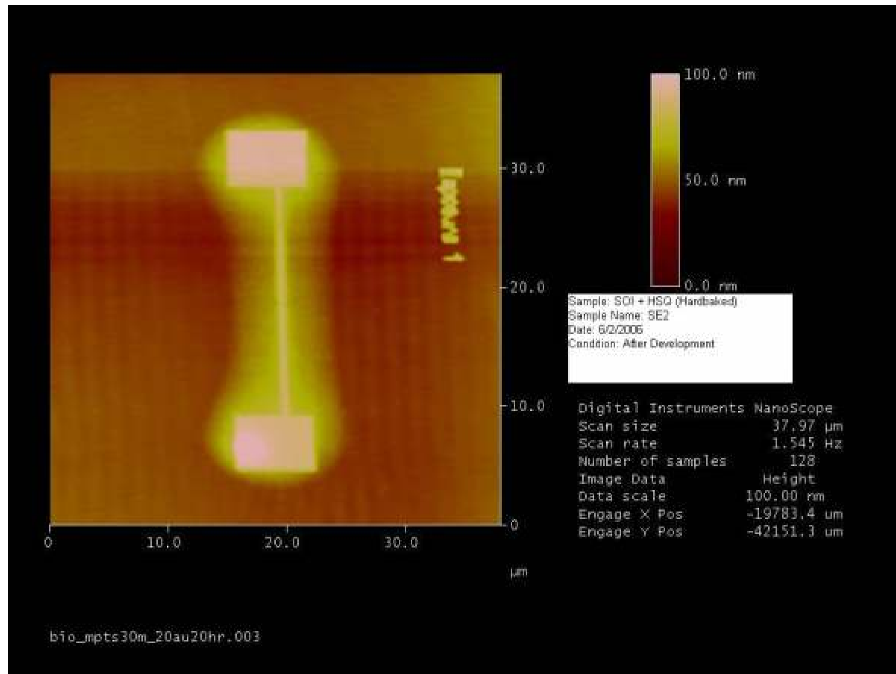


Figure 4.23 AFM image of SET structure after developing in 300 MIF

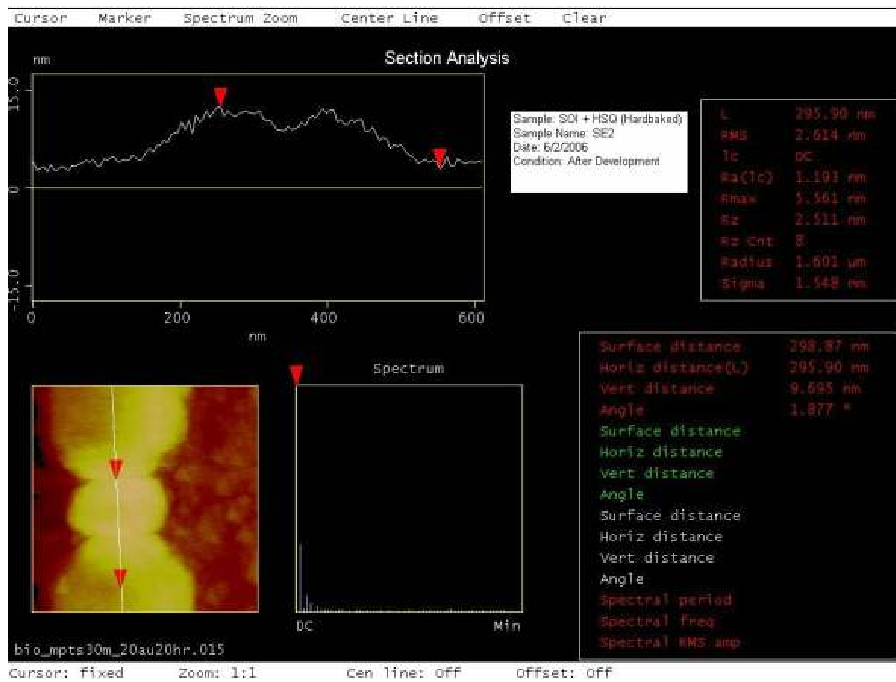


Figure 4.24 AFM image of island of SET.

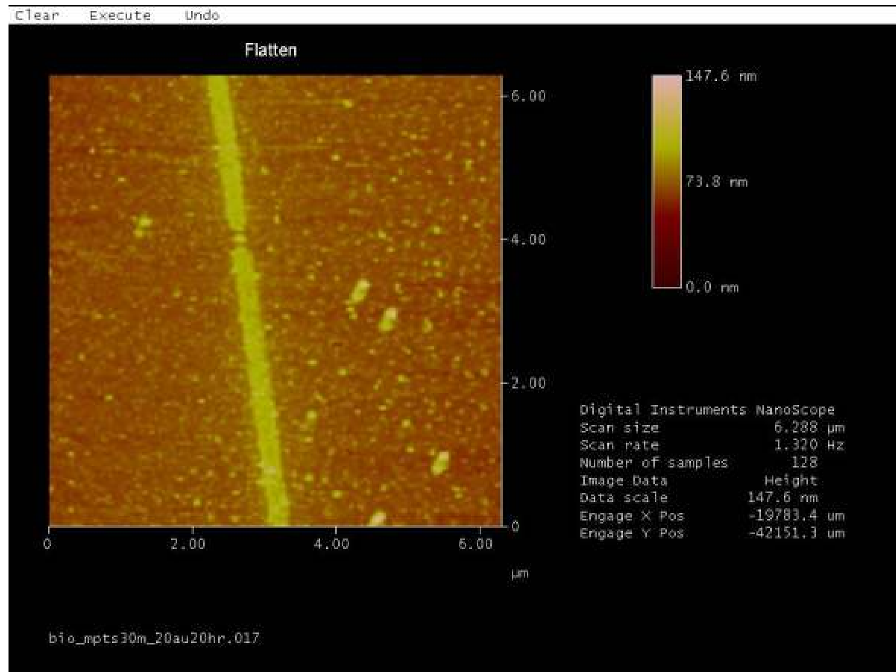


Figure 4.25 SEM image after RIE of silicon

If we look closely at figure 4.25, we can see that, after etching there is a gap between the island and finger electrodes. Thus the pattern is distorted and will not form tunnel junction for SET. This is a clear indication that HSQ has very poor dry etch resistance in CF_4 and O_2 Plasma.

Finally we used Trion Deep RIE which uses SF_6 as a process gas. Etch recipe is mentioned in appendix A. Using SF_6 as the process gas, we were able to demonstrate silicon etching without loosing linewidth and pattern. In this experiment the wafer was etched for one minute and we etched approximately 81 nm. This includes HSQ layer on top of silicon pattern. Figure 4.26 shows the pattern after DRIE and figure 4.27 shows three dimensional structure of SET pattern after DRIE. Finally HSQ is removed in CF_4 plasma to get final silicon thickness of 66nm figure 4.28.

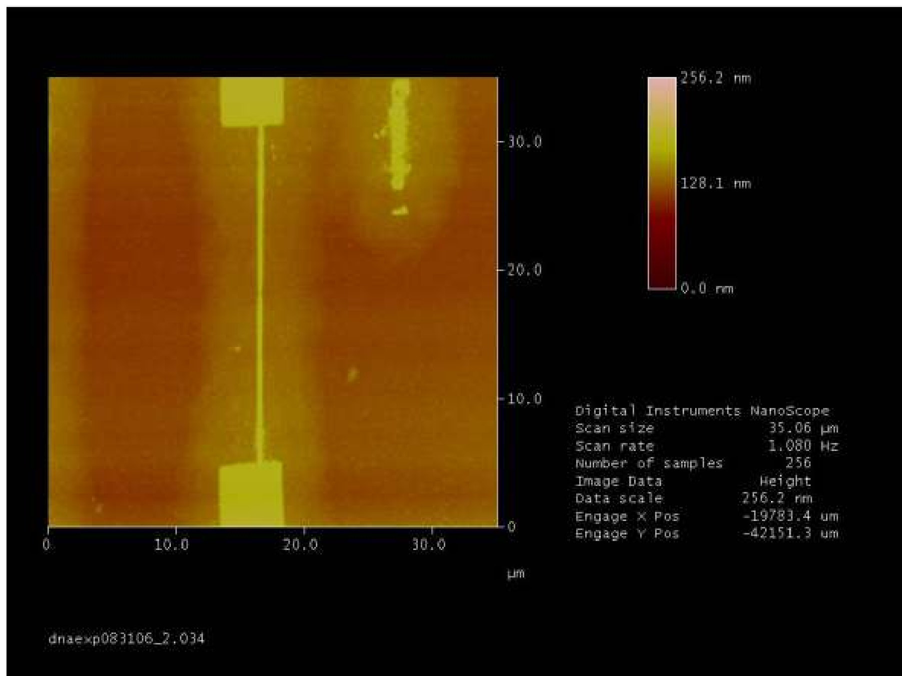


Figure 4.26 AFM image of SET pattern after DRIE

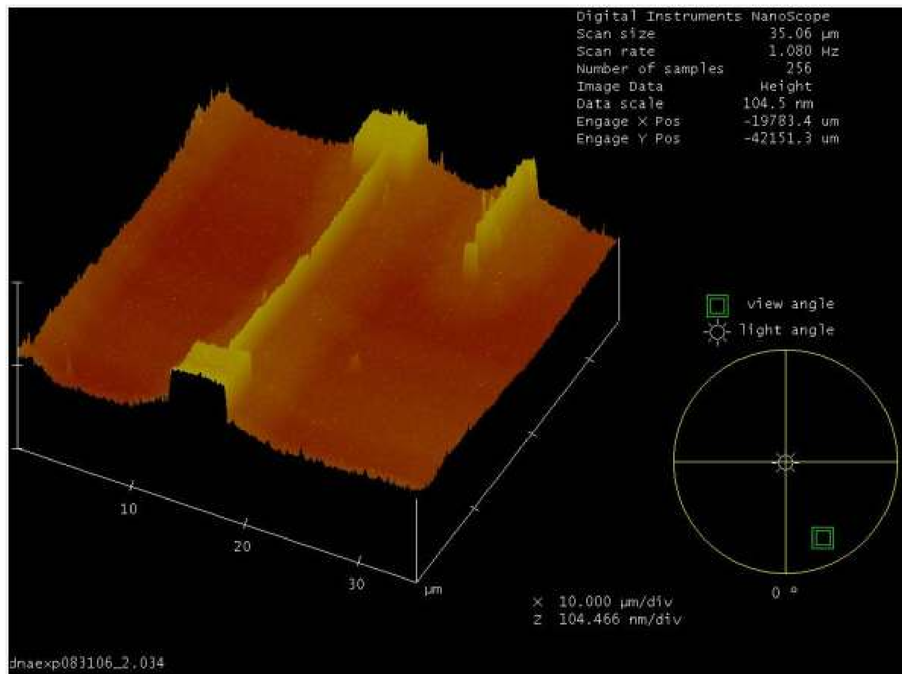


Figure 4.27 Three-dimensional AFM image of SET after DRIE

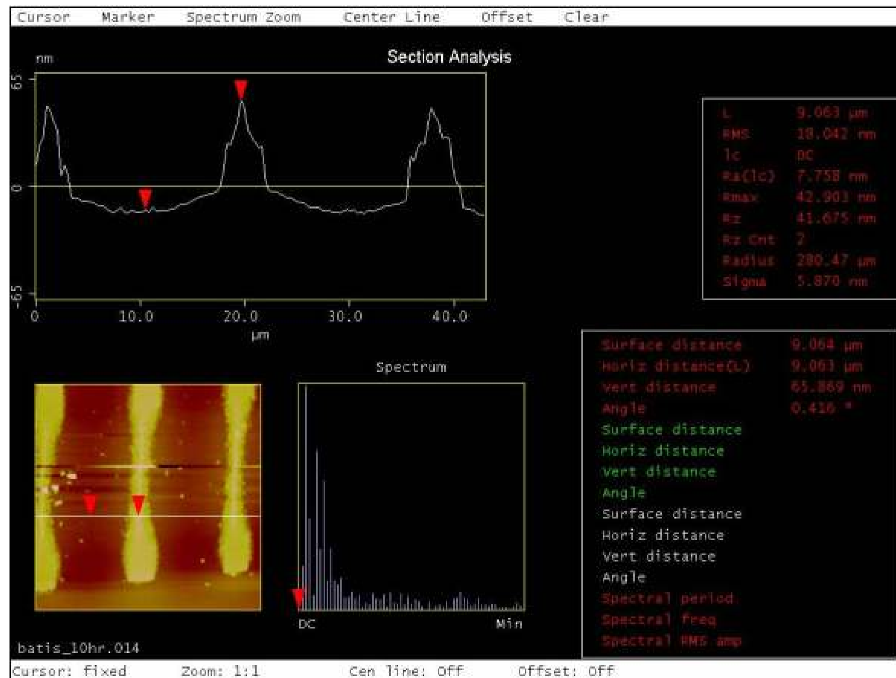


Figure 4.28 Thickness measurement after removing HSQ in CF_4 plasma

We also performed SEM on our etched SET structures as shown in figure 4.29 and 4.30. These structures still have HSQ on top of silicon and we still have a thin line connecting island and source and drain finger electrodes. This is a clear indication that after oxidation of structure it will form a tunnel junction for SET device. Figure 4.30 shows the SET pad at 45° tilt angle.

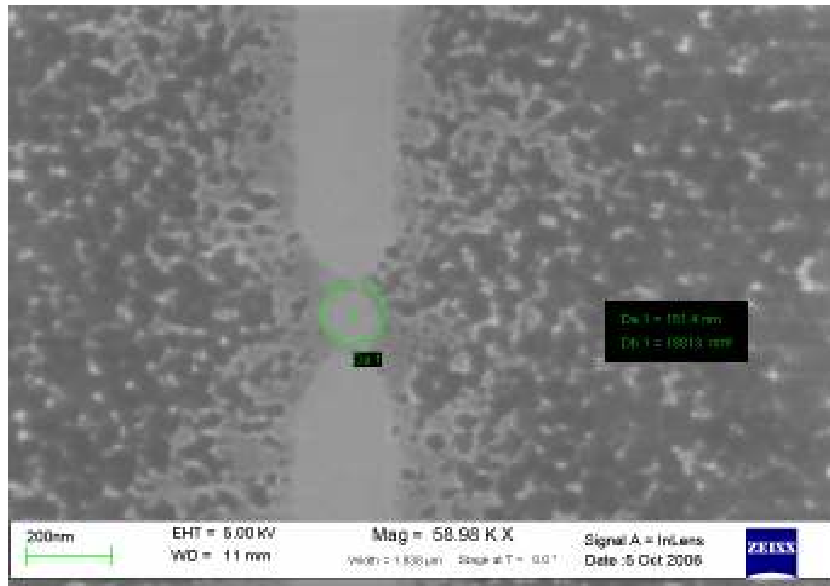


Figure 4.29 SEM Image of island after DRIE

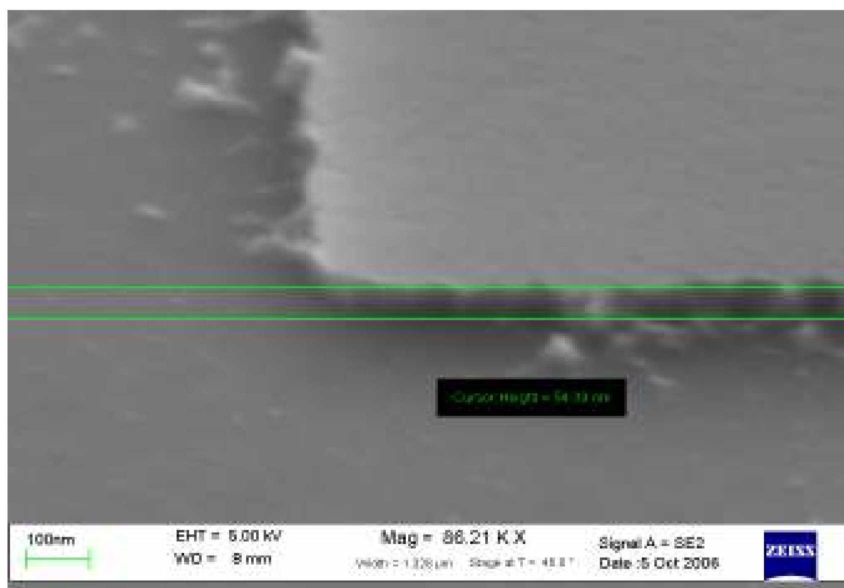


Figure 4.30 SEM image showing 5µm pad at 45° tilt

CHAPTER 5

SIMULATIONS OF SET

Computer simulations have emerged as a very powerful tool to analyze device performance [26]. This can help us to optimize device process and performance before we actually fabricate device. This increases device performance, reliability and yield. Due to exponential growth of computing, the simulation became widespread and cheap practice. Nobody can think to live without simulations in today's high tech society [2]. This chapter focuses on simulation techniques for single electron circuits.

5.1 Simulation Methods for Single Electronics

Conventional circuit simulators based on kirchhoff's law can be used when the electronics charge is assumed continuous, but all single electron circuits exhibit tunneling and therefore the charge transport is discrete. There are fundamentally three different approaches for simulation of single electron circuits, namely Monte Carlo, SPICE macro-modeling, Master Equation.

5.1.1 Monte Carlo

As mentioned earlier, all single electron circuits exhibit discrete transfer of charge and the event of the electron tunneling has stochastic nature. So we cannot use conventional approaches for SET simulation. All stochastic events are well simulated in with Monte Carlo approach [27]. The use of Monte Carlo method for simulation of single electron circuits was first proposed and implemented by Bakhvalov [28] and coworkers in 1989. Later on this method is adopted by other groups also [29] [30] [31].

K.K. Likharev explained orthodox theory and derived a tunnel rate equation for any junction in a large circuit [3] given by:

$$\Gamma(\Delta F) = \frac{\Delta F}{e^2 R_T (e^{\Delta F/(k_B T)-1})} \text{ ....5.1}$$

where ΔF is the change in free energy when an electron passes through the tunnel junction. Γ is tunnel rate and R_T is the tunnel resistance. The change is free energy has to be taken from the entire circuit [32]. For detailed calculation of ΔF readers are referred to book by Wasshuber [2]. Once we combine Poisson process and tunnel rate given by equation 5.1 we can assemble building blocks for Monte Carlo based simulation method. The Poisson distribution can be rearranged to yield

$$\tau = -\ln(r)/\Gamma \text{ ....5.2}$$

where r is the random number between [0,1] and Γ is the electron tunneling time.

The working of Monte Carlo method can be explained as follows. It starts form the list of all tunneling events with their tunnel rates. Then it calculates complete random tunneling times τ_i for all the events. The event that has smallest τ will happen first and is considered as winner of the Monte Carlo step. It updates charges and voltages on all circuit nodes. It uses stochastic sampling to calculate new tunnel rates and thus determines new winner. So we can analyze microscopic behavior of the circuit by performing this step repeatedly. For more details about this method reader is referred to ref. 2.

5.1.2 SPICE macro-modeling

SPICE is a software that can be used to model I-V characteristics of SET in the same way as we model MOSFET and BJT. SPICE is considered to be faster simulation tool as compared to Monte Carlo or Master Equation approach and therefore can be used to simulate large single electron circuits. Günther and coworkers have performed simulations of SET circuits as well as SET and FET integrated circuits [33]. Another practical model is developed by Kyung and co workers [34]. This model is based on physical phenomenon in realist silicon SETs. They compared SPICE simulation results with those of measured characteristics of silicon SETs.

The only disadvantage of SPICE is that, is does not capture any coulomb interaction between adjacent transistors, which is sometimes required for correct analysis [32]. In order to tackle this problem one needs to perform preprocessing step before single electron simulation is performed [2].

5.1.3 Master Equation

The master equation tries to solve equation 5.3 of charge transport process in single electron circuits.

$$\frac{\partial P_i(t)}{\partial t} = \sum_{j \neq i} \left[\Gamma_{ij} P_j(t) - \Gamma_{ji} P_i(t) \right] \quad \text{...} 5.3$$

where Γ_{ij} denotes transition form state *j* to *i* and $P_i(t)$ is the time dependent occupation probability of state *i*. This is called master equation. This is matrix exponential. It is difficult to evaluate matrix exponential accurately for general case. Krylov subspace and Schur-Frechet algorithms are the two methods to solve master equation [2].Another

method is demonstrated by K.K. Likharev and coworkers. They explained a new method based on a numerical solution of a new matrix equation for vector probabilities of various electric charge states of the system [35].

For Master Equation the tunnel rates are calculated the same way as we do for Monte Carlo method. The only disadvantage of this method is that one needs to have knowledge of all relevant states a circuit can occupy in order to define system of equations. It is considered that the possible states are infinites but one has to look for the most relevant ones. This is impossible for most circuits because if we have too many states it makes matrix complex and if we have few states it does not tells the whole story. In order to solve Master Equation one has to apply adaptive scheme as mentioned in ref. [35]. Master Equation is a good approach for small circuits but it becomes cumbersome as complexity of the circuit increases.

5.2 Simulation Software

All commercial single electron simulation packages available today are based on one of the three approaches mentioned above in section 5.1. In this section I will list and explain briefly some of the important software packages used for single electron circuit simulation.

5.2.1 SIMON

SIMON is a single electron device and circuit simulator. It simulates propagation of electrons through network consisting of small tunnel junctions, capacitors, current and voltage sources. It calculates probabilities for every possible tunnel event and uses Monte Carlo method to choose one event from a set of possible

event. The probabilities of tunnel events will change over time as distribution of electrons in network changes for every tunnel event and voltage sources also vary with time. So it calculates a new set of probabilities for every tunnel step. It also has capability of simulating co-tunneling by using only Monte Carlo approach or by using combination on Monte Carlo and Master Equation. It is available for both Windows and Mac based machines. It has a graphical user interface to pick and drop various components [36].

5.2.2 MATLAB

MATLAB is another software tool used by engineers to do all kind of simulations in the field of mechanical engineering, electrical engineering, etc. One such SET program is developed by David Berman from MIT. This program calculates the current through SET as a function of source-drain V_{ds} voltage for a given value of gate voltage V_g. The gate voltage V_g is predefined in the program. Capacitance, resistance and temperature are also predefined in the program. We performed our SET simulation using this MATLAB program. Although this program was written for just one value of gate to source voltage but, we modified it for five different values of gate voltages. Simulations are performed at temperatures at 4.2 Kelvin and 77 Kelvin. The program correctly simulates the characteristics of SET device. The tunneling rate equations are mentioned in reference [38].

5.3 Simulation Results

The simulations shown in figure 5.1 and 5.2 demonstrate SET I-V characteristics and are performed at 4.2K and 77K respectively. I-Vs for SET are

plotted using MATLAB software as mentioned earlier. This software will calculate current through SET for a given values of gate voltage V_g and drain-source voltage V_{ds}. We defined capacitance, tunnel resistance and temperature in the program itself.

In figure 5.1 the flat region in the I-V curve near V_{ds} = 0V and I_d =0nAmp demonstrate a coulomb blockade region. This occurs at small values of V_{ds}. The maximum width of Coulomb blockade region is $2E_C/e$. It can be observed that the width of the coulomb blockade region reduces from $2E_C/e$ to 0 as V_g is increased from 1 to 1.8 Volts. At higher temperatures of about 77K and gate bias between -0.8 to 0.8 V the coulomb oscillations almost die as shown in figure 5.2.

Table 5.1 SET Simulation Parameters for T= 4.2 K

Parameter	Value
Temperature	4.2 Kelvin
Drain capacitance (C_d)	3.3af
Source Capacitance(C_s)	4.8af
Gate capacitance (C_g)	1 af
Drain Tunneling Resistance(R_d)	7.3M Ω
Source Tunneling Resistance (R_s)	4M Ω
Gate Bias (V_g)	1 to 1.8V

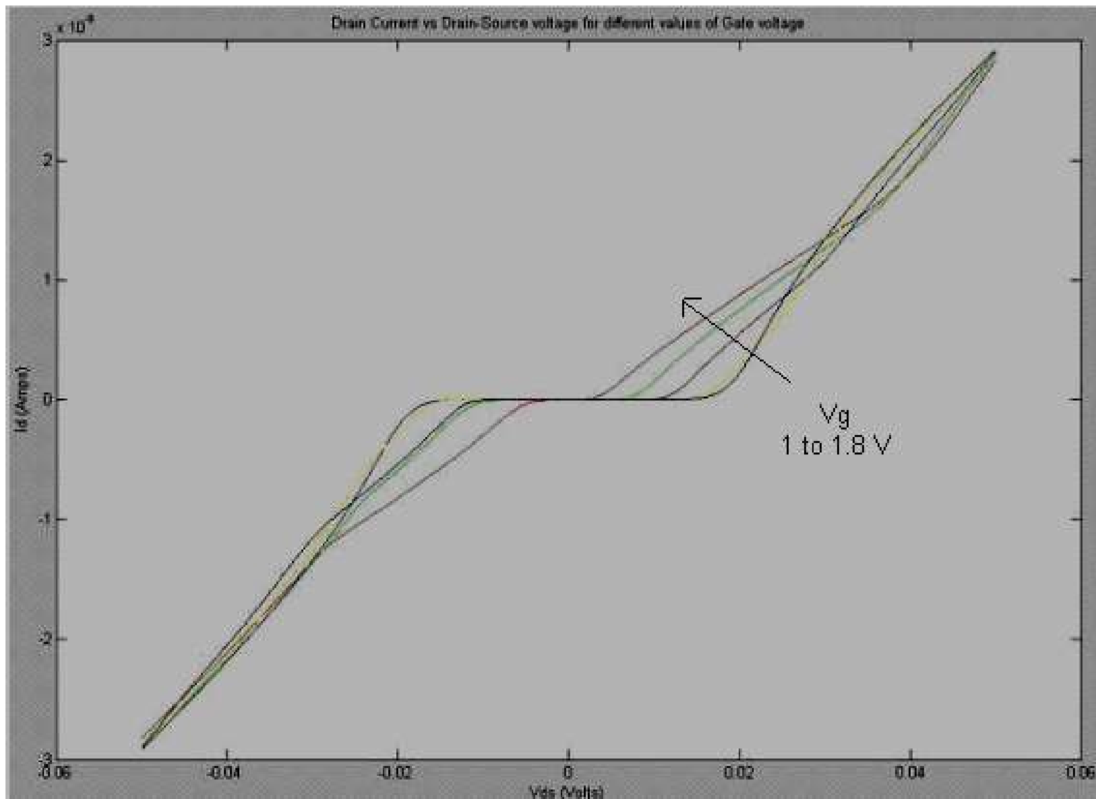


Figure 5.1 SET I-V characteristics at T= 4.2K

Table 5.2 SET Simulation Parameters for T= 77 K

Parameter	Value
Temperature	77 Kelvin
Drain capacitance (C_d)	1.045af
Source Capacitance(C_s)	1.045af
Gate capacitance (C_g)	1 af
Drain Tunneling Resistance(R_d)	2.65M Ω
Source Tunneling Resistance (R_s)	2.65M Ω
Gate Bias (V_g)	-0.8 to +0.8V

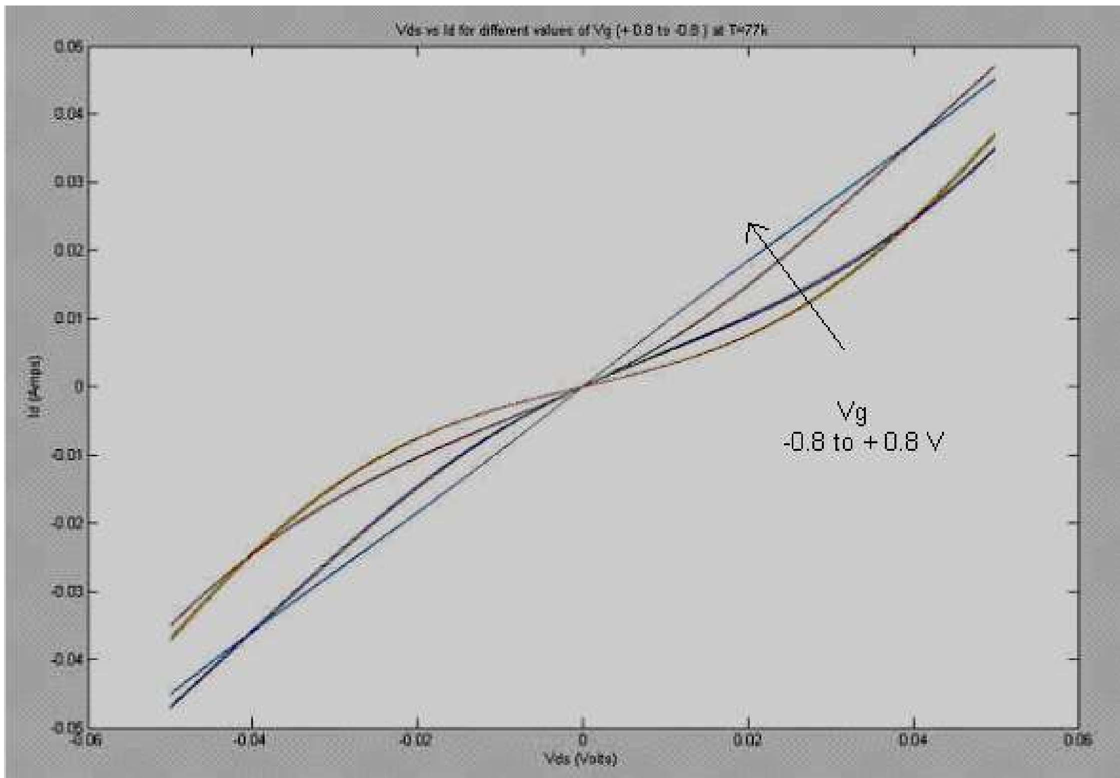


Figure 5.2 SET I-V characteristics at T= 77K

CHAPTER 6

SUMMARY AND FUTURE WORK

In this thesis, advances have been made in enhancing and developing performance of electron beam resist to pattern SET structures using high resolution e-beam lithography.

SET patterning technique was demonstrated using PMMA, UVN 30 and HSQ on silicon on insulator wafer. We used negative e-beam resists such as HSQ and UVN 30. PMMA is a positive e-beam resist which is converted to negative e-beam resist by using a very high exposure dose. We also performed evaluation tests for HSQ, UVN 30 and PMMA. We were able to demonstrate line width of approx. 26 nm using PMMA resist system.

Patterns on the resist are also transferred on silicon underneath resist using dry etching. It was found that HSQ and PMMA has very poor dry etch resistance in presence of CF_4 and O_2 plasma , but HSQ works good in SF6 plasma in presence of helium and argon as inert gases. UVN 30 offers a good dry etch resistance at the cost of low resolution.

It has also been observed that, for PMMA the width of line joining island to source and drain electrodes increases with increase in e-beam dose. If, somehow we can manage to etch silicon using PMMA as etch mask we can precisely form a tunnel junction of desired size and capacitance.

We also demonstrated the evaporation of aluminum on our wafers to use it as an etch mask to etch silicon underneath it but, it was observed that there is a severe loss of resolution and undercut. This happens due to aluminum wet etching.

We discussed SET simulation methods such as Monte Carlo, Master Equation and SPICE Macro modeling. SET simulations are performed at temperatures 4.2K and 77 K using MATLAB program. It is observed that as the voltage increases the width of coulomb blockade region decreases. At temperature of 77K we were not able to observed coulomb blockade oscillations. So in order to simulate SET we need low value of temperature and small value to capacitance in attofarads.

The future work involves the formation of tunnel junction for SET after defining source, drain and island on silicon substrate. We can form tunnel junction using PADOX (pattern dependent oxidation) approach [39, 40]. The next step involves the growth of oxide by dry oxidation. This will further reduce width of the tunnel junction. N-type poly silicon will be deposited by LPCVD to form control gate. Next a small layer of isolation oxide will be grown to isolate device. Finally contact holes for source, drain and gate regions will be opened followed by aluminum evaporation to form device pads. Further, we also plan to evaluate PMMA as etch mask in SF_6 Plasma.

APPENDIX A

FABRICATION RECIPIES

All processing steps are performed at UTA NANOFAB, except the SIMOX SOI wafers which are from IBM.

WAFER SPECIFICATIONS

Device layer: 55nm

Preparation Method: SIMOX

Buried oxide layer (BOX): 140nm

Orientation: 100

Doping: P-type

1. Cleaning

This is one of the most important steps and is common to all of our resist processes.

a. RCA cleaning was performed on all the samples to remove any contaminants or metal impurities. Mix 3:1 H_2SO_4: H_2O_2. Warm liquid to 135^oC. Immerse wafers for 10 minutes. Rinse them in DI water. Mix NH_4OH, DI water and H_2O_2 in ratio of 1:10:1. Then warm solution to 70^oC. Immerse wafers in solution for 5 minutes. Rinse wafers in DI water. Mix HCL, DI water and H_2O_2 in ratio of 1:10:1. Warm solution to 80^oC. Immerse wafers for 5 min. Rinse them in DI water and blow dry with nitrogen.
b. Immerse wafers in HF for 30 seconds to remove native oxide.
c. Rinse in DI water and blow with nitrogen gun.

2. Spin Coating, Soft Bake, Exposure, Post Exposure Bake, Develop

PMMA

950K Molecular weight PMMA is used.

a. Prepare 2% PMMA by mixing 11 ml PMMA and 51 ml Anisole.

b. Spin PMMA at 4000 RPM for 60 seconds.

c. Bake using temperature controlled hot plate at 180 ^{o} C for 90 seconds.

d. Expose six SET patterns and one 50μm pad using NPGS at line dose range between 40nC to 80nC and area dose of 80,000μC/cm^2. The e-beam current used is 40pA and variable beam aperture depending on pattern size. It takes about 14 minutes to write six patterns.

e. The time between step c and d is critical. To get best results, expose within two hours of spin coating resist.

f. Post exposure bake at 180 ^{o} C for 90 seconds.

g. Develop wafer by dipping in using acetone for 1 min followed by rinse in isopropanol and blow dry.

UVN 30

a. Bake wafer on hot plate for 10 minutes at 140 ^{o} C. This will remove moisture

b. Spin HMDS at 3000 RPM for 30 seconds.

c. Spin UVN 30 at 5000 RPM for 30 seconds to get 0.4μm thickness.

d. Bake on hot plate for 90 seconds at 140°C.

e. Expose six SET patterns and one 50μm pad using NPGS, The e-beam current used is 40pA and variable beam aperture size depending on pattern size.

f. Post Exposure bake on hot plate at 130°C for 40 sec.

g. Develop wafer in MF 702 developer for 90 sec followed by rinse in DI water.

HSQ

a. Spin HSQ (XR 1541) at 4000 rpm for 60 seconds to get approx. 40-55 nm thickness.
b. Bake on hot plate with temperature feedback control at 225°C for 120 seconds. This step is critical.
c. Expose six SET patterns and one 50µm pad using NPGS. The e-beam current used is 40pA and variable beam aperture size. It takes 41 Sec to write 6 SET patterns.
d. Perform post exposure bake 225°C for 120 seconds.
e. Develop in MIF 300 for 70 Sec followed by rinse for 10 sec in 9 parts DI water and 1 part MIF 300. Rinse in DI water for 10 Sec and blow dry.

3. Etching

RIE

Reactive ion etching is performed using Technics RIE. We performed silicon etching on SOI substrate using PMMA as mask, aluminum as mask and HSQ as mask respectively. In this report, I am going to discuss etching of silicon using aluminum as mask and HSQ as mask.

A. Silicon etching using aluminum as etch mask

We used CF_4, 10sccm as process gas with base pressure of 27 mtorr. Pressure with gas flow is 106 mtorr. Power used is 100 watts. Pressure with power is 120 mtorr. The sample is etched for 12 minutes. We did not used oxygen as it might form aluminum oxide

B. Silicon etching using HSQ as etch mask

The resist is hard baked at 400°C for 30 minutes after develop step. We used CF_4 and O_2 with flow rates of 25sccm and 3 sccm respectively. Base pressure is 35 mtorr. Power used is 100W and sample is etched for 110 sec. Etch rates are very small about 10-20 nm per minute and HSQ has poor dry etch resistance in CF_4 and O_2 plasma. So HSQ also gets removed along with silicon during RIE.

DRIE

Deep RIE is performed using Trion DRIE equipment. We used Trion Deep RIE to etch silicon using HSQ as etch mask. We performed this operation in three stages after mounting 1cmX 1cm sample on top of 4 inch wafer. We performed this process four times.

Stage I

SF_6: 20sccm

He: 200sccm

Ar: 20sccm

Time: 10 sec

Pressure: 50 torr

No etching was performed during this step. This step is to stabilize the gas flow and set initialize pressure.

Stage II

SF_6: 20sccm

He: 200sccm

He pressure Set Wafer backside: 7 torr

Ar: 20sccm

Time: 15 sec

ICP Power Upper Electrode: 1000 Watts

RIE Power Lower Electrode: 50 Watts

Etching was performed during this step

Stage III

This is to vent the system and purge He

He: 200sccm

Pressure Set: 150 torr

Time: 20 sec

ALUMINUM ETCH PROCESS

After depositing approximately 50nm of aluminum using thermal evaporation followed by resist spin coating, bake, exposure, post exposure bake and resist develop; image is transferred onto aluminum underneath it. This step involves removal of aluminum using wet etching. The solution comprises of 160 parts phosphoric acid, 10 parts acetic acid, 10 parts nitric acid and 20 parts DI water. It is finally heated to 40° C to initiate etching. Aluminum etch rate is approx. 6nm per second.

E-BEAM PATTERNS AND DOSE

As mentioned earlier in report about the source pad, drain pad, wheel pattern and a 50μm pad. Now I will give some specifications about our experiments. We defined line dose by dotted line and area dose by solid line.

1) 50 X 50 micron pad

The following are the specifications:

Magnification: 5000

Centre to centre distance: 4.5nm

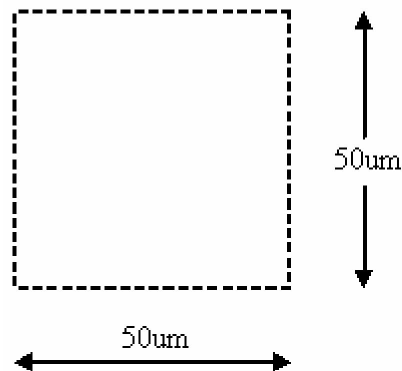
Line spacing: 4.5nm

Aperture size: Select No. 1 (30µm)

Measured beam current: 40pA

Dwell time: 1.6139µsec

Area dose: 3500µC/cm^2



2) Wheels

The following are the specifications:

Magnification: 3000

Centre to centre distance: 8.04nm

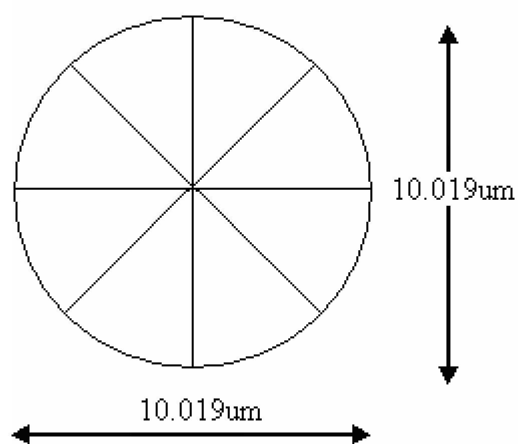
Line spacing: 8.04nm

Aperture size: Select No. 3 (10µm)

Measured beam current: 40pA

Dwell time: 703.8µsec to 140.76µsec

Line dose: 35- 80nC



3) SET

SET pattern is exposed in two layers Layer 1 define island, source and drain electrodes.

Layer 2 defines source and drain pads

Layer1

The following are the specifications:

Magnification: 3000

Centre to centre distance: 7.51nm

Line spacing: 7.51nm

Aperture size: Select No. 3 (10µm)

Measured beam current: 40pA

Dwell time: 93.84µsec

Line dose: 5nC/cm

Layer 2

The following are the specifications

Magnification: 3000

Centre to centre distance: 16.89nm

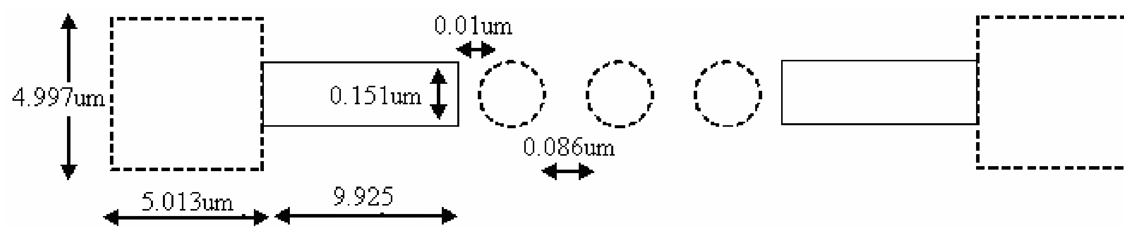
Line spacing: 50.67nm

Aperture size: Select No. 4 (20µm)

Measured beam current: 40pA

Dwell time: 30.57µsec

Area dose: 500µC/cm^2



APPENDIX B

SEM AND E-BEAM WRITER SPECIFICATIONS

At UTA Nanofab we have Zeiss Supra 55VP Scanning Electron Microscope and Zeiss 1540 XB

Zeiss Supra 55VP Scanning Electron Microscope

It has sub-nanometer resolution. It is used to Image nano devices with the latest in X-ray microanalysis. Customized to also study MEMS and NEMS devices.

Figure B1. Zeiss Supra 55VP Scanning Electron Microscope

Key Features

- EDAX 4000 Electron Dispersive Analysis System.
- 1 nanometer resolution.
- Maximum wafer size, 8 inches.
- Large 5-axes motorised eucentric stage.

Zeiss 1540 XB cross Beam e-beam writer

It is a three-gas Focused Ion Beam system with Electron Beam and Ion Beam Lithography and TEM sample preparation. A uniquely configured, very versatile

research tool that designs, generates, analyzes and characterizes patterns for future nano devices.

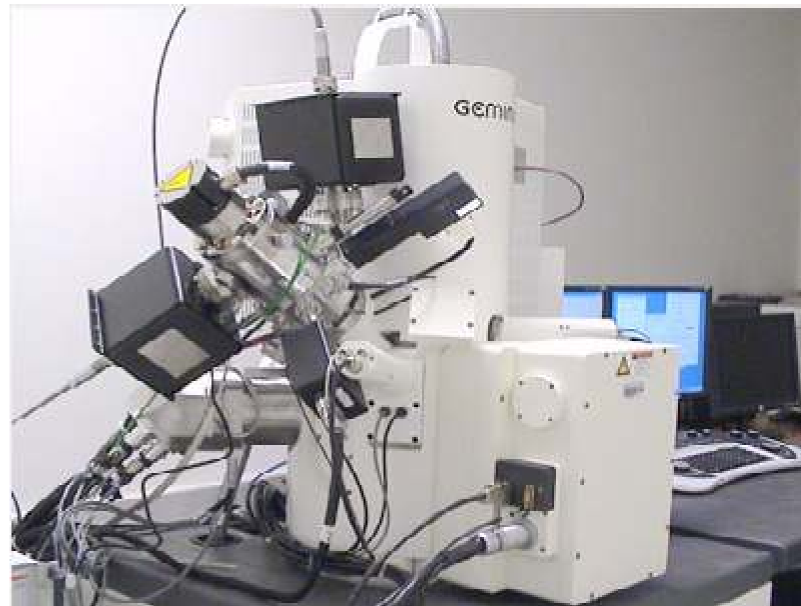


Figure B2 Zeiss 1540 XB cross Beam e-beam writer

Key Features

- High performance CANION FIB column
- Maximum wafer size, 8 inches
- Automated TEM preparation software package
- Focused Ion Beam

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BIOGRAPHICAL INFORMATION

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