THERMAL ENHANCEMENT OF STACKED DICE REPLACING WIRE BONDS WITH THROUGH SILICON VIAS AT LOCATION OF DIE PADS

By

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Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

Of the Requirements

For the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2007

ACKNOWLEDGEMENTS

I would like to first express my deepest gratitude to my advisor, Dr.Dereje Agonafer. His continued support and encouragement helped me throughout the course of my research at University of Texas at Arlington. I thank Dr. A.Haji-Sheikh and Dr. Seiichi Nomura for taking their time in being a part of my thesis committee.

I thank Dr.Senol Pekin of Intel Corporation for helping me in my thesis.

I would also like to thank Baek Sung and Abhijit Kaisare of EMNSPC. Their motion and suggestions encouraged me to understand and implement my thesis in an efficient manner.

I thank my family members in India for their support during my research

July 23, 2007

ABSTRACT

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Publication No:

VENKATA CHEPURI KRISHNA TEJA, M.S.

The University of Texas at Arlington, 2007

Supervising Professor: Dereje Agonafer

Through Silicon vias can offer quick time to market of circuits designed in a modular manner and can also be used to customize the product according to the needs of the customers. This gives a way to avoid both excess inventory risks and larger footprints. A through silicon via could be described as, a vertical component through which a backside interconnect for a pair of bonded wafers forming a wafer stack is ultimately cut into a number of stacked dice. Various embodiments have been patented [1, 2] but implementation of these architectures can be inhibited based on thermal, mechanical and electrical requirements. Also as discussed in the previous work [3], on the thermal enhancement of stacked dice using the thermal vias the primary heat flow

path for stacking is through the substrate. As the number of stacks increase, the cooling problem is amplified.

Through silicon vias are emerging as a viable technology for transferring heat and in effect creating a thermal short circuit from individual die to the substrate. This was simulated in Ansys workbench, where comparison of maximum junction temperature with and without the use of vias was done.

In the present thesis, extensive thermal analysis is carried out, focusing on the heat transfer enhancement using through silicon vias. However the interconnects are placed at the location of the die pads, instead of placing the vias strictly to optimize thermal management. An existing wire bond die is modified to include through silicon vias and stacked in a 3D form. This is done in order to replace the stacked die wire bond packaging or application specific circuits tailored in the mask level. The CAD models required for this study are developed in Pro/Engineer® Wildfire™ and thermal simulation is carried out using ANSYS® Workbench™. Results are discussed in light of applications and economic implication.

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CHAPTER 1

INTRODUCTION

1.1IC Packaging Technology

Over the last several years Integrated Circuit packaging technology had played a vital role in electronics interconnection technology. With the ever-increasing demand for low cost, highly although electronics and to meet the requirements for new generations of electronic products IC packaging has emerged as a high potential solution. Advances in this type of packaging are leading the way in both performance increases and product miniaturization.

An Integrated Circuit is said to complete only when it has a suitable package. In addition to protecting the IC suffering damage from outside elements, a package also provides power to the chip and gives appropriate heat dissipation path to it. There are many types of chip packaging technologies available, out of which 3D packaging is considered to be one of the most efficient packages available. The various options available in 3D packaging technology are the focus of this report.

3D packaging technology

As the name suggests, this technology can be described as stacking two or more dies to form a single package. Multiple packages can also be stacked together for forming a single package. The technology is used primarily because of the present day requirements for reduction in IC package sizes, though it also offers additional

advantages like reduction in power consumption and an increase in performance and reliability. This technology, hence, is a method which is use to provide volumetric packaging solution in products. It uses the height, otherwise known as z- dimension, for achieving higher levels of integration and performance in products. Figure 1.1 shows packaging architecture.

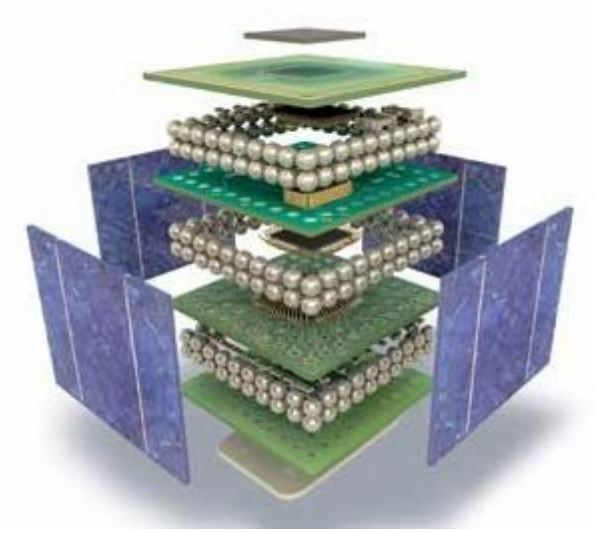


Fig-1.1 Example of 3D packaging architecture (sst.pennnet.com)

The current trend among the consumers is to look out for products, having the maximum functionality in the smallest and lightest possible package. This demand for more functions in the smallest volume, calls for higher memory capacity, which in turn demands more complex and efficient architectures. In addition, the new product designs in digital handbook, cell phones, digital cameras, PDAs and music players, require that these features are integrated using innovative technical form factors and architectures.

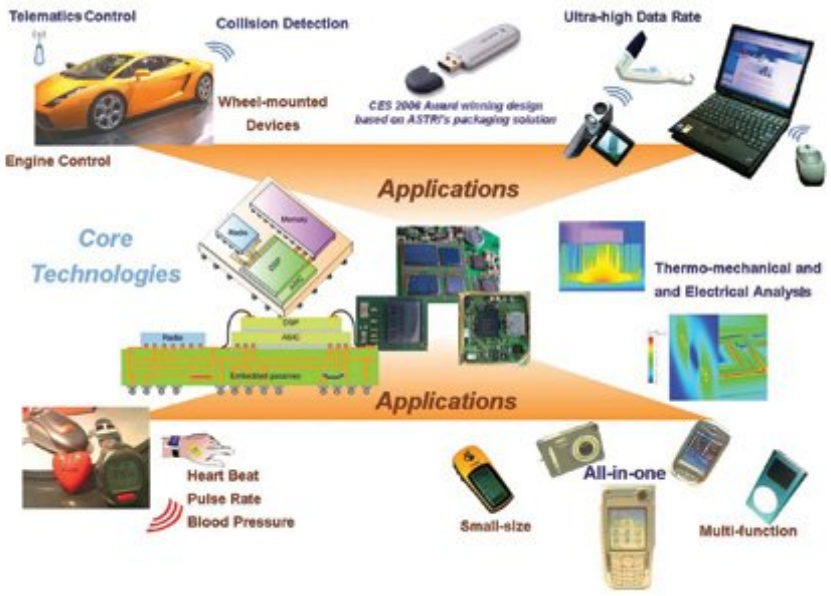


Fig-1.2 Applications in Packaging Technologies (http://www.astri.org)

The 3D packaging in recent times has been associated with the delivering of the highest level of silicon integration and area efficiency at the lowest cost, smallest size and best performance. This has resulted in higher growth and brought in newer applications, for the technology. This growth trend in the 3D technology can be seen since the year 1995. Prior to this, the most efficient and economic way to provide more functionality to an electronic system was to integrate all these functions onto the individual chips using the system on Chip, SOC. However, this method was becoming costlier and also less efficient, as the number of functions to be integrated in a single chip further increased. In addition, some chips that could be integrated together logically were mechanically incompatible, due to the different die materials used. The present day technologies in high density packaging have reached a very advanced stage. Now a single chip system

can be very efficiently split into multiple dies, so as to provide better performance at lower manufacturing costs.

Over the past few years, die stacking has emerged as a powerful packaging option for satisfying challenges in packaging industry. It works by integrating chips vertically in a single package. This increases the amount of silicon per unit area, which leads to a smaller package footprint, hence conserving system-board real estate. In addition, it enables shorter routing interconnects from chip to chip, speeding the signaling between them. Heterogeneous devices can also be stacked using this technology. There is an additional benefit of the simplification of surface-mount system-board assembly, due to the lesser number of components being placed on the board.

1.1.1.1 Advantages of 3D packaging technologies

- Size and Weight – The size and weight are reduced to up to 50% using 3D packaging.
- Silicon Efficiency – This factor which is defined as the ratio of total silicon footprint area to the substrate area can never exceed 100 % using any type of 2D packaging technology. This can be achieved using 3D packaging technology where there are multiple footprints which overlap, within one stack.
- Delay Reduction – Using 3D technology the size of interconnects is reduced. As this is directly proportional to the delay time, the delay time also gets reduced drastically.

- Noise Reduction – The reduction of interconnect length by the 3D technology also results in the reduction of noise as it means lesser parasitic disturbances.
- Power Consumption – Capacitance which is directly related to energy and hence power consumption, is also related to interconnect length. Hence, 3D technology also helps in reducing power consumption.
- Speed – The power saving as seen above allows the device to achieve more transitions per second without any increase in power consumption.

1.1.1.2 Limitations of 3D packaging technologies

As in case of any technology, designers using the 3D technologies also have to perform some tradeoffs that have to be done for efficient operations.

- Thermal Management – Due to the high power density in the Ics using 3D packaging technology, thermal management is a very pertinent factor in the design of stacked devices. Designers should be aware of this issue and must factorize it while designing packages.
- Flexibility of Design – Applying Moore's law to the change of IC design each technology generation lasts roughly for 18 months. Due to the rapid increase in the circuit density and functional integration, the sizes of wafers have been increasing at a faster rate than the present 3D technology allows for.

- Cost – The costs associated with 3D technology are high. This is primarily due to lack of suitable infrastructure and also the inherent reluctance of manufacturers to switch to newer technologies due to the risks involved.
- Delivery time – The time required for the fabrication of a device using 3D packaging technology is of the order of 6-10 months depending on the complexity of design and size of the device. This is 2-4 times longer than the other 2D technologies.
- Design Software – This is one of the problem areas of the 3D technology as most of the design tool kits used is limited to manufactures rather than having universal software. There is a need for manufacturers to put their design rules in a format that is available in the popular designing tools which would make it more accessible to the designers.

1.1.2 Flip-Chip technology

This is one of the methods used for connecting the die carrier to the package carrier. It is a type of semiconductor device like the Integrated circuit chips without any wire bonds. The process was invented by IBM. In general there are two ways of making the connections in the flip-chip technique: solder balls and conductive adhesive on the chip pads instead of wire bonds. That is to say the wire bonds are replaced by a conductive bump which is placed directly on the die surface. Similar to the packaging process, the flip chips use the under-fill process to cover the sides of the die. Under-fill is

actually a specially made epoxy which encapsulates the area between the die and the carrier that is surrounding the area between the die and the carrier. This reduces the strain on the solder contact by taking away the stress. After using the under-fill, the chip is flipped face down on the package carrier using the re-flow process. Figure 1.3 shows schematic of an area-array package with a flip-chip and figure 1.4 shows slip chip BGA packaging. The pictures show the difference between the wire bond technology and flip chip technology.

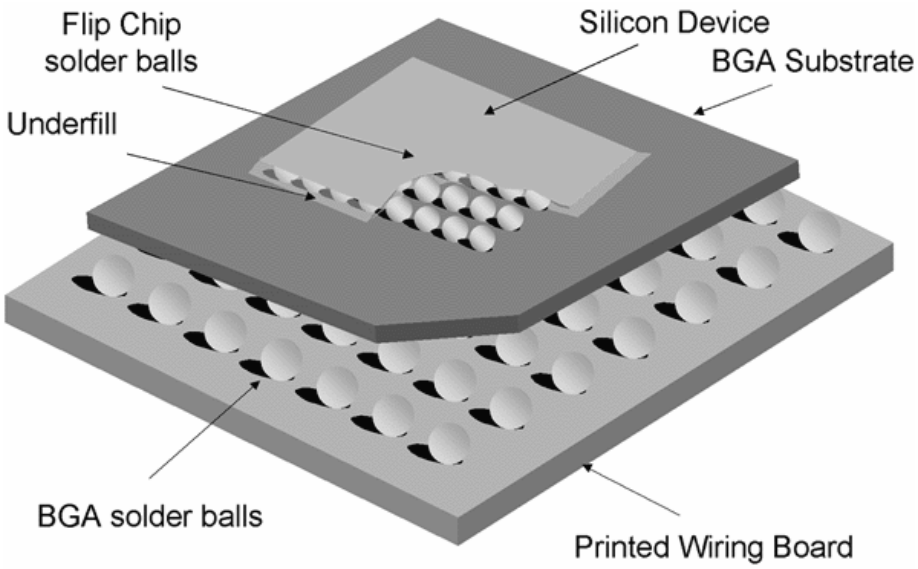


Fig-1.3 A schematic of an area-array package with a flip-chip

(http://www.tms.org/pubs/journals/JOM/9903/Frear-9903.html)

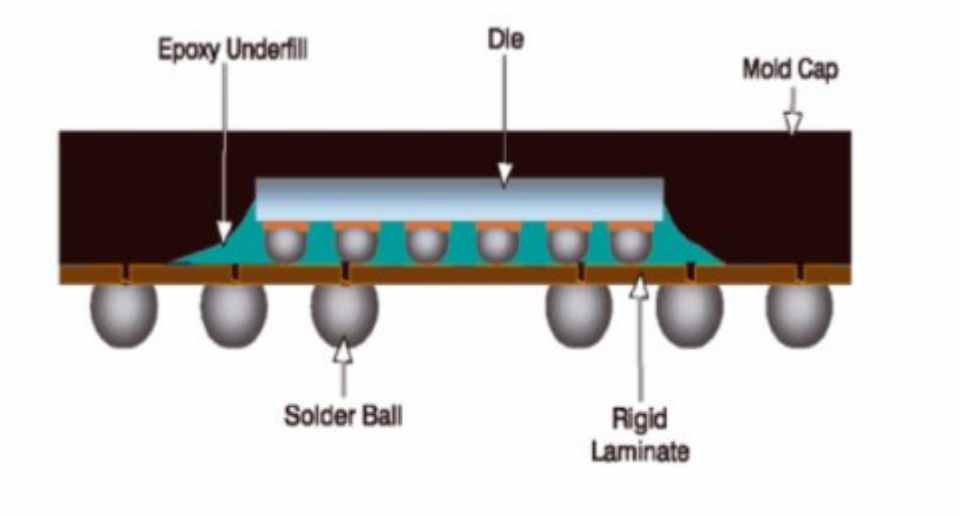


Fig-1.4 Amkor's Flip chip BGA section

1.1.2.1Advantages of Flip-chip technology

By using the flip-chip technology there are many advantages which can be achieved.

- By using the entire surface of the die for establishing interconnect, package size can be reduced. This is because there is no need for spacer for wire in the flip chip technology.
- The inductance of the interconnect path is reduced a lot because of the short length of the interconnect inductance and capacitance. This is an important condition for high speed connection and switching devices.
- Using the flip chip technique also decreases the noise of core power which in turn improves the performance of silicon. This is because the power can be directly brought to the core of the device.

- The flip chip packaging can also hood up extremely large number of interconnects on the same die size which helps in increasing the signal density.
- The I/O does not control the core size which is because of area array placement and the possibility of die shrinking.

1.1.3 System- in-Package (SiP) technology

System-in-Package or SiP defined as an IC package which consists of multiple die. These are traditionally found on the system mother board. These products can be fully functional systems or sub-systems in an IC format. A SiP may have one or more IC chips which could be either wire bonded or flip-chip and other components which are found on a traditional system mother board like filters, EMI shields, mechanical parts, connectors and one or more passive components. Figure 1.5 shows a general system in packaging.

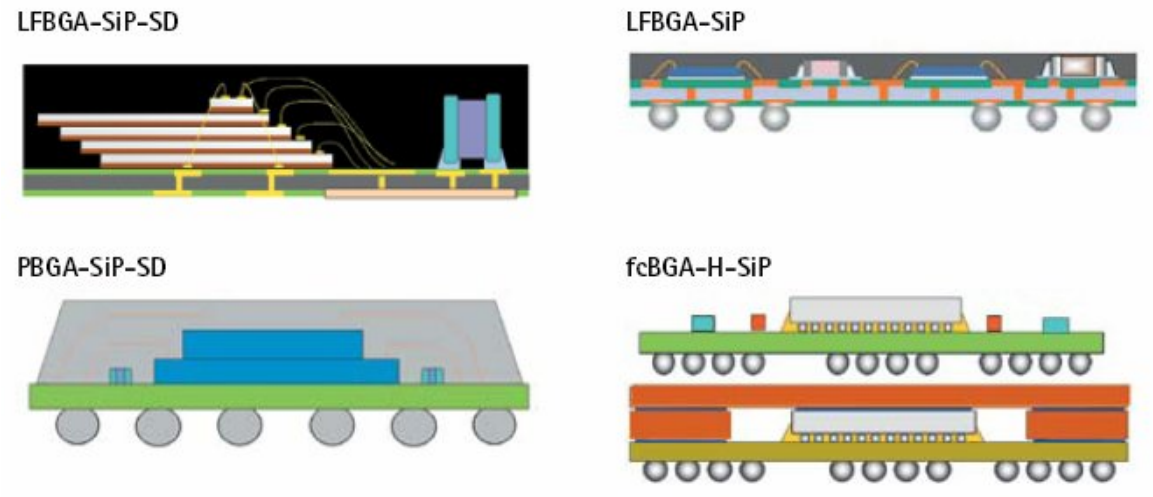


Fig-1.5 Schematic of System in Packaging (www.statschippac.com)

The important capacity of SiP is the ability to bring together many package assemblies and Integrate Circuits. System in packaging and system on chip provide a key point that is smaller in size with increased functionality. However, System in packaging gives faster time to market, lower research and development cost, more integration adaptability and lower product cost than system on chip (SOC). System in packaging includes implementations that need low cost higher density substrates and high speed simulation tools for doing electrical and mechanical analysis.

The System in packaging has emerged as the fastest growing packaging technology segment as the solution to facilitate the needs of these market demand which is cellular phones, laptops, cameras and commercial products. If statistics are viewed 1.89 billion systems in packaging had been developed in the year 2004 and this number is expected to reach 3.25 billion by the year 2008. In other words the quality has been growing at an average rate of 12% per year approximately. The package has three factors of cost, size and performance which are factors of packaging, substrate and assembly methodology. As one research puts, the first 20 percent of the development phase actually determines 80 percent of the cost of the product, which means that the choice of technology determines the cost of the function.

1.1.4 Wafer-level packaging (WLP)

The wafer level Packaging technique is a type of chip-scale packaging technology. In this technique all the steps of IC packaging are performed at the wafer level. This technique is completed on the wafer by dicing for the assembly in a flip-flop fashion. Packaging with a few interconnects can be processed on the complete wafer

before separation. This is done when the package is already formed on the wafer and separation becomes the last process step. All the wafer level packages are real chip size rather than chip scale due to wafer level processing.

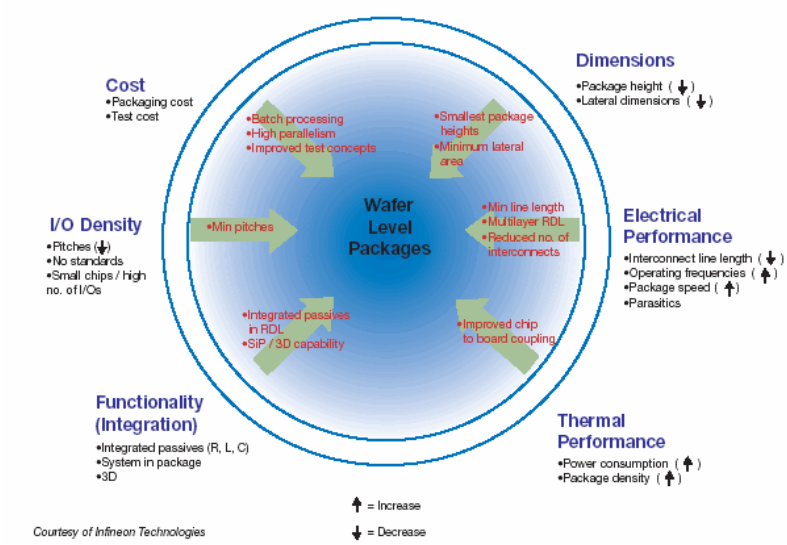


Fig-1.6 Steps of Wafer level packaging.

By redistributing technology, wafer level package is used to enlarge the pad of the standard Ics. One of the important advantages of wafer level packages is that the die and package in the wafer level packaging are manufactured and inspected on the wafer prior to the outstanding products. This can cut down the cost of the wafer level packaging. This is because as the wafer size increase the die size shrinks unlike the other packaging techniques that are assembled after the simulation of the die from the wafers. There are three technologies competing in the market: redistribution technology, encapsulation technology and flex tape technology.

This type of packaging technology is used for small die with low I/O, for example linear, analog and integrated passive devices. However, in future Wafer level packaging

may be extended for larger die and high I/O devices like baseband processors and ASICs also.

1.1.5 Package-on-package technology (PoP)

The Package-on-package (PoP) technology is fairly new, but has become a very important part of the handheld market like mobile phones, digital cameras, portable players, gaming and other mobile applications. The handheld market looks for smaller and more compact devices which had led to an increase in demand for smaller and thinner packages for Ics. This technology leads to improved memory density and performance and also reduces memory area. The technology was designed for products which required efficient memory architectures including multiple memory buses.

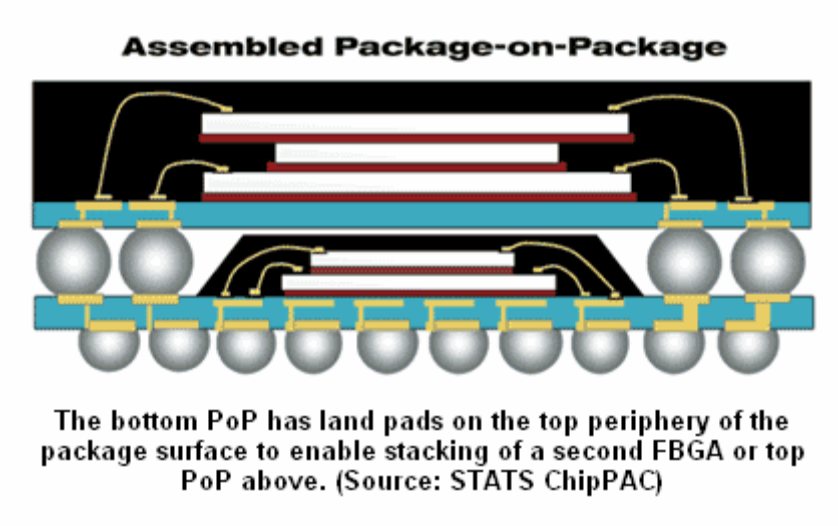


Fig-1.7 Schematic view of the PoP technology.

The technology usually integrates stacked memory devices in a fine-pitch ball-grid array (FBGA) configuration while the bottom of the package can consist of some

other logic device. The challenge is the design compatibility of this top and bottom layers is essential to avoid solder re-flow issues.

1.2 New Packaging Technology

There are various new types of packaging technologies which have appeared in the recent years. The latest among them is the package with silicon through-via chip (TSV) stacks, which have began to develop and substitute the conventional interconnection and packaging. Some examples are the wire-bond chip stack packages and ceramic or organic chip carriers. The use of the silicon carrier with silicon through-via provides a means of tightly integrating different chip technologies. Silicon carriers with through-vias can support heterogeneous semiconductor technologies can provide passive or active circuits and high-density I/O wiring interconnections with electro-optic technology, and support three-dimensional circuit integration. System on packaging within silicon-via technology can provide both high performance and low cost packaging solutions. This is extendible with advances in semiconductor lithography.

1.2.1 Through-Silicon vias

Through silicon vias, TSV's are vertical structures in between the chips that are used as an interconnection to eliminate the existing wire bonds. These allow for the shortest electrical path between two sides of wafers or die, used for 3D die-to-die, die-to-wafer, MEMS wafer level packaging. A TSV, 3-D chip stacking process hence provides a means of implementing complex, multi chip systems entirely in silicon. TSV's. By the vertical stacking of the blocks using this technology, the wire length of interconnects can significantly be reduced. While there has been a lot of research in the field of through-

silicon via (TSV) technology, the commercial products have yet to reach the market. Some of the examples of the 3D technologies with TSV options are the stacked wafers, die on wafers or die on die structures. These involve integrating the TSV process with the 3D integration process. Some of the operations are through-wafer via formation, deep via etching, laser-drilled vias, deep trench capacitor technology, via filling, deposition of diffusion barrier and adhesion layers, metallization, wafer thinning, dicing, alignment and bonding.

1.2.2 Advantages of Through-Silicon vias

- Through silicon vias are vertical structures in between the chips (in flip-chip technology) used as an interconnection to eliminate the existing wire bonds.
- A through-silicon via (TSV), 3-D chip stacking process provides a means of implementing complex, multi chip systems entirely in silicon.
- After a decade of research the TSV's have gone from "lab to fab" extending Moore's law to new limits dramatically reducing chip size while boosting speed.
- It is able to reduce the distance information travels on a chip by 1000 times.
- This technology is being applied to the chips in wireless communications, power processors, blue gene supercomputers (IBM) and in high bandwidth memory applications.

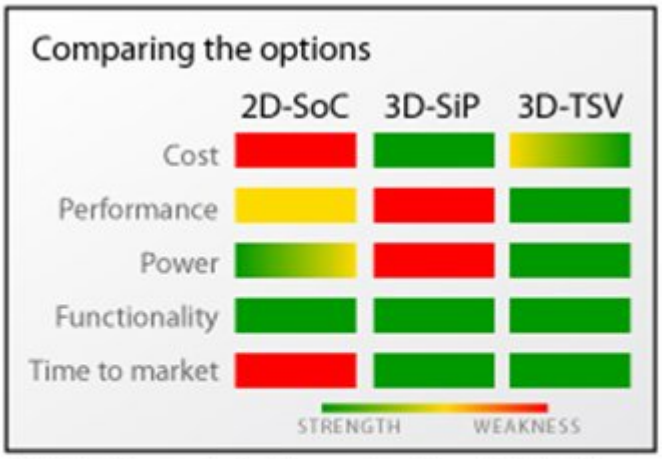


Fig-1.8 the advantages of 3D-TSV over the alternatives (sematech.org)

Currently there are 3 process sequences which are available for the formation of through-wafer via for the 3D wafer level devices. First is the front-end process sequence where the vias are fabricated using deep trench capacitor technology. This sequence put the load of via formation in the hands of the fab and eliminated the need for leaving any space within or between cells for post fab via creation. Second process sequence requires that the chips are specifically designed for 3D stacking. There are specific areas in the layers of interconnect and on the top pad surfaces which are set apart as exclusion zones. The connection of the through-wafer is created by via etching through these zones and finally these are filled with insulators and conductive metals. The third process sequence is used when the chips which are not specifically designed for 3D integration scheme have to be stacked. Here, the vias can be formed by redistributing the pads in the area between

peripheral pads and other free areas. Then the etching process takes place and are finally filled in these naturally present etching zones. Figure 1.9 shows this third process where polysilicon or chemical vapor deposition tungsten is used for fabrication of the via from the top.

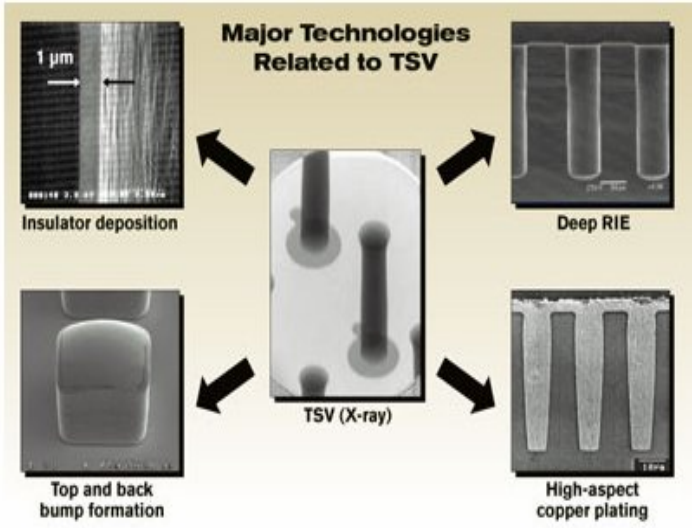


Fig-1.9 Processes in making of TSV

The TSV technology is being used by many companies for DRAMs like Slpida, NEC and Oki. The commercial versions are said to hit the market in the year 2009 or 2010. While there is a very good technical possibility of the stacking of TSV structures there are certain cost and performace trade-offs also involved which have to be taken into acount. This tehnique is hence supposed to hit the commercial market by the year 2008.

CHAPTER 2

LITERATURE REVIEW

2.1 Thermal vias and TSVs

This section gives a brief review of papers on different packaging technologies. Many papers have been published on 3-D packaging technologies in the recent years but the package using through silicon vias in stacked die has been receiving attention due to more advantages in enhancing the thermal management as well as prominent electrically in the package. The following section describes an overview of the papers on new packaging technology.

Li et al.,in 2000 presented a simple analytical model to provide an efficient approach for analysis of thermal via pads. This paper presented the functional relationship between the thermal resistance and the via design parameters which can also serve as a design guideline for engineers to properly select design namely, thermal performance of via cluster depends on dimensionless design parameters. Hence, designers can know the different functions of thermal via as the dimensionless design parameter.

A paper published in 2001 by Yasuhiro et al., described the thermal characteristics of 3D modules. In these modules, four bare-dies with Cu through vias are vertically stacked and electrically connected through Cu-vias and metal bumps. To get more

accurate thermal analysis for 3D-modules at earlier stages of the process development, a series of simple thermal resistance measurements by laser-flash method and parametric numerical analysis was carried out. This paper confirmed that the Cu-vias in dies are not so effective to thermal performance, while bumps between dies can function as thermal vias effectively. At the same time, the thermal effect of the die thickness is not negligible. Die-thinning is a minus effect from the viewpoint of thermal management.

A paper published by Marc et al., in 2002 described the high performance thermal vias in low temperature co-fire ceramic substrates. New developments in low temperature co-fire ceramic (LTCC) have allowed the fabrication of highly thermally conductivity vias arrays. This paper introduces high-density thermal via arrays in LTCC technology by providing a low thermal resistance path for through substrate applications. The thermal vias with 80% via density and internal reader layers have been demonstrated. Typical via arrays with functions of less than 20% would be able to provide heat transport through the substrate for near-future anticipated thermal loads. This would require the use of enhanced via arrays with high area fractions over 50%, with through-plane effective thermal conductivity over 100W/m-k.

In 2003 Seogjoon et al., published a paper describing the details of the fabrication of high density, high aspect ratio through-wafer electrical interconnect that includes deep dry etching hole through the substrate, deposition of an insulation layer and a conductive layer. For doing this the paper described two different processes. One is to fabricate the through-wafer electrical interconnect after the fabrication of MEMS devices while the other is to fabricate the through-wafer electrical interconnect before the fabrication of

MEMS device. This paper demonstrated that the through-wafer electrical interconnect could be made after the MEMS devices are first fabricated using the post-process sequence presented in the paper. The pre-process would be a favorable choice, unless it is necessary for fabricating the MEMS devices before the through-wafer electrical interconnect creation.

In the year 2005 Kazumi et al., evaluated optimizing the chip stack in 3-D packaging. He was successful in optimizing the structure for connections in a chip stack without degrading the features of the chips. The structure enabled a stable and rigid connection for designing a four-layer chip stack assembled on a ceramic substrate which exhibited adequate thermal cycle performance. In the corresponding paper, they discuss about the way the structure of terminals was optimized for chip stacking. A finished package assembled from static random access memory with through-type electrodes was confined to operate and exhibit normal functioning.

Also in the year 2005 Ricky et al., presented a new package design for multi-chip modules. Chips are assembled on a silicon chip carrier with eutectic solder joints. He proposed a through-silicon via hole made at the center of the silicon chip carrier for optional under-fill dispensing. The whole multi-chip module would be mounted on printed circuit board by the standard surface mound reflow process. The under-fill material could then be dispensed through the center through-silicon via hole on the silicon chip carrier to encapsulate the solder joints for smaller chips.

A paper published by Spiesshoefer et al., in 2005 described the formation of TSV. According to then the TSV enables 3D interconnects for chip-stacking applications which

would important especially for integrating heterogeneous devices. The paper described many processing steps such as via information, deposition of via insulation, barrier, Cu seed films, Cu electroplating for via-fill and backside processing. In addition it discussed the process flow and integration of processes useful in through-silicon technology. This paper is a useful guideline for getting to know the processes of TSVs.

In the year 2006 Bivragh Majeed et al., presented paper on Thermo-Mechanical Modeling and thermal Performance of a 3-D Folded Flex Module. In the course of his research, investigation into the thermo-mechanical stress and thermal performance of a folded flexible substrate module was done. The module consisted of flip chip bare die silicon onto a flex and interconnected via conductive adhesive and folding the flex to obtain the final module. Thermal performance althrough□ization revealed that for the current module set-up total power to the module rather then power to the individual chip is an important criterion for the selection of thermal management scheme. They concluded that by decreasing the chip thickness there is an increase in the thermal density and there by increases the total temperature for the stack for any given power.

In the year 2006 Baek Sung Young et al., presented paper on the enhancement of thermal vias in different stacked die architectures. In the course of there research three die architectures were simulated: spacer stacked rotated stack and pyramid stacked. In this present paper, the heat transfer enhancement using silicon vias on various stacking schemes were discussed. The thesis had used Pro-Engineer Wildfire 3.0 as a Computer-Aided design tool and imported the results into Ansys Workbench 11.0, where meshed analysis was conducted. As there are different numbers of thermal vias with every

packaging, the thesis compared the junction temperature and heat flux for the different number of thermal vias.

The author of the present thesis used all these papers as a guideline, in addition to other reading materials. The main objective was to perform extensive thermal analysis with a focus on the heat transfer enhancement using through silicon vias, and also to reduce the maximum junction temperature.

CHAPTER 3

OBJECTIVE AND METHODOLOGY

3.1 Summary

The present day technologies in high density packaging have reached a very advanced stage. Now a single chip system can be very efficiently split into multiple dies, so as to provide better performance at lower manufacturing costs.

Over the past few years, die stacking has emerged as a powerful packaging option for satisfying challenging IC packaging requirements. It works by integrating chips vertically in a single package. This increases the amount of silicon per unit area, which leads to a smaller package footprint, hence conserving system-board real estate. In addition, it enables shorter routing interconnects from chip to chip, speeding the signaling between them. Heterogeneous devices can also be stacked using this technology. There is an additional benefit of the simplification of surface-mount system-board assembly, due to the lesser number of components being placed on the board.

3.1.1 Vias

Due to the increasing number of dies in a stack, the designers are facing the challenge of meeting the temperature design specification. One method to counter this is to provide a thermal path from each individual die to a substrate using thermal vias.

These thermal vias can be implemented using several methods. One of the approaches is to have a thermal die that thermally connects each die to the substrate. The heat from each die is conducted rapidly from one end of the board to another, either through the die attach or the vias. Thermal vias are made of copper runs providing the a path of least thermal resistance, and so heat is transferred through the vias in a proportion much greater than the area of the vias. Usually one end of via is attached to the IC and the other end is attached to a heat sink. Thermal vias work very well with flip-chip devices. With no additional space required for the heat conduction, these are considered as a mini-thermal solution.

Vias can also provide a means of customizing the heat transfer process for devices with a highly non-uniform power distribution. This is especially important for high density interconnects where the device has highly non-uniform power map.

3.1.2 Through Silicon Vias (TSVs)

Through Silicon Vias, TSVs are vertical structures in between the chips that are used as an interconnection to eliminate the existing wire bonds. These allow for the shortest electrical path between two sides of wafers or die, used for 3D die-to-die, die-to-wafer, MEMS wafer level packaging. A TSV, 3-D chip stacking process hence provides a means of implementing complex, multi chip systems entirely in silicon. TSVs. By the vertical stacking of the blocks using this technology, the wire length of interconnects can significantly be reduced.

Vias provide both electrical and thermal path. In this paper, the thermal enhancement realized by the vias is discussed along with trying to find out a way to remove heat from the dies. The power applied to the dies is between 5-10 watts power. We found that one such method was to use silicon dies.

3.1.3 Methodology of the present experiment

The figure 3.1 below explains the methodology used for this study.

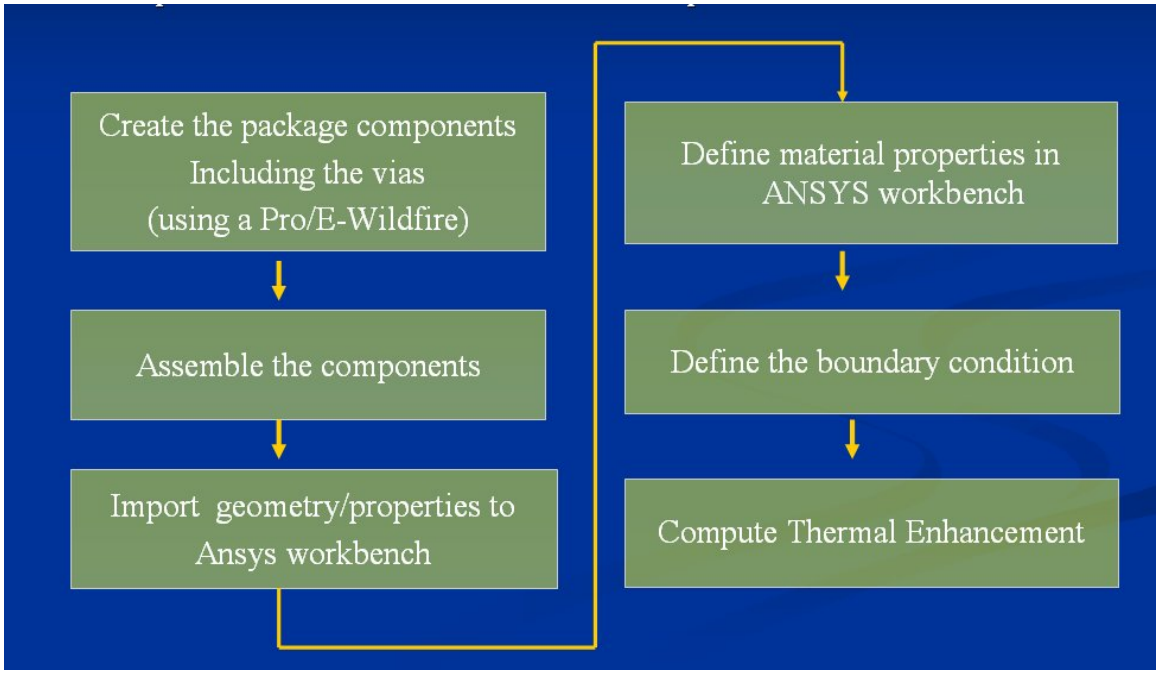


Fig-3.1 Methodology of the Experimental program.

First, the package components including the vias were created using Pro-Engineer Wildfire 3.0. After this the material property was defined and the various components were assembled. The entire geometry and the properties were then imported to Ansys

workbench. Here, the Boundary conditions were defined and implemented. Finally, the end result, which is the thermal enhancement of the die geometry, was evaluated.

3.2 Objective of the Present study

The main objective of the present study is to achieve effective heat flow path away from the stacked dies by using silicon vias althrough the periphery of the die. To perform extensive thermal analysis with a focus on the heat transfer enhancement using through silicon vias. To reduce the maximum junction temperature at the devices and to get rid of larger footprints. Placing the vias strictly to optimize thermal management.

3.3 Motivation

The study on thermal vias developed interest in me to continue work on vias for various packages. Dr.Senol Pekin of Intel encouraged and helped me understand the role of vias in 3-D stacked die. The experimental work on TSV done by S.W.Ricky Lee ***et al.*** ECTC (2005) "3D Stacked Flip Chip Packaging with Through Silicon Vias and Copper Plating or Conductive Adhesive Filling" motivated me to further study on effect of copper vias.

CHAPTER 4

MODELING OF THE GEOMETRY

4.1 Package and Dimensions

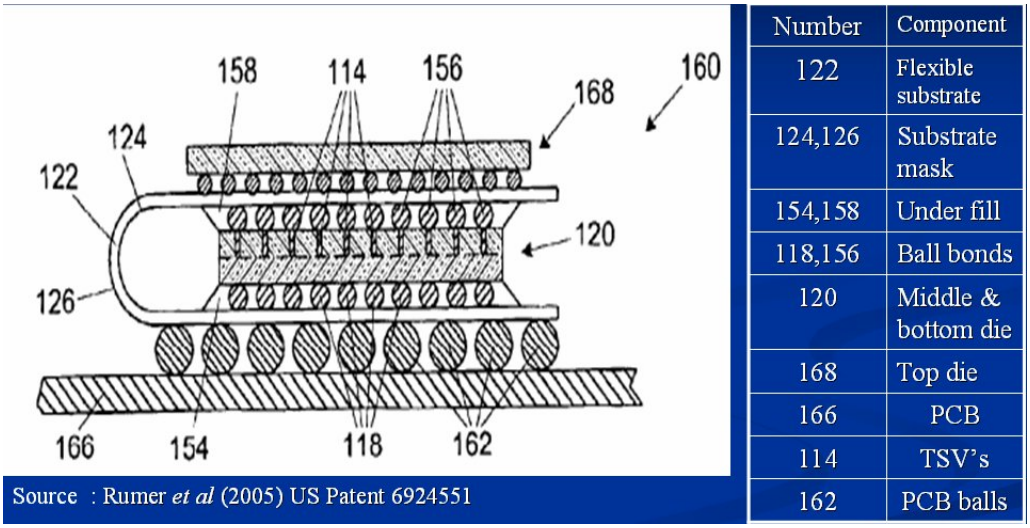
In the present thesis the modeling of all the parts of this particular Intel package is done using Pro/ENGINEER Wildfire 3.0 as a computer aided tool. All the components were assembled after creating them separately and saving them in the UDF library. Dimensions of all the elements were parameterized which is used in the creation of different models which are used to get solution multi-design variable optimization problems, a capability that exists in Ansys/Workbench which is used as Finite Element Analysis tool in getting the results. Pro/ENGINEER is used in variety of industrial applications as it has many advantages listed as follows: [ptc.com]

- Complete 3D modeling capabilities enable any body to exceed any product quality and time-to-market goals.
- Maximum production efficiency through automated generation of associative tooling design, assembly instructions, and machine code.
- Ability to simulate and analyze virtual prototypes to improve product performance and optimize product design.
- Ability to share digital product data seamlessly among all appropriates any people.

- Compatibility with myriad CAD tools- including associative data exchange- and industry standard data formats.

Here, assigning material properties and dimensional parameterization are done in two stages while modeling.

The present package is taken from Intel's patent no: 6924551 which have two dice attached on the inner side of the flexible substrate where as the top die placed at that side of the substrate which is exposed to the ambience. The two chips which are in the substrate are 18mm x 18mm wide and 0.35mm thick. These are connected to the substrate with die attach of 0.08mm thick and bond balls which are 0.4mm in diameter and stand off height of 0.35mm.There is a chip on the top of the substrate which is 20x20mm and is placed with the help of bond balls and die attach. The Through Silicon Vias are placed in the upper die inside the substrate peripherally which have the dimensions of 0.40 die and height of 0.43mm and are 60 in number when the full geometry is considered. The two chips which are connected to the substrate have their bond balls covered in underfill material as shown in the Fig-4.1.



Number	Component
122	Flexible substrate
124,126	Substrate mask
154,158	Under fill
118,156	Ball bonds
120	Middle & bottom die
168	Top die
166	PCB
114	TSV's
162	PCB balls

Fig-4.1 The package showing flexible substrate and vias

Fig-4.1

The PWB which is 44mm x36mm x0.6mm is coated with resist (0.08mm) and copper (0.1mm) layers on both sides. A total of 169 solder balls connect the printed wiring board to the outer surface of the flexible substrate. The vias are arranged peripherally in the die as shown in the figure 4.2 below.

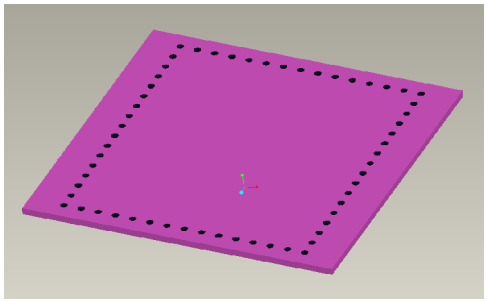


Fig-4.2 the die showing vias on the periphery

The flow of pro-E figures will explain the process in which the assembly was done and the complete package is evolved finally.

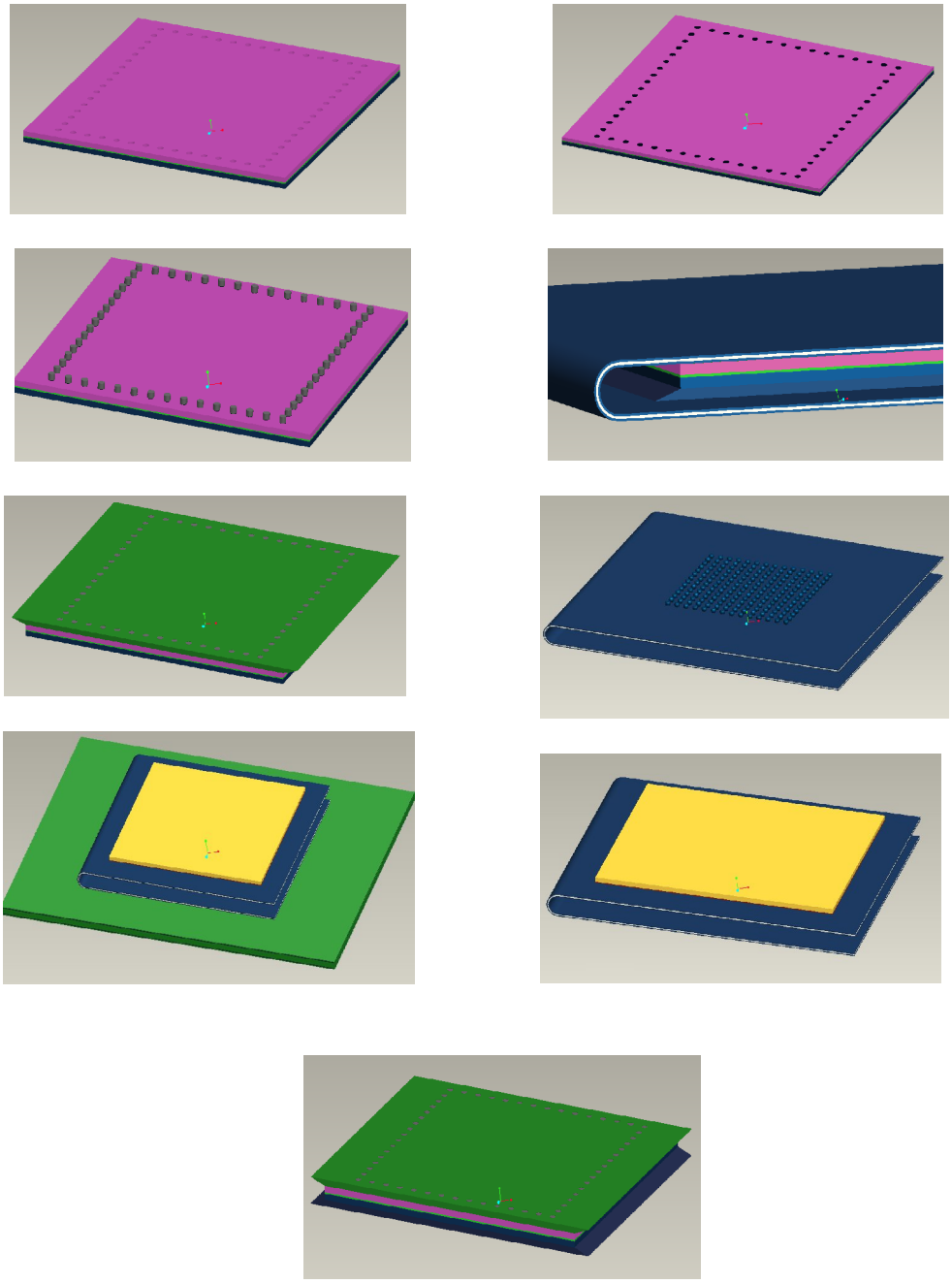


Fig-4.3 Process of package formation

The complete package after the assembly is done is saved as a IGES file which allows the geometry to get directly imported to the analysis software which is ANSYS workbench after which all the boundary conditions can be applied and is ready for simulation.

4.2 Thermal Conductivity

Heat transfer by conduction involves transfer of energy within a material without any motion of the material as a whole. The rate of heat transfer depends upon the temperature gradient and the thermal conductivity of the material. In order to serve the purpose of the through silicon vias ie to reduce the temperature from the package we must choose the vias with a very thermal conductivity. We must choose a material for the vias such that they are thermally effective and low as per the cost. For example we cannot use a material as diamond for vias which though has higher conductivity of 1000W/mk but is extremely expensive. The table below shows the material properties of the components used:

Table 4.2 Thermal conductivity of components

Element	Thermal conductivity(W/m-k)
Solder ball	54
Die	120
PCB	0.18

Table 4.2-Contined

PCB resist	250
PCB copper	380
Die attach	0.3
Substrate	0.418
Substrate mask	200
Underfill	0.18
Through silicon vias	400

4.3 Simulation Results in ANSYS Workbench

The assembled package completed in Pro/Engineer, which was saved as an IGES file is directly imported in the ANSYS/Workbench in which the purpose and challenge for the "through silicon vias" is to bring down the maximum junction temperature. In the present day 3-D die stacking the power requirement which the package has to handle has shot up drastically. This present package taken from Intel's Corporation patent is being tested for higher powers ranging from 0.5-10Watts.So,for this to fulfill we have made the package to undergo simulation iterations in which the power and the film co-efficient have been varied keeping the ambient temperature constant at 22°C.

In this study various different cases have been brought into light where boundary conditions have been changed trying to get the most optimum solution. One particular

case is taken into consideration in which the boundary conditions and the simulation results with and without vias is explained.

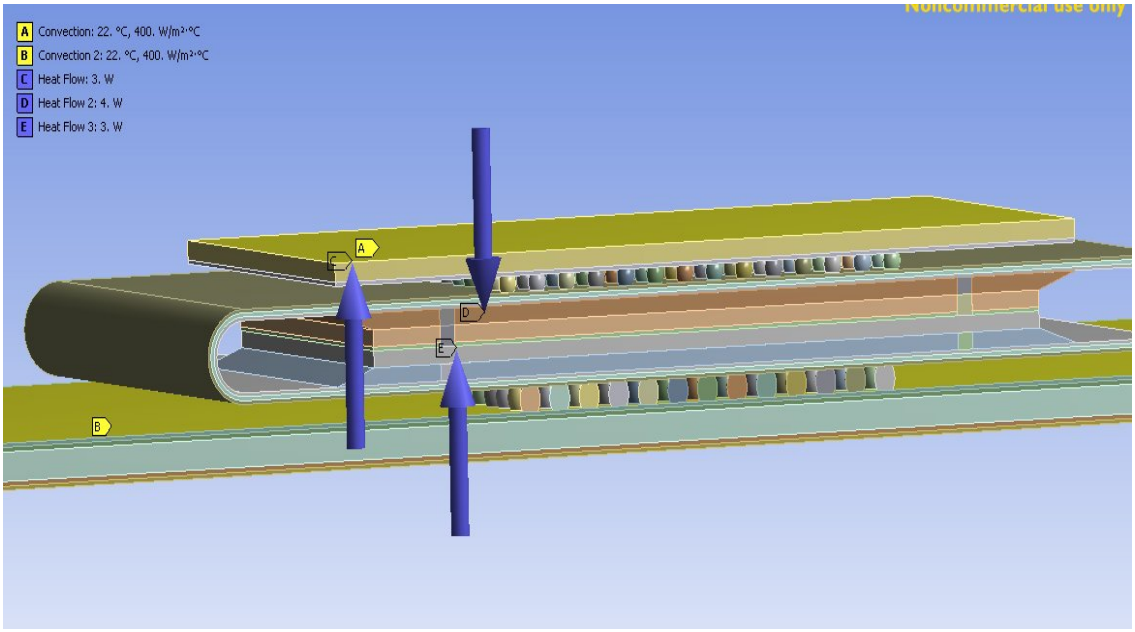


Fig-4.5 Shows boundary conditions of temperature, film coefficient and power applied

The power 10 watts is distributed in such a way that 4 watts of power is applied on the middle die and 3 watts each applied on the top and bottom dice.

Ambient temperature applied is 22ºC and for the present context of through silicon vias the material properties were applied in the simulation tool and was carried out as a baseline study in steady state conditions on the geometry with and without vias to major focus on the advantages of the through silicon vias.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Compare the maximum junction temperature of a silicon die with and without vias

The simulation of the package with through silicon vias is carried out using ANSYS Workbench. In this paper two different aspects have been taken into consideration performance and role of through silicon vias when high power is applied on the die and the same when low power trend is maintained. As for as the high power matters, 10 watts is applied with 5 watts on each die. Initially for the first case an effective film co-efficient of 400 W/m²°C was applied on the die and the PWB with an ambient temperature of 22°C.In the next case the material copper has been used as a substrate mask with the same boundary conditions. This resulted in the maximum junction temperature of 179°C without the vias and reduced the temperature by 1°C to 178°C when vias applied.

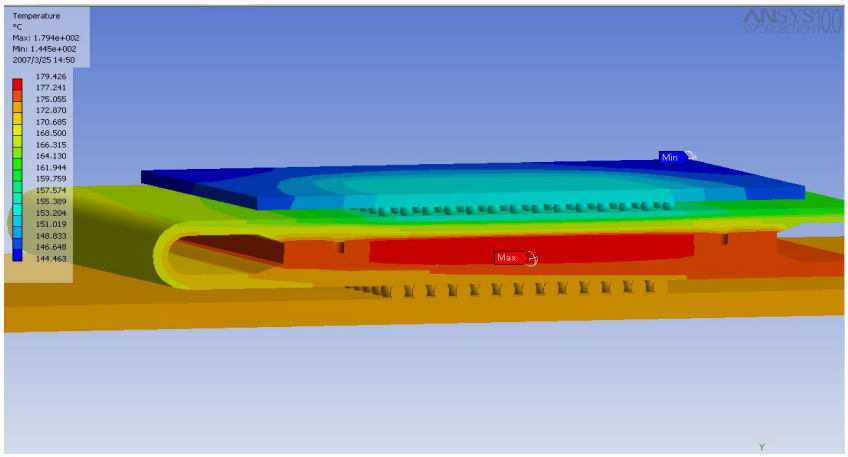


Fig-5.1 Simulation results with no vias

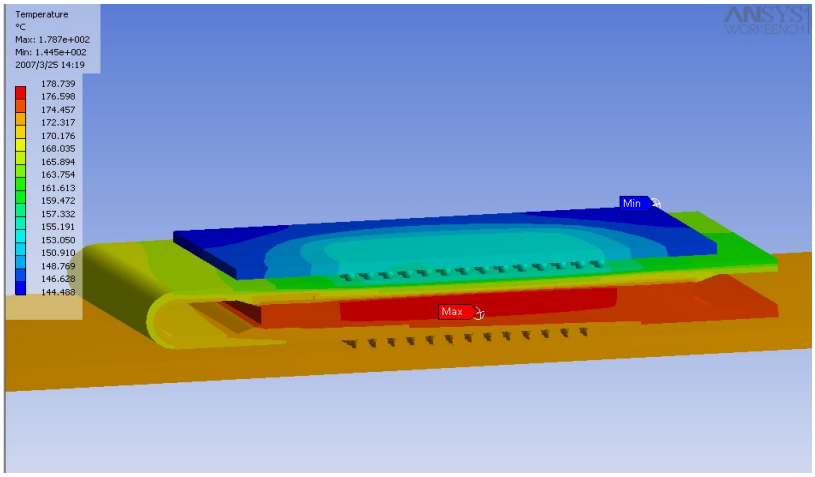


Fig-5.2 Simulation with TSV

In the next case the power was applied only on the die with via and the die attached to it. Power of 5 watts was distributed among the three dice as 1.5 watts on both top and bottom die and 2watts on the middle die with a film co-efficient of 400 W/m²°C on the top surface if the die and 15 W/m²°C on the printed wiring board. After simulation the temperature at the die was 209°C with vias and without the vias it raised to 210.6°C giving a temperature difference of 1.6°C. In the next case a germanium die was used in place of silicon die to test the vias for heterogeneous components. The boundary conditions were kept the same as the silicon die.

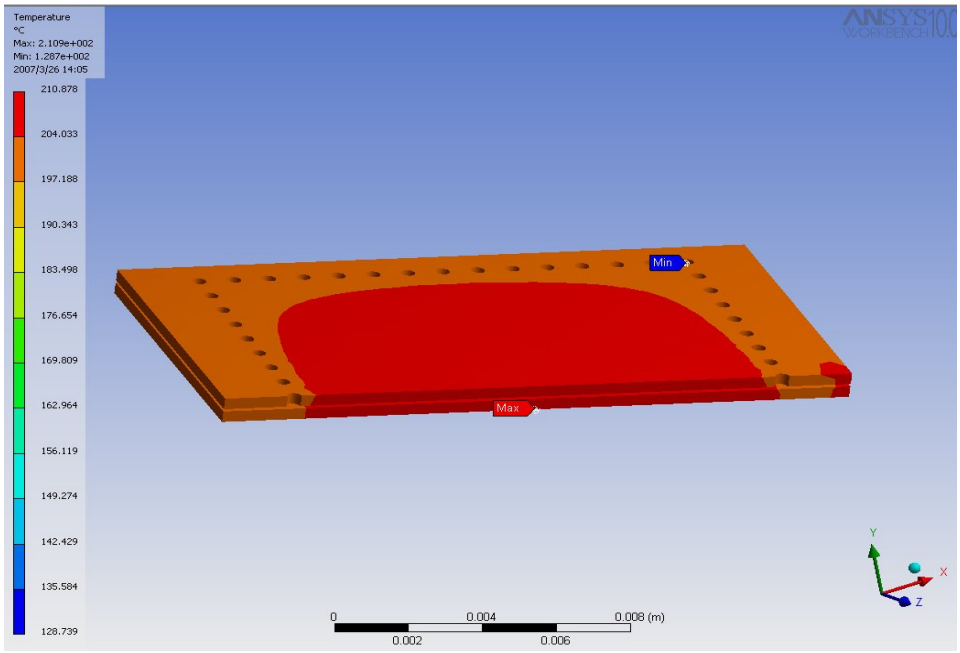


Fig-5.3 Simulation results without vias

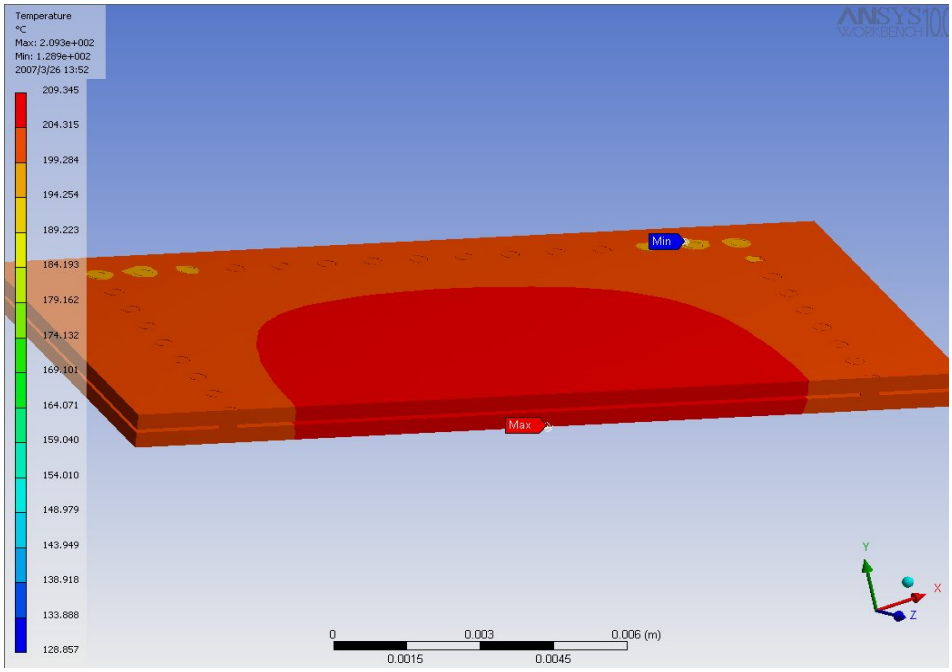


Fig-5.4 when vias applied in the die.

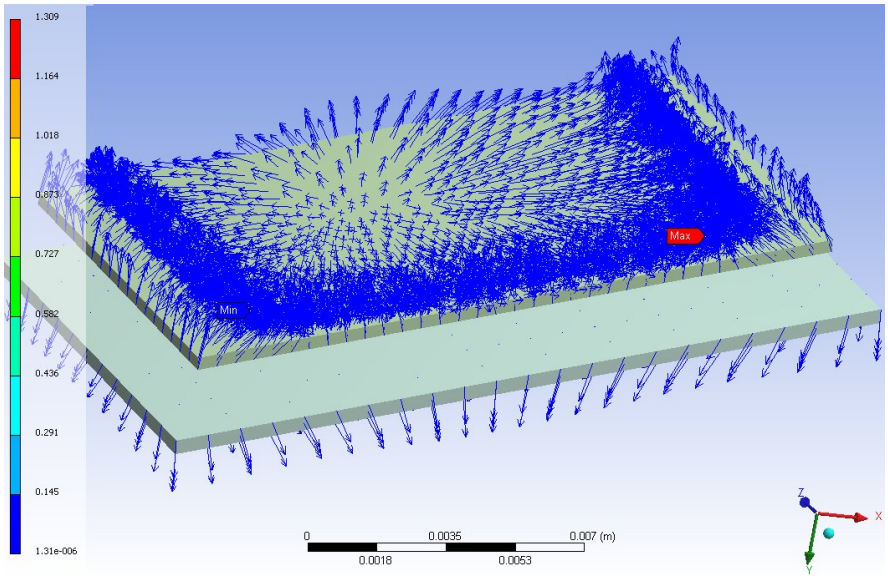


Fig-5.5 Shows heat flux plot with a heat flow path away from the die

In the coming simulation it is shown that vias are quite effective for high powers and is an important one as the role of through silicon vias is very obvious here. With the same boundary conditions as applied above and just changing the die material from silicon to germanium there is a decent number in the simulation figures having a junction temperature of 223°C when vias were placed and a temperature of 225.5°C without the vias showing a maximum junction temp reduction by **2.5°C**.

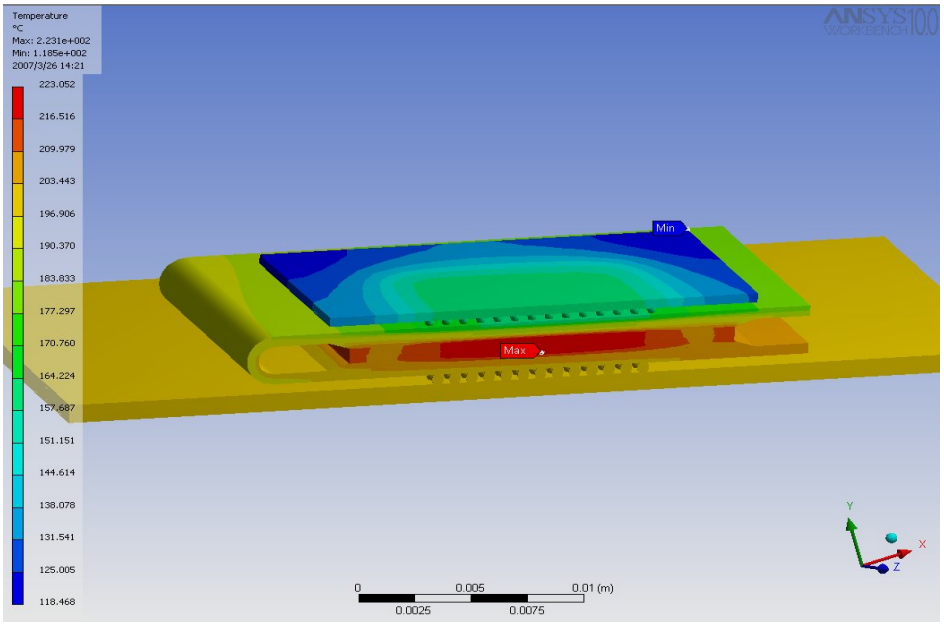


Fig-5.6 Result showing temperature with vias

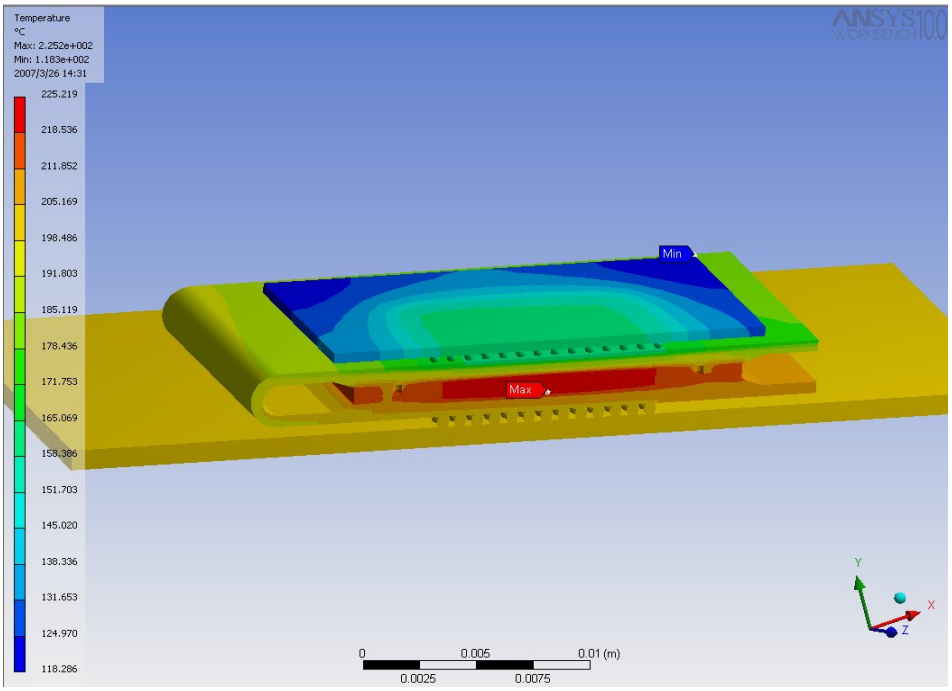


Fig-5.7 showing results without the vias

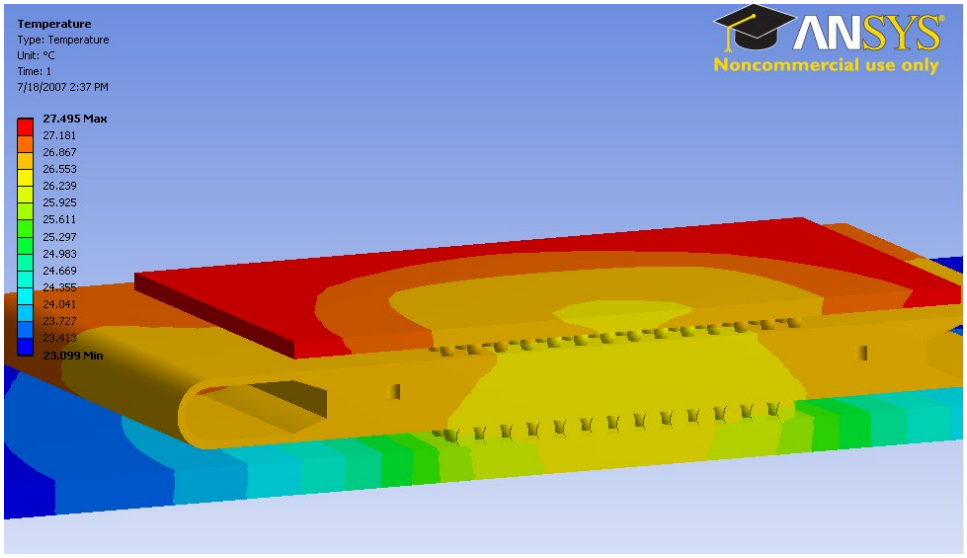


Fig-5.8 Simulation without vias

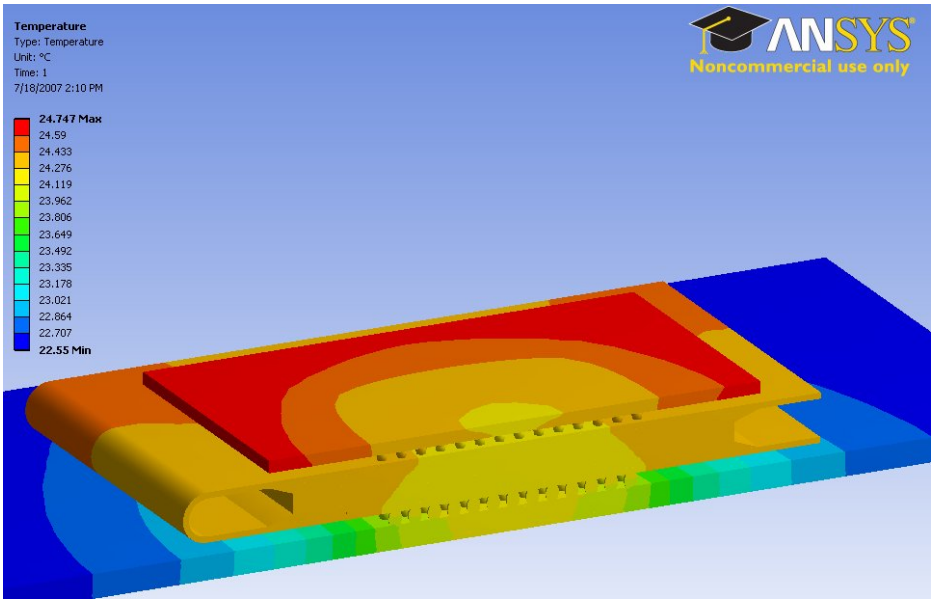


Fig-5.9 Simulation with vias

For low power trend of 0.5 watts one can observe that the results with and without through silicon vias have a difference of 3.1°C.If for the same boundary conditions we

apply 0.75 watt of power can still see a 3.3°C reduction in the maximum junction temperature. In this case 0.35 watts applied on middle die with vias and 0.2 watts each distributed on middle and bottom dice.

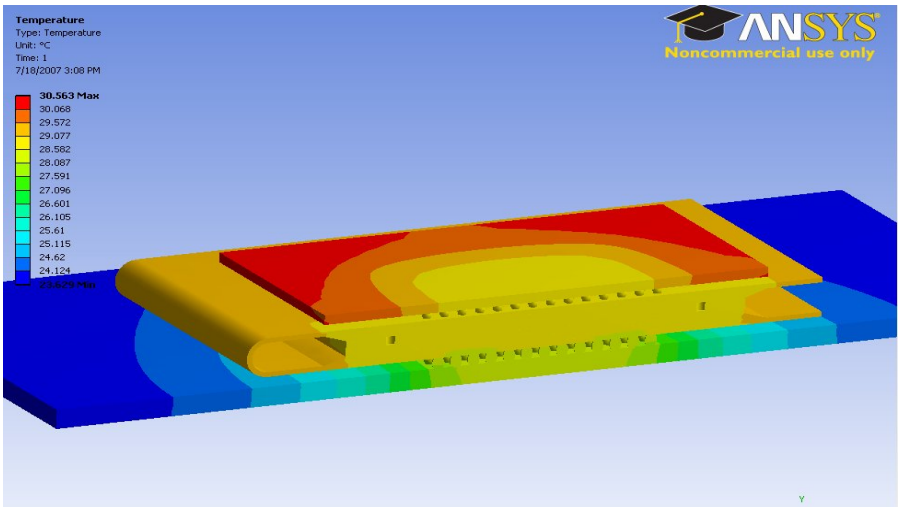


Fig-5.10 Temperature plot without vias

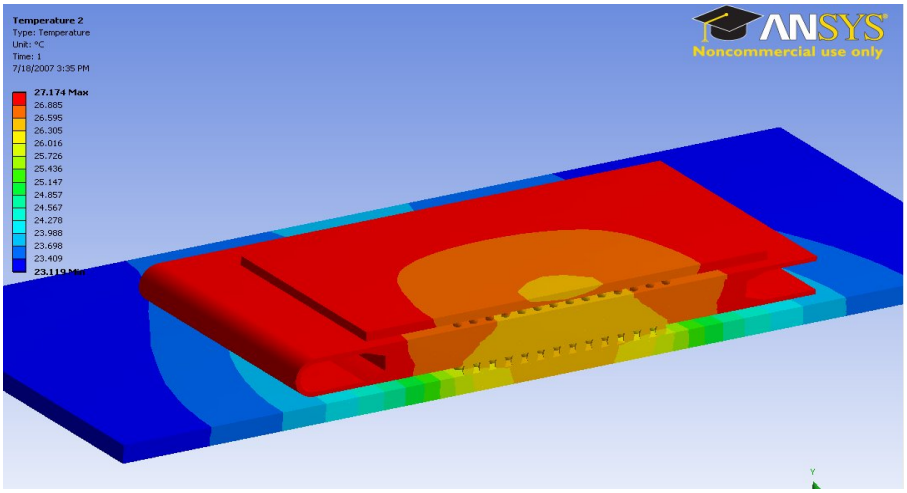


Fig-5.11 Temperature plot with vias applied

5.2 Conclusion

In this thesis report elaborate study has been done in analyzing the effect of thermal vias on the die and ways to bring down the junction temperature by reduce count. Thermal enhancement was tested by running the thermal simulation with various test cases, and also with / without thermal vias. The Temperature profile of the entire stacked die geometry was plotted in Ansys Workbench. From the simulation results it is evident that through silicon vias makes a decent temperature reduction in the die when low power of 0.5 and 0.75 watts is applied.

The heat flux plot shows that a effective heat flow path is created from vias towards the PWB taking heat away from the package. The use of silicon die did give a lesser temperature as compared to other materials.

The architecture of the package considered where the vias are placed in only in one die; through silicon vias contribution is less significant for higher power trend.

Table 5.1 Shows the Maximum JT difference with and without vias

Total power applied (Watts)	Max JT with Vias (°C)	Max JT without Vias (°C)	Difference in max JT (°C)
10	209	210	1
5	178	179	1
0.75	27	30.5	3.3
0.5	24.5	27.5	3.1

5.3 Future Scope

One could study the mechanical issues (reliability) of the package with vias as thermally it is helping to improve the package performance.

A logic processor in a flip chip configuration could be stacked with heterogeneous devices. The simulation models will be validated with experiments. The experimental work will be done in conjunction with industry.

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BIOGRAPHICAL INFORMATION

Venkata Chepuri Krishnateja received his Bachelor of Engineering degree in Mechanical Engineering from Jawaharlal Technological University, INDIA (A.P.), in May, 2005. He received his Master of Science degree in Mechanical Engineering from the University of Texas at Arlington in December 2007. His research interests are in Electronic Packaging and Vias in 3-D packaging. He has modeled geometry of 3-d package with through silicon vias with the use of PRO-E/wildfire 3.0 and has done the simulation of results using ANSYS workbench 11.0.