

SUPPRESSING DELTA-I NOISE IN MCML CIRCUITS IN  
MIXED SIGNAL ENVIRONMENT

by

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## ABSTRACT

### SUPPRESSING DELTA-I NOISE IN MCML CIRCUITS IN MIXED SIGNAL ENVIRONMENT

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This work addresses the problem of simultaneous switching noise (SSN) in mixed signal environment. It is shown that the Metal Oxide Semiconductor Current Mode Logic (MCML) can be used to minimize the SSN. In short channel devices, Drain Induced Barrier Lowering (DIBL) effect causes the current mismatch problem. It is seen that this current mismatch problem aggravates SSN. Basic logic gates were designed using MCML topology at 5 Gbps. Parasitic model was introduced at power supply lines and substrate to study the behaviour of these logic gates in the presence of

parasitics. Interpolation type delay cells were used to suppress the detrimental effect of SSN caused by the parasitics in power supply lines and substrate of these MCML circuits. This allows us to introduce variable delays at input terminals. The results in this work show that the variable delay minimizes the current mismatch problem thus, suppressing SSN. The analysis of peak to peak noise amplitude at the output of MCML circuits with and without the delay cell illustrates that delay cells can be successfully employed to minimize current mismatch to reduce SSN. Delay cell increases the number of transistors which in turn adds to the complexity of the circuit. With the advancement in technology, new variable delay cells can be designed using less number of transistors, thus reducing the complexity.

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## CHAPTER 1

### INTRODUCTION

Research on high-speed low-power circuit design has increased to improve the amount of data transfer through communication networks. There is particular emphasis on improvement of digital logic units for DSP chips which carry out arithmetic operations. CMOS gate lengths have scaled down to several nanometers and frequency of operation scaled up to several gigahertz, helping create faster digital circuits. Despite these advantages, technology scaling has brought several challenges too. The problems include the increase in power consumption with increasing frequency, higher noise due to faster switching, and integration of analog and digital circuits on the same die.

The integration of analog and digital circuits on the same die brings in simultaneous switching noise [1], [2] which is a major part of substrate coupling noise [3]. New topologies and techniques are required to reduce substrate coupling noise and provide better performance at high frequencies as the conventional CMOS logic families cannot meet the speed and power requirements simultaneously.

Introduction of differential topologies has offered higher immunity to environmental noise [4], higher achievable voltage swings, better slew rates, etc. The speed of a topology depends on the region of operation of transistors. In conventional CMOS logic topologies, transistors switch saturation region (ON) to cut-off (OFF) causing a slow transition as the charge underneath the gate has to be completely

removed and then brought back in order to turn ON the transistor. To help achieve high speed, differential topologies can be designed to always keep the transistors switched ON. The MCML family is a differential topology which employs this technique.

The MCML achieves much lower power consumption [5] as compared to complementary CMOS logic for high speeds. MCML inverter, XOR gate and AND gates were designed to work at a speed of 5 Gbps. Power consumption of all these circuits was 3.6 m W.

A parasitic model was then developed to study the behaviour of the designed MCML circuits in the presence of these parasitics. Variations at the output were seen due to simultaneous switching noise. MCML inverter showed a variation of about 4 m  $V_{p-p}$  while XOR and AND gates showed about 20 m  $V_{p-p}$  and 18 m  $V_{p-p}$  respectively.

Despite relatively better noise performance, MCML logic has significant simultaneous switching noise at high frequency with the inclusion of the parasitic model in the simulation. In this thesis, a method to suppress this noise has been demonstrated. By introducing a delay cell at the inputs of MCML circuit helps reducing the current mismatch problem, described in chapter 3, in turn helping to reduce the simultaneous switching noise.

Chapter 2 gives a general background explaining substrate noise, simultaneous switching noise, package models, and MCML circuits. Chapter 3 focuses on the design of some basic digital blocks with MCML: Inverter, XOR and AND gates. Chapter 4 introduces the parasitic model which was used to study the behaviour of MCML circuits in the presence of parasitics. Chapter 5 illustrates the proposed method of using delay

cells to improve the performance of MCML circuits in the presence of parasitics.

Finally, chapter 6 gives the concluding remarks.

## CHAPTER 2

### BACKGROUND

Advantages of MCML circuits are multifold: (1) due to their differential nature they have high noise immunity, (2) achieves high speed consuming less power, (3) high power/ground supply noise rejection. These features have made MCML circuits suitable for high speed applications.

#### 2.1 MOS Current Mode Logic circuits

MCML employ differential topology to reduce environmental and power supply noise. Basic MCML block diagram is shown in the figure 2.1. [6] It consists of two load devices, resistors or pmos active loads, nMOS input transistors and a current mirror which acts as the current source. The pMOS load transistor is usually used as resistor and hence is forced to work in linear region. Resistance of pMOS along with the amount of current flowing through it determines the voltage swing at the output. The nMOS input transistors are employed to perform the required logic operation. It is also called the pull down network and the load devices are called the pull up network. The current source is used to provide a constant current through the circuit so as to reduce the fluctuations in the power supply lines and also to maintain constant power consumption irrespective of the frequency of operation. Some of the MCML circuits also employ a source follower stage at the output. Source follower stage has no contribution to required logic but is placed just to make sure that the outputs are



maintained within the certain noise margin limits. For better and faster operation of the MCML circuits the nMOS transistors of the differential pair are forced to work in saturation region [7], so that the turn on time of the transistor is avoided.

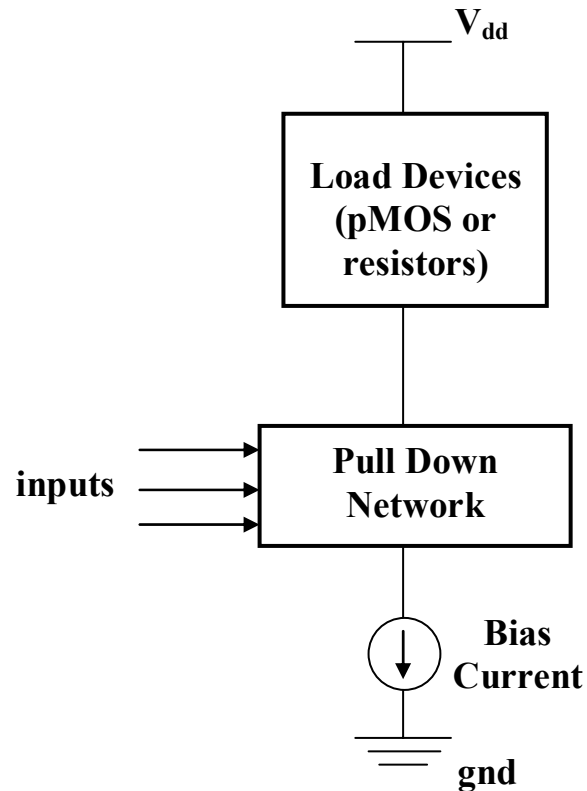


Figure 2.1. General block diagram of MCML circuits

### 2.1.1 Operation

MCML circuits are based on current steering logic wherein the current is ideally steered by one of the branches depending on the inputs to the nMOS input transistors. The branch which steers most of the current i.e., the ON branch has a high voltage drop across its load device and hence generates a logic low output. The branch which has minimal amount of current flowing through it generates a logic high output because of less amount of voltage drop across the load device. The voltage swing is decided by the

resistance offered by the load device and the amount of current through the load device. A simple current mirror is used for the current source, since it consumes less voltage headroom and is simple to design. The architecture for current source can change depending upon the amount of accuracy required by the current source and the amount of voltage headroom that can be tolerated. Since the circuit employs a differential topology it produces true output and its inverted logic.

Some of the other MCML topologies are as shown in the figures 2.2, 2.3, 2.4, 2.5.

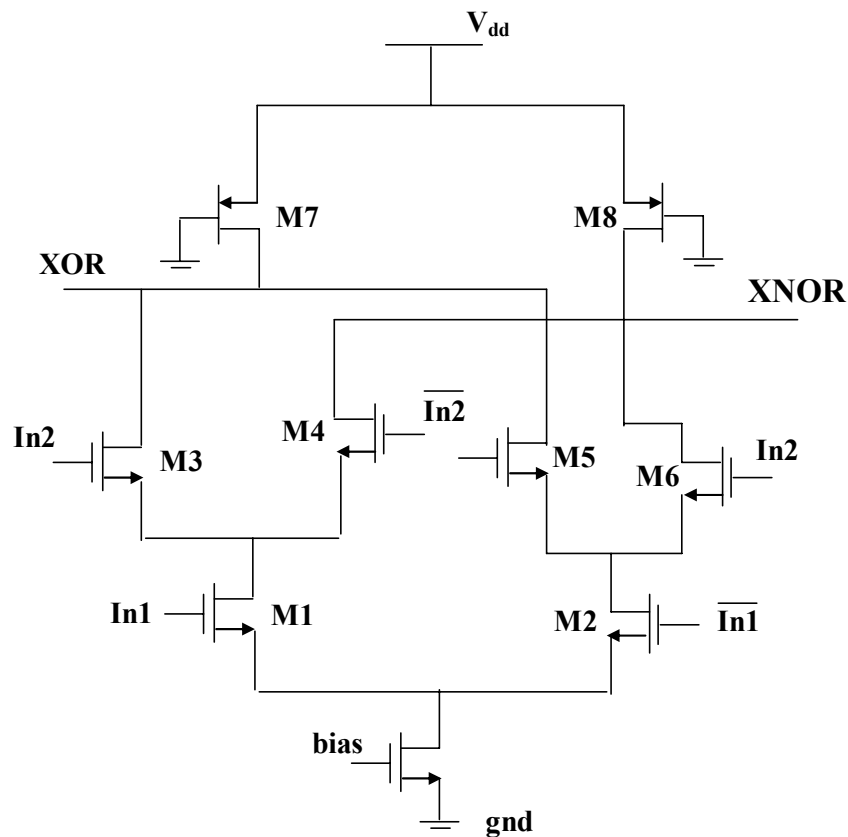


Figure 2.2. Schematic for XOR gate using MCML topology

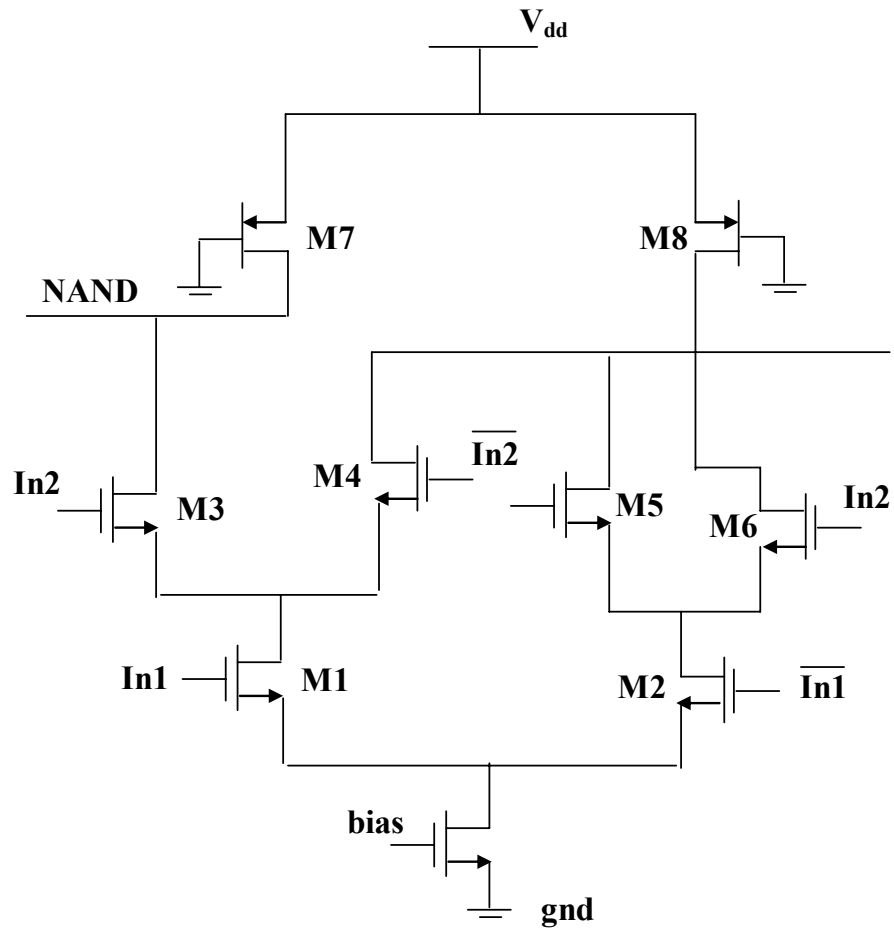


Figure 2.3. Schematic for AND gate using MCML topology

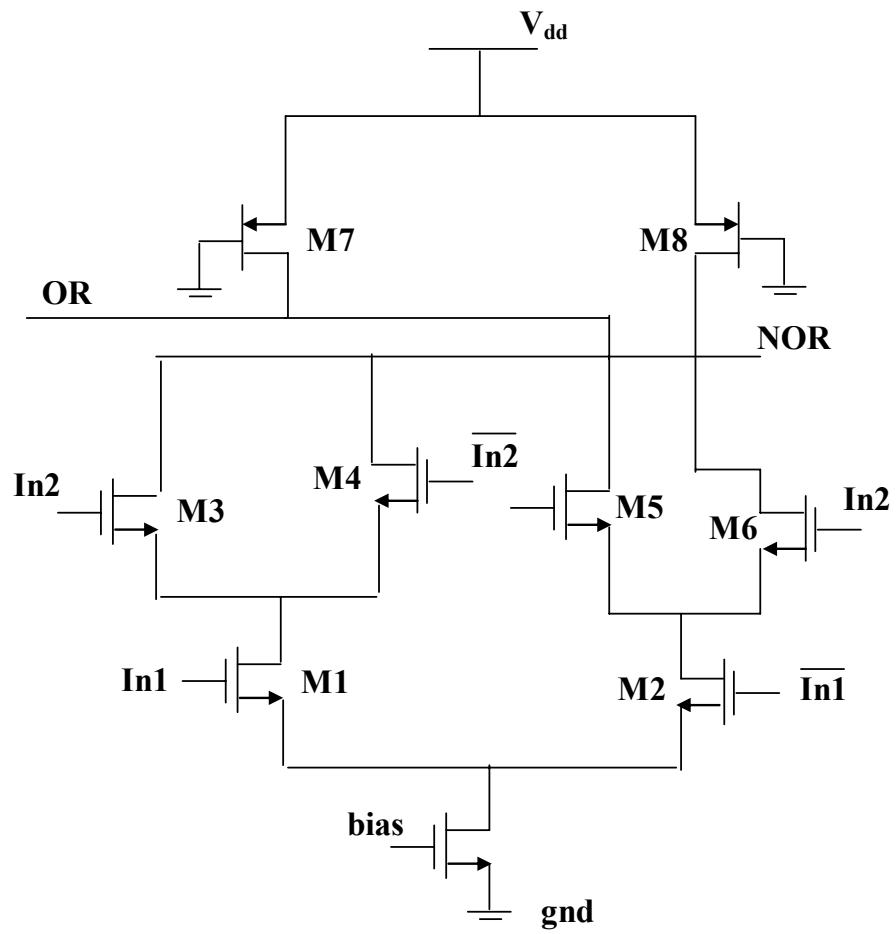


Figure 2.4. Schematic for OR gate using MCML topology

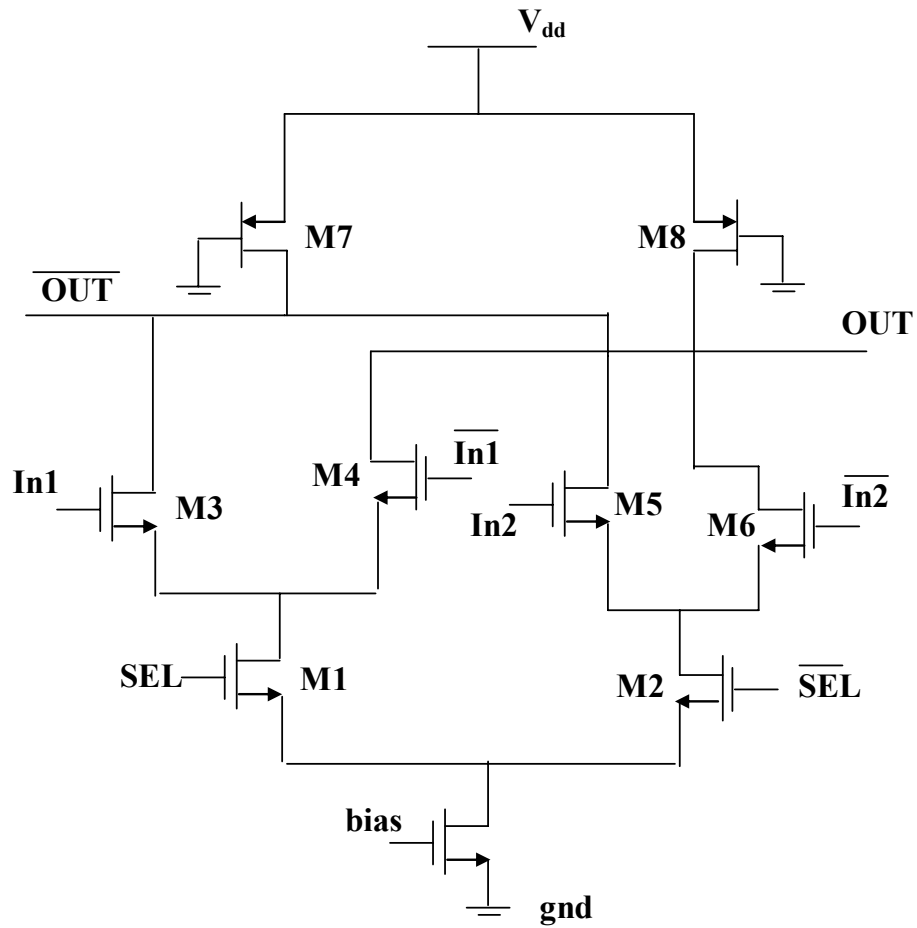


Figure 2.5. Schematic for Multiplexer using MCML topology

### 2.1.2 Design parameters

Design parameters [8] for typical MCML circuit include circuit delay ( $T_d$ ), Power consumption ( $P_d$ ), Voltage swing ( $V_{swing}$ ) and Noise Margin (NM).

#### 2.1.2.1 Circuit delay ( $T_d$ )

The delay of the circuit is a direct replica of its faster performance. The circuit delay for a MCML circuit is calculated using the simple RC approximation, where R comes from the resistance of the pull up networks and C comes from the total

capacitance seen at the output node. A simple small signal model for MCML inverter is shown in the figure 2.6.

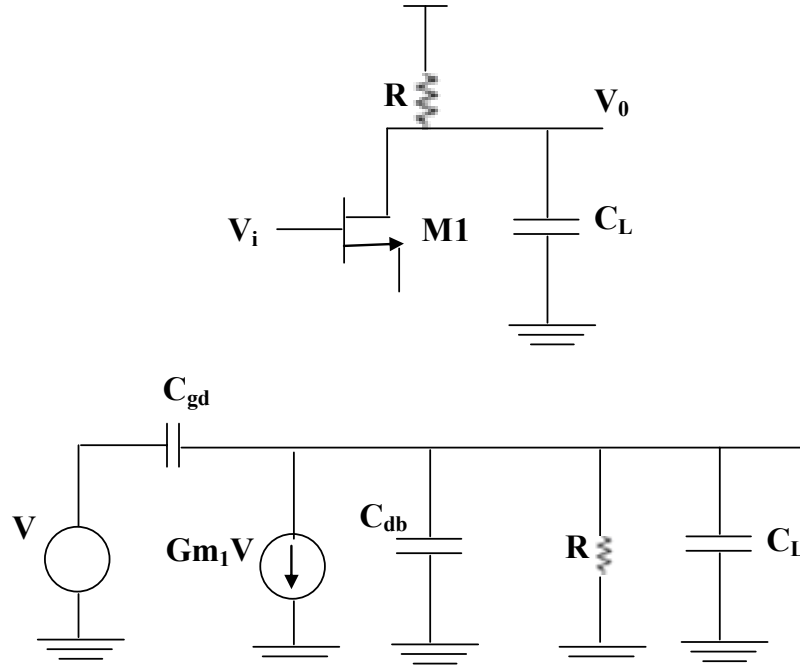


Figure 2.6. Small signal model for MCML inverter

It can be seen that the total capacitance comes from the gate to drain capacitance and the drain to bulk capacitance of the input transistors along with the load capacitance. For a step rise in the input, the circuit delay is given by,  $T_d = 0.69 RC$ . The delay of the circuit can be minimized by increasing the bias current, but there is a limit up to which the current can be increased since the current is directly proportional to the power dissipation. Thus if we increase the current, the power dissipation increases and hence there is a trade-off between delay and power dissipation.

#### 2.1.2.2 Power consumption ( $P_d$ )

Power consumption of conventional CMOS logic increases with the increasing frequency. This is not true for MCML circuits. The power consumption in MCML is

constant irrespective of the frequency of operation [9]. Thus, it is advisable to use CML logic styles only at considerable high frequency where power consumption of CMOS logic style becomes greater than that of MCML. The MCML consumes static power due to the use of constant current source [10]. Power consumption for MCML circuits is given by,

$$P_d = V_{dd} \times I_{bias} \quad (2.1)$$

It can be seen that the power consumption is function of power supply and the bias current. The power supply ( $V_{dd}$ ) for any circuit is usually fixed, thus once the bias current is fixed, the power consumption ( $P_d$ ) is also fixed.

### 2.1.2.3 Voltage Swing ( $V_{swing}$ )

The voltage swing of the circuit usually depends on the technology used, it keeps on becoming smaller and smaller with technology because as the levels in the circuit increases, the sum of the voltage drops across each transistor also increases in turn reducing the available voltage swing at the output node. As the technology scales down it becomes more and more challenging to keep all the input transistors in saturation all the time, since the voltage available for the input transistors reduces. Voltage swing is given by,

$$V_{swing} = (I_{bias} \times R) / 2 \quad (2.2)$$

where,  $I_{bias}$  is the bias current used,  $R$  is the resistance offered by the load device and  $V_{swing}$  is the output voltage swing. The factor of 2 comes because if all the transistors are to remain in the saturation region, in the ideal case, the current should be equally divided among the two branches. Upper bound on voltage swing is decided by

the load device and the lower bound is defined at the point where all the input transistors remain in the saturation region.

#### 2.1.2.4 Noise Margin (NM)

Noise Margin is defined as the amount of noise a gate can tolerate without causing a significant change in its output. In MCML circuits noise margin is an important parameter because of the reduced voltage swings. Practically, a noise margin of 40% of  $V_{swing}$  is sufficient for a proper functioning of the circuit. The figure 2.7 depicts the general concept of noise margins.

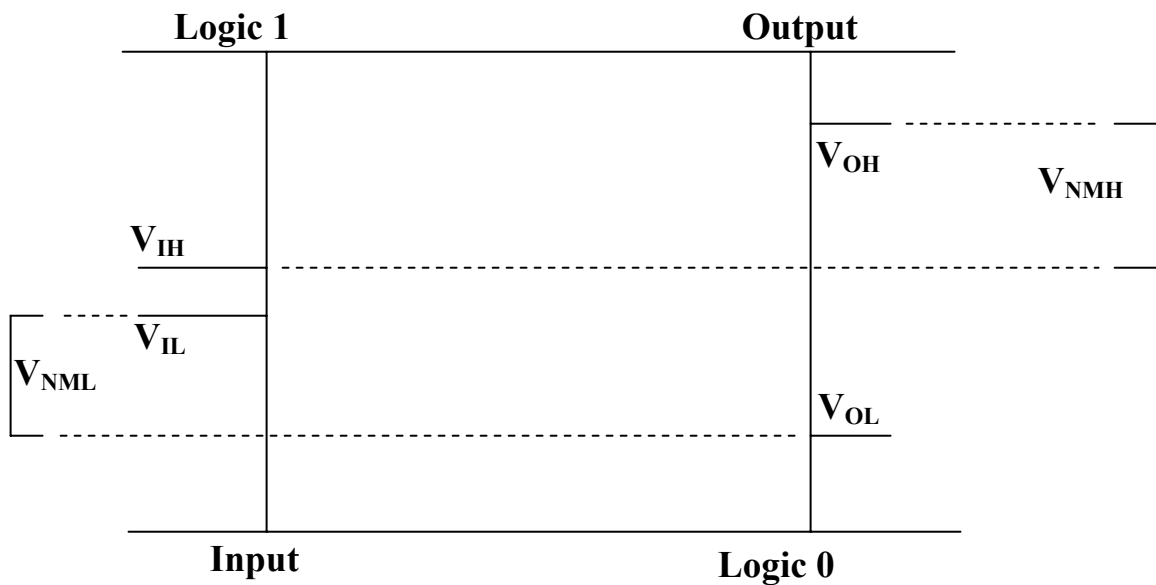


Figure 2.7. Noise Margin representation

where,  $V_{IH}$  is the minimum allowable input voltage that can be detected as logic high,  $V_{IL}$  is the maximum allowable input voltage that can be detected as logic low,  $V_{OH}$  is the minimum allowable output voltage that can be detected as logic high and  $V_{OL}$  is the maximum allowable output voltage that can be detected as logic low.



Thus,  $V_{NMH} = V_{OH} - V_{IH}$  and  $V_{NML} = V_{IL} - V_{OL}$ , where  $V_{NMH}$  and  $V_{NML}$  are the high and low noise margin levels for a given circuit.

### *2.1.3 Design variable*

Design variables include the total circuit bias current ( $I_{bias}$ ), pull-up and pull-down network transistor sizes  $W_1, L_1, W_2, L_2$  and so on and current source transistor size  $W_{cs}, L_{cs}$ .

#### *2.1.3.1 Bias current ( $I_{bias}$ )*

This is the most important design variable in the design process of any MCML circuit. All the other design variables can be designed only after fixing the bias current. The bias current decides the delay of the circuit and also the power consumption. There are two ways to decide bias current: slew rate or power consumption. Voltage swing of the circuit is also decided by the bias current.

#### *2.1.3.2 Differential pair transistor sizes*

The transistor sizes of the differential pairs are decided based on the overdrive voltages across them. Increasing the width of these transistors help to increase the gain but it adds to the delay due to the addition of parasitic capacitance. But while designing logic gates since it is required to have unity gain the width is kept as small as possible. This minimizes the parasitic capacitance due to increase in transistor size. But in situations where gain is the important factor, width can be chosen with a compromise between the gain and the delay. The length of the transistors is kept minimum, because length adds to the parasitic capacitance and eventually increases the delay.

### 2.1.3.3 Current source transistor sizing

A constant current is very important to ensure that power supply fluctuations are reduced. To maintain a constant current through the current source transistor, it should be in saturation all the time. Constant current is maintained using a simple current mirror topology, wherein the transistor sizes of the current mirror transistors are properly matched so as to achieve the maximum current matching. The length of this transistor is increased to an extent that it can have higher output impedance. Slope of the current in saturation region is inversely proportional to the output impedance of the transistor [11]. The output impedance of the transistor in saturation is,

$$r_{out} = 1 / (\lambda I) \quad (2.3)$$

where,  $\lambda$  is the channel length modulation parameter and  $I$  is the current in the saturation region. Since,  $\lambda$  is directly proportional to the length of the transistor, increasing the length of the transistor, increases  $\lambda$  and thus increases the output impedance. Thus, by increasing the length we can keep the current to be constant in saturation region, so it is advisable to increase the length of the current source transistor.

## 2.2 Substrate noise

Integrating analog and digital circuitry on the same die is one of the main goals of circuit designers; the problems caused by the digital circuits can cause deterioration of the outputs from the analog circuits. The noise transferred from the digital circuits to the analog circuits, in a mixed signal environment, via the coupling through the substrate is called the substrate noise. This type of noise is detrimental to the performance of mixed signal environment circuits because it disrupts the output of

analog circuits. The substrates having less resistivity can transfer this type of noise easily from noisy digital circuits to sensitive analog circuits.

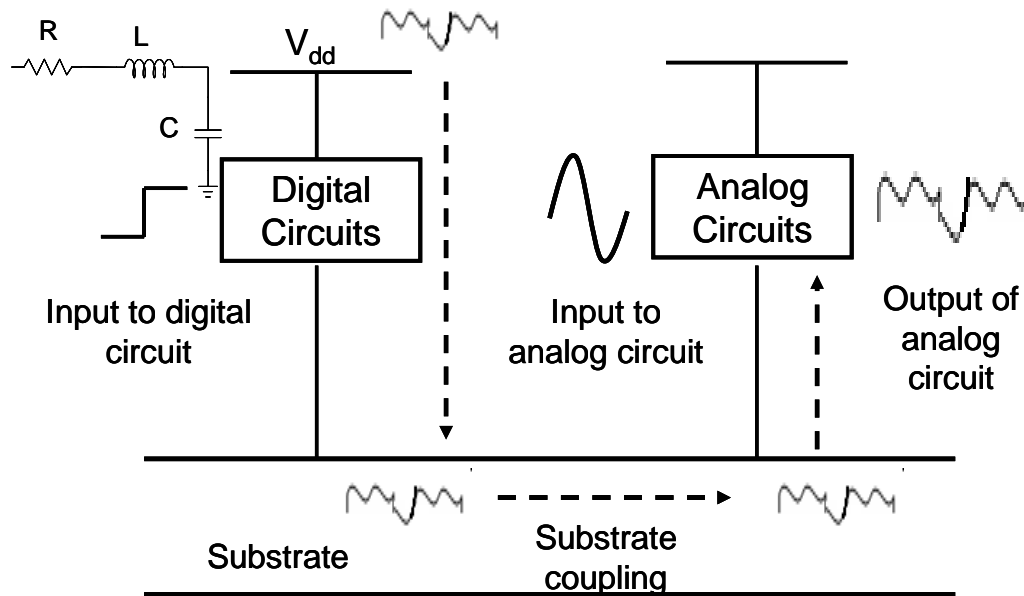


Figure 2.8. Substrate noise in mixed signal environment

There are two types of substrates: 1. Lightly (uniformly) doped substrate and 2. Heavily doped substrate with an epitaxial layer.

The features of Lightly doped substrate are:

- a. The substrate is uniformly doped from surface to bottom.
- b. It has high resistivity due to less number of dopants.
- c. Substrate resistance increases with separation.
- d. Low substrate noise due to high resistivity.
- e. Latch up problems.

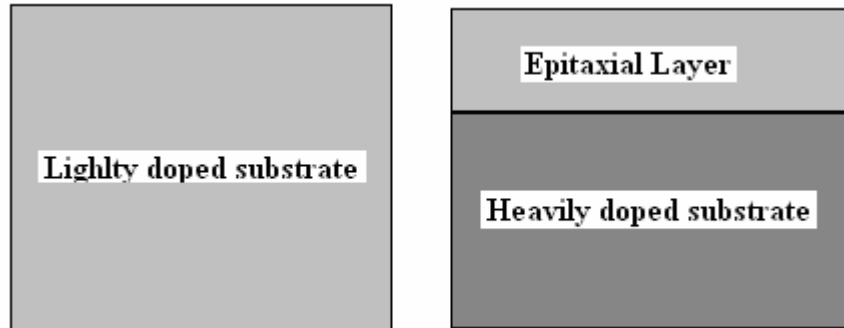


Figure 2.9. Lightly doped substrate and heavily doped substrate with an epitaxial layer

The features of heavily doped substrate are:

- a. Substrate consists of two layers the upper layer is the epitaxial layer and the bottom one is heavily doped.
- b. Epitaxial layer has high resistivity while the heavily doped layer has low resistivity.
- c. Helps to prevent Latch up problems.
- d. Exhibits more substrate noise because of low resistivity of the heavily doped part.

### *2.2.1 Latch up*

Latch up is the mechanism by which a low resistance path is created within the substrate in such a way that the current through the device reaches a destructive level.

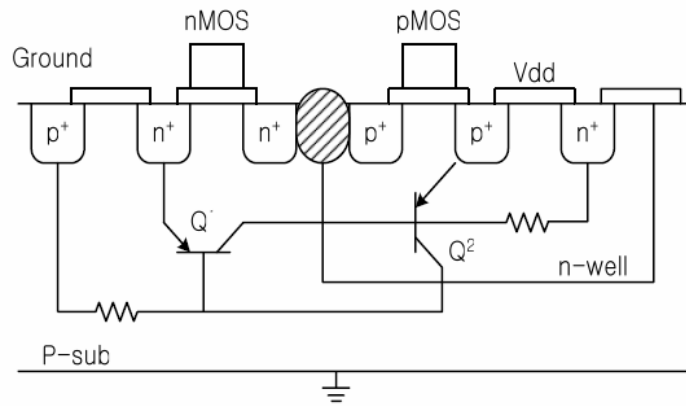


Figure 2.10. Latch up in substrates due to parasitic transistors

As seen in figure 2.11, whenever the potential of substrate goes above the source potential of the nMOS transistor the parasitic transistor Q1 turns ON. Its emitter current increases and turns ON Q2. This in turn increases the base current of Q1 and the cycle repeats until a destructive level. This problem arises because the parasitic transistor Q1 turns ON. If Q1 is not allowed to turn ON this problem can be eliminated which can be done by using a heavily doped substrate with an epitaxial layer.

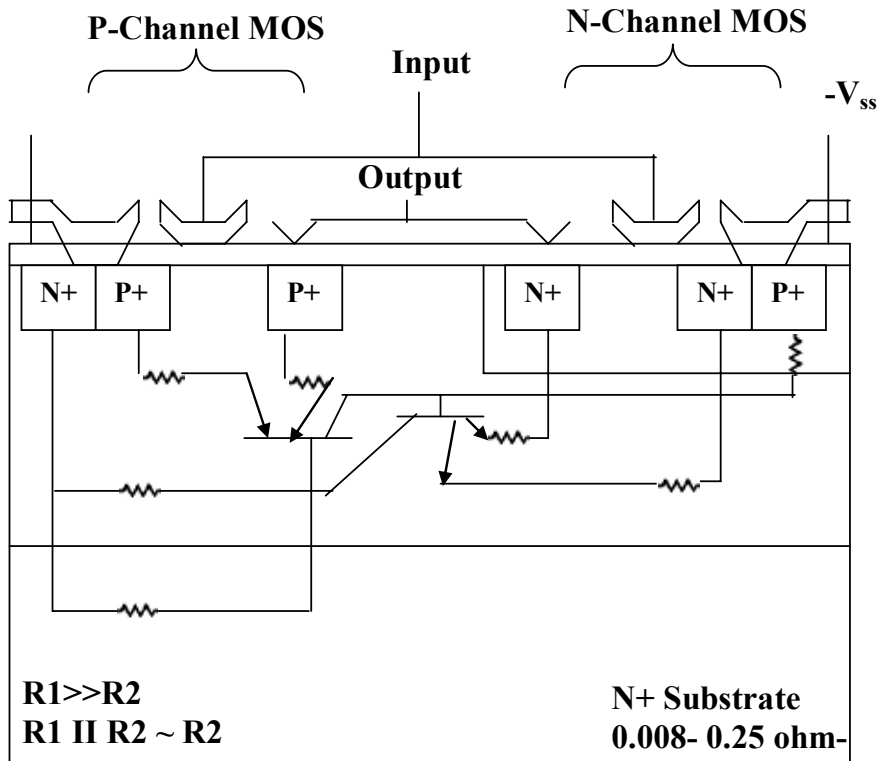


Figure 2.11. Solution to latch up problem [12] shown in figure 2.11

In this type of substrate the effective parallel resistance is very less and hence a high amount of current is required to develop the required amount of voltage drop across the transistor to turn it ON.

The source of substrate noise are: 1. Simultaneous switching noise 2. Hot electron effect.

### 2.2.2 Simultaneous switching noise

In the process of scaling down the device dimensions, power supply and threshold voltage are also being scaled down. The device dimensions are scaled down to achieve higher frequencies of operation. But the problems like simultaneous switching noise, short channel effects, sub threshold leakage current, Drain Induced Barrier

Lowering (DIBL) [13] effects are encountered. The simultaneous switching is problem seen in almost all the CMOS digital logic family circuits. This was not a problem until the channels of the transistors were scaled down. Switching noise is generated whenever output switches states from low to high or from high to low. This abrupt change in the current at the power supply will cause a voltage fluctuation in the parasitics inductor in the power supply and the ground lines in accordance to the formula,

$$V = L di/dt. \quad (2.4)$$

These voltage fluctuations raise the potential of the device ground with respect to the system ground. This kind of noise is cumulative when a large number of outputs switch at the same time. This effect is also called delta I noise or di/dt noise. Slew rate is the dominating factor that affects the simultaneous switching noise problem. Higher slew rates are required for faster switching but it would show these types of problems. Thus, there is a trade-off.

### *2.2.3 Hot electron effect*

The hot electron effect is seen in deep submicron circuits. A very high electric field is developed in between the pinch off point and the drain region in a transistor operating in saturation region. Due to this, some fraction of the carriers in this region will gain enough energy to become hot. They will eventually scatter, dissipating their excess energy by creating additional energetic electron-hole pair, this is called impact ionization. This gives rise to substrate current. Some of these pairs can also get embedded into the gate oxide leading its degradation. This can also shift the threshold

voltage of the device. Thus, either the electric field needs to reduce or channel length should be increased. The pMOS has better performance in these scenarios since the mobility of holes is less than that of electrons. Hot electron effect is worst in nMOS than in pMOS.

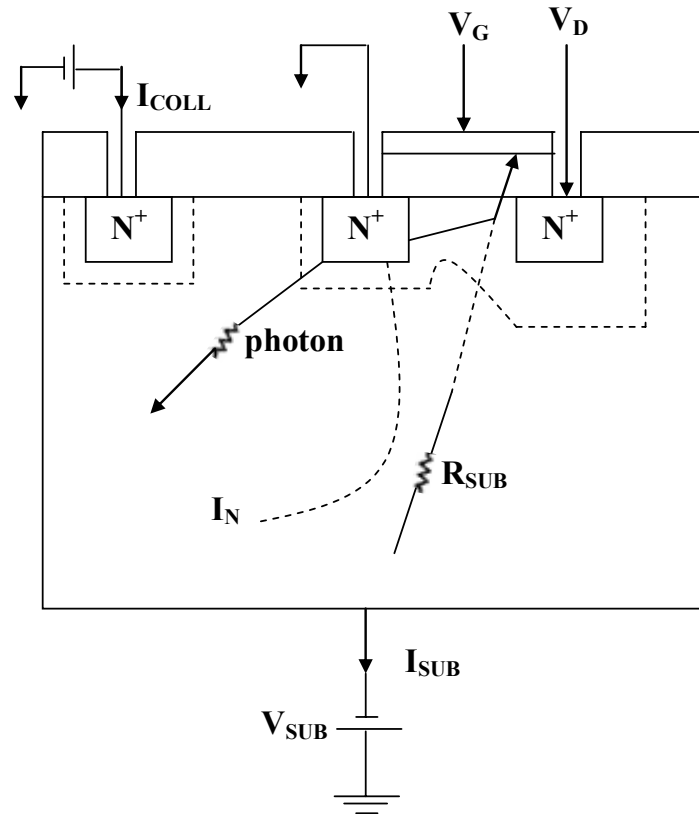


Figure 2.12. Hot electron effect in substrates

### 2.3 Package models

Package models are important while working with high speed application. They play a major role in designing of high speed circuits. All the discussion on substrate noise and simultaneous switching noise comes into play when the package models are considered. These models come from the interconnecting wires, the bond wires, the



PCB traces, the output pads and the output pins. When the slew rates of the signal is in picoseconds range, the package model deteriorates the performance. Package models affect the signal quality because of the reflections and the distortions from the impedance mismatches. Some of the proposed models are shown in figure 2.14 and 2.15.

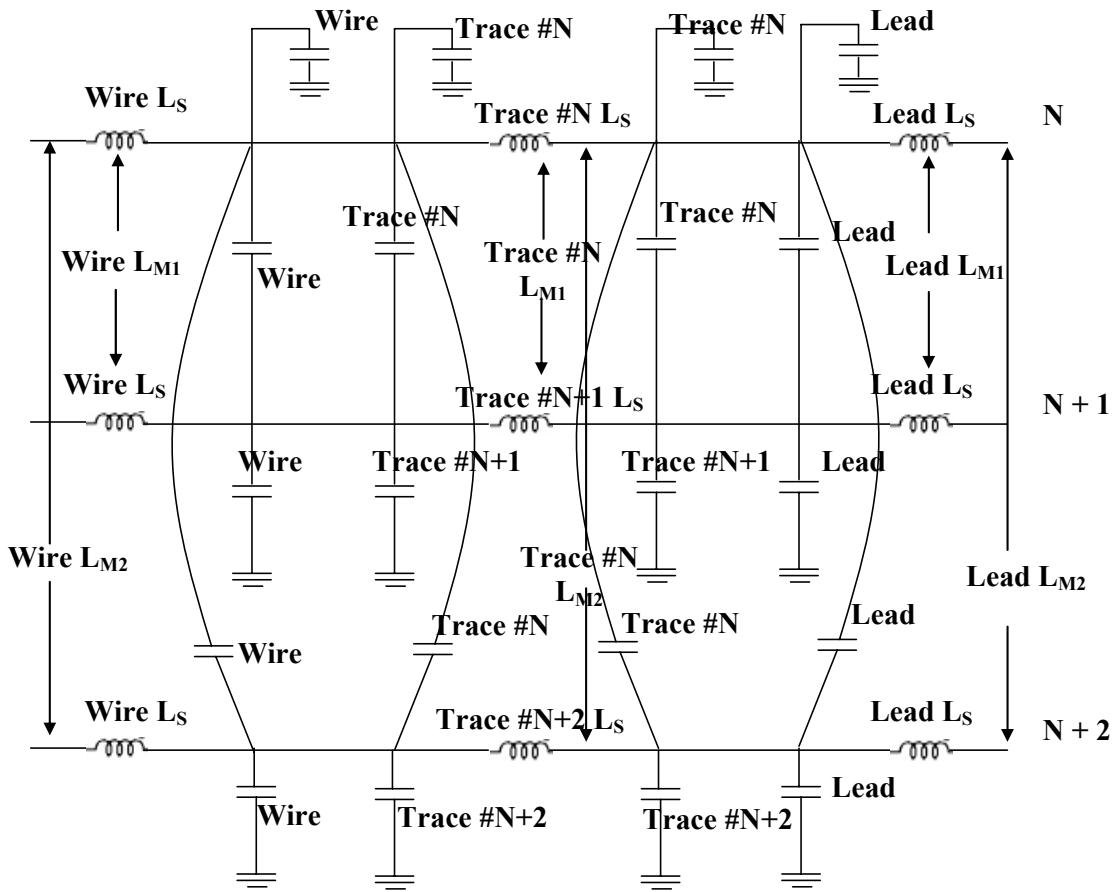


Figure 2.13. Package Model- 1 [14]

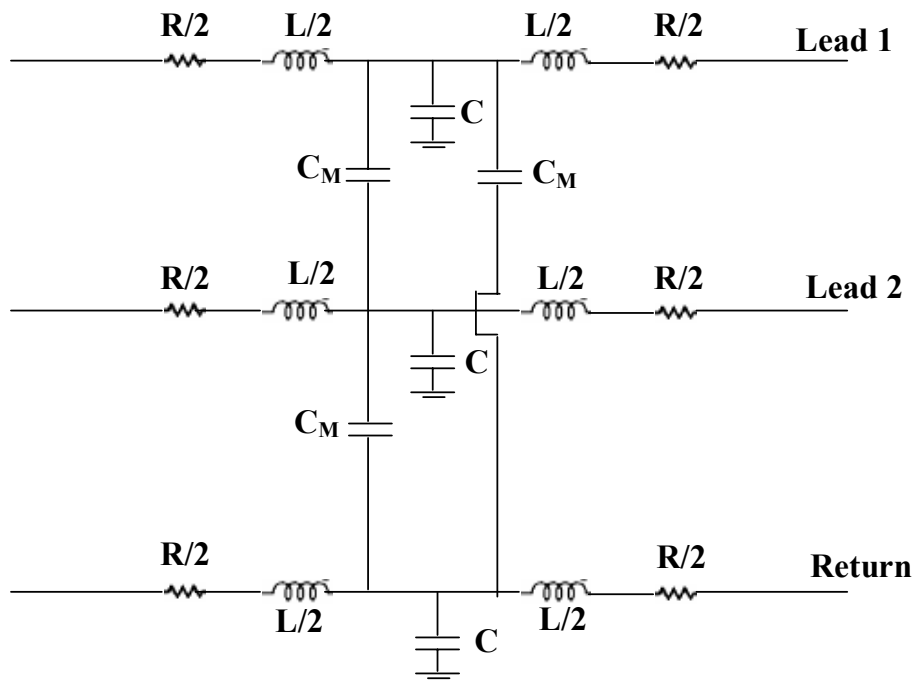


Figure 2.14. Package Model- 2

## CHAPTER 3

### MOS CURRENT MODE LOGIC CIRCUITS

This chapter introduces the designing of MOS Current Model Logic circuits. Design procedure for MCML inverter is shown first which is then followed by design for XOR gate and AND gate.

#### 3.1 MCML Inverter design

Figure 3.1 shows the circuit diagram of a MCML inverter. PMOS acts as the load device, nMOS performs the logic operation and the current source provides constant current. For designing the circuits, TSMC 0.18 um technology was used. The two input nmos transistors receive inverted inputs.

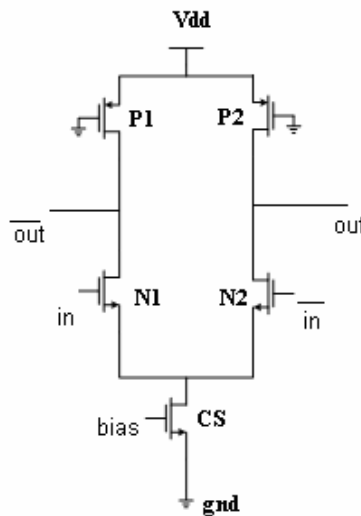


Figure 3.1. Schematic of CML Inverter

### 3.1.1 Design Procedure

The flowchart for design procedure starts with setting the bias current, followed by overdrive voltage settings for transistors and then finally the transistors sizes are calculated. The details for the flowchart are explained below.

Step 1: Setting the bias current.

The bias current is set either by slew rate or through power dissipation.

The equation for slew rate is described as,

$$I / C_L = V_{swing} / \Delta t \quad (3.1)$$

where  $C_L$  denotes the load capacitance and  $\Delta t$  is the small change in time during the switching event and  $I = I_{bias} / 2$ , since half the current is going to flow through each branch during common mode DC.

The equation for power dissipation is,

$$P_d = V_{dd} \times I_{bias} \quad (3.2)$$

where,  $P_d$  is the maximum power consumption and  $V_{dd}$  is the power supply voltage.

Step 2: Setting the overdrive voltages for the transistors.

Overdrive voltage for a transistor is given by,

$$V_{OV} = V_{GS} - V_{TH}$$

where,  $V_{GS}$  is the gate to source voltage for a transistor and  $V_{TH}$  is the threshold voltage for the transistor. The current for a transistor in saturation region is given by,

$$I = 1/2 \mu C_{OX} W/L (V_{GS} - T_{TH})^2.$$

From the above equation it is seen that overdrive voltage is directly proportional to the current flowing through it. Thus the transistor carrying the maximum current

should have the maximum overdrive voltage. Also, the equation shows that the overdrive voltage increases with the decrease in mobility due to which pMOS transistors are allotted higher overdrive voltage. The remaining voltage is then assigned to the nMOS differential pair transistors.

Step 3: Calculating the transistor sizes.

Once the current passing through a transistor and the overdrive voltage across it are set, the aspect ratio of the transistors can be calculated by,

$$I = 1/2 \mu C_{OX} W/L (V_{GS} - T_{TH})^2 \quad (3.3)$$

where,  $\mu$  = mobility of the electrons or holes in nMOS or pMOS respectively,

$C_{OX}$  = Oxide capacitance,

$W/L$  = aspect ratio for a transistor.

### 3.1.2 Simulated results

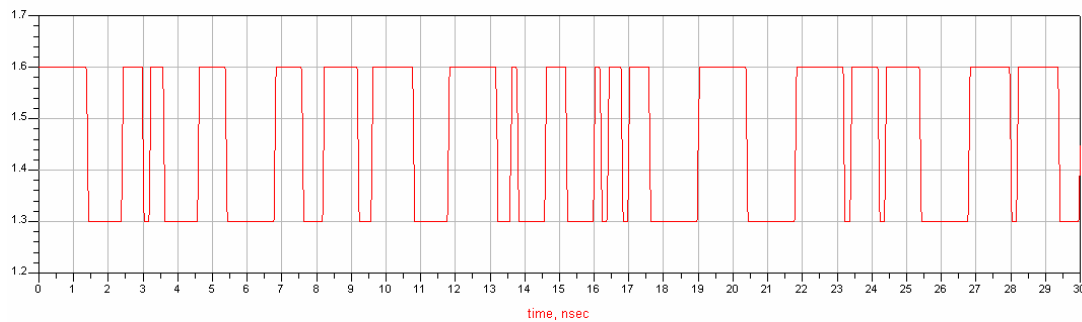


Figure 3.2 Input to MCML inverter.

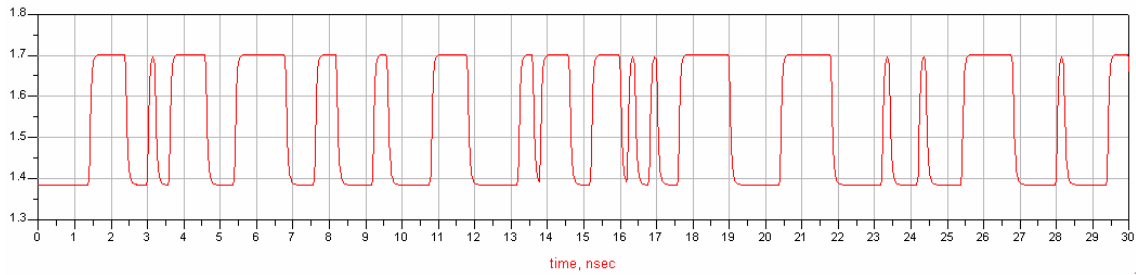


Figure 3.3. Output of MCML inverter at 5 Gbps.

Figure 3.3 shows that the output is inverted with respect to the input thus providing the expected logic operation for an inverter. The power consumed by the designed MCML inverter was 3.6 m W at 5 Gbps and it introduced a delay of 20 psec at the output.

### 3.1.3 Current mismatch problem in MCML Inverter

In figure 3.4, current flowing through the two branches is assumed to be equal to  $I_1$  and  $I_2$ .  $I_1$  flows in the branch where the input varies from high to low and  $I_2$  flows in the branch where input varies from low to high. Thus with respect to each other, the drain voltage of N1 will be higher and that of N2 will be lower after transition.

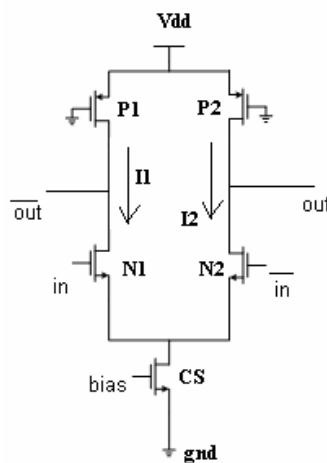


Figure 3.4. MCML Inverter

The circuit was designed in such a way that both the transistors remain in saturation all the time. But practically, since the drain voltage of N1 is higher than that of N2, transistor N1 will be in more saturation region than transistor N2. Thus, due to Drain Induced Barrier Lowering (DIBL) effect, the current variations in N1 were exponential while that in N2 were quadratic and this led to a current mismatch. This mismatch in the current flowing through the two transistors created a mismatch in the total amount of current flowing through the power supply. Figure 3.5 demonstrates this effect.

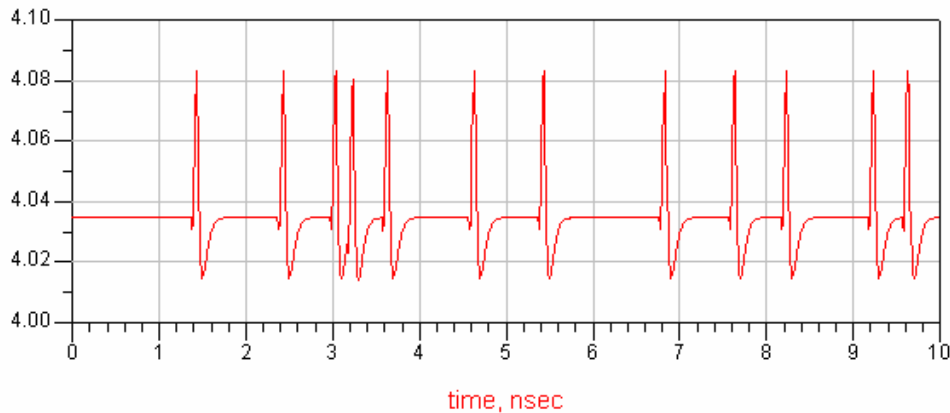


Figure 3.5. Current variations at power supply in MCML Inverter

### 3.1.3.1 Drain Induced Barrier Lowering (DIBL) Effect

Short channel transistors have different current variation in the saturation region when compared with long channel transistors. The threshold voltage of a long channel device is independent of the channel length and the drain voltage and is more dependent on the body bias effect. Dependence of threshold voltage on channel length and on drain voltage is higher in short channel transistors, while its dependence on body bias is less. The reason for this kind of behavior in short channel transistors is due to the

control on depletion region. In long channel devices, gate is completely responsible for depleting the transistor, but in short channel devices part of depletion is accomplished by drain and source voltages. Hence, as drain voltage increases more depletion is achieved and hence threshold voltage decreases. This effect is called Drain Induced Barrier Lowering (DIBL), since it effectively reduces the barrier for electron injection.

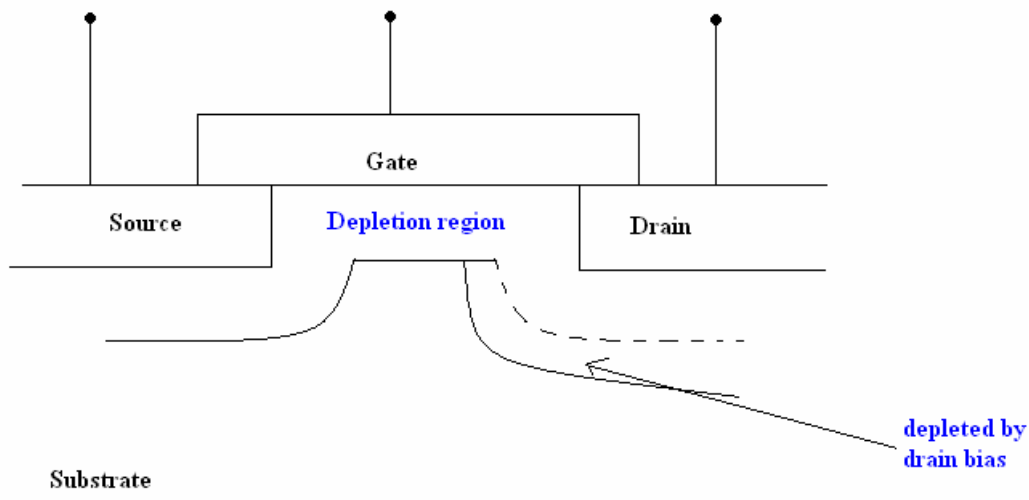


Figure 3.6. Drain Induced Barrier Lowering effect in short channel transistors

DIBL results in increased current flow for less amount of gate voltage. Also the behavior of current in this region is exponentially proportional to the drain voltage.

### 3.2 MCML XOR gate design

#### *3.2.1 Logic Operation*

Table 3.1 explains the logic operation for an XOR gate. Whenever both the inputs are at the same logic levels either high or low, output will be low. In figure 3.7, whenever both the inputs are high i.e.  $in1 = 1$  (logic 1) and  $in2 = 1$  (logic 1), all the current is steered by transistors M1 and M3 and the XOR output goes low.



Table 3.1. Truth table for MCML XOR gate

In1	In2	Out
0	0	0
0	1	1
1	0	1
1	1	0

Similarly when one of the inputs is high for e.g. if  $in1 = 1$  and  $in2 = 0$ , all the current is steered by transistors M1 and M4 and the XOR output goes high.

The circuit diagram for MCML XOR gate is shown in figure 3.7. The design procedure for an MCML XOR gate closely resembles that of an operational amplifier.

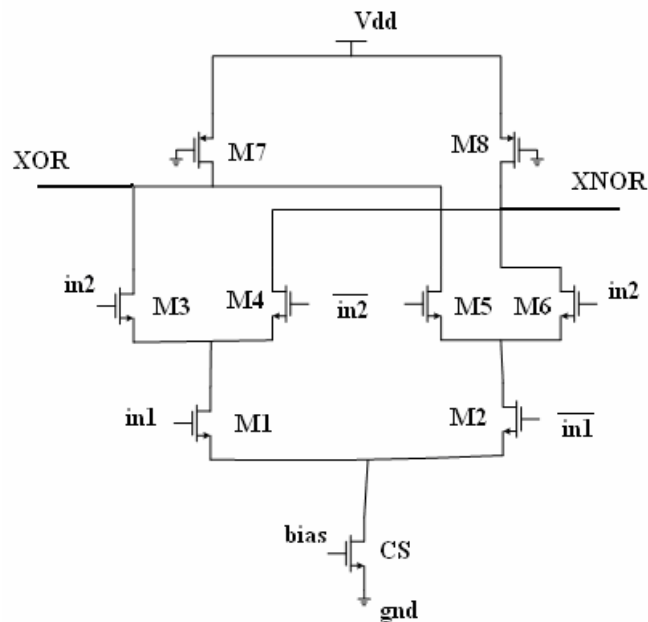


Figure 3.7. Schematic for MCML XOR gate

### 3.2.2 Design Procedure

The design procedure for MCML XOR gate is similar to that of MCML inverter explained in section 3.1.1 until the step of calculating transistor sizes.

Once the transistor sizes are set, the next step is to set the input common mode levels. The minimum allowable level for the input common mode for transistor M1 is given by

$$V_{GS,1} + V_{OD,CS} = V_{TH,1} + V_{OD,1} + V_{OD,CS}$$

where,  $V_{GS,1}$  is the gate to source voltage for transistor M1,

$V_{OD,CS}$  is the overdrive voltage for the current source transistor CS,

$V_{TH,1}$  is the threshold voltage for the transistors,

$V_{OD,1}$  is the overdrive voltage for transistor M1.

The input common mode level for the other input is also set in a similar fashion.

### 3.2.3 Simulated Results

Simulated results for the designed MCML XOR gate are shown below.

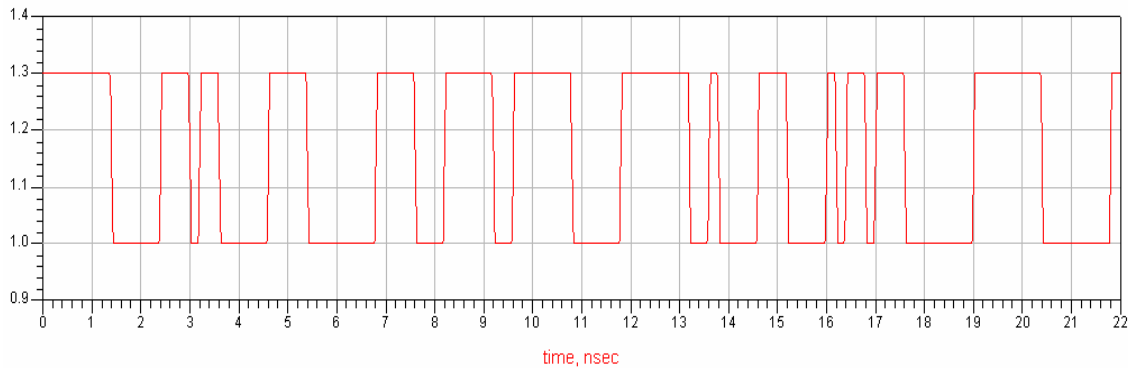


Figure 3.8. Input-1 to MCML XOR gate

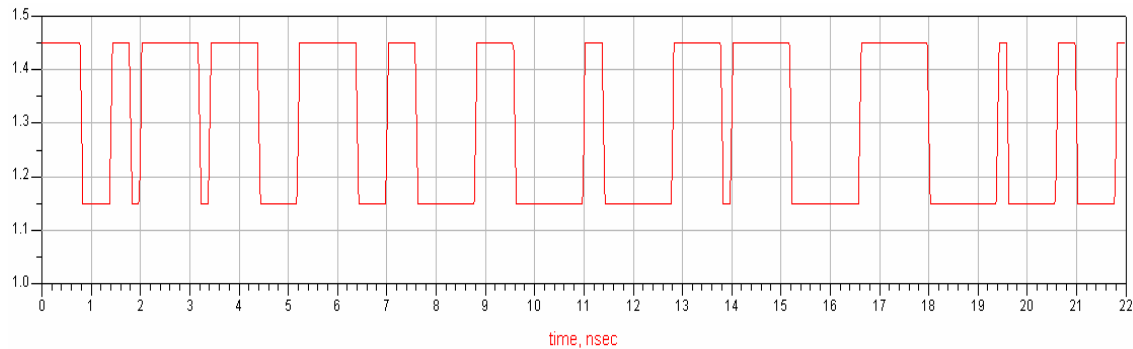


Figure 3.9. Input-2 to MCML XOR gate

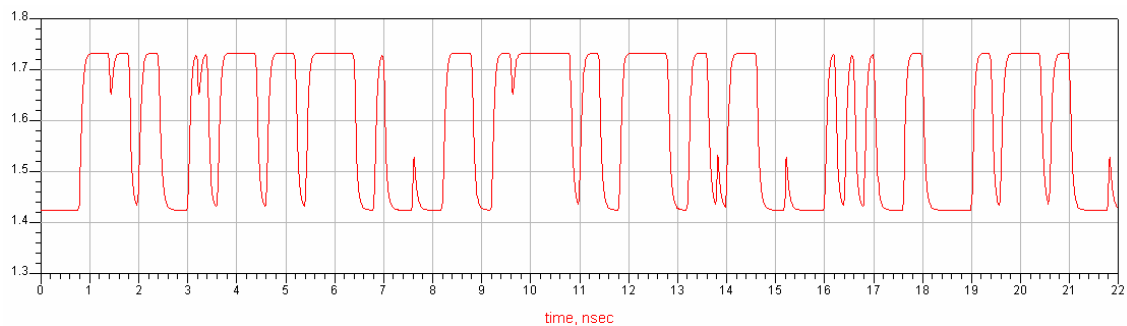


Figure 3.10. Output of MCML XOR gate at 5 Gbps

The output of the designed circuit is shown in figure 3.10. It is seen that whenever both the inputs are at the same logic level either high or low, the output gives a logic low or when both the inputs are different, the output is logic high. This follows the logic operation of an XOR gate. The designed circuit consumed 3.6 m W of power at 5 Gbps, introducing a delay of 40 psec.

In figure 3.10, the problem of glitch is noticed. This problem is observed in those gates which employ two inputs. Glitch occurs under two conditions:

- (1) When both the inputs switch states from high to low or low to high
- (2) When one input switches from high to low and the other switches from low to high.

The reason for this is whenever both the inputs change states, for some amount of time, the transistors attached to both the output branches will be active and they together will allow more current to pass and hence there will be a glitch.

### 3.3 MCML AND gate design

#### *3.3.1 Logic Operation*

Table3.2 Truth table for MCML AND gate

In1	In2	Out
0	0	0
0	1	0
1	0	0
1	1	1

Table 3.2 explains the logic operation for AND gate. Whenever both the inputs i.e., in1 and in2 goes high the output is high. In figure 3.11, when in1=0 (logic 0) and in2=0 (logic 0), all the current would be steered through transistor M1 and the output at AND is logic 0 and that at NAND is logic 1. When in1=0 and in2=1, again all the current is steered through M1 giving logic 0 at AND. When in1=1 and in2=0, all the current is steered through transistors M2 and M3 again pulling down the voltage at AND to logic 0. Finally, when both the inputs are high, all the current would be steered through transistors M2 and M4 pulling down the voltage at NAND to logic 0 and that at AND to logic 1. Thus, it gives an ideal AND gate operation.

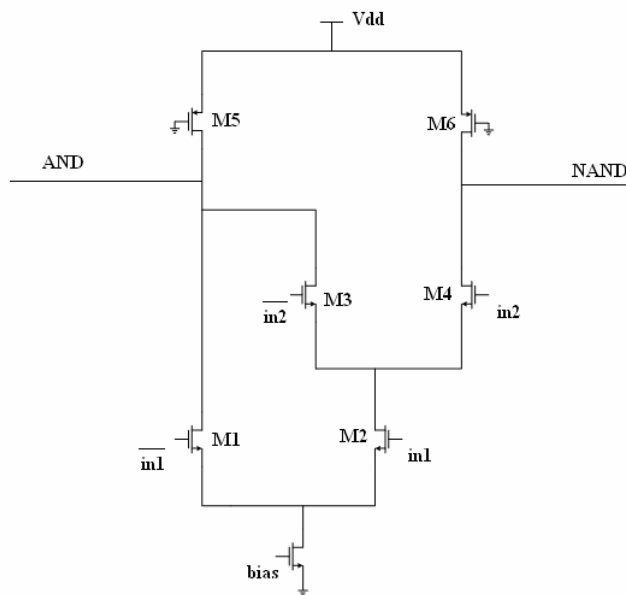


Figure 3.11. Simplest architecture for MCML AND gate

### 3.3.2 Design Procedure

The design procedure for AND gate is the same as that for an XOR gate. But while implementing this topology a few problems occur. This circuit operates in four different logic levels instead of two (logic 0 and logic 1).

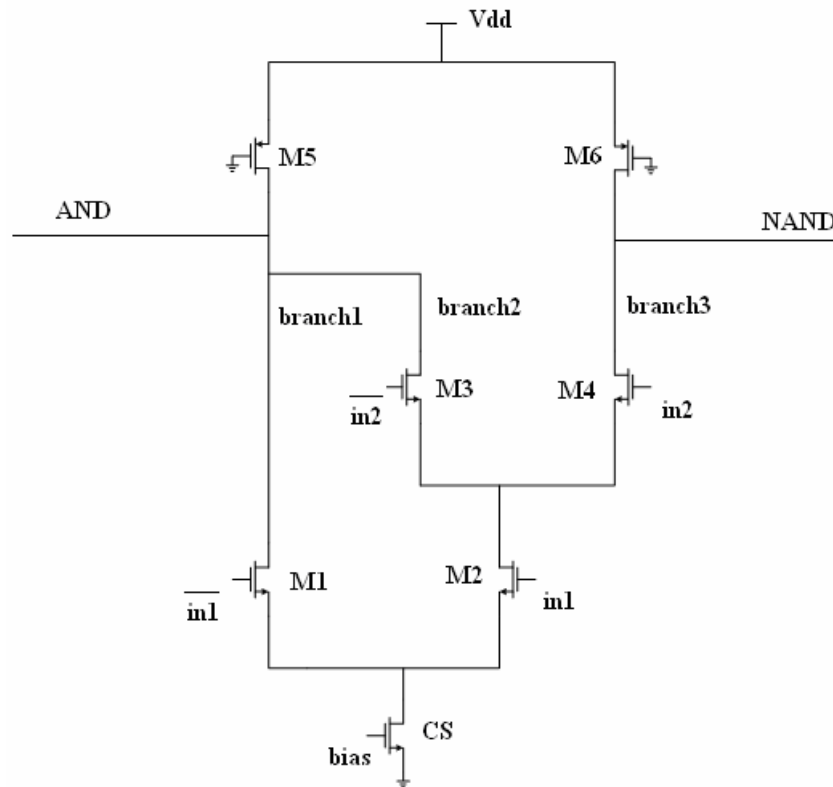


Figure 3.12. Architecture explaining AND gate operation

In figure 3.12, when  $in1=0$  and  $in2=0$ , all the current is steered through branch1 and a logic 0 is obtained at AND. But now when  $in1=1$  and  $in2=0$ , transistor M2 is on and transistor M3 is on, so ideally all the current should be steered through branch2 but since the circuit is designed in such a way that all the transistors work in saturation region, M1 will also steer some current and the logic 0 voltage level will not be able to reach the same as it reached when  $in1=0$  and  $in2=0$ . Similarly, it can be explained when  $in1=0$  and  $in2=1$  case and when both the inputs are high. Thus, there are four operating states rather than two operating states. Thus, it becomes necessary to introduce a pair of dummy differential transistors. The architecture for this work is shown in figure 3.13.

### 3.3.3 Designed architecture

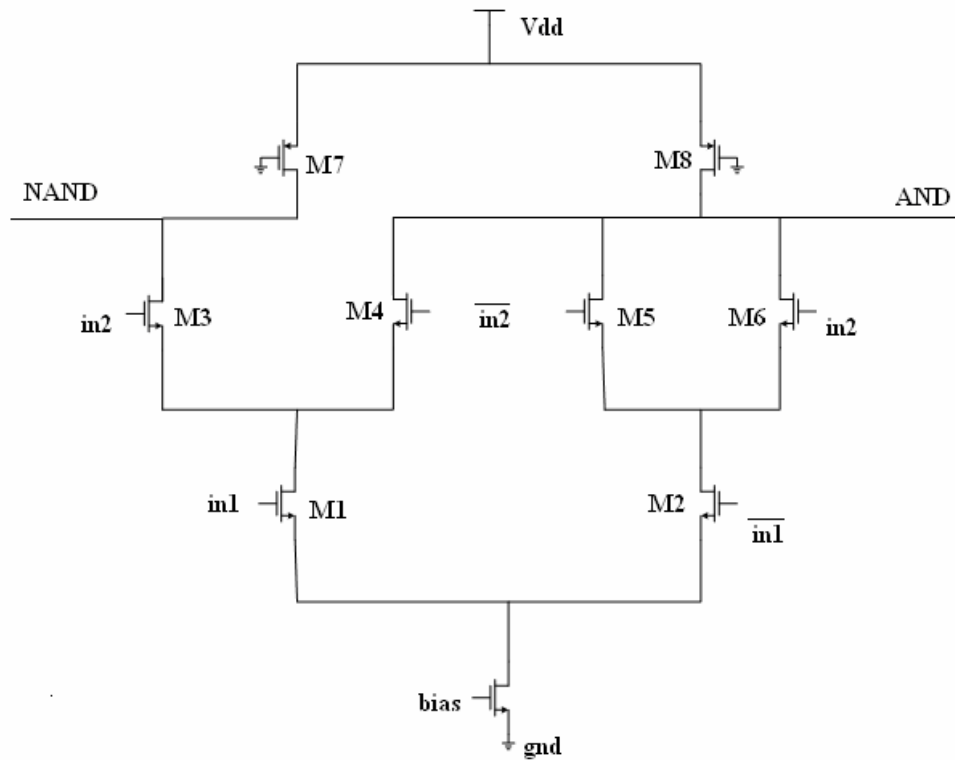


Figure 3.13. MCML AND gate architecture with dummy nMOS transistors

The logic operation and the design procedure of the above circuit remains the same. The simulated result for the designed circuit is shown in figure 3.16.

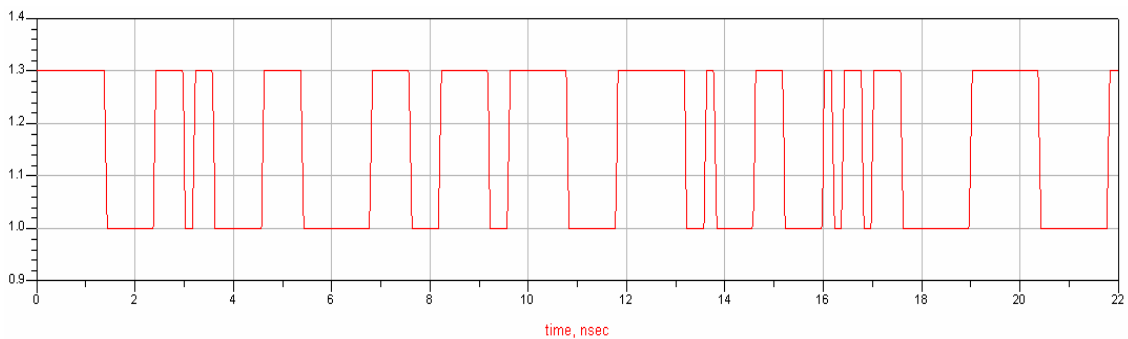


Figure 3.14. Input-1 to MCML AND gate

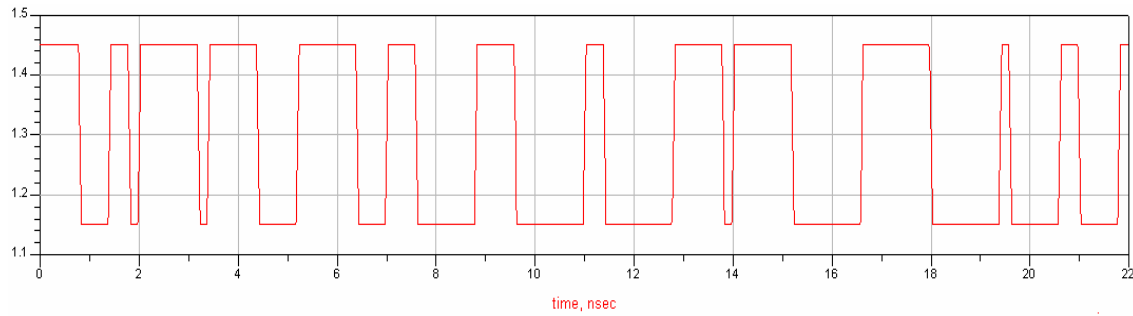


Figure 3.15. Input-2 to MCML AND gate

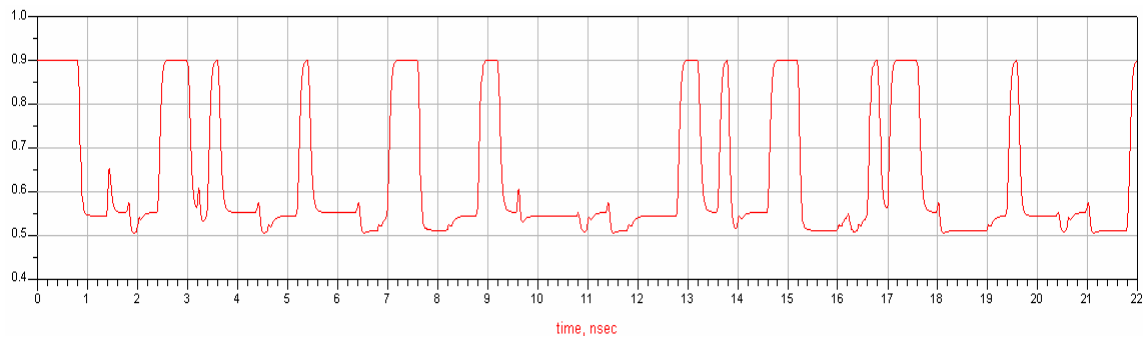


Figure 3.16. Output of MCML AND gate at 5 Gbps

The output of the designed circuit is shown in figure 3.16. It is seen that the output attains logic 0 in all cases except when both the inputs are high. The designed circuit consumed 3.6 m W of power at 5 Gbps, introducing a delay of 40 psec. As seen in the output the logic low level is not stable because of the same problem as discussed in section 3.3.4. But these variations still remain within the required noise margin level, which was calculated to be 0.1 V. This was acquired with using architecture with dummy transistors. The problem of glitch adds to the above mentioned problem.



## CHAPTER 4

### PARASITIC MODELING

As technology scales down and the frequency of operation keeps on increasing the noise generated from internal parasitics cannot be neglected. These type of noises are usually generated when rise/fall time of signal roughly matches the propagation time of the signal through the interconnects. All the relevant problems can be combined into one single word named “Signal Integrity” [15], [16].

#### 4.1 Signal Integrity

Signal integrity is gaining more and more attention as the technology scales down. Signal integrity means how clean the signal is, i.e., whether logic 1 stays steady at logic 1 or keep on fluctuating. If it stays steady then its called good signal integrity or else its bad signal integrity. In digital circuit case, the output should not cross  $V_{OH}$  or  $V_{OL}$  more than once. If it crosses more then one than it becomes very difficult for the next stage to decide whether its logic 1 or logic 0. A simple explanation can be provided from the figure 4.1.

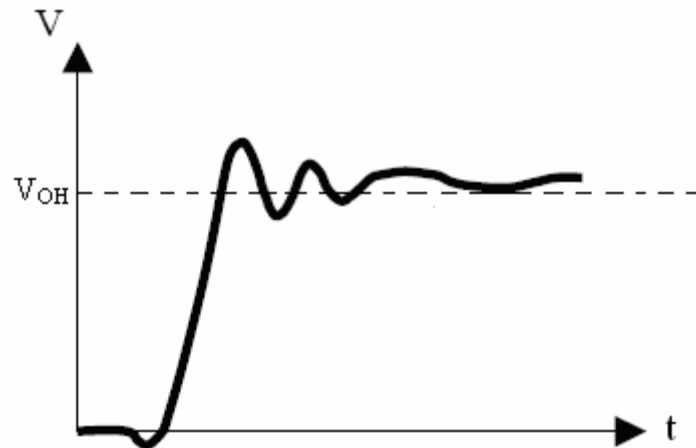


Figure 4.1. Signal crossing  $V_{OH}$  more than once

If the output from the previous stage fluctuates as shown in figure 4.1 [17], it becomes very difficult for the next stage to decide whether it has logic high or logic low at its input.

#### 4.1.1 Causes of bad signal integrity

There are three main causes for bad signal integrity namely, Reflection noise, Crosstalk noise and Power/ground noise or simultaneous switching noise. Reflection noise is caused because of improper terminations. The signal does not completely get absorbed at the other end due to which there are back and forth reflection of the signal and hence the name reflection noise. There is also one more effect in this case called ringing, where a damped sine wave gets superimposed on the rising and the falling edge of the signal. Figure 4.2 explains the concept in a better manner.

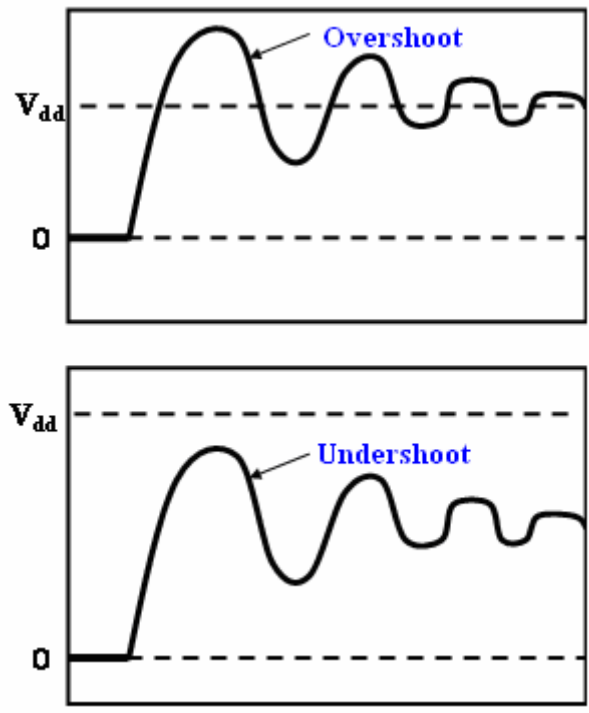


Figure 4.2. Overshoot and undershoot in signals

Crosstalk noise is generally caused due to capacitive or inductive coupling between traces. Capacitive coupling [18] occurs when traces lie in close vicinity. When traces are very close to each other signal can couple from one trace to another causing a speedup or an additional delay in the victim trace. Figure 4.3 demonstrate the capacitive coupling between two nearby traces.

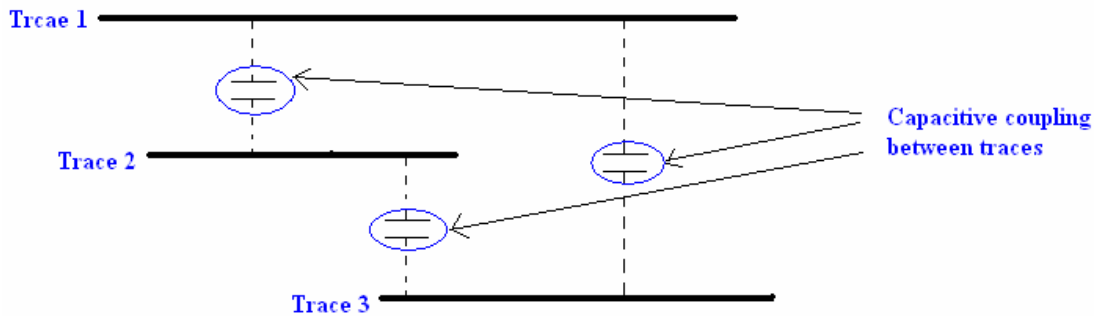


Figure 4.3. Capacitive coupling in very close by traces

Inductive coupling [19] results from expanding and contracting of electromagnetic fields produced by switching currents in the trace. The coupling is proportional to the value of the inductance and the rate of change of the current with respect to the time.

Interconnect wires can be modeled as a capacitor in parallel with the series combination of the resistance and the inductance usually called the parasitics. Current changes in inductors can be modeled as  $V = L di / dt$ , where  $V$  is the change in the voltage across the inductor due to the changing current. Due to large changes in the current during switching activity supply voltages see a large switching generating noise called simultaneous switching noise (SSN). SSN on power supply lines can travel to other circuitry having the same power supply bus, thus causing variations in the output in these circuits also. These parasitics comes from various parts on a chip like the output pads, the bond wires, the traces and the output pins. Figure 4.4 would better explain the nodes of parasitic generation.

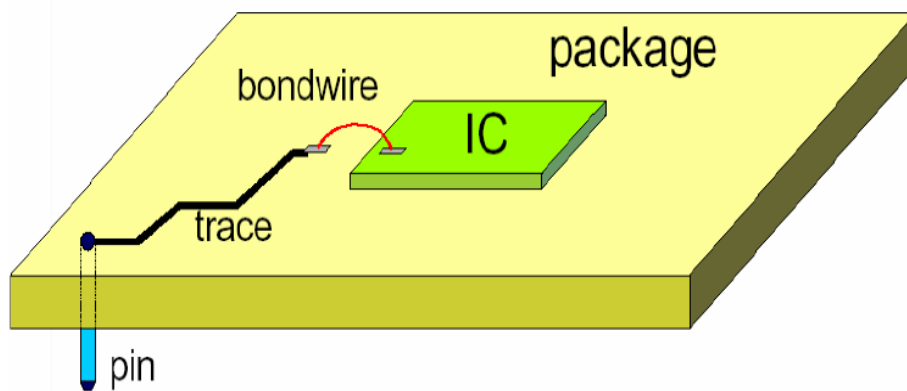


Figure 4.4. A chip showing the places from where parasitics originate

#### 4.1.2. Techniques to reduce bad signal integrity

Bad signal integrity can be reduced by: Noise constrained routing, repeater insertion, lines switching at different times and keeper circuits.

In this work we concentrate on simultaneous switching noise. To understand it better we first need to have a proper model of the parasitics in the power supply lines.

#### 4.2. Parasitic modeling

In figure 4.4 we can see that the parasitics mainly comes from the output pads, the bond wires and the trace, so concentration is more in modeling them.

##### 4.2.1 Models for pads, bond wires and traces

Model for output pad is fairly simple; output pads are usually modeled as a capacitance to ground. Bond wire is modeled as an inductor and is measured in nH/mm, longer the wire more is the inductance offered and hence more are the problems. Figure 4.5 shows the modeling of a bond wire along with the model for the output pad.

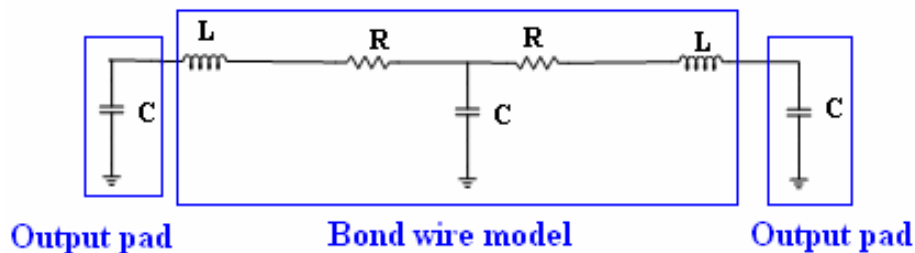


Figure 4.5. Parasitic model for bond wire along with the output pads

Some of models for a bond wire also include a resistance in series with the inductance. The resistance of the wire can change drastically depending on the skin effect. Skin effect can be defined as the tendency of the current within a conductor to flow in such a way that the current density at the surface is greater than at the core.

Higher the frequency more is the skin effect and hence more resistance is being offered to the flowing current and hence resistance increases. Formulas for calculating the resistance depending on the skin effect is covered in the following topics. It is also necessary to understand the model for coupled bond wires. Figure 4.6 shows the model for a coupled bond wire.

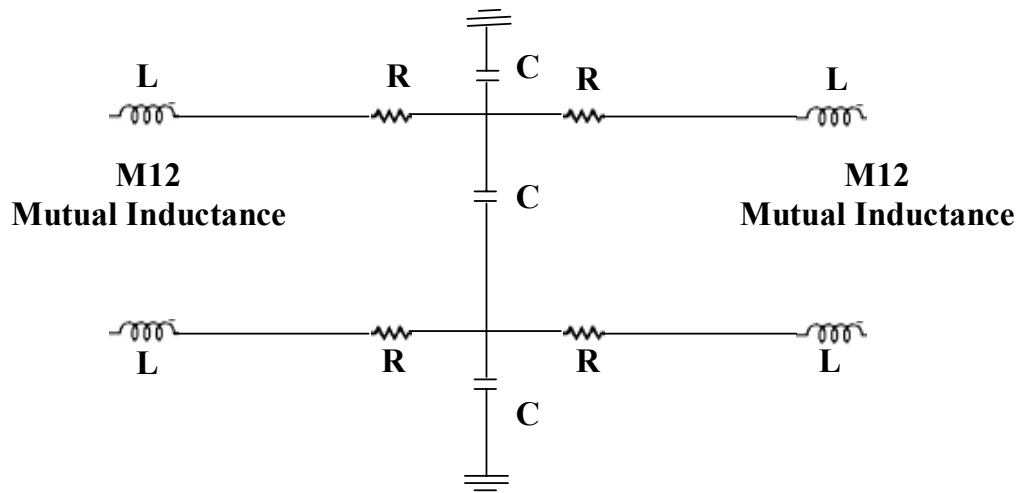


Figure 4.6. Parasitic model of two bond wires showing mutual inductance between them

M12 is the mutual inductance co-efficient between the two inductors of the two neighboring bond wires.

Trace is the path taken by the input signal to reach the chip from the input pins. At very high frequencies trace is assumed to be a transmission line and the lumped component model can be used for modeling it. Thus, we model the trace as a resistance in series with an inductor and together in parallel with a capacitor. Figure 4.7, shows the model for a trace.

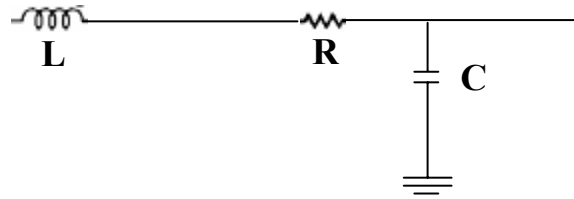


Figure 4.7. Model for a trace

#### 4.2.2 Hand calculations for the model

Here we model a trace with lumped component model. Now since a transmission line can be modeled as a lumped component model only if we consider a section of about 0.1 times the wavelength of the signal passing through it i.e.,  $0.1 \lambda$ .

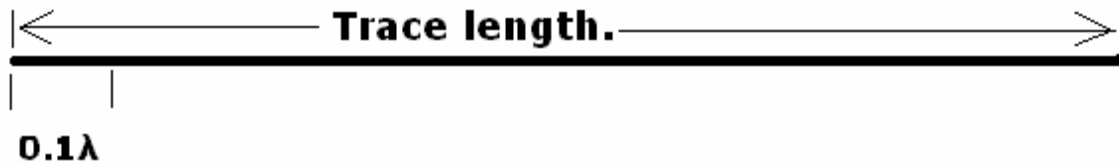


Figure 4.8. Representation of a trace

The length of the trace under test was 20 mm. The frequency of the signal passing through it was assumed to be 10 GHz i.e.,  $\lambda = 30$  mm. Thus,  $0.1 \lambda = 3$  mm.

So, the number of ladders required to model is equal to trace length /  $0.1 \lambda = 20 / 3 \approx 7$ .

To calculate the values of R, L and C the formulas used are as follows.

$$L_o = 0.001 * (C_o * (Z_o * Z_o)) \quad [\text{nH/in}] \quad (4.1)$$

$$C_o = (0.67 * (E_r + 1.41)) / LN ((5.98 * H) / (0.8 * W + T)) \quad [\text{pF/in}] \quad (4.2)$$

$$R = \rho * L / \delta * W, \quad \text{where } \delta = \text{skin depth} = L * \sqrt{(\rho / \mu f)} / W \quad [20] \quad (4.3)$$

$$\text{where, } Z_o = (87 / (\text{SQRT}(E_r + 1.41))) * LN ((5.98 * H) / (0.8 * W + T)) \quad (4.4)$$

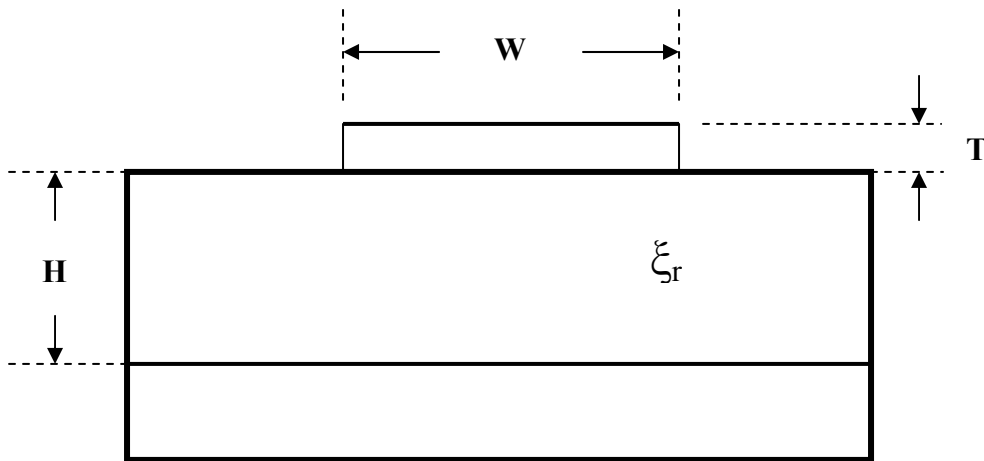


Figure 4.9. Dimensions of a trace

$W=27$  mils,  $H=15$  mils,  $T=1.4$  mils,  $\epsilon_r = 4.2$ .

Above are the dimensions for the trace we have tested.

Substituting these values into the above equations we get,  $L$  (nH/in) = 6.902,  $C$  (pF/in) = 2.762,  $Z_o = 50$  ohms. Thus,  $L = 6.902 * 0.1\lambda = 0.81$  nH,  $C = 2.762 * 0.1\lambda = 0.31$  pF,  $R = 41.5$  m $\Omega$ .

The model is then introduced into the power supply lines and the substrate of all the designed circuits to learn the detrimental effect of the parasitics model on the performance of MCML circuits.

#### 4.3 MCML inverter behaviour in the presence of parasitics

The designed parasitic model was introduced into MCML inverter circuit at power supply line, the ground and the substrate. After introducing the parasitics model the inverter circuit looked as shown in the figure 4.10.



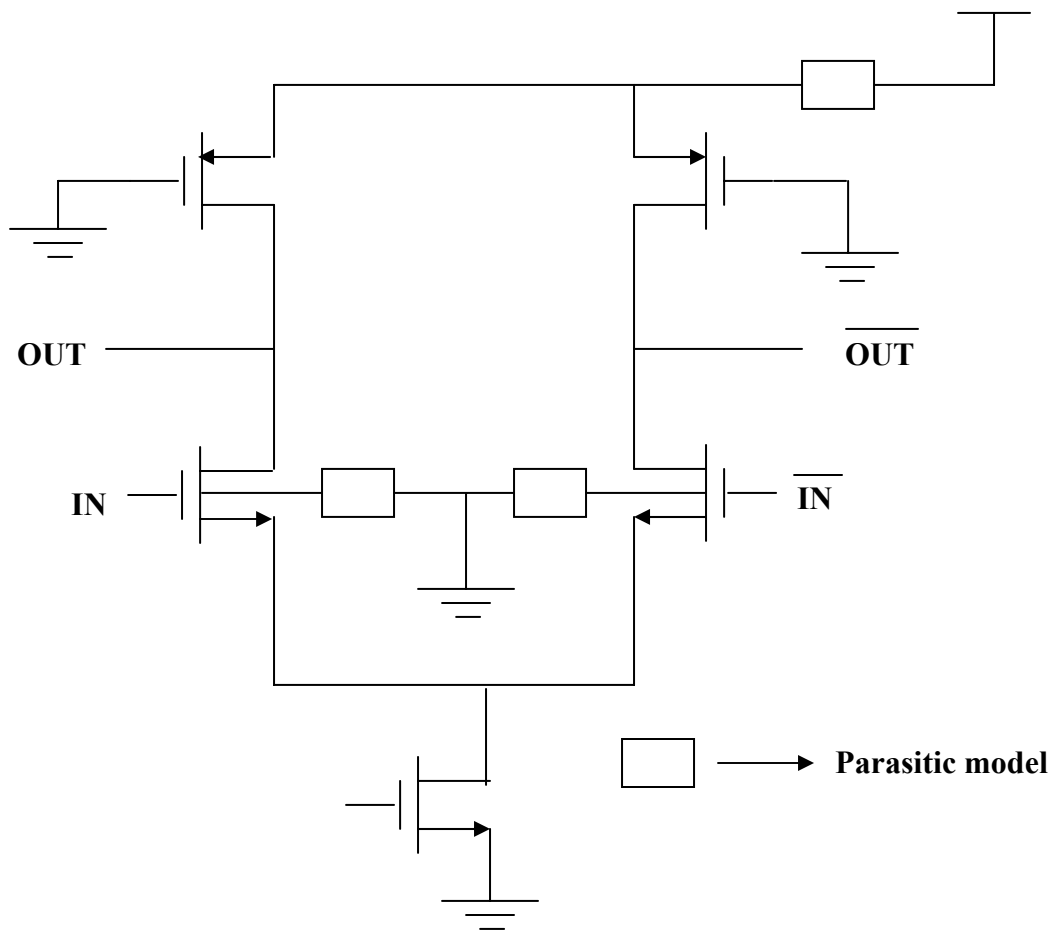


Figure 4.10. MCML Inverter showing the parasitics at power supply, ground and substrate

The output seen after introducing all the parasitics in the circuit is shown in Figure 4.11. From the output it can be concluded that the logic levels are not stable, i.e., fluctuations are seen at the logic levels. The zoomed in version of the output shows this effect clearly.

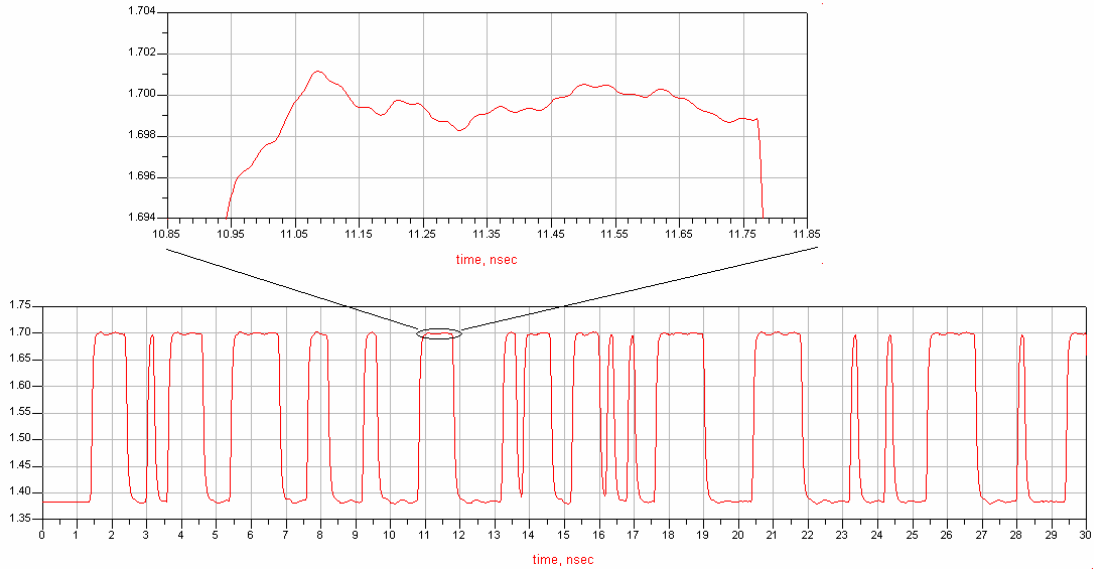


Figure 4.11. Output of the MCML inverter in the presence of parasitics

These types of variations are seen at the output because of the simultaneous switching noise problem. Whenever the inputs switch states there is variation of current at the power supply. When these variations of current pass through the parasitics inductor in the power supply or ground or substrate it creates a fluctuation of voltage. Now since the V<sub>dd</sub> or gnd neither have stable logic 1 or logic 0 voltage respectively, the variations are seen at the output. The noise amplitude at the logic level is 4 m V<sub>p-p</sub>.

#### 4.4 MCML XOR gate in the presence of parasitics

The developed parasitic model was then introduced into the power supply, ground and the substrate of each and every transistor of the XOR gate. The results obtained after introducing the parasitics model at the power supply, the ground and the substrate are shown in Figure 4.12.

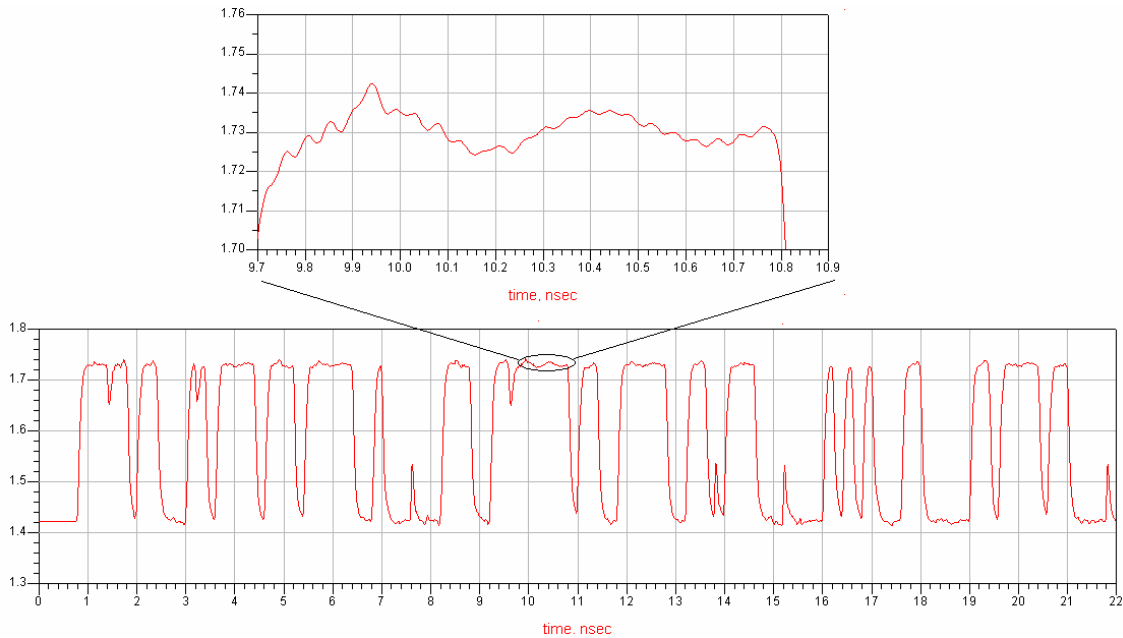


Figure 4.12. Output of the MCML XOR gate in the presence of parasitics

In the case of XOR gate too, the fluctuations at the output are seen. The switching of the inputs creates a current spike in the power supply lines. The inductor in the power supply lines then converts this current spike to a voltage spike which affects the output at the static logic levels. The noise amplitude here is  $20 \text{ mV}_{\text{p-p}}$ .

#### 4.5 MCML AND gate in the presence of parasitics

The parasitics model was finally introduced in the power supply, the ground and the substrate of the MCML AND gate. The resulting output is shown in Figure 4.13.

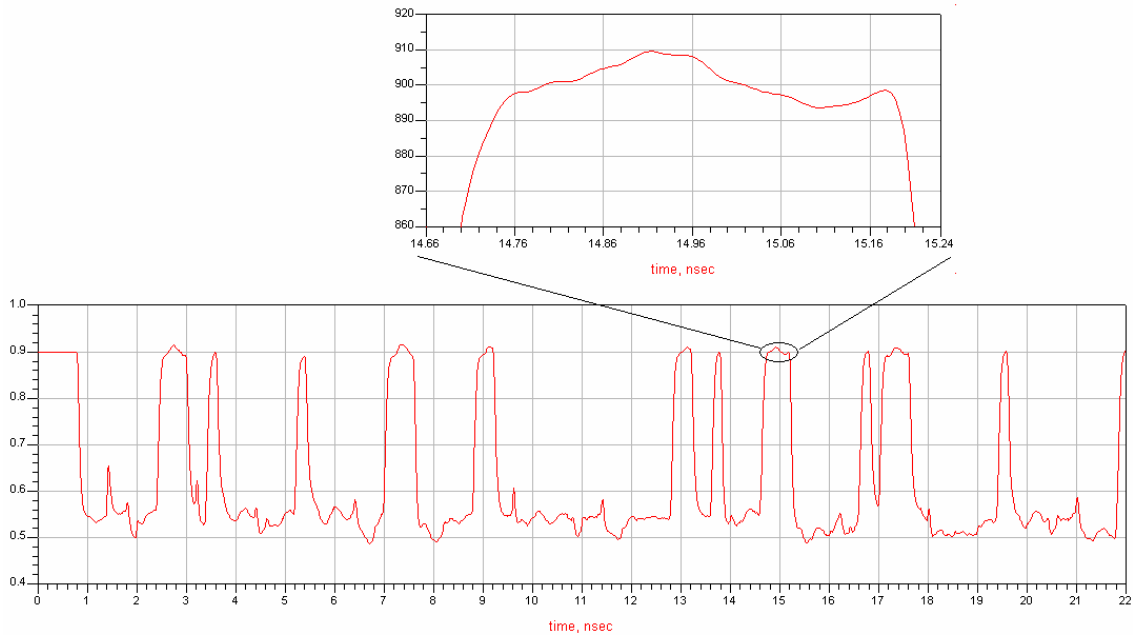


Figure 4.13. Output of the MCML AND gate in the presence of parasitics

The noise amplitude here is  $18 \text{ m } V_{p-p}$ . Thus it is seen that the parasitic model has introduced switching at the output logic levels. Effective methods need to be developed to minimize switching noise problem to improve the performance of the mixed signal environment circuits.

## CHAPTER 5

### PROPOSED METHOD TO IMPROVE MCML PERFORMANCE USING DELAY CELLS

The problem of current mismatch as discussed earlier can be reduced by using delay cells at the inputs of the MCML circuits. Addition of delay cell helps to reduce the current mismatch problem by adding a variable delay to the inputs in such a way that their current behaviour becomes similar. The general block diagram of the proposed method is shown below.

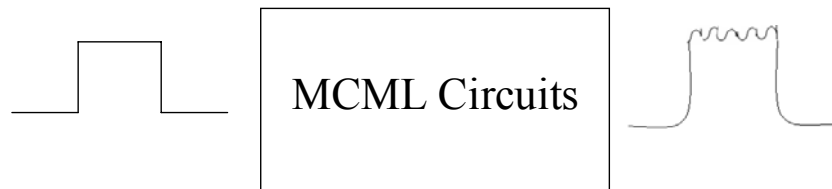


Figure 5.1. Block diagram showing the simultaneous switching noise problem in MCML circuits

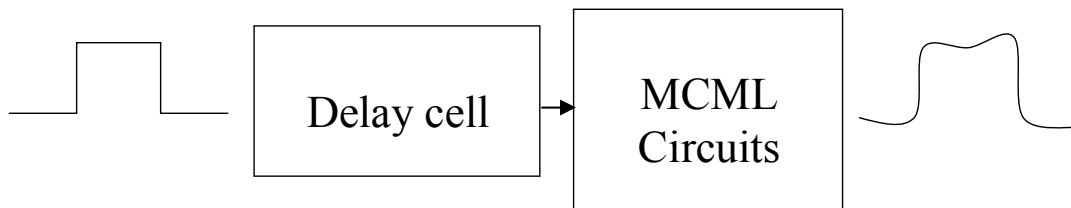


Figure 5.2. Block diagram showing the reduction in simultaneous switching noise problem in MCML circuits using delay cell

## 5.1 Delay Cell

### *5.1.1 Delay Cell Architecture*

The architecture used for designing the delay cell [21] is the interpolation type delay cell as shown in the Figure 5.3. The delay consists of a fast path and a slow path so that there is room to adjust the delay. The delays given by these paths are controlled by control voltages.  $V_{slow}$  and  $V_{fast}$  are the control voltages in the Figure 5.3. When  $V_{slow}$  is set to logic high voltage, only slow path is activated and the circuit gives the maximum delay since the input travels through the transistors M1, M2, M5, M6 and then to the output.. When  $V_{fast}$  is set to logic high voltage only fast path is activated and the circuit gives the least delay since the input travels only through the transistors M3, M4 and then to the output. Differential to single ended converter circuit is used at the end to convert the differential output of the delay to a single ended output. Current folding topology is used to maintain a constant current through the output load devices so that the output swing is always constant. Transistors M7, M8, CS4 and CS5 are used for this purpose. The gates of CS4 and CS5 are connected to the gates of CS3 and CS2 resembling a current mirror topology so that the sum of the current through them is always constant. The output of the delay cell is shown in the Figure 5.4. The graph of the achieved delay is shown in Figure 5.5.

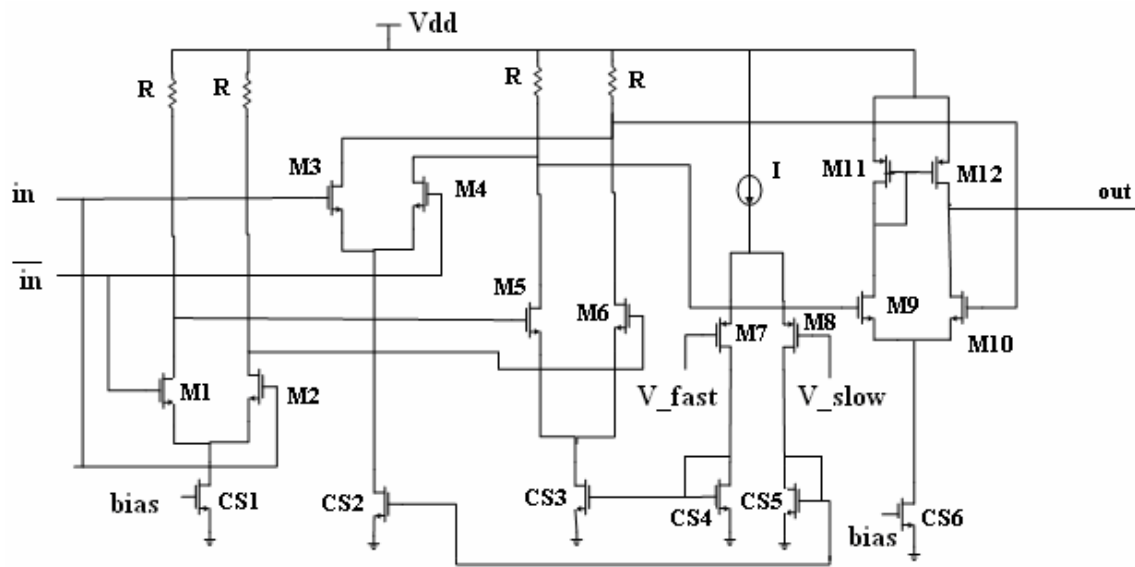


Figure 5.3. Architecture of interpolation type delay cell

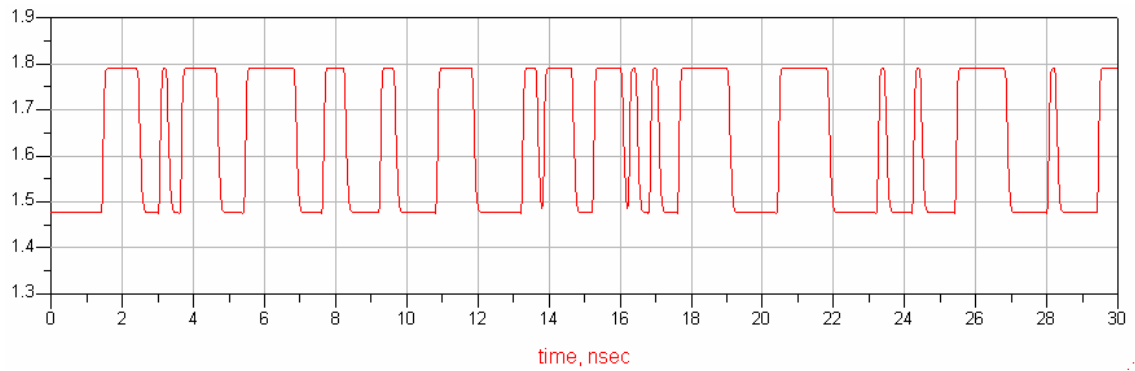


Figure 5.4. Output of the delay cell

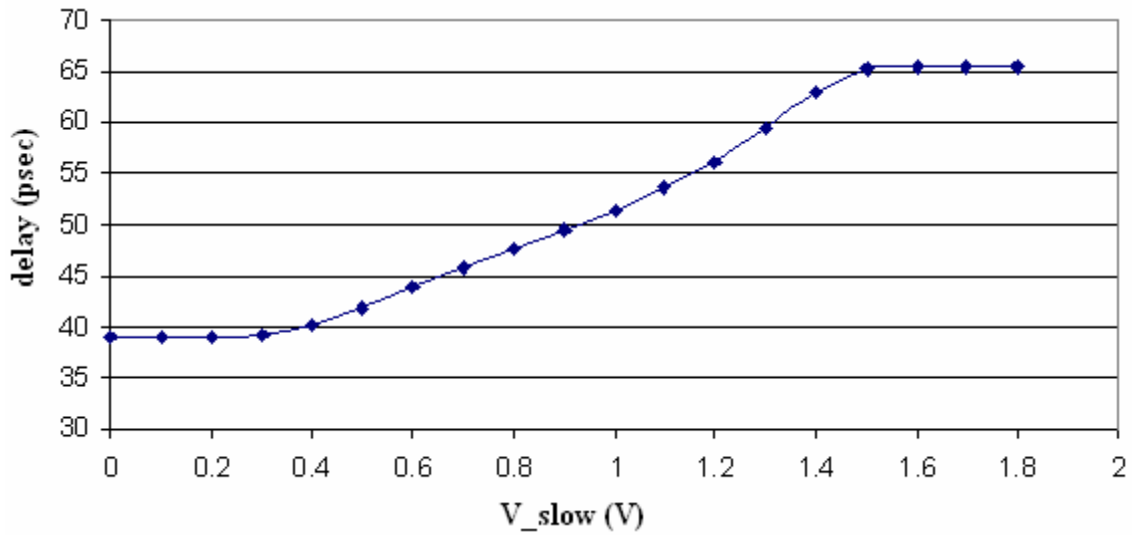


Figure 5.5. Delay versus control voltage for the delay cell

The delay cell thus designed is then introduced in MCML circuits designed so far to reduce the switching noise effect.

### 5.2 MCML inverter with parasitics and the delay cell

The figure below shows the output obtained after introducing the delay cell at the input of the MCML inverter. The output is seen to improve. The peak to peak variation of noise amplitude is reduced to 3 m V<sub>p-p</sub>. The distortion of noise is also reduced when compared to the results obtained without the delay cell.



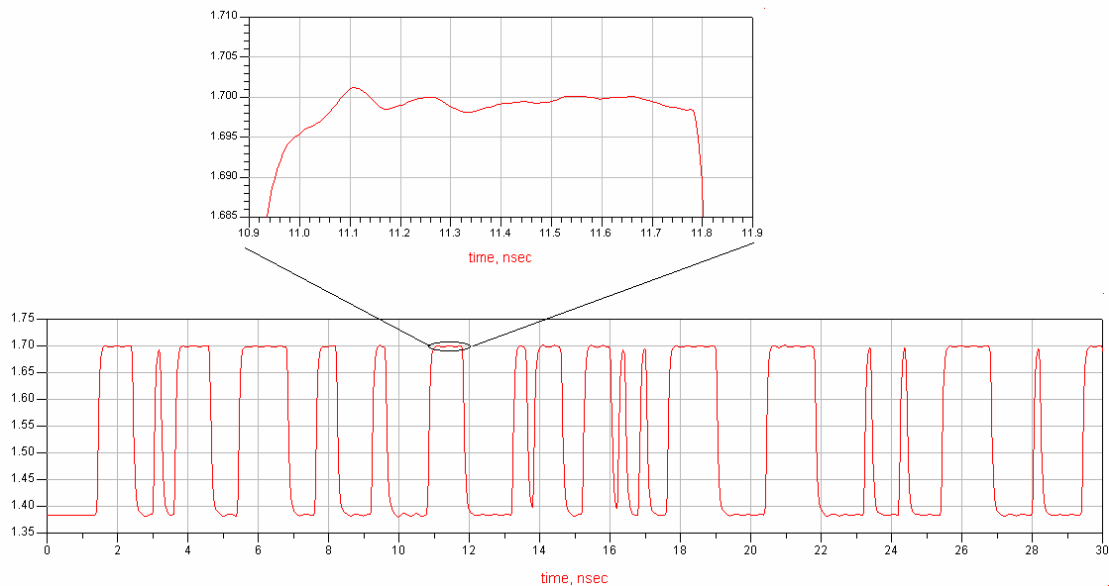


Figure 5.6. Improved performance of MCML inverter in the presence of parasitics using delay cells

### 5.3 MCML XOR gate with parasitics and the delay cell

Delay cell is then introduced at the input of the MCML XOR gate to see the amount of improvement it can provide. The Figure 5.5 shows the obtained output after introducing the delay cell. The peak to peak amplitude of noise is reduced to  $5 \text{ m V}_{p-p}$  from the original of  $20 \text{ m V}_{p-p}$ . Thus delay cell improved the performance of the XOR gate.

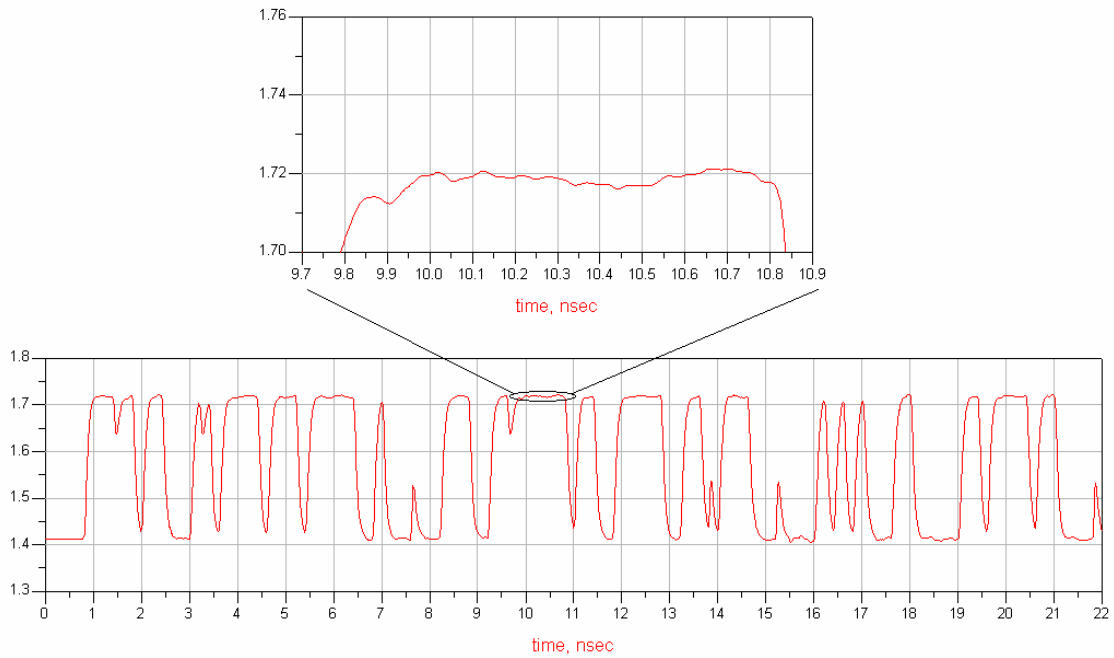


Figure 5.7. Improved performance of MCML XOR gate in the presence of parasitics using delay cells

#### 5.4 MCML AND gate with parasitics and the delay cell

Finally, the delay cell was introduced at the inputs of an MCML AND gate. The Figure 5.6 shows the resulting outputs. The peak to peak amplitude of the noise is reduced to 6 m  $V_{p-p}$  from the original value of 18 m  $V_{p-p}$ . Thus, delay cell proved to be beneficial for AND gate too.

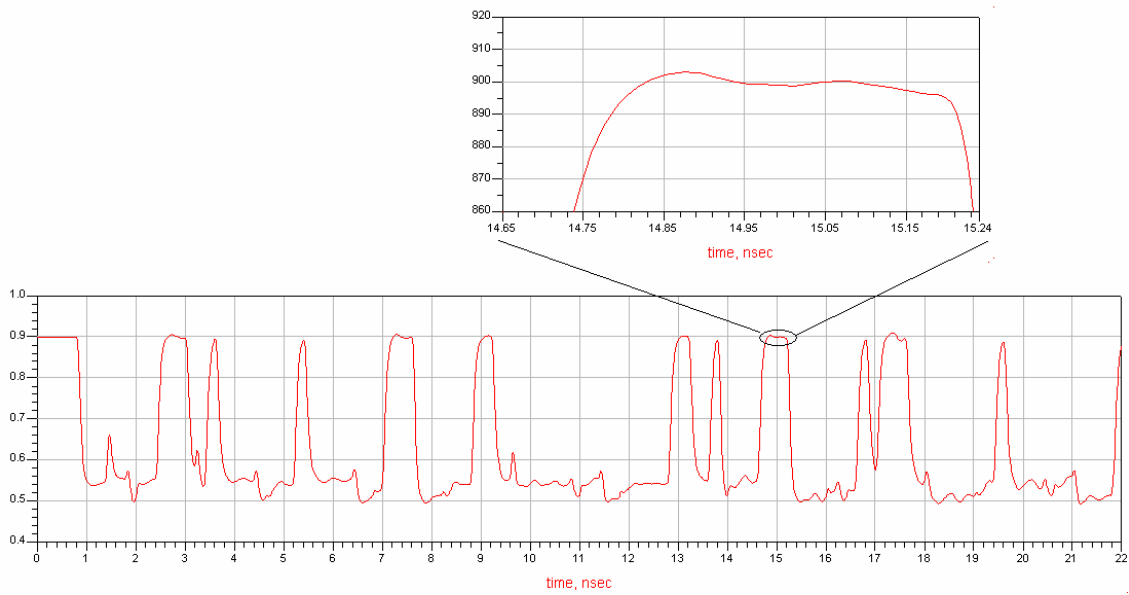


Figure 5.8. Improved performance of MCML AND gate in the presence of parasitics using delay cells

Table 5.1 Comparison in the noise amplitude of MCML circuits with and without the delay cell

MCML Circuit	Noise amplitude without the delay cell. ( $V_{p-p}$ )	Noise amplitude with the delay cell. ( $V_{p-p}$ )
Inverter	4 mV	3 mV
XOR	20 mV	5 mV
AND	18 mV	6 mV

## CHAPTER 6

### CONCLUSION

In the current work, we discussed the contribution of the MCML circuits to the mixed signal environment. The MCML circuits for basic logic gates were designed at 5 Gbps to study the detrimental effects of substrate noise in mixed signal environment. Parasitic models were introduced to illustrate the effects of these models on the MCML circuits. It was observed that introduction of parasitics at power supply; ground and substrate of the MCML circuits had adverse effects at the output. One of the causes, the current mismatch in the MCML circuits was studied. It was found that this current mismatch problem occurred because of Drain Induced Barrier Lowering (DIBL) effect in short channel devices. The analysis of the causes for this kind of behaviour propelled the introduction of proposed interpolation type delay cells. The delay cells at the input terminals have proven to be effective in minimizing the current mismatch which reduces the SSN as demonstrated by results. The performance of the MCML circuits was seen to have improved by after using the delay cells.

The proposed method has a drawback of increasing the design complexity of the MCML circuits. This is because of the increase in the total number of design transistors due to the delay. The increase in the number of the transistors adds to the increased power consumption of the circuit. This can be overcome by optimizing the design

blocks of Interpolation type delay cells. The proposed method provides a basic solution to minimize the SSN and with due course the method can be optimized.

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