DESIGN AND FUNCTIONALITY ANALYSIS OF OPERATIONAL AMPLIFIERS WITH RAIL-TO-RAIL INPUT AND OUTPUT CAPABILITY

by

MINGSHENG PENG

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Dedicated to My Family

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ABSTRACT

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The operational amplifier (op amp) is a fundamental building block in analog integrated circuit design. For low power-supply voltages, the common-mode input voltage and the output voltage of op amps are always required to be able to swing from the negative power-supply rail to the positive power-supply rail, i.e., rail-to-rail. In this dissertation, op amps with rail-to-rail input and output capability are investigated. This dissertation mainly focuses on the rail-to-rail input stage design. Two different rail-to-rail input stages with a single differential pair and a common-mode adapter are presented. The common-mode adapter is used to shift the common-mode input voltage. Two new common-mode adapters for the input stage with a single differential pair are developed. The first common-mode adapter is based on a pseudo-differential pair, and

the second one is based on current subtraction. Three bipolar and two CMOS op amps with rail-to-rail input and output capability are designed. The circuit simulation and chip test results are given in this dissertation. There are many aspects of performance for op amps. With different topologies, op amps may have different performance. One certain op amp may be good at some aspects but poor at others. The General System Performance Theory is a systematic method for system performance analysis. In order to get a single figure of merit, the General System Performance Theory is applied to compare the overall performance of the designed three different bipolar rail-to-rail op amps.

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CHAPTER 1

INTRODUCTION

The operational amplifier (op amp) was originally designed to perform mathematical operations like addition, subtraction, integration, and differentiation. However, the op amp has become one of the most versatile and important building blocks in analog integrated circuit design. It has numerous applications such as active filters, buffers, digital-to-analog converters, analog-to-digital converters, audio amplifiers, voltage regulator, and so on [1-7].

1.1 Background and Motivation

There is a trend toward lower power-supply voltage for integrated circuits [8]. Why low supply voltage? [4]. First, due to the scaling down, the integrated devices become smaller and smaller. A component with a smaller dimension is subjected to breakdown at a lower voltage, so it requires low supply voltage for device reliability. Second, it is due to the demand of battery-powered portable systems. For one single regular battery cell, the voltage is about 1.5 volts. The third reason is for low power consumption. For digital circuits, a low supply voltage always means low power consumption. It is not always true for analog circuits. Usually, in a system, the analog circuit is only a small part compared to the digital circuit part. Thus the lower supply voltage means the lower power consumption for the overall system.

With a lower supply voltage, the common-mode input range (CMIR) and the output voltage swing range of op amps are always reduced. In order to obtain a high signal-to-noise ratio and a large dynamic range, the output signal needs to be as large as possible [2]. The largest output signal swing is from the negative power-supply rail to the positive power-supply rail, i.e., rail-to-rail. This is true for either non-inverting gain amplifiers or inverting gain amplifiers.

Figure 1.1 shows an inverting gain amplifier configuration. Generally, the open-loop gain of an op amp is very high, so the voltages at the two input terminals are forced to have nearly the same value. This value or more precisely the average of the voltages at the two inputs is called the common-mode input voltage [9]. In this configuration, the non-inverting terminal is biased at a fixed voltage, so the requirement for the CMIR of the op amp in an inverting gain amplifier configuration is not high.

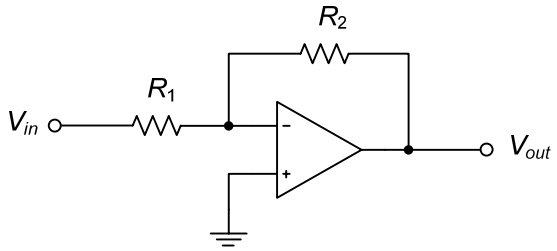

Figure 1.1 Inverting gain amplifier configuration.

Figure 1.2 shows a non-inverting gain amplifier configuration. The common-mode voltage at the input terminals of the op amp changes with the changing of the input signal voltage. If the input voltage swing is large, then requirement of the CMIR of the op amp in a non-inverting gain amplifier configuration is high.

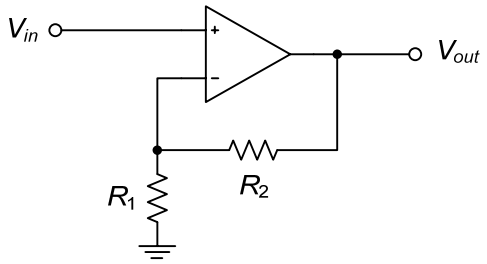

Figure 1.2 Non-inverting gain amplifier configuration.

For applications like a voltage buffer, the large common-mode input voltage range and output voltage swing are preferred. The best CMIR and output swing are from rail to rail. An output stage with a rail-to-rail swing is relatively easy to design with class-A or class-AB topology [10]. The key problem is to design a rail-to-rail input stage with constant transconductance over the CMIR.

For rail-to-rail op amps, there are many different kinds of input stages and output stages [3, 11-15]. For example, the rail-to-rail input stage can have complementary differential pairs or a single differential pair with a common-mode adapter. One topology may be good at some aspects of performance but poor at others. The question is "which op amp is the best in overall performance?" The General System Performance Theory (GSPT) [16-18] is a systematic method for system performance analysis. The GSPT can be used to compare the performance of op amps and obtain a single-valued figure of merit.

1.2 Organization of the Dissertation

This dissertation is divided into six chapters. Following this introduction, the design of rail-to-rail input stages is described in Chapter 2. Two types of rail-to-rail input stages are discussed. The first type of input stages use complementary differential

pairs, and the second type of input stages use a single differential pair with a common-mode adapter. In this chapter, a rail-to-rail bipolar complementary input stage with improved CMRR is presented, and two rail-to-rail input stages with a single differential pair and a common-mode adapter are designed. Two new common-mode adapters are developed. The first common-mode adapter is based on a pseudo-differential pair, and the second one is based on current subtraction.

Other circuit parts needed to complete the design of op amps are discussed in Chapter 3. It includes the output stage, the intermediate stage, and the output protection circuit. The frequency compensation for stability is also discussed in this chapter.

In Chapter 4, the overall operational amplifier circuits are discussed. Three different three-stage bipolar and two different two-stage CMOS rail-to-rail input and output op amps are designed. The simulation results and chip testing results are given in this chapter.

In Chapter 5, the General System Performance Theory is applied on the functionality analysis and comparison of the designed three bipolar rail-to-rail op amps.

Finally, the conclusion and future work are given in Chapter 6.

CHAPTER 2

INPUT STAGE

The task of the input stage of an op amp is to amplify the differential-mode input signals but to reject the common-mode input signals. One important specification of the input stage is the common-mode input range (CMIR). The CMIR is defined as the valid range of the common-mode input voltage that maintains the normal operation of the input stage. Other important specifications of an input stage are the input offset voltage, common-mode rejection ratio, and input referred noise. To some degree, the input stage also determines the gain-bandwidth product, phase margin, and slew rate [19].

In this chapter, rail-to-rail input stages are discussed. Section 2.1 describes differential pairs for input stages. Section 2.2 discusses rail-to-rail input stages with complimentary differential pairs. Section 2.3 discusses rail-to-rail input stages with a single differential pair and a common-mode adapter.

2.1 Differential Pair

The differential pair is commonly used in the input stage of op amps. It can be either an n-type or a p-type differential pair as shown in Figure 2.1 and Figure 2.2.

Figure 2.1(a) shows an npn bipolar differential pair. When the common-mode voltage is too high, both Q_1 and Q_2 go to the saturation region; when the common-mode

voltage is too low, Q_3 goes into the saturation region. The upper limit of the CMIR, $V_{CM(\max)}$, is the maximum common-mode input voltage to keep Q_1 and Q_2 in the forward active region. The condition to keep Q_1 and Q_2 in the forward active region can be expressed as

$$V_{CB} + V_{BE} = V_{CE} \geq V_{CE(\text{sat})} \Rightarrow V_{CB} \geq V_{CE(sat)} - V_{BE} \tag{2.1}$$

where $V_{CE(\text{sat})}$ is the saturation voltage for Q_1 and Q_2, which is the minimum collector-emitter voltage to keep Q_1 and Q_2 in the forward active region. Assuming that the voltage across R_1 or R_2 is $V_{R1,2}$, then

$$V_{CM(\max)} = V_{CC} + V_{BE} - V_{CE(\text{sat})} - V_{R1,2} \tag{2.2}$$

where V_{CC} is the positive power-supply voltage. With proper values of resistors R_1 and R_2, $V_{CM(\max)}$ can exceeds V_{CC} by $V_{BE} - V_{CE(\text{sat})} - V_{R1,2}$. The lower limit of the CMIR, $V_{CM(\min)}$, is the minimum input voltage to keep Q_1, Q_2, and Q_3 in the forward active region. So it must be V_{BE} of Q_1 and Q_2 plus $V_{CE(\text{sat})}$ of Q_3 above the negative power-power supply voltage, V_{EE}. It can be express as

$$V_{CM(\min)} = V_{EE} + V_{BE} + V_{CE(\text{sat})} \tag{2.3}$$

From (2.2) and (2.3), the CMIR of the npn differential pair can be represented as

$$V_{EE} + V_{BE} + V_{CE(\text{sat})} \leq V_{CM} \leq V_{CC} + V_{BE} - V_{CE(\text{sat})} - V_{R1,2} \tag{2.4}$$

Figure 2.1(b) shows a pnp bipolar differential pair. Similarly, the CMIR can be represented as

$$V_{EE} - V_{BE} + V_{CE(\text{sat})} + V_{R1,2} \leq V_{CM} \leq V_{CC} - V_{BE} - V_{CE(\text{sat})} \tag{2.5}$$

The common-mode input voltage cannot reach V_{CC}. The lower limit of the common-mode voltage can exceed V_{EE} by $V_{BE} - V_{CE(\text{sat})} - V_{R1,2}$.

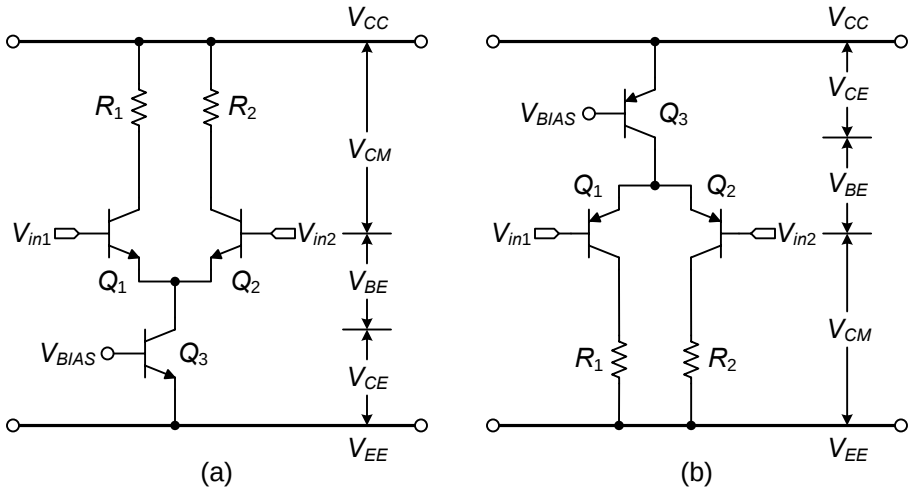

Figure 2.1 Common-mode input voltage range for (a) an npn differential pair and (b) a pnp differential pair.

CMOS differential pairs are shown in Figure 2.2. The CMIR for CMOS differential pairs are similar to the bipolar counterparts. For the NMOS differential pair in Figure 2.2(a), the CMIR is given by

$$V_{SS} + V_{GS} + V_{DS(\text{sat})} < V_{CM} < V_{DD} + V_{TH} - V_{R1,2} \tag{2.6}$$

where V_{TH} is the threshold voltage of the MOS transistor, and $V_{DS(\text{sat})}$ is the saturation voltage. For the PMOS differential pair shown in Figure 2.2(b), the CMIR is given by

$$V_{SS} - V_{TH} + V_{R1,2} < V_{CM} < V_{DD} - V_{GS} - V_{DS(\text{sat})} \tag{2.7}$$

In Figure 2.1 and Figure 2.2, the loads for the differential pair are resistors. They could be active loads [20]. For the active load case, the CMIR of the differential pair is similar.

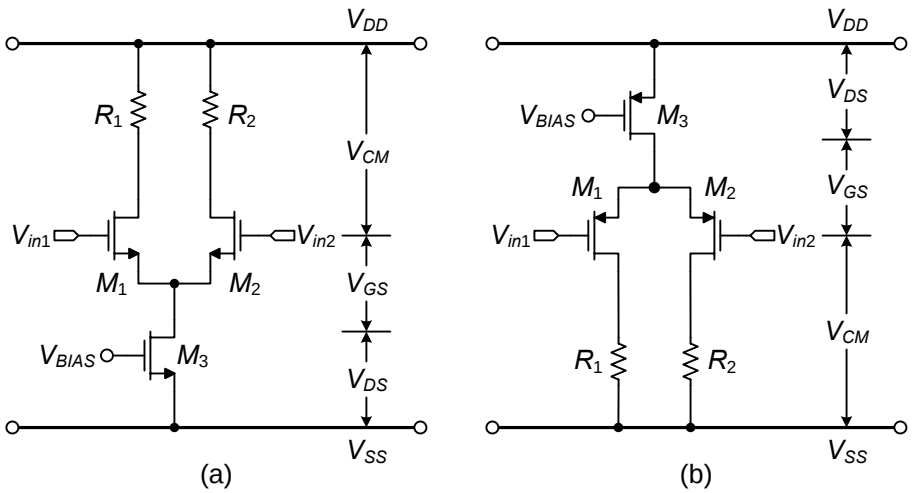

Figure 2.2 Common-mode input voltage range for (a) an NMOS differential pair and (b) a PMOS differential pair.

2.2 Rail-to-Rail Input Stage with Complementary Differential Pairs

As shown in previous section, for a single differential pair, the common-mode input voltage cannot be rail-to-rail. One popular way to implement a rail-to-rail input stage is to use complementary differential pairs by placing a p-type differential pair and an n-type pair in parallel [3, 11], which is shown in Figure 2.3 and Figure 2.4.

2.2.1 Simple Complementary Input Stage

By placing an n-type differential pair and a p-type differential pair in parallel [3, 11], when common-mode voltage is high, the n-type pair conducts, and when common-mode voltage is low, p-type pair conducts.

Figure 2.3 shows a bipolar rail-to-rail complementary input stage; Figure 2.4 shows a CMOS rail-to-rail complementary input stage. In Figure 2.3 and Figure 2.4, the right-hand part is the current summing circuit [11]. The folded cascode transistors sum

the n-type and p-type differential pair currents into one output current. V_{BIAS} provides a bias voltage for Q_5 and Q_6.

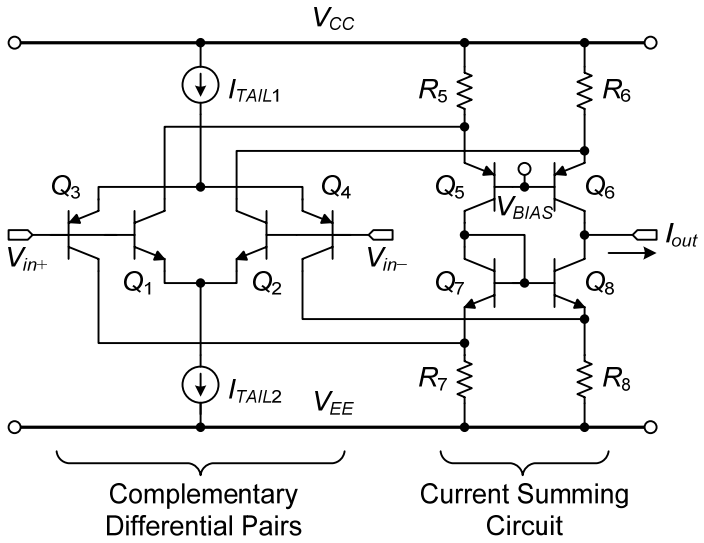

Figure 2.3 Bipolar rail-to-rail complementary input stage.

For the circuit in Figure 2.3, in order to obtain a rail-to-rail common-mode input range, at least one of the differential pairs should conduct for any common-mode input voltage. To avoid a forbidden voltage range in the middle between the negative and positive power-supply rails, the supply voltage should have a minimum value [3, 21] of

$$V_{SUP(\min)} = 2V_{BE} + 2V_{CE(\text{sat})} \tag{2.8}$$

For the CMOS rail-to-rail input stage with complementary differential pairs as shown in Figure 2.4, the minimum supply voltage is

$$V_{SUP(\min)} = 2V_{GS} + 2V_{DS(\text{sat})} \tag{2.9}$$

A drawback of the simple complementary input stage in Figure 2.3 or Figure 2.4 is that the transconductance, G_m, varies as the common-mode input voltage changes. In

Chapter 3, it will be shown that the non-constant-G_m input stage impedes an optimal frequency compensation and introduces distortion [11, 22, 23].

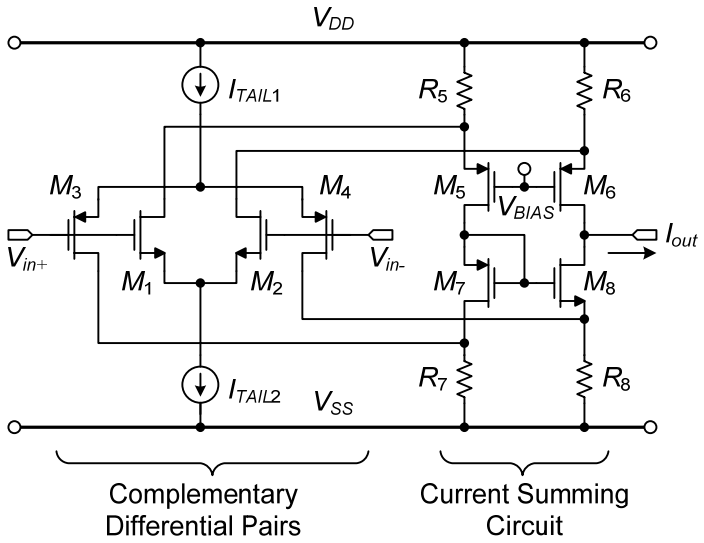

Figure 2.4 CMOS rail-to-rail complementary input stage.

Figure 2.5 shows the simulation result of the normalized tail current for the npn and pnp pairs over the common-mode input range of the input stage in Figure 2.3. The bipolar transistor SPICE models [24] for the simulation are given in Appendix A. Because the current through the differential pairs and the total transconductance of the input stage is a function of I_{TAIL1} and I_{TAIL2}, the simulated results are normalized [25]. Figure 2.5 shows when the V_{CM} is low, the pnp pair is on, the npn pair is off, and the tail current through the npn pair is zero; when the V_{CM} is high, the npn pair is on, the pnp pair is off, and the tail current through the pnp pair is zero; when V_{CM} is in the middle of the power-supply rails, both npn and pnp pairs are on, and the transconductance of the input stage doubles in this range, which is shown in Figure 2.6.

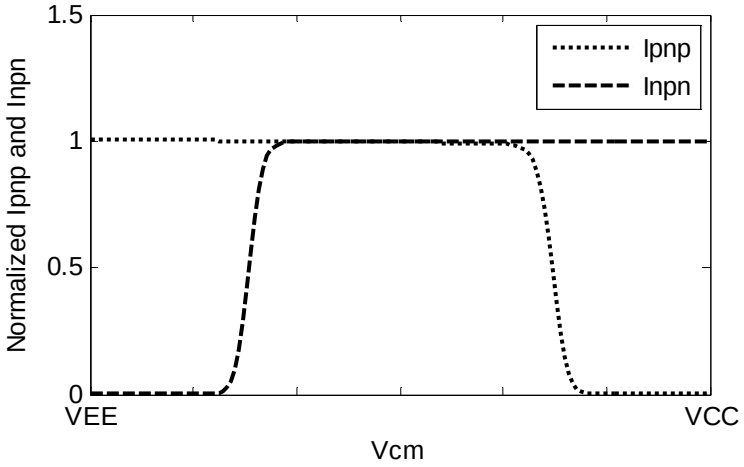

Figure 2.5 Normalized tail current versus the common-mode input voltage for pnp and npn pairs in the input stage of Figure 2.3.

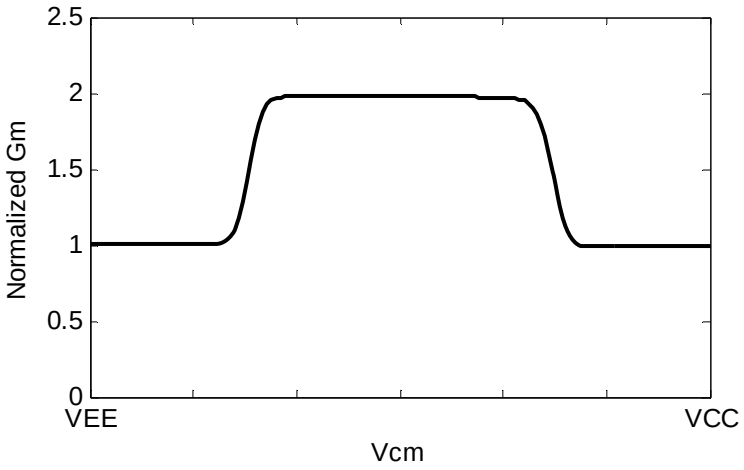

Figure 2.6 Normalized transconductance versus the common-mode input voltage for the input stage of Figure 2.3.

2.2.2 Constant-G_m Complementary Input Stage

In the saturation region, the transconductance of a MOS transistor is proportional to the square root of the drain current. It can be expressed as

$$g_m = \sqrt{2k'\left(\frac{W}{L}\right)I_D} \tag{2.10}$$

where k' is the transconductance parameters [20] for the MOS transistor, which equals the product of the carrier mobility and the oxide capacitance density; W/L is the channel width to length ratio; I_D is the drain current.

The constant transconductance of a CMOS complementary input stage is realized by developing a bias circuit, which produces the tail current I_n for the NMOS pair and the tail current I_p for the PMOS pair, so that the total transconductance is constant over the entire common-mode input range. It can be expressed as

$$\sqrt{2k_n'\left(\frac{W}{L}\right)_n I_n} + \sqrt{2k_p'\left(\frac{W}{L}\right)_p I_p} = \text{constant} \tag{2.11}$$

where k'_n and k'_p are the transconductance parameters for the NMOS and PMOS transistors, respectively; $(W/L)_n$ and $(W/L)_p$ are the channel width to length ratios for the NMOS and PMOS transistors, respectively.

There are many ways to implement CMOS rail-to-rail constant-G_m complementary input stages [10, 12, 21, 25-30]. In this section, bipolar rail-to-rail constant-G_m complementary input stages will be discussed in detail. For the bipolar technology, the transconductance of a transistor is proportional to the collector current [20], which can be described as

$$g_m = \frac{I_C}{V_T} \tag{2.12}$$

where I_C is the collector current, and V_T is the thermal voltage. A bipolar constant-G_m complementary input stage can be realized by keeping the sum of the tail current

through the npn pair, I_{npn}, and the tail current through the pnp pair , I_{pnp}, constant. It can be expressed as

$$I_{npn} + I_{pnp} = \text{constant} \tag{2.13}$$

A realization of a bipolar constant-G_m complementary input stage is shown in Figure 2.7 [11]. V_{REF} is used to set the base voltage of Q_{12}, V_{B12}, i.e., to set the base voltage of Q_{12} at $V_{EE} + V_{REF}$. The npn differential pair, Q_1 and Q_2, is normally activated by the current source I_{TAIL} via Q_{12} and the current mirror, Q_{13} and Q_{14}, while the pnp differential pair is not operating. When V_{CM} decreases through V_{B12}, the emitter current is gradually steered from the emitter of Q_{12} to the pnp pair, Q_3 and Q_4, removing current from the npn pair. A turn over between 10 to 90 percent of the current takes place in a voltage turnover range of about 120 mV [11], centered at V_{B12}. The total current through the npn and pnp differential pairs is I_{TAIL}. Since the total current is constant, the transconductance of the combination of the pnp and npn differential pairs is constant.

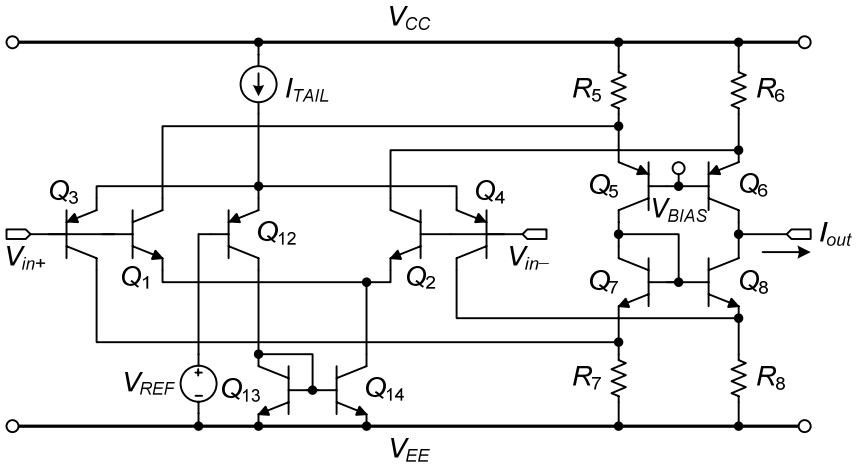

Figure 2.7 Rail-to-rail constant-G_m complementary input stage.

Figure 2.8 shows the simulation results of the normalized tail current of the npn and pnp pairs. When V_{CM} is a little bit smaller than base voltage of Q_{12}, V_{B12}, the pnp pair conducts, and the npn pair is off; when the V_{CM} is a little bit greater than V_{B12}, the npn pair conducts, and the pnp pair is off. The normalized transconductance of the whole input stage is shown in Figure 2.9. The transconductance is almost constant over the common-mode input voltage range.

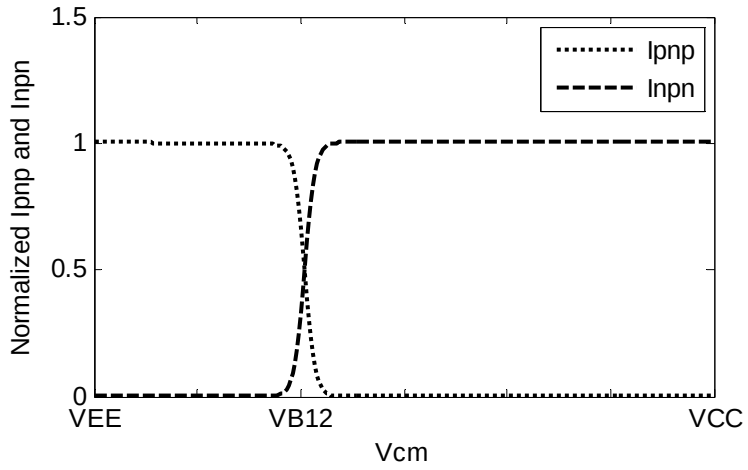

Figure 2.8 Normalized tail current versus the common-mode input voltage for pnp and npn pairs in the input stage of Figure 2.7.

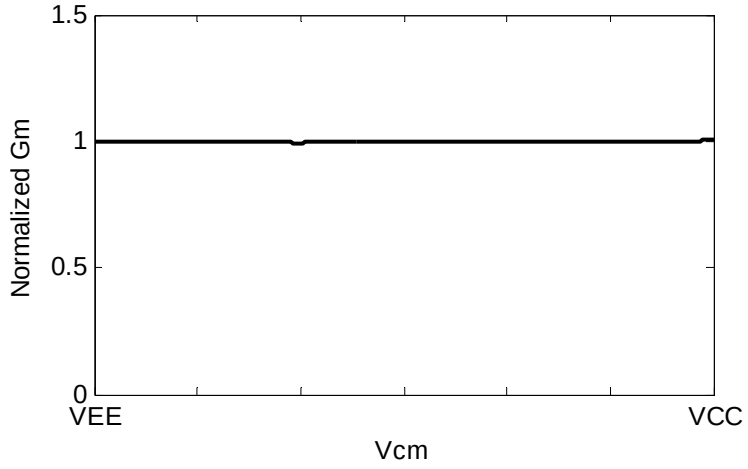

Figure 2.9 Normalized transconductance versus the common-mode input voltage for the input stage of Figure 2.7.

One disadvantage of this kind of input stage is that the offset voltage may vary for different common-mode input voltages, and this causes a low common-mode rejection ratio (CMRR) [31]. When the npn differential pair conducts, the offset voltage is shown to be [4]

$$V_{OS(\text{npn})} = V_T \cdot \left(2\frac{\Delta R_{5,6}}{R_{5,6}} + \frac{\Delta R_{7,8}}{R_{7,8}} + \frac{\Delta I_{S1,2}}{I_{S1,2}} \right) \tag{2.14}$$

where $\Delta R_{5,6}$ and $R_{5,6}$ are the difference and average of R_5 and R_6, respectively; $\Delta R_{7,8}$ and $R_{7,8}$ are the difference and the average of R_7 and R_8, respectively; $\Delta I_{S1,2}$ and $I_{S1,2}$ are the difference and the average of the saturation current of Q_1 and Q_2. Similarly, when the pnp differential pair conducts, the offset voltage is shown to be [4]

$$V_{OS(\text{pnp})} = V_T \cdot \left(\frac{\Delta R_{5,6}}{R_{5,6}} + 2\frac{\Delta R_{7,8}}{R_{7,8}} + \frac{\Delta I_{S3,4}}{I_{S3,4}} \right) \tag{2.15}$$

where $\Delta I_{S3,4}$ and $I_{S3,4}$ are the difference and the average of the saturation current of Q_3 and Q_4.

The CMRR is defined as the ratio of the differential-mode gain to the common-mode gain. From an application point of view, the CMRR can be considered as the change in the input offset voltage results from the change in the common-mode input voltage [20]. It can be expressed as

$$CMRR = \left(\frac{\Delta V_{OS}}{\Delta V_{CM}} \right)^{-1} \tag{2.16}$$

In the case of perfect match, the offset voltage and the variation of the offset voltages are very small over the common-mode voltage range. According to (2.16), the CMRR is

very high. In reality, the component mismatch is a statistical process, and the offset voltages may be different when the different pair conducts.

Figure 2.10 shows the simulated offset voltage over the common-mode input voltage range for the op amp of UTA242, which uses the input stage in Figure 2.7. The details of UTA242 will be discussed in Section 4.1. A 2% emitter error mismatch between the transistors of the differential pairs is assumed. When the pnp pair is on, the offset voltage is about 0.5 mV; when the npn pair is on, the offset voltage is about -0.5 mV.

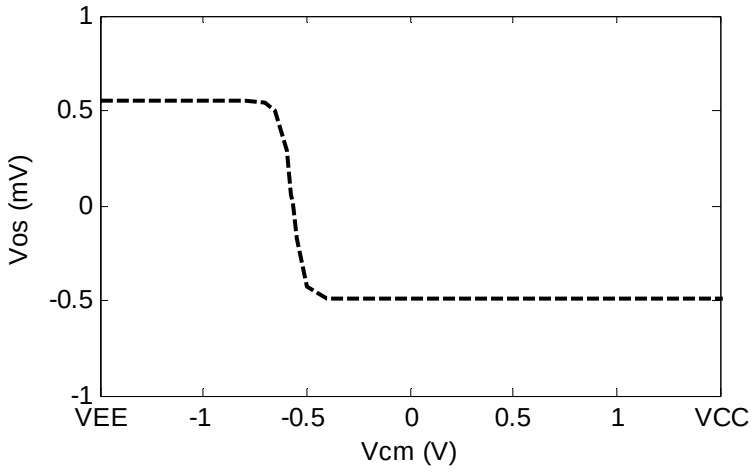

Figure 2.10 Offset voltage versus the common-mode input voltage.

The simulated CMRR over the common-mode voltage range is shown in Figure 2.11. From this figure, it can be seen that the CMRR is very poor at the transition range between the pnp and npn pairs. The minimum value of the CMRR is about 40 dB which is at around the V_{REF} above V_{EE}. The poor CMRR dues to the short transition range and the large offset voltage difference between the pnp and npn pairs.

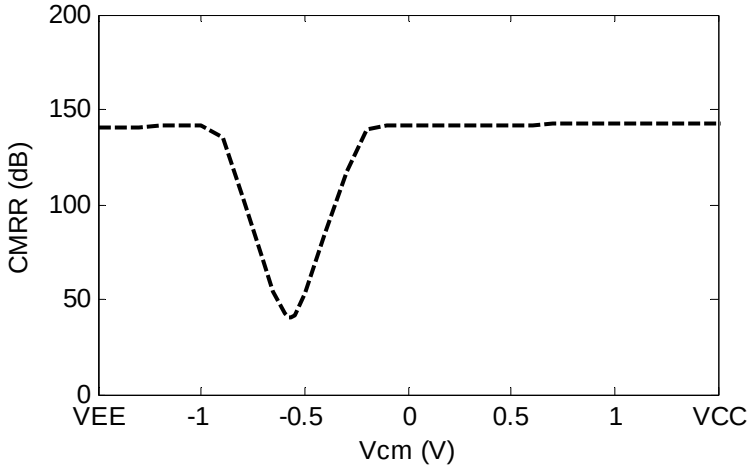

Figure 2.11 CMRR versus the common-mode input voltage.

2.2.3 Constant-G_m Complementary Input Stage with Improved CMRR

As mentioned in previous subsection, for a complementary input stage, the CMRR is poor in the transition region between the pnp and npn differential pairs. One solution to improve the CMRR is to increase the transition range [32-34]. Figure 2.12 shows a bipolar input stage with improved CMRR. The difference from the input stage in Figure 2.3 is that Q_{12} is diode connected, and a resistor R_1 is inserted between Q_{12} and Q_{13}. Resistor R_1 and transistor Q_{12} pull a current almost proportional to the common-mode input voltage and hence distribute I_{TAIL} over the two differential pairs. When the common-mode input voltage changes, the tail current of one pair gradually increases, and the tail current of the other differential pair gradually decreases. So it increase the transition region between the pnp pair to the npn pair. The offset voltage changes progressively, which improves the CMRR according to (2.16).

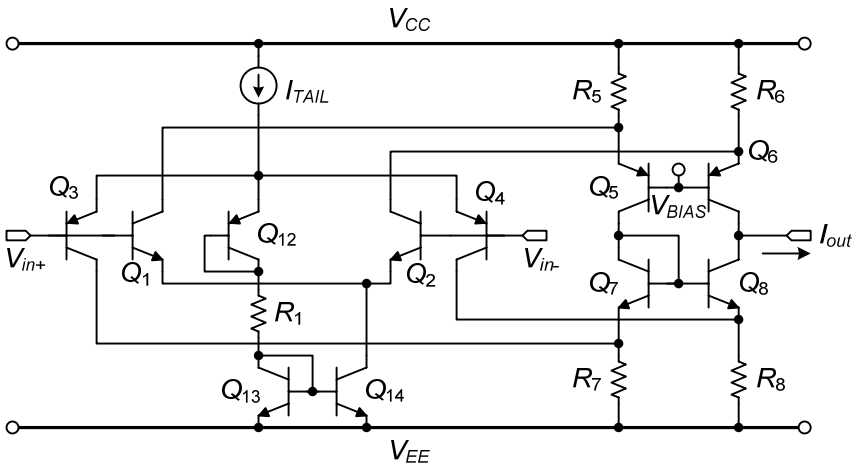

Figure 2.12 Rail-to-rail constant-G_m complementary input stage with improved CMRR.

The simulated normalized tail current of the npn and pnp pairs is shown in Figure 2.13. It can be seen that the transition region between the pnp and npn pairs is increased compared to the results in Figure 2.8. The size of the transition range is determined by the value of the resistor R_1.

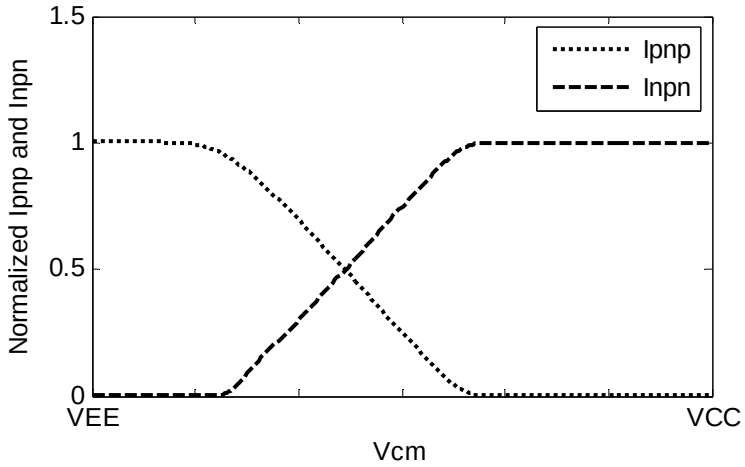

Figure 2.13 Normalized tail current versus the common-mode input voltage for pnp and npn pairs in the input stage of Figure 2.12.

The simulation result of the normalized transconductance of the whole input stage is shown in Figure 2.14. The transconductance is almost constant over the common-mode input voltage range. There is a small variation when transition is made between the npn and pnp pairs.

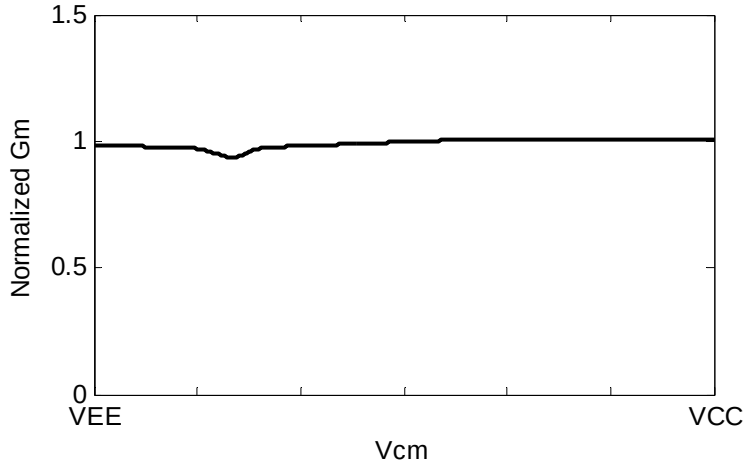

Figure 2.14 Normalized transconductance versus the common-mode input voltage for the input stage of Figure 2.12.

Figure 2.15 shows the simulated offset voltage over the common-mode voltage range for the op amp of UTA243, which uses the input stage in Figure 2.12. UTA243 will be discussed in Section 4.2. As in the previous section, a 2% emitter area mismatch between the transistors of the differential pair is assumed. The simulated CMRR over the common-mode input voltage range is shown in Figure 2.16. Figure 2.16 shows the minimum CMRR is about 60 dB, which is about 20 dB higher than the result of the input stage in Figure 2.7.

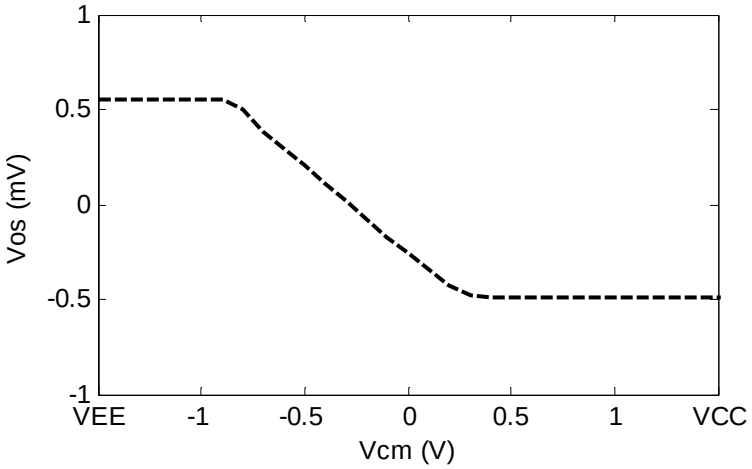

Figure 2.15 Offset voltage versus the common-mode input voltage.

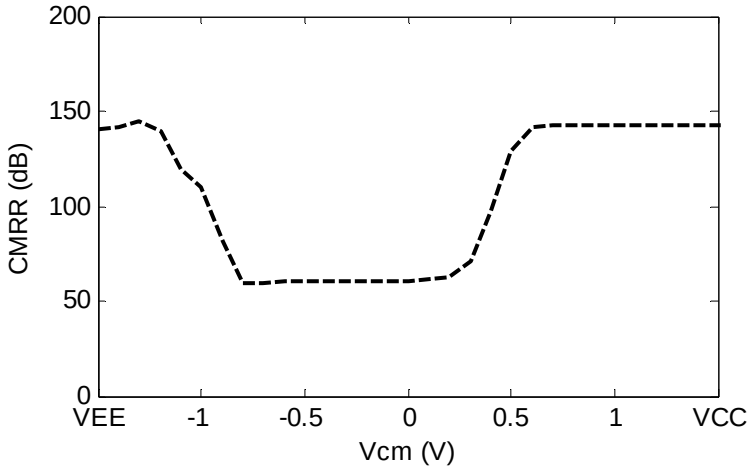

Figure 2.16 CMRR versus the common-mode input voltage.

2.3 Rail-to-Rail Input Stage with a Single Differential Pair

For a CMOS complementary input stage, the required minimum supply voltage is $2V_{GS} + 2V_{DS(\text{sat})}$, and for the bipolar counterpart, it is $2V_{BE} + 2V_{CE(\text{sat})}$. When the supply voltage is less than the minimum voltage, there is a forbidden common-mode region [35], in which both n-type and p-type differential pairs are off.

For a CMOS complementary input stage, to obtain a constant transconductance over the common-mode input voltage range, the NMOS and PMOS transistors should be matched, which can be expressed as

$$k_n'\left(\frac{W}{L}\right)_n = k_p'\left(\frac{W}{L}\right)_p \tag{2.17}$$

The matching can be achieved by sizing the NMOS and PMOS transistors properly [23] with the knowledge of k'_n/k'_p ratio. In general, the values of k'_n/k'_p ratio are different for different processes. Even for the same process, the ratio can change significantly from run to run [23]. Figure 2.17 shows the histogram of the k'_n/k'_p ratio for TSMC 0.18 μm CMOS technology [36]. It can be seen that the variation of k'_n/k'_p ratio is about 10%.

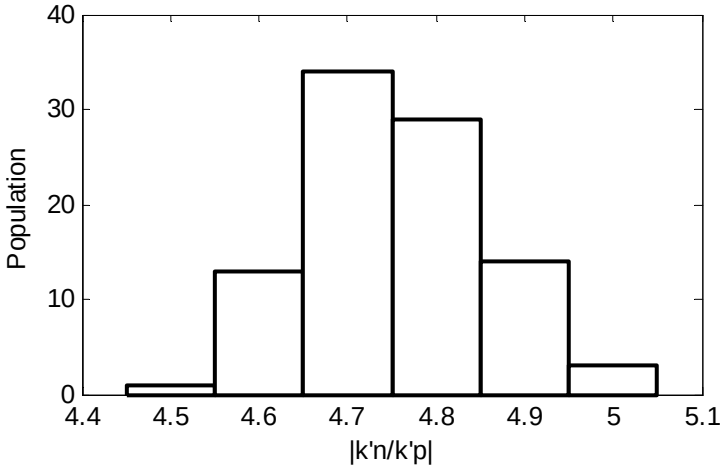

Figure 2.17 Histogram of the k'_n/k'_p ratio for TSMC 0.18 μm CMOS technology.

If only a single differential pair is used, the required minimum supply voltage is about $V_{GS} + 2V_{DS(\text{sat})}$, which is one V_{GS} less than that of a complementary input stage. As long as the tail current through the differential pair does not change, the transconductance is constant over the common-mode input range.

For a conventional differential pair, as seen from Section 2.1, the common-mode input voltage range cannot be rail-to-rail. Some solutions have been proposed. A bulk-driven CMOS differential pair was proposed [14, 37]. The disadvantage of the bulk-driven CMOS differential pair is the small transconductance and poor high frequency response. In [38], a floating gate transistor input stage was proposed. The floating-gate transistor needs special process steps [39], which is costly. In [40], a local charge pump was designed to provide a higher local supply voltage for the input differential pair. Recently, common-mode adapters were proposed to extend the common-mode input range [13, 41, 42].

In this section, the operation of the common-mode adapter is described. Then two new input stages with common-mode adapters are introduced. The first common-mode adapter is based on a pseudo-differential pair, and the second one is based on current subtraction.

2.3.1 Common-Mode Adapter

For an op amp with a PMOS differential pair input stage, the common-mode voltage cannot be near the positive power supply rail. Otherwise the tail current source transistor goes into the triode region. In order to solve this problem, a common-mode voltage adapter can be used. A two-stage op amp with a common-mode adapter [13] is shown in Figure 2.18. The common-mode adapter is placed in front of the input differential pair. The adapter circuit shifts the common-mode signal voltage, and keeps the differential-mode signal voltage unchanged.

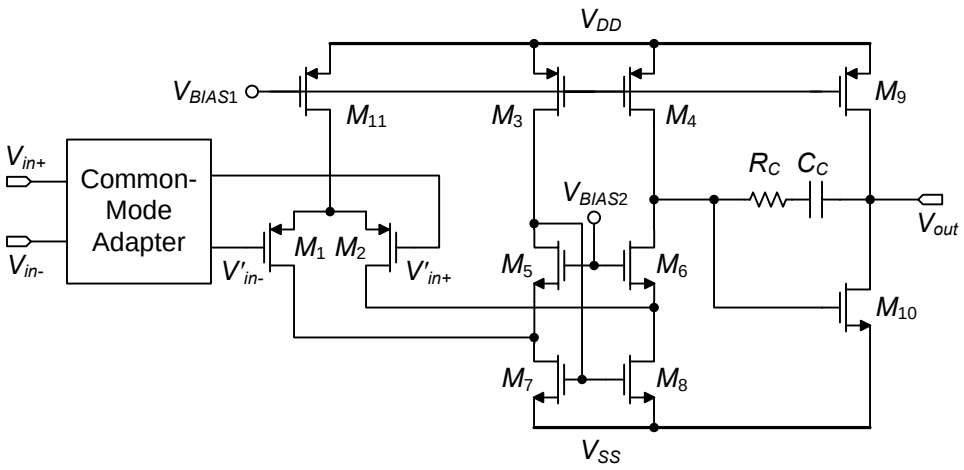

Figure 2.18 Two-stage op amp with a common-mode adapter.

According to (2.7), the common-mode voltage at the gates of the differential pair M_1 and M_2, V'_{CM}, should be at least $V_{GS}+V_{DS(\text{sat})}$ below V_{DD}. The common-mode adapter is used to shift the common-mode input voltage to a lower value when the input common-mode input voltage, V_{CM}, is too high.

Figure 2.19 illustrates the operation of a common-mode adapter. The common-mode adapter is implemented by inserting level-shift resistors between the input terminals, which are labeled as V_{in+} and V_{in-}, and the gates of the differential pair of M_1 and M_2, which are labeled as V'_{in+} and V'_{in-}, respectively. The current through the level-shift resistors is controlled by level-shift current sources, I_{LS}, which is a function of V_{CM}. I_{LS} should have the shape as in Figure 2.19.

From the common-mode adapter circuit in Figure 2.19, the relationship between the corresponding input voltages can be expressed as

$$V'_{in+} = V_{in+} - R_{LS}I_{LS} \tag{2.18}$$

$$V'_{in-} = V_{in-} - R_{LS}I_{LS} \tag{2.19}$$

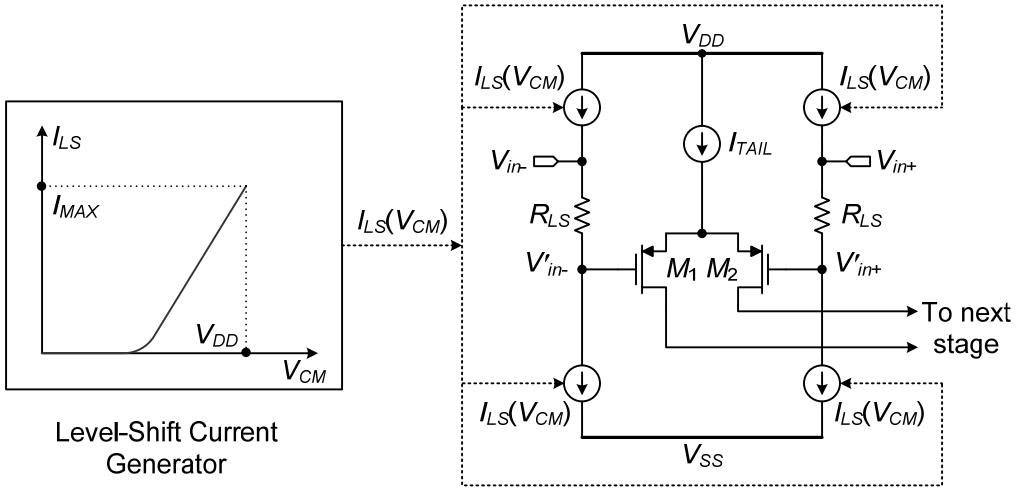

Figure 2.19 Diagram of the operation of a common-mode adapter.

If the components are perfect matched, the differential-mode signal is unchanged, and the common-mode voltage is shifted to a lower value, which can be described by

$$V'_{CM} = \left(V'_{in+} + V'_{in-}\right)/2 = V_{CM} - R_{LS} I_{LS} \tag{2.20}$$

$$V'_{dm} = V'_{in+} + V'_{in-} = V_{dm} \tag{2.21}$$

where V_{CM} and V_{dm} are the common-mode voltage and differential-mode voltage at the input terminals, respectively; V'_{CM} and V'_{dm} are the common-mode voltage and differential-mode at the gates of the differential pair, respectively; R_{LS} is value of the level-shift resistors; I_{LS} is the level-shift current, which is a function of V_{CM}.

For the PMOS differential pair in Figure 2.19, when V_{CM} is lower than $V_{DD} - V_{GS} - V_{DS(\text{sat})}$, it is low enough for the PMOS differential pair to work even without a common-mode adapter. In this range, the common-mode adapter is not active, and almost no current goes through the level-shift resistors. When V_{CM} is higher than

$V_{DD} - V_{GS} - V_{DS(\text{sat})}$, the adapter circuit starts to be active, and the current I_{LS} starts to go through the level-shift resistors. If V_{CM} increases more, then more current goes through the level-shift resistors. It reaches the highest level-shift current I_{MAX} when V_{CM} is near the positive power supply rail. So the maximum common-mode voltage can be shifted is $R_{LS} \cdot I_{MAX}$. This value should be equal or greater than $V_{GS} + V_{DS(\text{sat})}$.

For an ideal case, there is no mismatch between components, so the offset voltage is low, and the CMRR is high. For a practical case, a mismatch exists in the current sources or level-shift resistors between the left and the right branches. The extra offset voltage of $\Delta(R_{LS} I_{LS})$ is introduced. Because I_{LS} is a strong function of the common-mode input voltage, according to (2.16), the CMRR may be very low when the adapter circuit is active. Another drawback of this input stage with adapter circuit is that the level-shift resisters introduce extra noise. The value R_{LS} and I_{MAX} must be chosen as the best tradeoff among the noise, die area, and power consumption.

In [13] and [42], the authors proposed two common-mode adapters based on common-mode feedback. With the feedback loop, it could cause stability problems. In this section, two new common-mode adapters for single differential pair input stages are presented. The first one is based on a pseudo-differential pair, and the second one is based on current subtraction.

2.3.2 Input Stage with a Common-Mode Adapter Based on a Pseudo-Differential Pair

Figure 2.20 shows a rail-to-rail input stage with a new common-mode adapter [43]. M_{LS1}, M_{LS2}, M_{LS3}, and M_{LS4} are the level-shift current sources. R_{LS1} and R_{LS2} are the

level-shift resistors, which have the same value. M_{15} and M_{16} are used to transfer the level-shift current to the NMOS level-shift current source transistors. The level-shift current is controlled by the level-shift current generator on the left part of Figure 2.20.

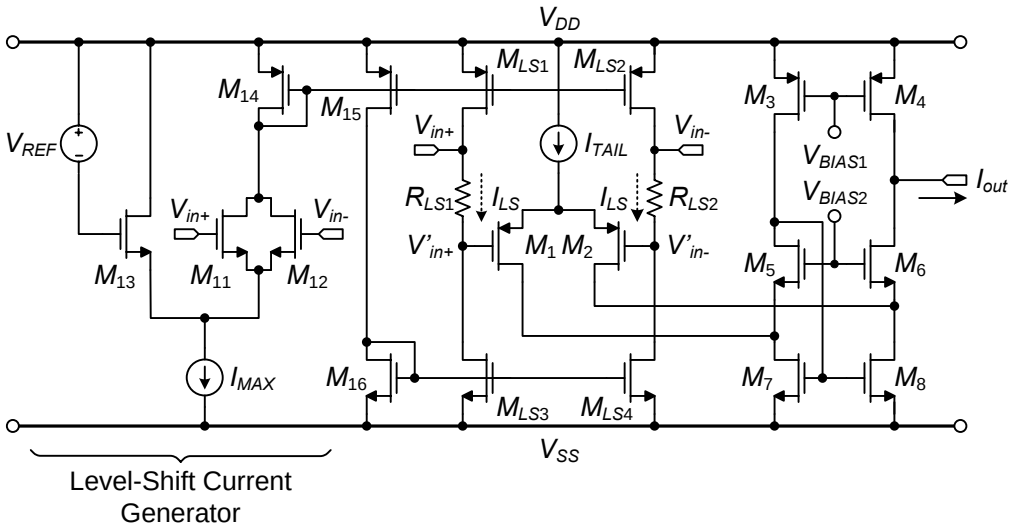

Figure 2.20 CMOS rail-to-rail input stage with a common-mode adapter based on a pseudo-differential pair.

The input signals V_{in+} and V_{in-} are applied on the gates of M_{11} and M_{12}. The sources of M_{11} and M_{12} are connected together, and the drains are also connected together. Because the open-loop gain of an op amp is usually very large, the differential-mode voltage, V_{dm}, is very small. So the effect of V_{dm} on the adapter circuit can be neglected. Thus M_{11} and M_{12} can be considered as one double-sized transistor. Transistor M_{13} and the combination of M_{11} and M_{12} form a differential pair structure. It is not a true differential pair, so this common-mode adapter is named as common-mode adapter based on a pseudo-differential pair. The tail current of the pseudo-differential pair is I_{MAX}. The gate voltage of M_{13}, V_{G13}, is fixed by the voltage source of V_{REF}. Neglect the effect of the differential input voltage, the voltage at the gate of the

equivalent transistor of M_{11} and M_{12} is V_{CM}. Suppose M_{11} and M_{12} have the same size, and the size of M_{13} is W/L, which is twice the size of M_{11} or M_{12}, then the current through M_{11} and M_{12} can be approximately expressed as [20]

$$I(V_{CM}) = \frac{1}{2} I_{MAX} + \frac{k_n'}{4} \frac{W}{L} \left(V_{CM} - V_{G13}\right) \cdot \sqrt{\frac{4 I_{MAX}}{k_n' \left(W/L\right)} - \left(V_{CM} - V_{G13}\right)^2} \qquad (2.22)$$

If V_{CM} equals to V_{G13}, then the current though M_{14} is $I_{MAX}/2$, and the current is mirrored to the level-shift transistors; if V_{CM} is high then V_{G13}, then there is more current goes through M_{14}; if V_{CM} is lower then V_{G13}, then there is less current goes through M_{14}. The W/L ratio of the transistors controls the slop of the curve [20].

It should be pointed out that the common-mode voltage cannot be higher than $V_{DD} - V_{DS(\text{sat})}$. When V_{CM} is between $V_{DD} - V_{DS(\text{sat})}$ and V_{DD}, the level-shift current source transistors M_{LS1} and M_{LS2} operate in the triode region. So strictly speaking, it is not a true rail-to-rail input stage but quasi-rail-to-rail input stage [42].

The level-shift current versus the common-mode input voltage is shown in Figure 2.21, which is similar to the curve in Figure 2.19. Figure 2.22 shows common-mode voltage on the gates of the differential pairs, V'_{CM}, for different V_{CM} at the input. This figure shows the common-mode voltage is adapted to a lower value when the V_{CM} is large. The values of the level-shift current and V'_{CM} in Figure 2.21 and Figure 2.22 may be different for different cases. The normalized transconductance of the input stage is shown in Figure 2.23. It shows the transconductance is almost constant over the common-mode voltage range. The common-mode input voltage can reach within $V_{DS(\text{sat})}$ of the positive power-supply rail, V_{DD}.

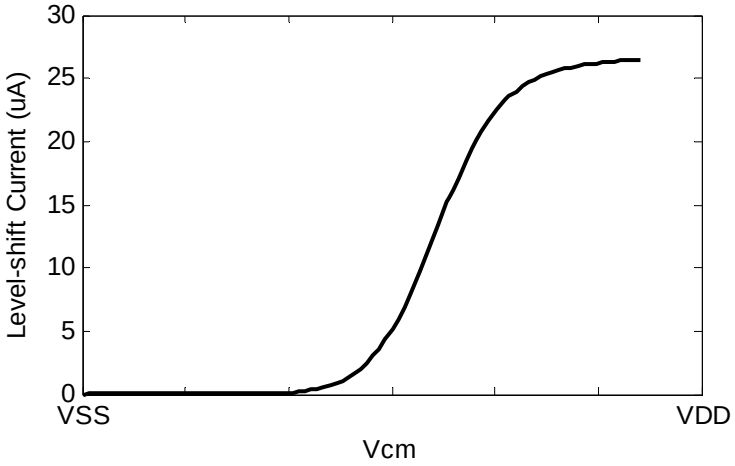

Figure 2.21 Level-shift current versus the common-mode input voltage.

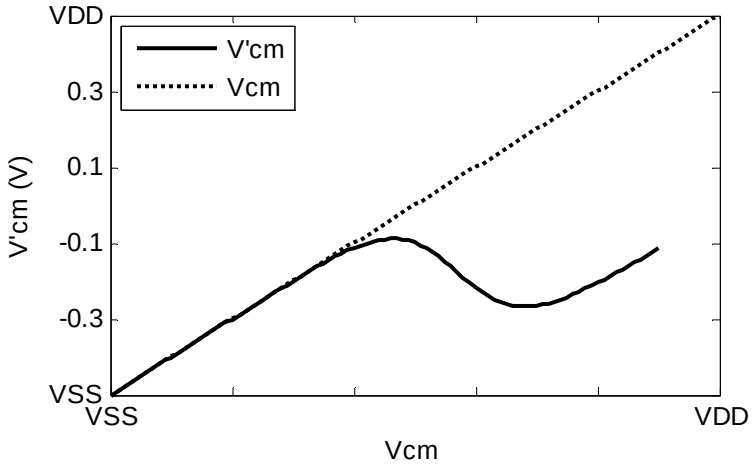

Figure 2.22 Corresponding common-mode voltages.

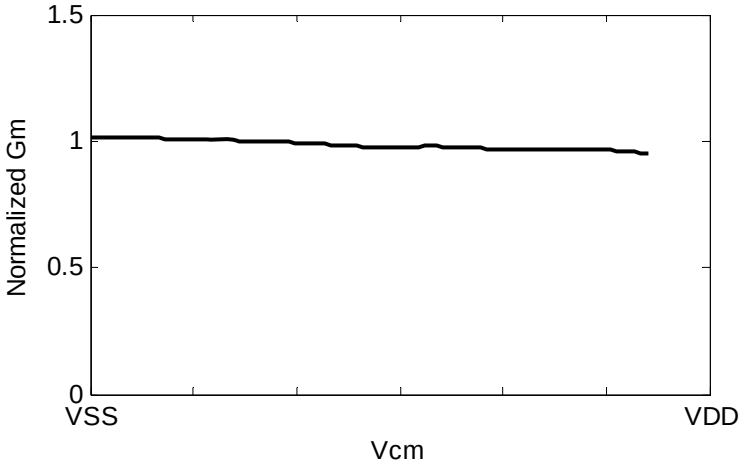

Figure 2.23 Normalized transconductance versus the common-mode input voltage for the input stage of Figure 2.20.

The input stage with a common-mode adapter in Figure 2.20 can also be transformed to a bipolar version, which is shown in Figure 2.24. In Figure 2.20, the PMOS differential pair is used. Here the npn differential pair is used. The operation of the input stage in Figure 2.24 is similar to the input stage in Figure 2.20. In Figure 2.24, the two emitter degeneration resistors R_{12} and R_{13} are used to increase the linearity of the level-shift current as a function of the common-mode input voltage.

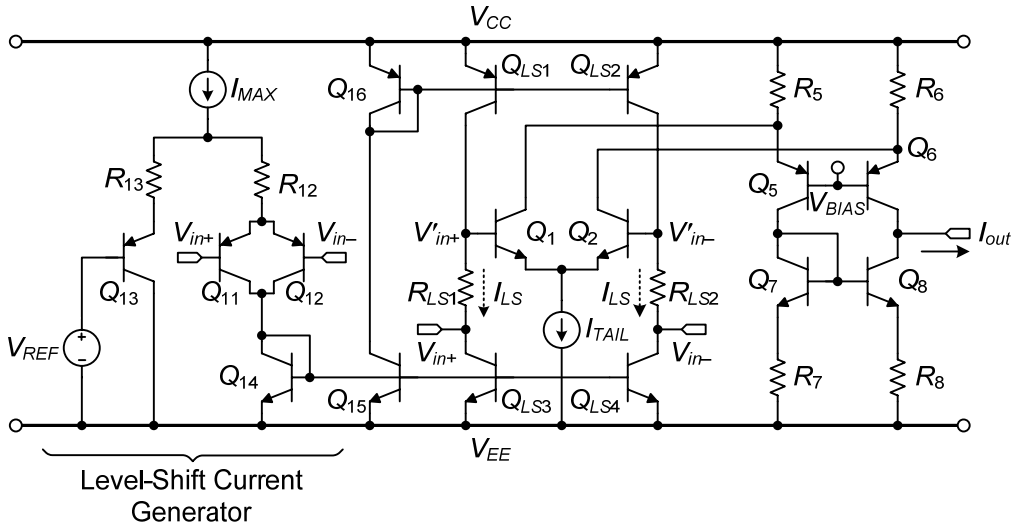

Figure 2.24 Bipolar rail-to-rail input stage with a common-mode adapter based on a pseudo-differential pair.

Figure 2.25 shows the level-shift current versus the common-mode input voltage. It shows that when the common-mode voltage is low, the level-shift current is high; when the common-mode voltage is high, the level-shift current is low. Figure 2.26 shows the common-mode voltage at the bases of the differential pair, V'_{CM}, versus the common-mode input voltage. Figure 2.27 shows the normalized transconductance of the input stage versus the common-mode input voltage.

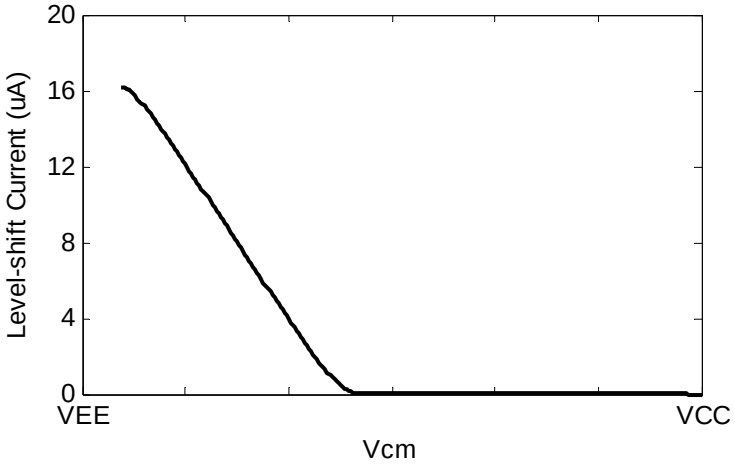

Figure 2.25 Level-shift current versus the common-mode input voltage.

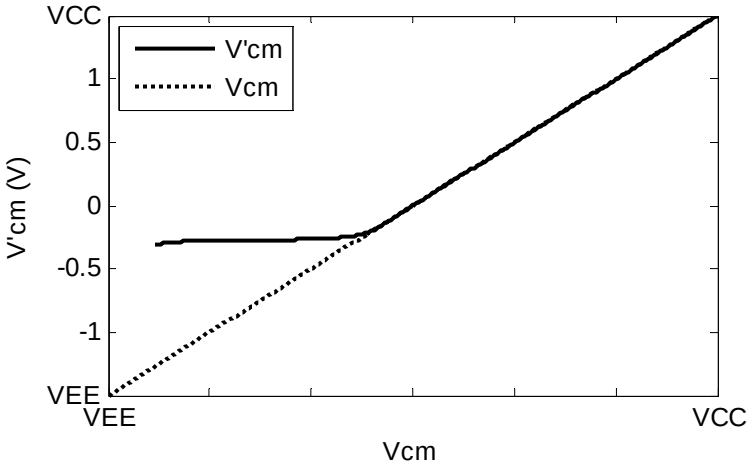

Figure 2.26 Corresponding common-mode voltages.

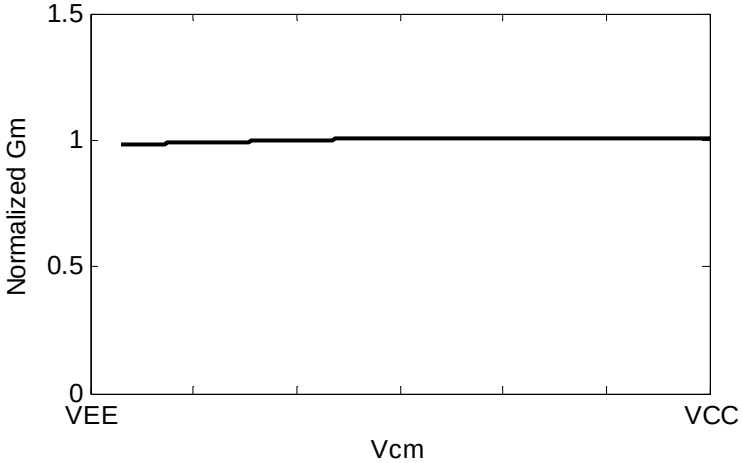

Figure 2.27 Normalized transconductance versus the common-mode input voltage for the input stage of Figure 2.24.

2.2.3 Input Stage with a Common-Mode Adapter Based on Current Subtraction

Figure 2.28 shows a rail-to-rail input stage with a single differential pair and a new common-mode adapter based on current subtraction. In Figure 2.28, the sources of M_{11} and M_{12} are connected, and the drains are also connected together. The input voltages are also applied at the gates of M_{11} and M_{12}. The current through M_{11} and M_{12} are controlled by the current source transistor M_{13}, and the maximum current through M_{13} is I_{MAX} when it is working is the saturation region. The sum of the drain current of D_{13}, I_{D13}, and the drain current of M_{14}, I_{D14}, is I_{MAX}, i.e., I_{D14} is the difference of I_{MAX} and I_{D13}. It can be expressed as

$$I_{D14} = I_{MAX} - I_{D13} \tag{2.23}$$

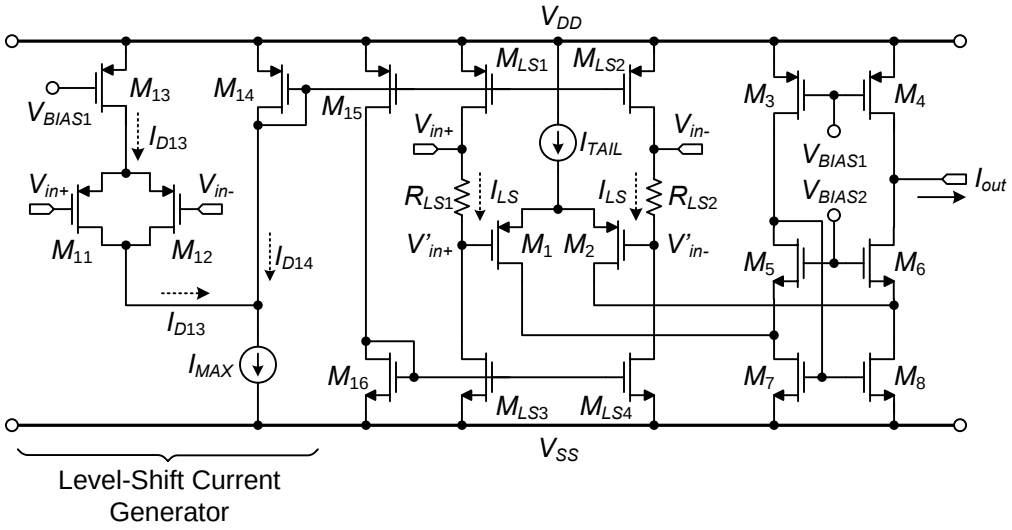

Figure 2.28 CMOS rail-to-rail input stage with a common-mode adapter based on current subtraction.

I_{D14} is then mirrored to the level-shift currents mirrors. When the common-mode input voltage, V_{CM}, is lower than $V_{DD} - V_{DS13(sat)} - V_{GS11}$, M_{13} is in saturation region. I_{D13} equals

I_{MAX}. According to (2.23), I_{D14} is zero. So the level shift current, I_{LS}, is also zero. When V_{CM} increases from $V_{DD} - V_{DS13(sat)} - V_{GS11}$ toward V_{DD}, M_{13} starts going into triode region, and I_{D13} starts decreasing, so I_{D14} starts increasing until I_{D13} equals to zero. The minimum value of I_{D13} is zero, so the maximum value of I_{D14} is I_{MAX}. Because of the current subtraction operation, this common-mode adapter is named the common-mode adapter based on current subtraction.

Figure 2.29 shows the level-shift current versus the common-mode voltage. Figure 2.30 shows the common-mode input voltage at the gates of the differential pair, V'_{CM}, versus the common-mode input voltage. Figure 2.31 shows the normalized transconductance of the input stage versus the common-mode input voltage. The transconductance is almost constant over the input common-mode voltage.

This input stage can also be transformed to a bipolar version. The schematic of the bipolar input stage are not given here.

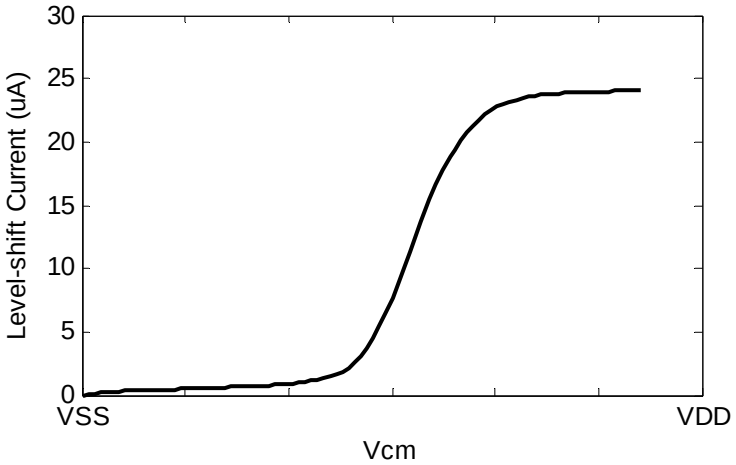

Figure 2.29 Level-shift current versus the common-mode input voltage.

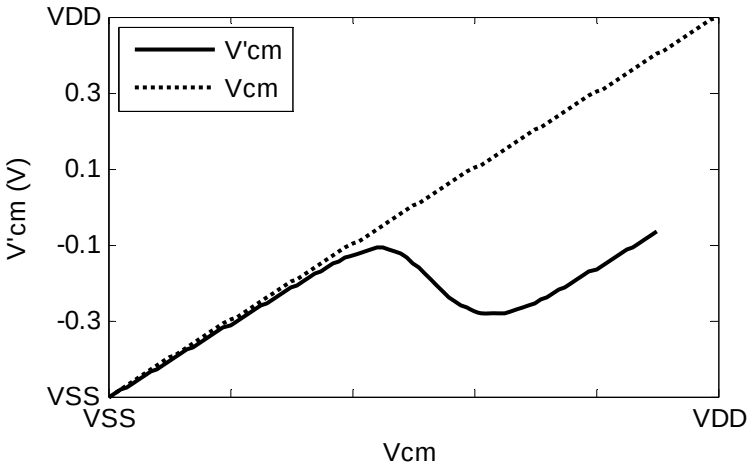

Figure 2.30 Corresponding common-mode voltages.

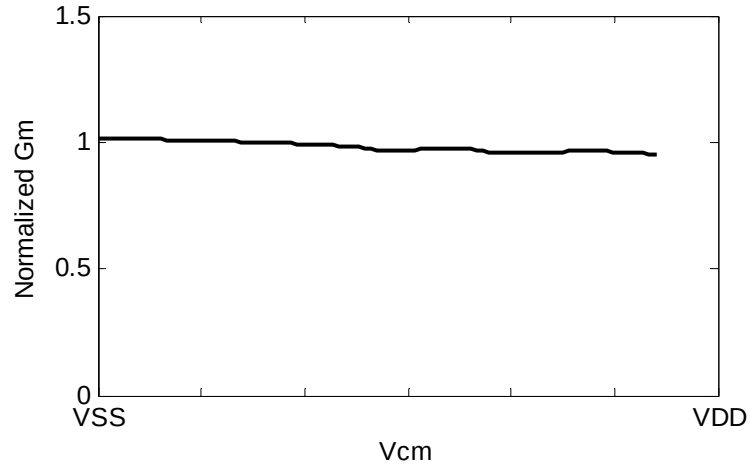

Figure 2.31 Normalized transconductance versus the common-mode input voltage for the input stage of Figure 2.28.

2.4 Summary

Two types of rail-to-rail input stages have been discussed in this chapter. The first one is based on complementary differential pairs, and the second one is based on a single differential pair and a common-mode adapter. One disadvantage of complementary input stages is the required minimum supply voltage is about

$2V_{BE} + 2V_{CE(\text{sat})}$ for bipolar technologies or $2V_{GS} + 2V_{DS(\text{sat})}$ for CMOS technologies. Another disadvantage is the CMRR is poor at the transition region between the p-type and n-type differential pairs. The CMRR was improved by means of increasing the transition region between the pnp and npn pairs. In this chapter, a bipolar constant-G_m complementary input stage with improved CMRR was designed. The required minimum supply voltage for the input stage with a single differential pair is about $V_{BE} + 2V_{CE(\text{sat})}$ for bipolar technologies or $V_{GS} + 2V_{DS(\text{sat})}$ for CMOS technologies. The disadvantage of the input stage with single differential pair is that the common-mode adapter increases the power consumption, and introduces extra noise and offset voltage. Two different rail-to-rail input stages with a single differential pair and common-mode adapter were presented. Two new common-mode adapters were introduced. The first one is based on a pseudo- differential pair, and the second one is based on current subtraction.

CHAPTER 3

OTHER CIRCUIT PARTS AND FREQUENCY COMPENSATION

The design of the rail-to-rail input stages have been discussed in Chapter 2. An op amp can have only one gain stage. Usually a one-stage op amp does not have enough open-loop gain for typical applications. In order to obtain enough open-loop gain, two or more gain stages are required for an op amp. The rail-to-rail output stage is discussed in Section 3.1; the intermediate stage is discussed in Section 3.2; the current reference circuit is discussed in Section 3.3; the output protection circuit is discussed in Section 3.4. For two-stage or three-stage op amps, compensation circuits are needed for stability. The Miller compensation and nested-Miller compensation methods are discussed in Section 3.5.

3.1 Output Stage

The purpose of the output stage is to deliver power into the load. The most important specifications of output stages are the output voltage swing range, power efficiency, and distortion. To obtain better power efficiency, a class-AB output stage should be used. The ideal output voltage swing is from rail to rail. To obtain a rail-to-rail output swing, the conventional emitter-follower or source-follower configuration is not suitable. The output transistors must be in a common-emitter or common-source configuration.

3.1.1 Class-AB Output Stage

The voltage follower, common-emitter or common-source configuration, is the most popular class-AB biasing topology because of the simplicity, low output impedance, and good linearity. Figure 3.1(a) shows a voltage-follower class-AB output stage configuration with complementary bipolar transistors. In Figure 3.1(a), Q_1, Q_2, Q_3, and Q_4 form a translinear loop [44]. It yields

$$V_{BE1} + V_{BE2} = V_{BE3} + V_{BE4} \tag{3.1}$$

Assuming that Q_1, Q_2, Q_3, and Q_4 transistors have the same size, because of the logarithmic relationship between the base-emitter voltage and the collector current of a bipolar transistor, the product of the push and pull currents is constant. It can be expressed as

$$I_{push} \cdot I_{pull} = I_{BIAS}^2 \tag{3.2}$$

where I_{push} is the push current through the pnp output transistor Q_1, and I_{pull} is the pull current through the npn output transistor Q_2.

The load for the output stage is not shown in Figure 3.1(a). The output current is the difference between I_{push} and I_{pull}. The quiescent current, I_Q, is the current through the output transistors when the output current is zero. According to (3.2), I_Q equals to I_{BIAS}. The push current and pull current versus output current relationship is shown in Figure 3.1(b).

One drawback of the voltage follower class-AB bias scheme is the output voltage swing cannot be from rail to rail. The maximum output voltage is

$V_{BE} + V_{CE(\text{sat})}$ below V_{CC}, and the minimum output voltage is $V_{BE} + V_{CE(\text{sat})}$ above V_{EE}. So the conventional voltage-follower configuration is not suitable for low voltage design. In order to have rail-to-rail output voltage swing, common-emitter configuration is often used, as shown in Figure 3.2(a).

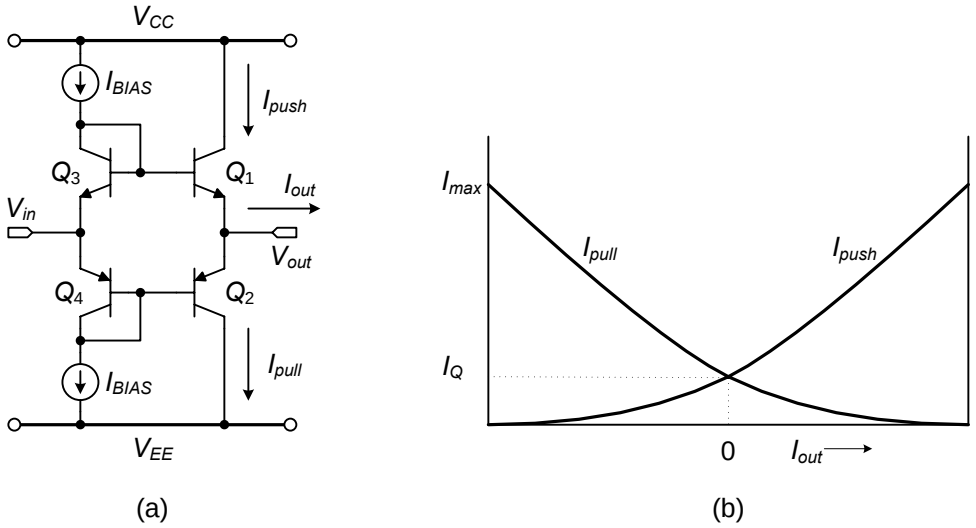

Figure 3.1 (a) Voltage follower class-AB output stage with complementary bipolar transistors and (b) the push current and pull current as a function of the output current.

An efficient class-AB biasing must satisfy following four requirements [21, 45]: (a) the ratio of maximum current, I_{max}, to the quiescent current, I_Q, must be high for high efficiency; (b) the minimum current, I_{min}, should not be much smaller than the quiescent current to avoid high-frequency distortion; (c) the class-AB transition must be smooth to avoid low-frequency distortion; (d) The output transistors must be driven by a preceding stage directly without delay from the class-AB control circuit. Figure 3.2(b) shows the push current and pull current for an ideal class-AB biasing.

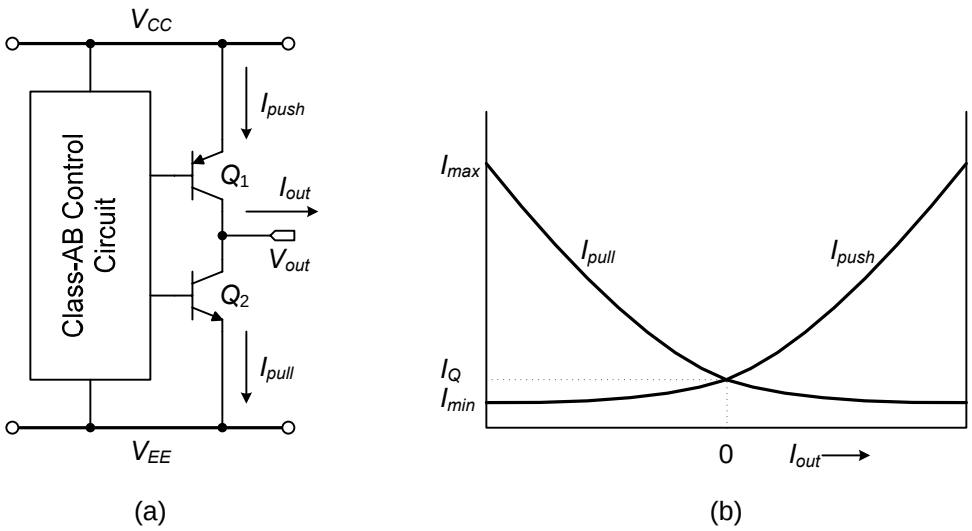

Figure 3.2 (a) Common-emitter rail-to-rail class-AB output stage with complementary bipolar transistors and (b) the ideal push current and pull current as a function of the output current.

3.1.2 Rail-to-Rail Class-AB Output Stage

Both class-A and class-AB circuits can be used to implement rail-to-rail output stages [10]. The class-A output stage has good linearity, but poor current efficiency. A class-AB output stage is commonly used to obtain good current efficiency.

In order to obtain a rail-to-rail output voltage swing, a common-emitter or common-source output stage must be used. Many rail-to-rail class-AB output stage topologies have been proposed. They are classified into two categories – the feedforward class-AB output stage [28, 46, 47] and the feedback class-AB output stage [11, 25, 26, 45, 48]. In [48], the authors proposed a feedback-controlled class-AB rail-to-rail output stage. Figure 3.3 is a modified class-AB rail-to-rail output stage based on the output stage in [48].

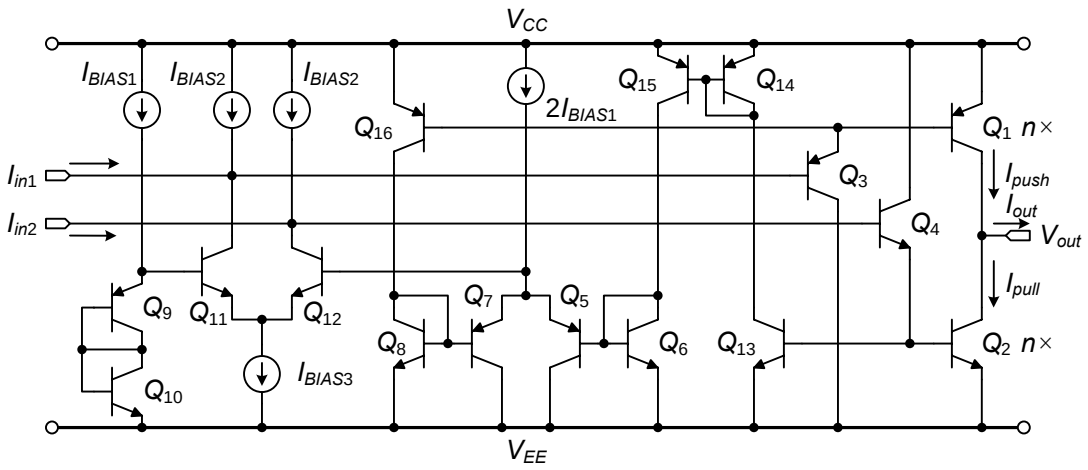

Figure 3.3 Rail-to-rail class-AB output stage with Darlington output transistors.

There are two inputs for this output stage, which drive the output Darlington pairs directly. They are in-phase signals, which have the same amplitude and polarity. In Figure 3.3, Q_1 and Q_3 are the pnp Darlington pair output transistors, and Q_2 and Q_4 are the npn Darlington pair output transistors. The Darlington topology is used to increase the gain [20]. The collector current of the pnp output transistor, I_{push}, is sensed by Q_{16}, and then transferred to Q_8. The collect current of npn output transistor, I_{pull}, is sensed by Q_{13}, and then transferred to Q_{14}, Q_{15}, and Q_6.

Q_{11} and Q_{12} form a differential pair, which compares the emitter voltage of Q_5 and Q_7 to the reference voltage of the two diode-connected transistors, Q_9 and Q_{10}. If the voltages are unequal, a correction signal is steered to both Darlington pairs by the feedback amplifier Q_{11} and Q_{12}, until the two voltages are equal. Q_5 and Q_7 form a minimum selector [3, 21, 49]. Suppose npn output transistor Q_1 is driven hard, the base-emitter voltage of Q_8 is higher than the base-emitter voltage of Q_6. Then all the tail current $2I_{BIAS1}$ flows to Q_5. So the Q_6 base-emitter voltage is fixed by the differential

feedback amplifier Q_{11} and Q_{12}. Then the collector current through Q_6 is fixed, and the pull current is fixed at a nonzero value. In a similar way, if pnp output transistor Q_2 is driven hard, the push current is fixed to a nonzero value.

The sizes of the output transistors are n times the size of the sensor transistors, Q_{13}, Q_{14}, Q_{15}, Q_6, Q_{16}, and Q_8, so the pull current is n times the collector current of Q_6, and the push current is n times the collector current of Q_8. It can be expressed as

$$I_{C6} = \frac{1}{n} I_{pull} \tag{3.3}$$

$$I_{C8} = \frac{1}{n} I_{push} \tag{3.4}$$

Transistors Q_5, Q_6, Q_7, and Q_8 form a translinear loop, therefore

$$I_{C5} \cdot I_{C6} = I_{C7} \cdot I_{C8} \tag{3.5}$$

The tail current for the differential pair Q_5 and Q_7 is $2I_{BIAS1}$. It yields

$$I_{C5} + I_{C7} = 2I_{BIAS1} \tag{3.6}$$

Because of the differential feedback amplifier Q_{11} and Q_{12}, the sum of the base-emitter voltages of Q_9 and Q_{10} is equal to the sum of the base emitter voltage Q_7 and Q_8. So

$$I_{C7} \cdot I_{C8} = I_{C9} \cdot I_{C10} = I_{BIAS1}{}^2 \tag{3.7}$$

From (3.3) through (3.7), we have

$$\frac{1}{I_{pull}} + \frac{1}{I_{push}} = \frac{2}{n \cdot I_{BIAS1}} \tag{3.8}$$

The quiescent current through the output transistors, I_Q, can be obtained by equaling I_{pull} and I_{push} in (3.8). It yields

$$I_Q = n \cdot I_{BIAS1} \tag{3.9}$$

The minimum value of I_{pull} and I_{push} can also be shown to be

$$I_{min} = \frac{1}{2} \cdot n \cdot I_{BIAS1} = \frac{1}{2} I_Q \tag{3.10}$$

Equation (3.8) can be rewritten as

$$\left(I_{push} - \frac{1}{2} I_Q \right) \cdot \left(I_{pull} - \frac{1}{2} I_Q \right) = \left(\frac{1}{2} I_Q \right)^2 = \left(\frac{1}{2} n \cdot I_{BIAS1} \right)^2 \tag{3.11}$$

The relationship among the push, pull, and output currents is similar to the curve in Figure 3.2(b).

One drawback of the feedback-controlled class-AB Darlington output stage is the minimum supply voltage is high. From the path of Q_1, Q_3, Q_{11}, Q_9, and Q_{10}, it can be observed that the minimum supply voltage for this output stage is about $3V_{BE} + V_{CE(\text{sat})}$.

3.2 Intermediate Stage

So far, the input and output stages have been discussed. A two-stage op amp only has an input stage and an output stage. However, if a high open-loop gain is required, then an additional intermediate stage is needed. An extra stage may cause a stability problem. Thus it requires a more complicated compensation scheme.

Figure 3.4 shows a differential intermediate stage [4]. The purpose of this intermediate stage is to amplify the current signal. The inputs are differential signals, and the outputs are two in-phase signals, which are required by the output stage in Figure 3.3. Q_7 and Q_8 are in an emitter-follower configuration with no voltage gain but with current gain, which increases the overall op amp gain.

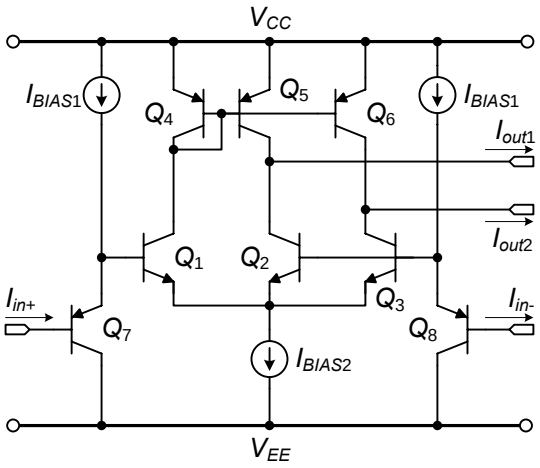

Figure 3.4 Intermediate stage.

3.3 Current Reference Circuit

A bias circuit is used as a reference current source for the biasing current of an op amp. The reference current source should be independent of the supply voltage. Figure 3.5 shows a current reference circuit [50].

In Figure 3.5, Q_1 and Q_2 are two identical current sources, which are controlled by a loop amplifier [50]. In this way, the equal bias conditions are maintained for different supply voltages, and the influence of the finite early voltage is eliminated. The emitter area ratio of Q_4 to Q_3 is n. From the above current reference configuration, the bias current [20] is given by

$$I_{BIAS} = \frac{V_T}{R_4} \ln(n) \tag{3.12}$$

where V_T is the thermal voltage. From (3.12), the bias current is independent of the supply voltage, and it is proportional to the absolute temperature. So it is called a proportional to absolute temperature (PTAT) current source.

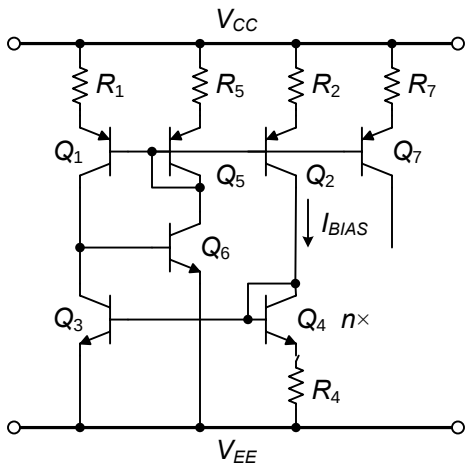

Figure 3.5 Current reference circuit.

There are two possible stable operating points in this circuit. A start-up circuit is needed to avoid the zero current state. In Figure 3.5, the start-up circuit is not shown. The reference circuit with a start-up circuit will be discussed in Chapter 4.

3.4 Output Protection Circuit

For a rail-to-rail output stage, the output transistors are very easy get into the saturation region. In order to avoid this, an output saturation protection circuit is needed. Figure 3.6 shows the npn half of a Darlington output stage, Q_1 and Q_2, driving a load, R_L [51]. If a large current is drawn by R_L, then the collector-emitter voltage of Q_1 is very small, and it gets into the saturate region. Heavy saturation of the output transistor should be avoided because it takes time to get rid of the charge stored in the base of the output transistor. In Figure 3.6, transistor Q_3 is used to measure base-collector voltage of Q_1. When Q_1 is in heavy saturation, the base-collector junction is forward biased, and Q_3 is in the reverse active region. There is current that flows

through Q_3, which reduce the current driving Q_2. The ratio of the emitter areas of Q_1 to the emitter area of Q_3 controls the amount of saturation allowed.

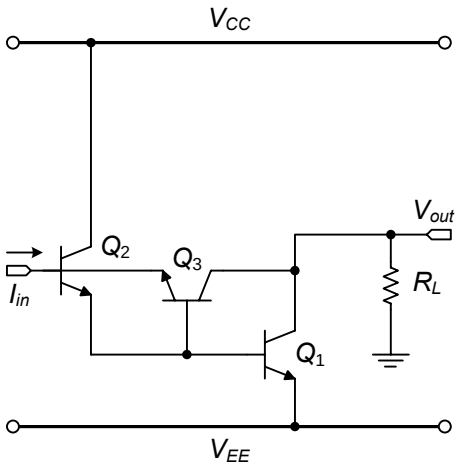

Figure 3.6 Saturation protection circuit for a Darlington output stage.

If the output stage is driven hard, then there is large current that flows through the output transistor. It dissipates lots of power, which may destroy the op amp. In order to prevent this from happening, an output current limiting circuit is needed. Figure 3.7 is the current limiting circuit for a npn Darlington pair of the output stage [4, 51].

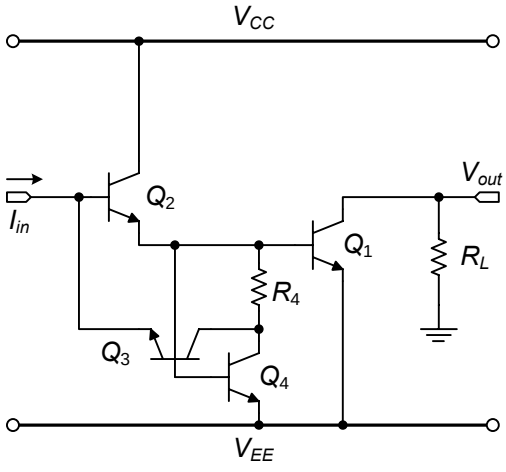

Figure 3.7 Current limiting circuit.

Transistor Q_4 is used to sense the current through the output transistor Q_1. If Q_1 is driven hard, then the current through Q_4 will be large. Because of a voltage drop over R_4, it causes Q_4 to go into the saturation region. Then Q_3 goes into the reverse active region. Some current goes through Q_3, which reduces input current through Q_2. Therefore it prevents a further increase in the current through the output transistor.

3.5 Frequency Compensation

The input stage, intermediate stage, and output stage have been discussed so far. When the signal passes through an op amp, it causes phase lag. When the phase shift exceeds 180° at a certain frequency, the open-loop gain must drop below unity. Otherwise, the closed-loop system oscillates. Furthermore, a phase margin must be large enough to avoid a peaking in the frequency domain or overshooting in the time domain [52]. For every common-emitter or common-source stage, it introduces a dominant pole, and every pole causes a 90° phase shift. If there are two or more dominant poles in an op amp, it may cause stability problems. In this case, frequency compensation is required. For a two-stage op amp, the Miller compensation is needed. For a three-stage op amp, the simple Miller compensation cannot remove the third pole. To stabilize three-stage op amps, nested-Miller compensation can be used [11, 22, 53].

3.5.1 Miller Compensation

Figure 3.8 shows a block diagram of a two-stage op amp with a Miller compensation capacitor, C_C. Each gain stage is assumed to have a high output resistance, and it is labeled as a transconductance block. C_1, C_2, R_1, and R_2 are the

capacitance and resistance associated with gain stages. C_2 and R_2 include load capacitance and load resistance, respectively.

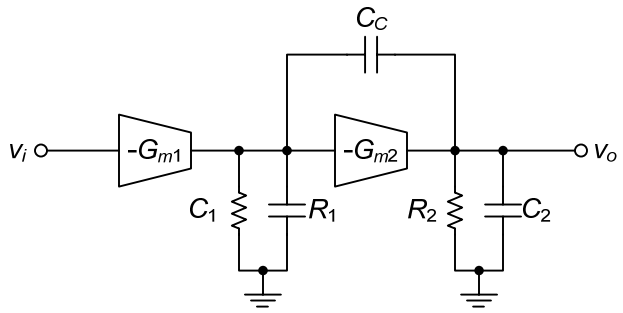

Figure 3.8 Block diagram for a two-stage op amp with Miller compensation.

The small-signal equivalent circuit of the two-stage op amp in Figure 3.8 is illustrated in Figure 3.9. Obviously, without compensation capacitor C_C, there are two poles in this circuit. They are

$$\omega'_{p1} = -\frac{1}{R_1 C_1} \tag{3.13}$$

$$\omega'_{p2} = -\frac{1}{R_2 C_2} \tag{3.14}$$

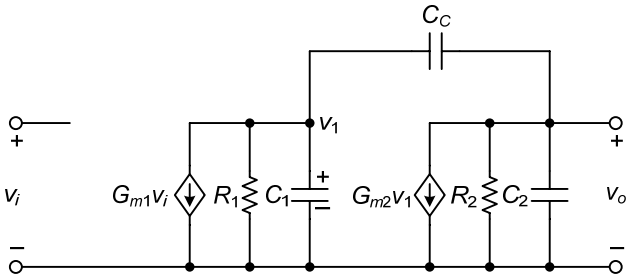

Figure 3.9 Small-signal model of the two-stage op amp in Figure 3.8.

By nodal analysis, the exact transfer function from the input v_i to the output v_o can be expressed as [54]

$$\frac{v_o}{v_i} = \frac{G_{m1}R_1G_{m2}R_2\left(1+s\cdot\frac{C_C}{G_{m2}}\right)}{1+s\cdot\left[R_1\left(C_1+C_C\right)+R_2\left(C_2+C_C\right)+R_1G_{m2}R_2C_C\right]+s^2\cdot R_1R_2\left(C_1C_2+C_1C_C+C_2C_C\right)} \tag{3.15}$$

From the above transfer function, the DC open-loop gain is

$$A_0 = G_{m1}R_1G_{m2}R_2 \tag{3.16}$$

There is a positive real zero in the transfer function of (3.15), which is at

$$\omega_Z = \frac{G_{m2}}{C_C} \tag{3.17}$$

For a bipolar op amp, the transistor transconductance is very high. Therefore the frequency of the zero is very large, and it can be neglected. For a CMOS op amp, this is not the case. This will be discussed later. It has two poles in the circuit. Typically the two poles are real and widely separated. The two poles are [54]

$$\omega_{p1} = -\frac{1}{\left(C_1+C_C\right)R_1+\left(C_2+C_C\right)R_2+G_{m2}R_2R_1C_C} \approx -\frac{1}{R_1G_{m2}R_2C_C} \tag{3.18}$$

$$\omega_{p2} \approx -\frac{G_{m2}C_C}{C_1C_2+C_C\left(C_1+C_2\right)} \tag{3.19}$$

where ω_{p1} is the dominant pole, and ω_{p2} is the non-dominant pole. The approximation is given under the condition of $G_{m1}R_1 >> 1$ and $G_{m2}R_2 >> 1$, which are usually true. Equation (3.18) and Equation (3.19) indicate $\left|\omega_{p1}\right|$ decreases as C_C increases, whereas $\left|\omega_{p2}\right|$ increases as C_C increases. So the Miller compensation is also called the pole splitting [20, 22]. Figure 3.10 shows the frequency response of the circuit before and

after the Miller compensation. It illustrates the movement of the poles after frequency compensation.

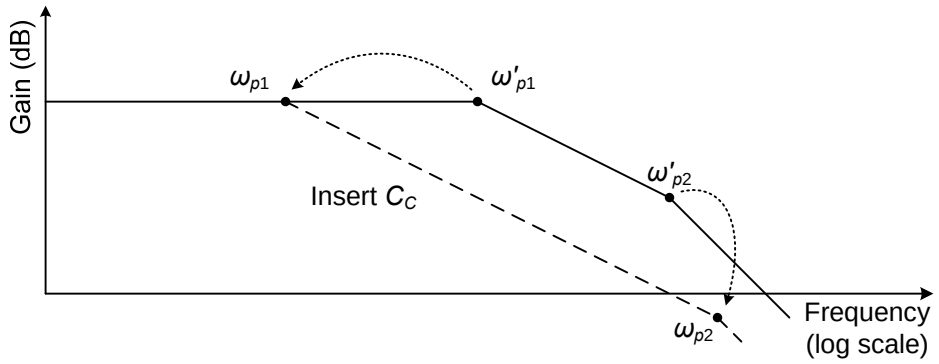

Figure 3.10 Frequency response of the circuit in Figure 3.9 before and after inserting compensation capacitor.

In a common situation where the load capacitance, C_2, and compensation capacitance, C_C, are significantly larger than the inter-stage parasitic capacitance C_1, Equation (3.19) can be further simplified as

$$\omega_{p2} \approx -\frac{G_{m2}}{C_2\left(1+C_1/C_C\right)+C_1} \approx -\frac{G_{m2}}{C_2} \tag{3.20}$$

From (3.16) and (3.18), the gain-bandwidth product can be obtained as

$$\omega_{GBW} = \frac{G_{m1}}{C_C} \tag{3.21}$$

The phase margin can be expressed as

$$\varphi_m = 90° - \tan^{-1}\left(\frac{G_{m1}C_2}{G_{m2}C_C}\right) \tag{3.22}$$

The required compensation capacitance for a specific phase margin can be expressed as

$$C_C = \tan(\varphi_m)\frac{G_{m1}}{G_{m2}}C_2 \tag{3.23}$$

Equation (3.17) indicates there is a positive zero in the two-stage op amp, which causes an extra phase shift. For bipolar op amps, the frequency of the zero is far from the frequency of the poles. For a CMOS op amp, this zero needs to be removed. In order to get rid of the zero, a nulling resistor, R_Z, can be inserted in series with the compensation capacitor [9]. The addition of the resistor shifts the zero to a location is given by

$$\omega_Z = \frac{1}{C_C\left(1/G_{m2} - R_Z\right)} \tag{3.24}$$

If R_Z is selected to equal to $1/G_{m2}$, then the zero disappears. If R_Z is larger than $1/G_{m2}$, the zero shifts to the right plane, and it increases phase margin.

3.5.2 Nested-Miller Compensation

For a three-stage op amp, the simple Miller compensation is not enough, a nested-Miller compensation [11, 22, 53, 55, 56] is can be used. The model of a three-stage op amp with compensation capacitors C_{C1} and C_{C2} is shown in Figure 3.11.

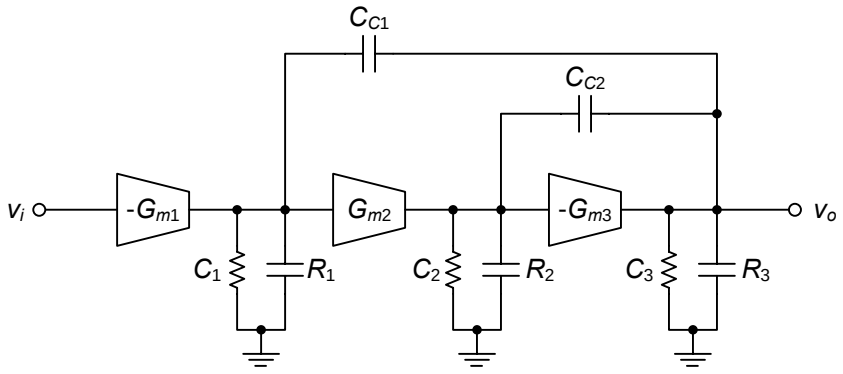

Figure 3.11 Block diagram for a three-stage op amp with nested-Miller compensation.

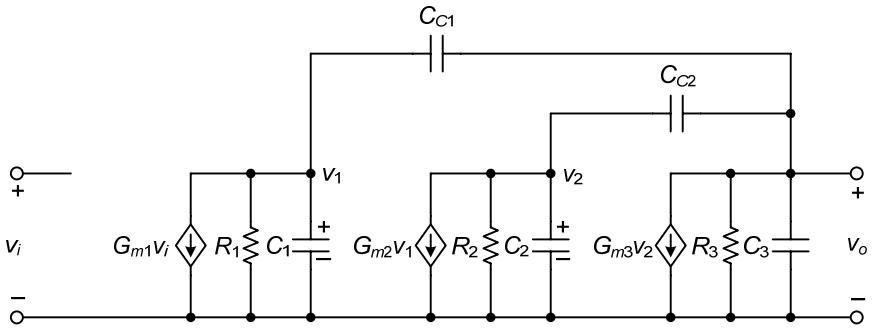

Figure 3.12 Small-signal model of the three-stage op amp in Figure 3.11.

Figure 3.12 illustrates the equivalent small-signal circuit corresponding to the block diagram of a three-stage op amp with nested-Miller compensation shown in Figure 3.11. For common situations, the load capacitor, C_3, and the compensation capacitors, C_{C1} and C_{C2}, are very large compared to the parasitic capacitors, C_1 and C_2. Under this assumption, analysis leads to the following transfer function [56]:

$$A(s) = \frac{v_o(s)}{v_i(s)} = \frac{N(s)}{D(s)} = A_0 \cdot \frac{1 + s \cdot b_1 + s^2 \cdot b_2}{1 + s \cdot a_1 + s^2 \cdot a_2 + s^3 \cdot a_3} \tag{3.25}$$

where

$$A_0 = G_{m1} R_1 G_{m2} R_2 G_{m3} R_3 \tag{3.26}$$

$$\begin{aligned} a_1 = {} & R_1 C_{C1} + R_2 C_{C2} + R_3 C_3 + R_3 C_{C1} + R_3 C_{C2} \\ & + R_2 G_{m3} R_3 C_{C2} + R_1 G_{m2} R_2 G_{m3} R_3 C_{C1} \end{aligned} \tag{3.27}$$

$$\begin{aligned} a_2 = {} & R_1 R_2 C_{C1} C_{C2} + R_1 R_3 C_{C1} C_3 + R_1 R_3 C_{C1} C_{C2} + R_2 R_3 C_{C2} C_3 \\ & + R_2 R_3 C_{C1} C_{C2} - R_1 G_{m2} R_2 R_3 C_{C1} C_{C2} + R_1 R_2 G_{m3} R_3 C_{C1} C_{C2} \end{aligned} \tag{3.28}$$

$$a_3 = R_1 R_2 R_3 C_{C1} C_{C2} C_3 \tag{3.29}$$

$$b_1 = -\frac{C_{C1}}{G_{m2} R_2 G_{m3}} - \frac{C_{C2}}{G_{m3}} \tag{3.30}$$

$$b_2 = -\frac{C_{C1}C_{C2}}{G_{m2}G_{m3}} \tag{3.31}$$

Assuming that there is only one dominant pole in the transfer function of (3.25), and also assuming that $G_{m1}R_1 >> 1$, $G_{m2}R_2 >> 1$, $G_{m3}R_3 >> 1$, and $G_{m3} >> G_{m2}$, then the denominator of (3.25) can be rewritten as

$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + s \cdot \frac{C_{C2}}{G_{m2}} + s^2 \cdot \frac{C_{C2}C_3}{G_{m2}G_{m3}}\right) \tag{3.32}$$

where ω_{p1} is the dominant pole in the system, and it can be expressed as

$$\omega_{p1} = \frac{1}{R_1 G_{m2} R_2 G_{m3} R_3 C_{C1}} \tag{3.33}$$

From (3.26) and (3.33), the gain-bandwidth product of the op amp can be expressed as

$$\omega_{GBW} = A_0 \cdot \omega_{p1} = \frac{G_{m1}}{C_{C1}} \tag{3.34}$$

Equation (3.34) shows that the gain-bandwidth product is proportional to the transconductance of the input stage. If the transconductance is a constant over the common-mode input range, optimized compensation can be obtained.

To obtain 60° of phase margin for the overall op amp, the compensation capacitors should have approximate [22, 55, 56] values of

$$C_{C1} = 4\frac{G_{m1}}{G_{m3}}C_3 \tag{3.35}$$

$$C_{C2} = 2\frac{G_{m2}}{G_{m3}}C_3 \tag{3.36}$$

The derivation details of (3.35) and (3.36) can be found in [22] and [56].

3.6 Summary

In this chapter, the output stage, the intermediate stage, and the output protection circuit is discussed. A feedback-controlled class-AB rail-to-rail output stage was discussed in detail. A PTAT current reference circuit for biasing was also discussed. The frequency compensation methods were also described in this chapter. For a two-stage op amp, Miller compensation can be used. For a three-stage op amp nested-Miller compensation can be applied.

CHAPTER 4

OVERALL OPERATIONAL AMPLIFIER CIRCUIT

So far, all necessary circuit parts for designing rail-to-rail op amps have been discussed. This chapter focuses on complete op amps design. Several different rail-to-rail input stages have been discussed in Chapter 2. In order to be able to compare the performance of the different input stages, three three-stage bipolar op amps with the same intermediate and output stages but different input stages are designed in Section 4.1, Section 4.2, and Section 4.3. In Section 4.4 and Section 4.5, two two-stage CMOS op amps with different common-mode adapters are designed.

4.1 UTA242: Three-Stage Bipolar Op Amp with a Constant-Gm Complementary Input Stage

In this section, a three-stage bipolar op amp with a rail-to-rail constant-G_m complementary input stage is designed. This op amp was fabricated with a chip ID of UTA242. For simplicity, this op amp is named UTA242 in this chapter.

The input stage of UTA242 is shown in Figure 4.1, which is similar to the input stage of Figure 2.7. The ideal current and voltage sources in Figure 2.7 are implemented with transistors and resistors. The input stage of Figure 2.7 has a single-ended output. Now the current summing circuit in Figure 4.1 has differential outputs. The outputs of the input stage are labeled as I_1 and I_2, which are connected to the intermediate stage in

Figure 4.4. The differential signals are required by the intermediate stage, which was discussed in Section 3.2.

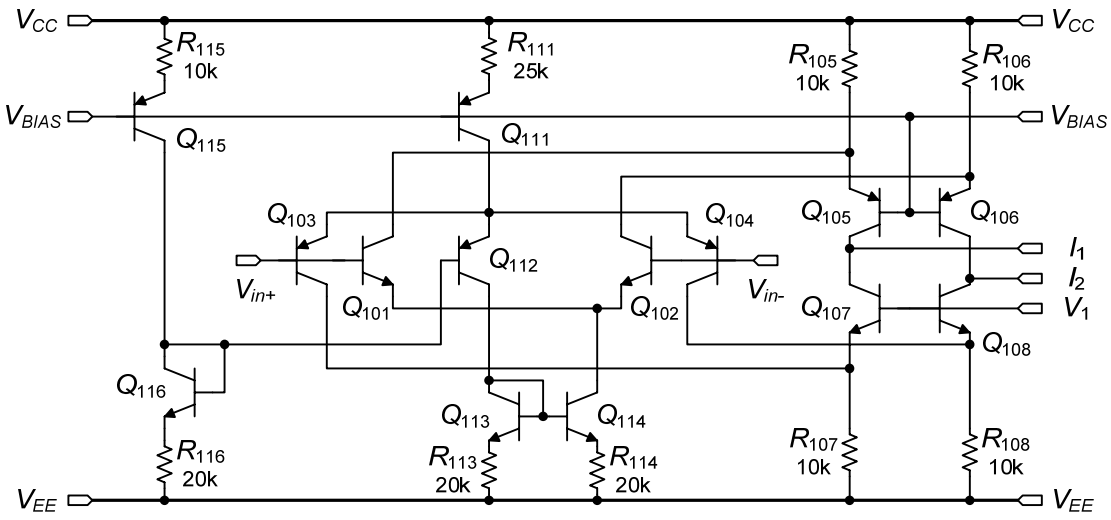

Figure 4.1 Rail-to-rail constant-G_m complementary input stage.

This input stage has constant transconductance, G_m. The constant transconductance is realized by making the total current through the pnp and npn differential pairs constant, which was discussed in Section 2.2.2. Q_{111} and R_{111} provide the total tail current about 4.5 μA. R_{115}, Q_{115}, Q_{116}, and R_{116} generate the bias voltage for Q_{112}. The base voltage of Q_{112} is biased at about 1 V above V_{EE}. The base voltage of Q_{112} determines the transition point between the pnp and npn pairs. The bases of Q_{107} and Q_{108} are labeled as V_1, which is connected to the intermediate stage. The bias voltage on the bases of Q_{107} and Q_{108} is controlled by a negative common-mode feedback loop. The components in the current summing circuit and intermediate stages form the common-mode feedback loop [4]. With the feedback loop, the bases of Q_{107}

and Q_{108} in the input stage of Figure 4.1 are biased at about 0.82 V above V_{EE}. The terminal V_{BIAS} is connected to the reference circuit in Figure 4.5.

The input stage in Figure 4.1 was fabricated with National Semiconductor's VIP10 [57] Process Technology. The fabricated input stage has single-ended output as in Figure 2.7. The reference circuit in Figure 4.5 is fabricated in the same chip to provide the bias current. The micrograph of the chip is shown in Figure 4.2. Three different rail-to-rail input stages were fabricated in the same chip. The other two input stages will be discussed in Section 4.2 and Section 4.3.

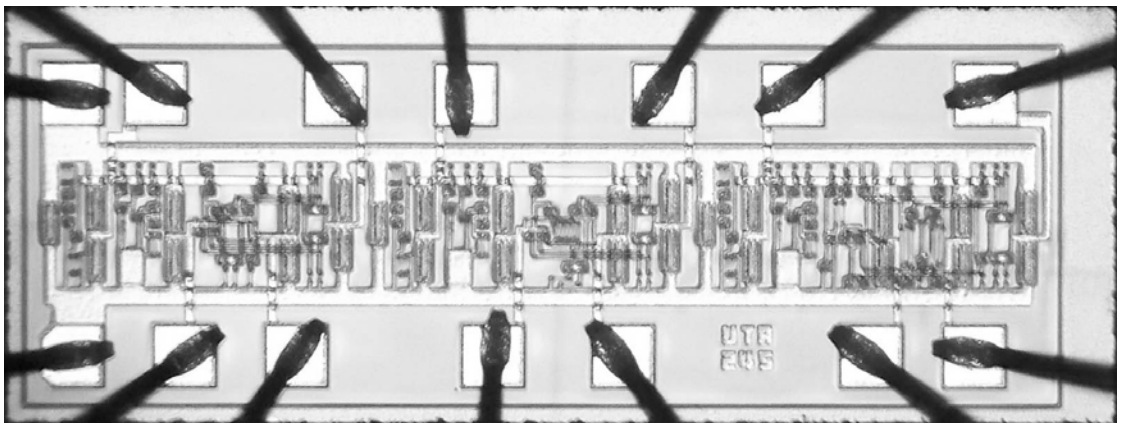

Figure 4.2 Micrograph of the three different rail-to-rail input stages.

The transconductance of the input stage over the entire common-mode input voltage range was measured, which is shown in Figure 4.3. The supply voltage V_{EE} equals -1.5 V, and V_{CC} equals 1.5 V. Two observations can be made from this plot. First, when the common-mode input voltage extends beyond both power supply rails by about 0.3 V, the input stage is still working. Second, the transconductance over the common-mode input range is roughly constant. The maximum value of the

transconductance is about 58.7 μS, and the minimum value is about 53.6 μS, so the variation is about 10%. The variation is due to the mismatch between the pnp and npn parts.

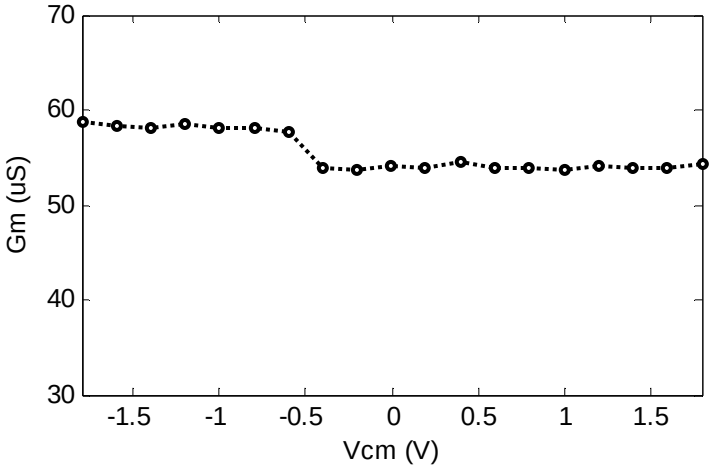

Figure 4.3 Measured transconductance versus the common-mode input voltage.

Figure 4.4 shows the intermediate stage, output stage, and frequency compensation circuit. The operations of these circuit parts have been discussed in Chapter 3. In this chapter, three three-stage bipolar op amps with different rail-to-rail input stages are designed. To be able to compare the performance of different input stages, those three op amps have the same intermediate and output stages in Figure 4.4 and reference circuit in Figure 4.5.

Nested-Miller compensation is applied to stabilize the three-stage bipolar op amps here. As shown in Figure 4.4, the frequency compensation is realized with capacitors C_{C1P} of 1.6 pF, C_{C1N} of 1.6 pF, C_{C2} of 0.8 pF, and R_C of 500 Ω. The resistor R_C is used to improve phase margin [55, 56].

The class-AB push current and pull current are controlled by a negative feedback loop. The details of the operation of the output stage were discussed in Section 3.1.2. Q_{301} and Q_{303} form a pnp Darlington pair; Q_{302} and Q_{304} form a npn Darlington pair. One draw back of the feedback-controlled class-AB Darlington output stage is that the required minimum supply voltage is about $3V_{BE} + V_{CE(\text{sat})}$. To be able push or pull output current up to 10 mA, the output transistors Q_{301} and Q_{302} have 24 times the emitter area of the regular transistor. At the quiescent state, the push current through the pnp output transistor Q_{301} and the pull current through the npn output transistor Q_{302} are about 200 μA. Q_{331} and Q_{332} are saturation protection transistors for pnp and npn output transistors, respectively. R_{331}, Q_{333}, and Q_{335} form the output current limiting circuit for pnp output transistor Q_{301}. R_{332}, Q_{334}, and Q_{336} form the current limiting circuit for npn output transistor Q_{302}. The maximum output current through the output transistors are limited to about 10 mA. The operation of the saturation protection and output current limiting circuit was discussed in Section 3.4.

The current reference circuit is shown in Figure 4.5, which is similar to the circuit in Figure 3.5. The emitter area of Q_{004} is two times the emitter area of Q_{003}. The value of R_{004} is 2 kΩ. According to (3.12), the bias current, I_{BIAS}, is about 9 μA at room temperature. R_{011}, Q_{011}, Q_{012}, Q_{013}, Q_{014}, and R_{014} form the start-up circuit. The start-up circuit makes sure that the current through the reference circuit does not remain zero when the power is switched on. Capacitor C_{001} is used to improve the stability of the reference circuit.

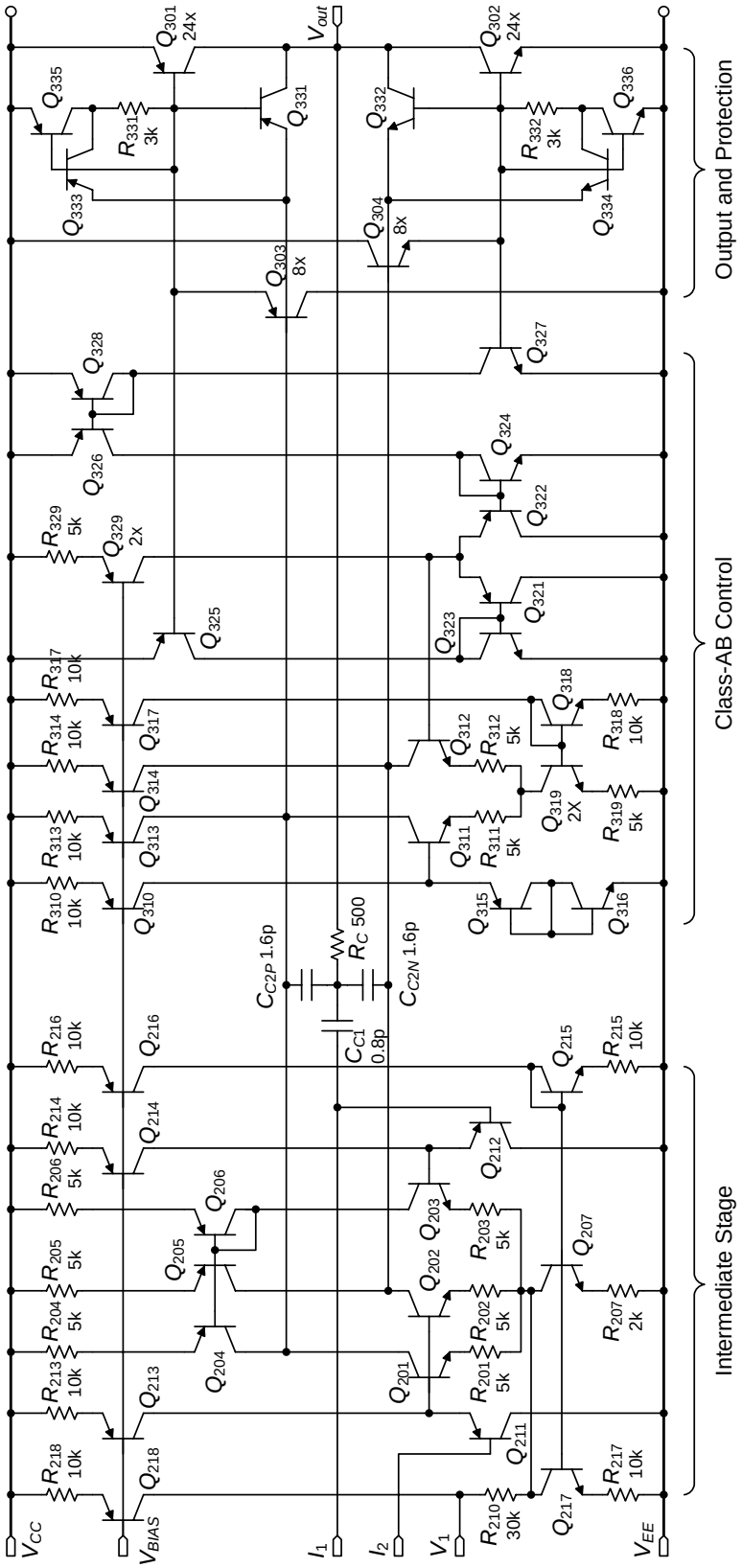

Figure 4.4 Intermediate and output stages.

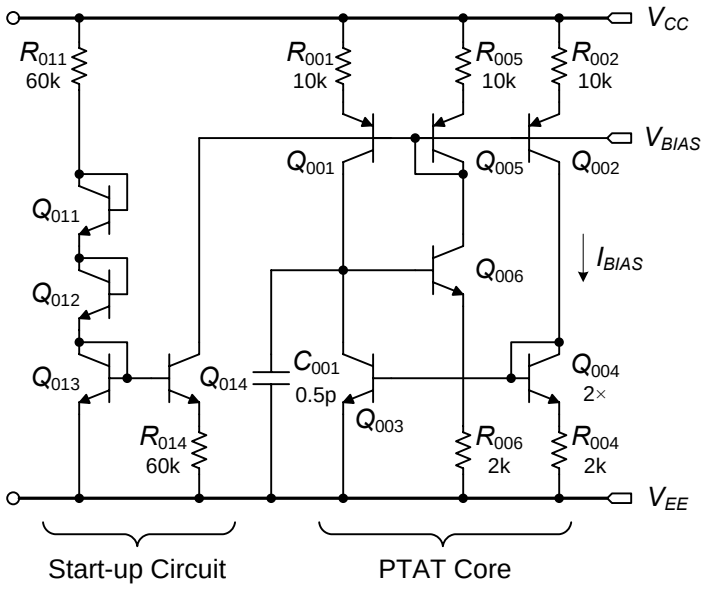

Figure 4.5 Current reference with start-up circuit.

The op amp of UTA242 is the combination of the reference circuit in Figure 4.5, the input stage in Figure 4.1, and the intermediate and output stages in Figure 4.4. The complete UTA242 was fabricated with National Semiconductor's VIP10 process, and the micrograph of the chip is shown in Figure 4.6.

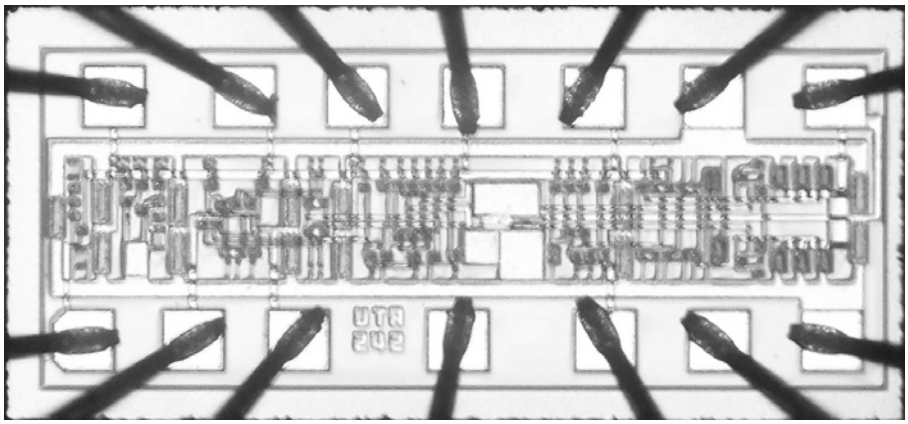

Figure 4.6 Micrograph of UTA242.

Some simulation and measurement are performed for UTA242. The SPICE models [24] of the pnp and npn transistors for simulation are given in Appendix A. The circuit setup conditions for simulation and measurement are: the positive-power voltage V_{CC} is +1.5 V; the negative power-supply voltage V_{EE} is -1.5 V; the common-mode input voltage is biased at 0 V; the load is a 2 kΩ resistor in parallel with a 20 pF capacitor; the temperature is 25˚C. The simulation and measurement described in Section 4.1, Section 4.2, and Section 4.3 are under these conditions if they are not specified.

Figure 4.7 shows the simulated open-loop frequency response of UTA242 for different common-mode voltages, 0 V and ±1.3 V. As expected, the magnitude and phase of the open-loop frequency response are almost the same for different common-mode input voltages. This is the benefit of the input stage with constant transconductance. The simulated low-frequency open-loop gain is about 110 dB, the unity-gain frequency is about 14 MHz, and the phase margin is about 65˚.

Figure 4.8 shows the measured closed-loop gain versus the frequency for UTA242 in a non-inverting amplifier configuration as shown in Figure 1.2 with 10 kΩ of R_2 and 1 kΩ of R_1. Ideally, the gain is 11 or 20.83 dB. Because of the constant gain-bandwidth product (GBW), this circuit setup is used to measure the GBW of the op amp. The measured gain-bandwidth product is about 10.8 MHz.

Figure 4.9, Figure 4.10, and Figure 4.11 show some experimental and simulated results of UTA242 in the unity-gain configuration. Obviously, the simulation

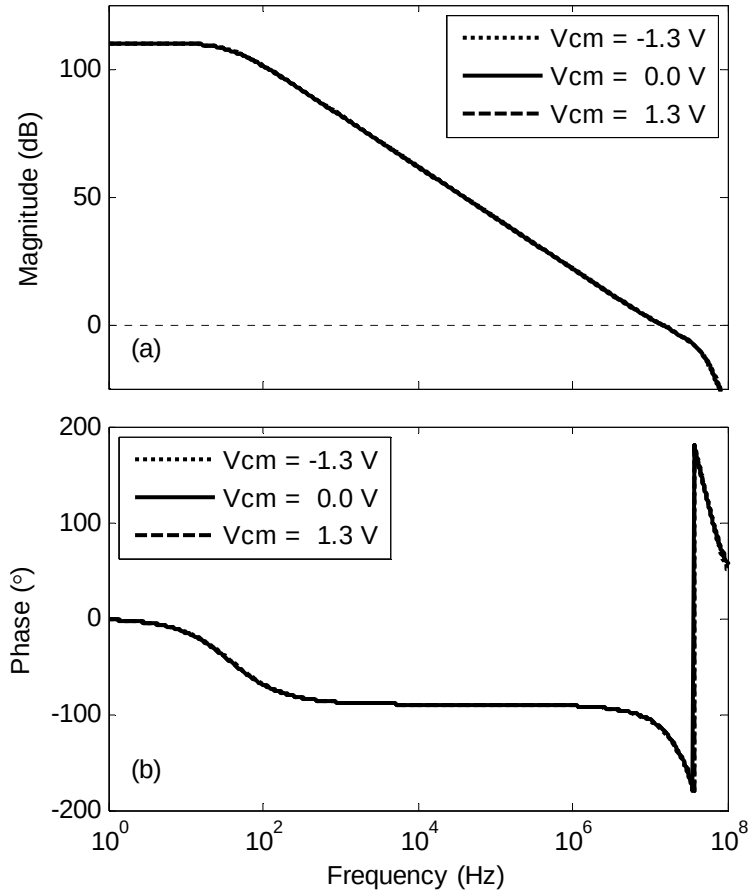

Figure 4.7 (a) Magnitude and (b) phase of the open-loop frequency response for UTA242 with different common-mode input voltages.

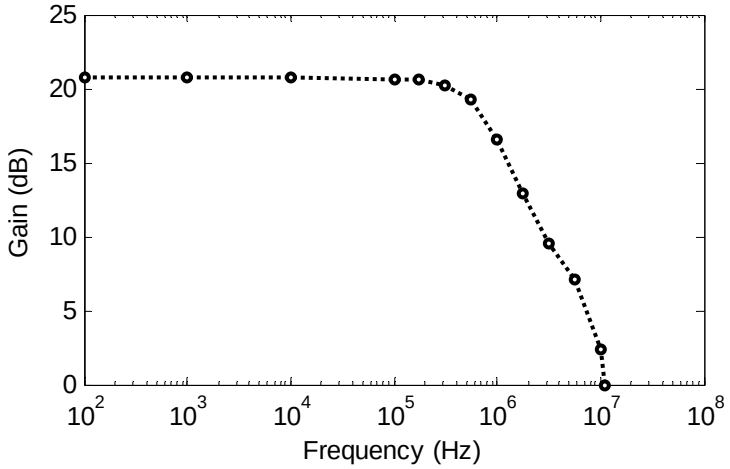

Figure 4.8 Measured closed-loop gain of UTA242 with a non-inverting amplifier configuration.

and experimental results are almost the same. Figure 4.9 shows the DC input-output transfer characteristic. It is linear with unity gain when the input voltage is in the range from -1.4 V to 1.4 V. The output voltage can swing from rail to rail within 100 mV. Figure 4.10 shows the transient response to a pulse. The measured positive slew rate is about 4.2 V/μs, and the negative slew rate is about 4.1 V/μs. Figure 4.11 shows the transient response to a sine wave with the frequency of 250 kHz and the peak-to-peak amplitude of 2.6 V.

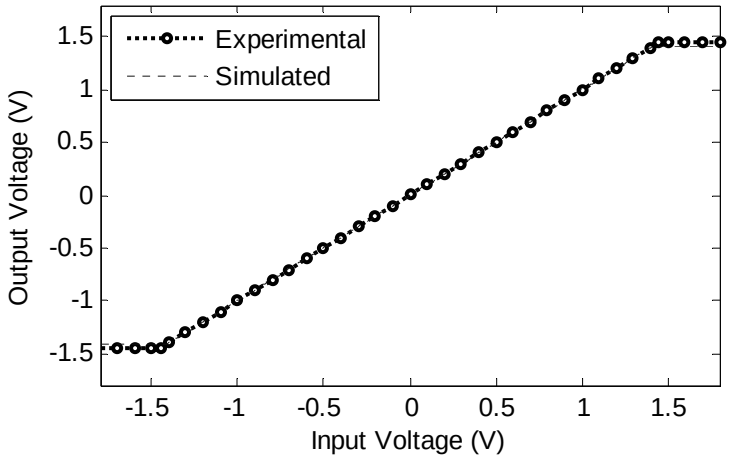

Figure 4.9 DC transfer curve of UTA242 in the unity-gain configuration.

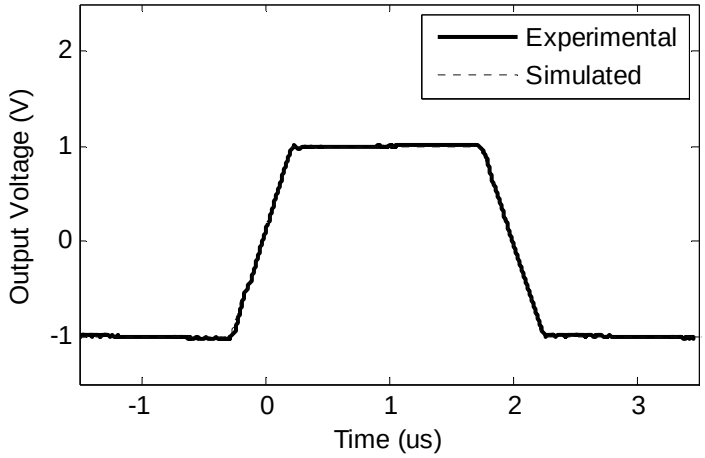

Figure 4.10 Transient response to a pulse of UTA242 in the unity-gain configuration.

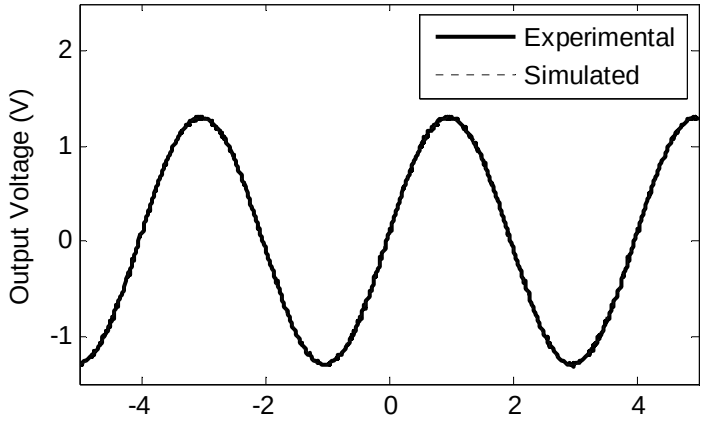

Figure 4.11 Transient response to a sine wave of UTA242 in the unity-gain configuration.

Figure 4.12 shows the measured [58-60] offset voltage over the entire common-mode input voltage range. When the pnp pair is on, the offset voltage is about -1.7 mV; when the npn pair is on, the offset voltage is about -0.05 mV. Due to the short transition range between the pnp and npn pairs, the CMRR is poor in this region. Figure 4.13 shows the measured CMMR over the entire common-mode input voltage range. The lowest CMRR is about 38.3 dB. It is around 100 dB when only the pnp or npn pair conducts.

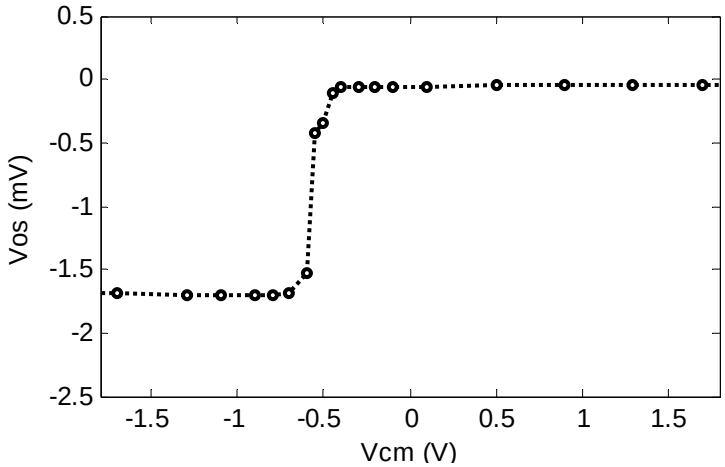

Figure 4.12 Measured offset voltage versus the common-mode input voltage for UTA242.

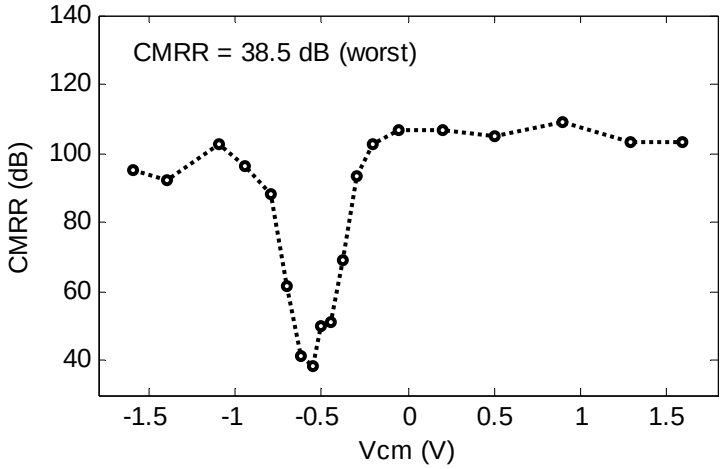

Figure 4.13 Measured CMRR versus the common-monde input voltage for UTA242.

As a summary, some aspects of performance of UTA242 are given in Table 4.1. In this table, $V_{SUP(\min)}$ is the required minimum power-supply voltage, i.e., required minimum value of $V_{CC} - V_{EE}$; V_{OUT} is the output swing range; I_{SUP} is the quiescent supply current; $I_{out(\max)}$ is the maximum output current; V_{OS} is the input offset voltage; $PSRR^+$ and $PSRR^-$ are the positive and negative power-supply rejection ratios, respectively; SR^+ and SR^- are the positive and negative slew rates, respectively; A_{DC} is the low-frequency open-loop gain; GBW is the gain-bandwidth product; φ_M is the phase margin, which is a simulation result.

Table 4.1 Performance Summary of UTA242.

Parameters	Value	Parameters	Value
$V_{SUP(\min)}$	2.4 V	$CMRR$	38.5 dB (min)
$CMIR$	V_{EE}-0.3V to V_{CC}+0.3V	$PSRR^+$, $PSRR^-$	92.9 dB, 96.4 dB
V_{OUT}	V_{EE}+0.1V to V_{CC}-0.1V	SR^+, SR^-	4.2 V/μs, 4.1 V/μs
I_{SUP}	462 μA	A_{DC}	105.2 dB
$I_{out(\max)}$	9.3 mA, -11.0 mA	GBW	10.8 MHz
V_{OS}	0.05 mV to 1.7 mV	φ_M	65.0°

4.2 UTA243: Three-Stage Bipolar Op Amp with a Constant-Gm CMRR-Improved Complementary Input Stage

Figure 4.14 shows the rail-to-rail constant-G_m complementary input stages with improved CMRR. The operation of this input stage is discussed in Section 2.2.3. Same as the input stage in Figure 4.1, the total tail current is about 4.5 μA. Resistor R_{101}, which is used to increase the transmission region between the pnp and npn pairs, is 140 kΩ. A three-stage bipolar op amp with this input stage is designed, and it is named UTA243.

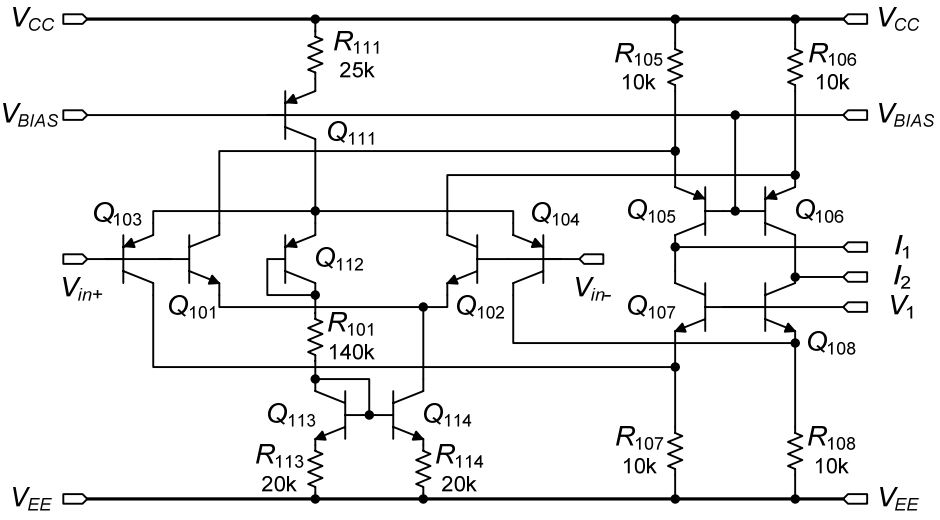

Figure 4.14 Rail-to-rail constant-G_m complementary input stage with improved CMRR.

The input stage in Figure 4.14 with a single-ended output was fabricated. The micrograph of the input stage is shown in Figure 4.2. The measured transconductance over the entire common-mode input range is shown in Figure 4.15. The maximum value of the transconductance is 56.8 μS, and the minimum value is 52.6 μS, so the variation

is about 8%. This figure also shows the common-mode input range is from V_{EE} – 0.3 V to V_{DD} + 0.3 V.

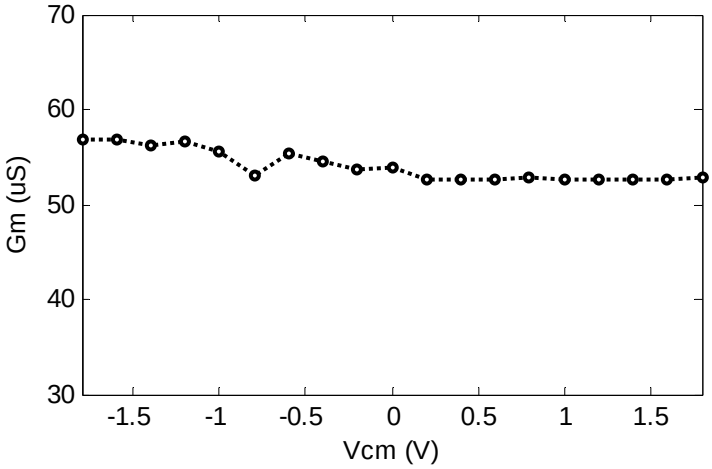

Figure 4.15 Measured transconductance versus the common-mode input voltage.

The op amp of UTA243 is the combination of the reference circuit in Figure 4.5, input stage in Figure 4.14, and intermediate and output stages in Figure 4.4. The complete three-stage op amp of UTA243 was fabricated. The micrograph of the chip is shown in Figure 4.16.

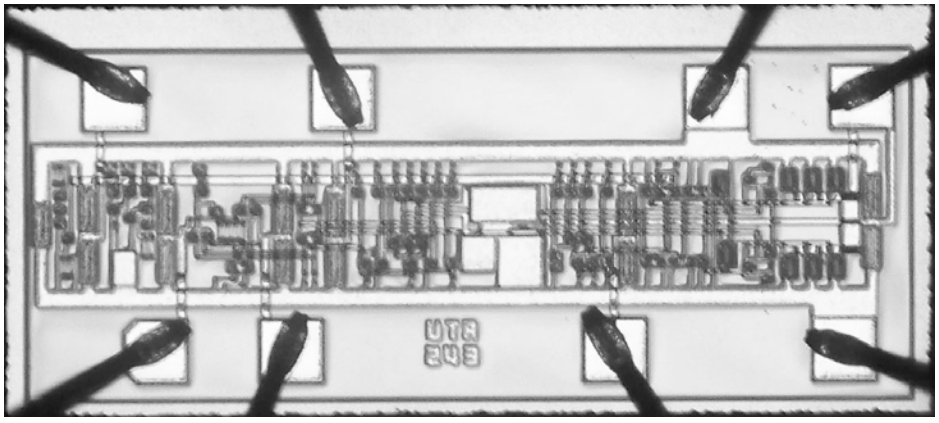

Figure 4.16 Micrograph of UTA243.

Figure 4.17 shows the simulated open-loop frequency response of the designed UTA243 for different input common-mode voltages, 0 V and ±1.3 V. Obviously, the open-loop frequency responses of UTA243 are almost the same for different common-mode input voltages. The simulated low-frequency open-loop gain is about 110 dB, the unity-gain frequency is about 14 MHz, and the phase margin is about 64˚.

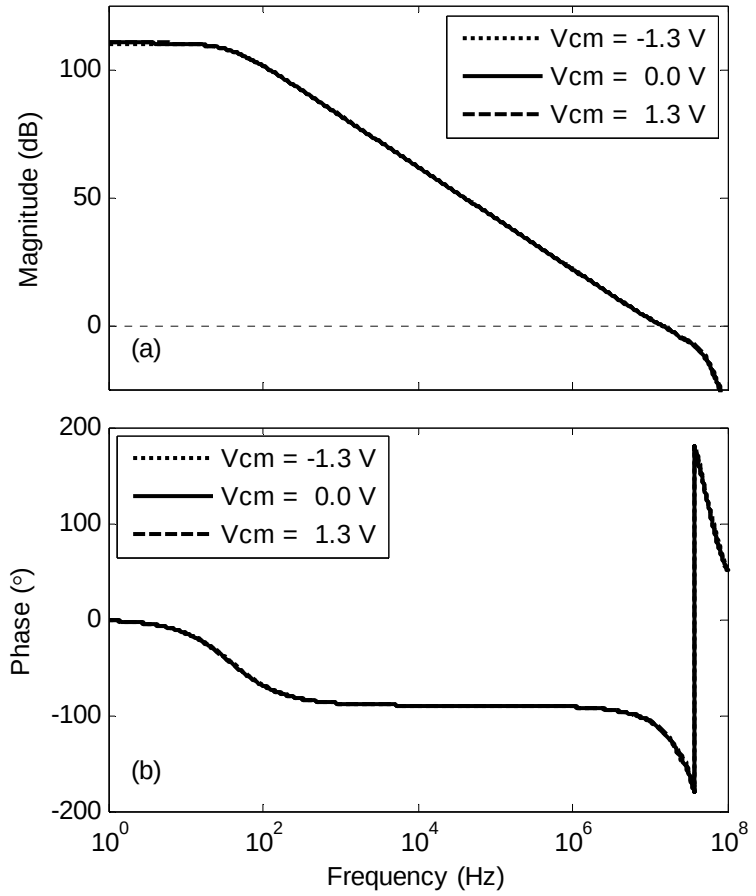

Figure 4.17 (a) Magnitude and (b) phase of the open-loop frequency response for UTA243 with different common-mode input voltages.

Figure 4.18 shows the measured closed-loop gain versus frequency of UTA243 in a non-inverting amplifier configuration with a gain of 11. The measured gain-bandwidth product is about 11.3 MHz.

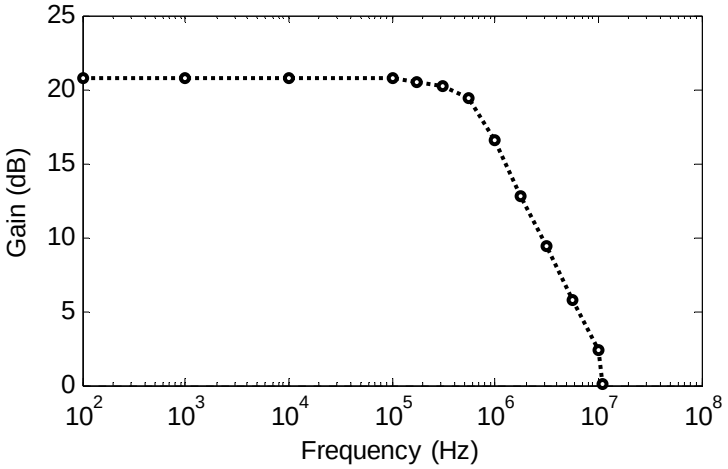

Figure 4.18 Measured closed-loop gain of UTA243 in a non-inverting amplifier configuration.

Figure 4.19, Figure 4.20, and Figure 4.21 show some experimental and simulated results of UTA242 in the unity-gain configuration. Figure 4.19 shows the DC input-output transfer characteristic. It is linear with unity gain when the input voltage is from -1.4 V to 1.4 V. Figure 4.20 shows the transient response to a pulse of in the unity-gain configuration. The measured positive and negative slew rates are 3.8 V/μs and 4.1 V/μs, respectively. Figure 4.21 shows the transient response to a sine wave with the frequency of 250 kHz and the peak-to-peak amplitude of 2.6 V.

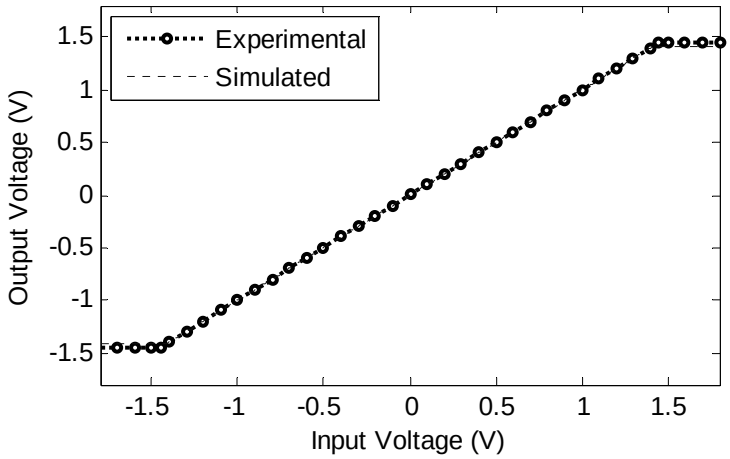

Figure 4.19 DC transfer curve of UTA243 in the unity-gain configuration.

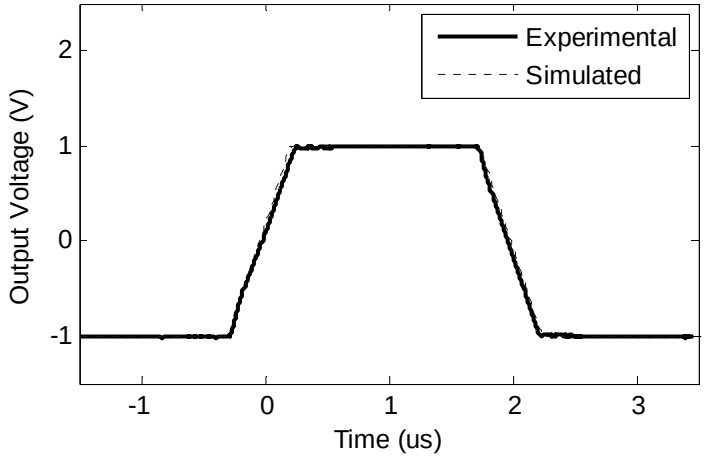

Figure 4.20 Transient response to a pulse of UTA243 in the unity-gain configuration.

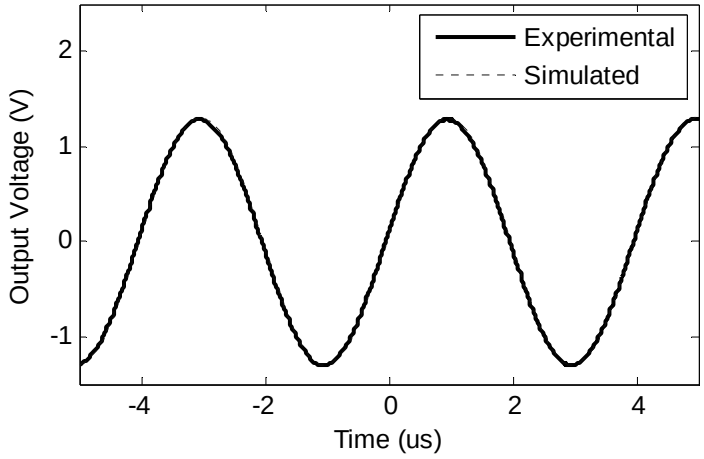

Figure 4.21 Transient response to a sine wave of UTA243 in the unity-gain configuration.

The advantage of the input stage in Figure 4.14 over the input stage in Figure 4.1 is that the CMRR is improved. The CMRR is improved by means of increasing the transition range between the pnp and the npn pairs, which was addressed in Section 2.2.2. Figure 4.22 shows the offset voltage over the entire common-mode input voltage. When only the pnp pair is on, the offset voltage is about -1.02 mV; when only the npn

pair is on, the offset voltage is about -0.58 mV. The transition range is about 1 V. Figure 4.23 shows the measured CMRR versus the common-mode input voltages. The minimum CMRR is about 64.0 dB, which is about 20 dB improvement compared to the input stage in Figure 4.1.

As a summary, some aspects of performance of UTA243 are given in Table 4.2.

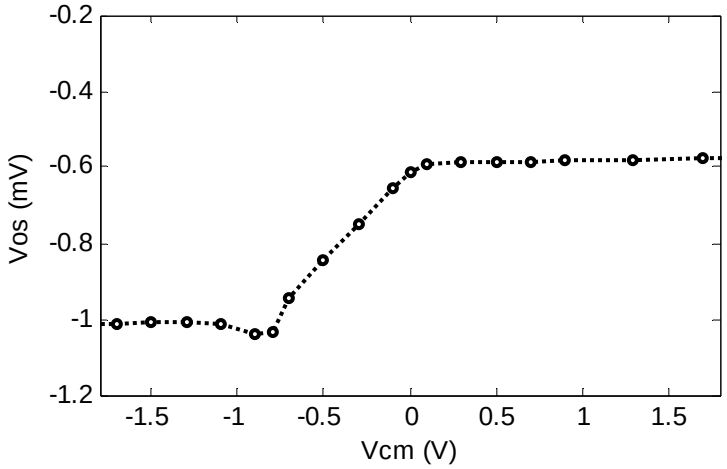

Figure 4.22 Measured offset voltage versus the common-mode input voltage for UTA243.

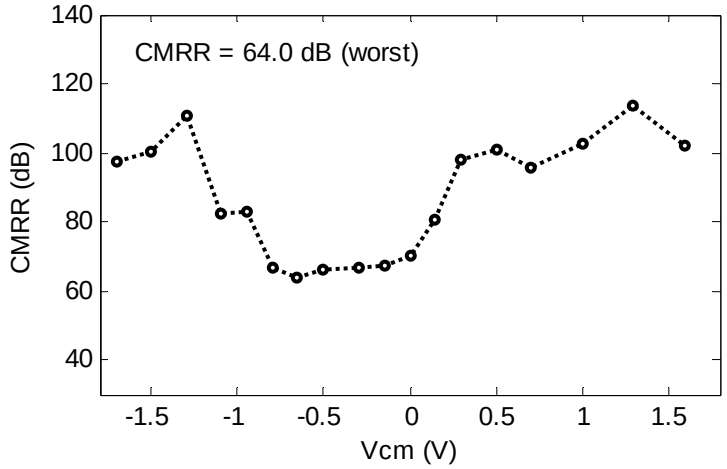

Figure 4.23 Measured CMRR versus the common-mode input voltage for UTA243.

Table 4.2 Performance Summary of UTA243.

Parameters	Value	Parameters	Value
V_{SUP}(min)	2.4 V	*CMRR*	62.9 dB (min)
CMIR	V_{EE} -0.3V to V_{CC}+0.3V	$PSRR^+$, $PSRR^-$	95.6 dB, 69.5 dB
V_{OUT}	V_{EE} +0.1V to V_{CC}-0.1V	SR^+, SR^-	3.8 V/μs, 4.1 V/μs
I_{SUP}	459 μA	A_{DC}	104.2 dB
I_{out} (max)	9.1 mA, -11.0 mA	*GBW*	11.3 MHz
V_{OS}	-0.58 mV to -1.02 mV	φ_M	64.5°

4.3 UTA244: Three-Stage Bipolar Op Amp with a Common-Mode Adapter Based on a Pseudo-Differential Pair

Figure 4.24 shows a single differential pair input stage with a common-mode adapter based on a pseudo-differential pair, which was discussed in Section 2.3.2. A three-stage bipolar op amp with this input stage is designed in this section. This op amp is named UTA244.

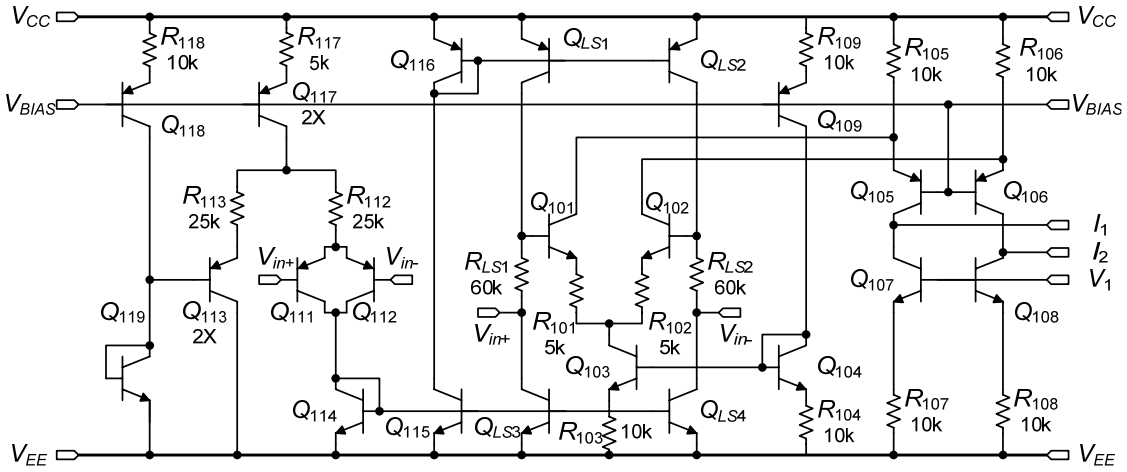

Figure 4.24 Rail-to-rail input stage with a single differential pair and a common-mode adapter based on a pseudo-differential pair.

The maximum level-shift current is limited by the current through Q_{117}, which is about 18 μA. The level-shift resistors, R_{LS1} and R_{LS2}, are 60 kΩ. So the maximum level-shift voltage is about 1 V. The emitter degeneration resistors R_{101} and R_{102} are added to the differential pair Q_{101} and Q_{102}. In order to use the same intermediate stage, output stage, and compensation circuit, the transconductance of the input stage should be the same as the transconductance of the input stages of UTA242 and UTA243. In this input stage, the tail current through the differential pair is about 9 μA, and the emitter degeneration resistors are 5 kΩ. So the transconductance is the same, but the slew rate is doubled [54]. For the complementary input stage, emitter degeneration resistors cannot be added, otherwise the total transconductance would not be constant in the transition region between the n-type and p-type pairs.

The input stage in Figure 4.24 with a single-ended output was fabricated. The micrograph of the input stage is shown in Figure 4.2. The transconductance of the input stage over the common-mode input range is given in Figure 4.25. The maximum value of the transconductance is about 57.3 μS, and the minimum value is about 54.3 μS, so the variation is about 6%. It also shows the common-mode input range is from $V_{EE} + 0.2$ V to $V_{DD} + 0.3$ V .

The op amp of UTA244 is the combination of the current reference circuit in Figure 4.5, the input stage in Figure 4.24, and the intermediate and output stages in Figure 4.4. UTA244 was fabricated with National Semiconductor VIP10 Process, and the micrograph of the chip is given in Figure 4.26.

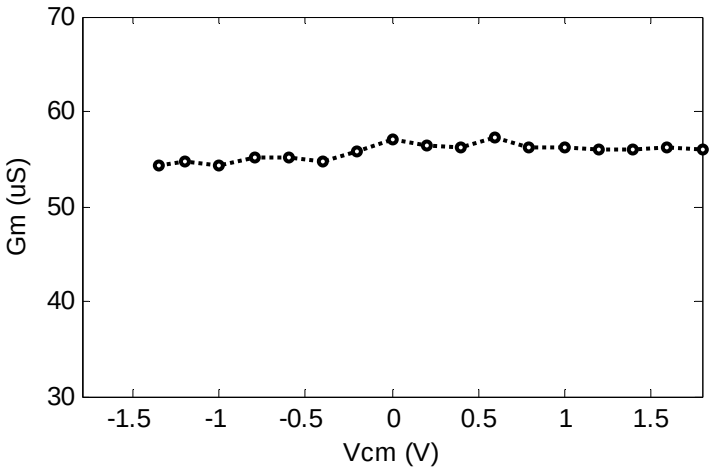

Figure 4.25 Measured transconductance versus the common-mode input voltage.

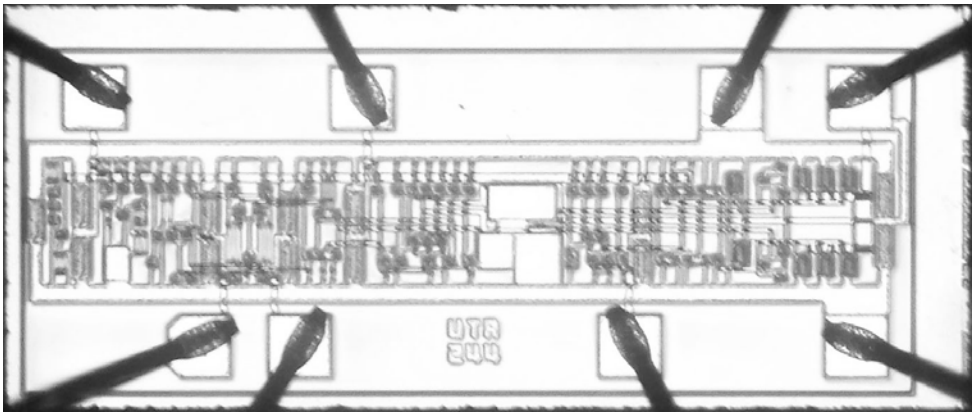

Figure 4.26 Micrograph of UTA244.

Figure 4.27 shows the simulated open-loop frequency response of the designed UTA244 for different common-mode input voltages, 0 V and ±1.3 V. The low-frequency open-loop gain is about 110 dB, the unity-gain frequency is about 13 MHz, and the phase margin is about 55˚.

Figure 4.28 shows the measured closed-loop gain versus the frequency for UTA244 in a non-inverting configuration with a gain of 11. The measured gain-bandwidth product is about 11.8 MHz.

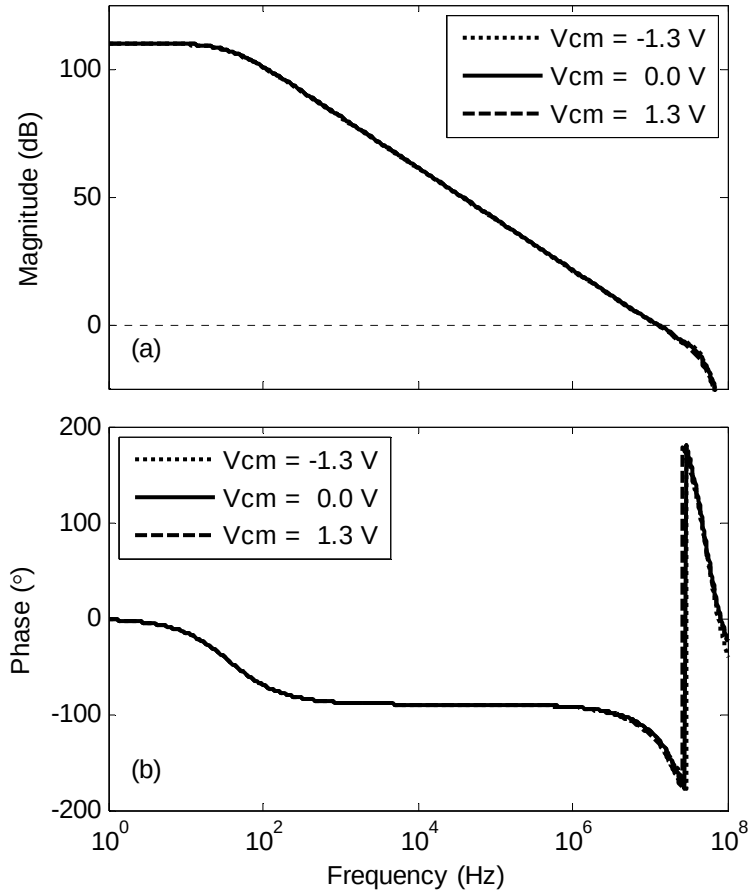

Figure 4.27 (a) Magnitude and (b) phase of the open-loop frequency response for UTA244 with different common-mode input voltages.

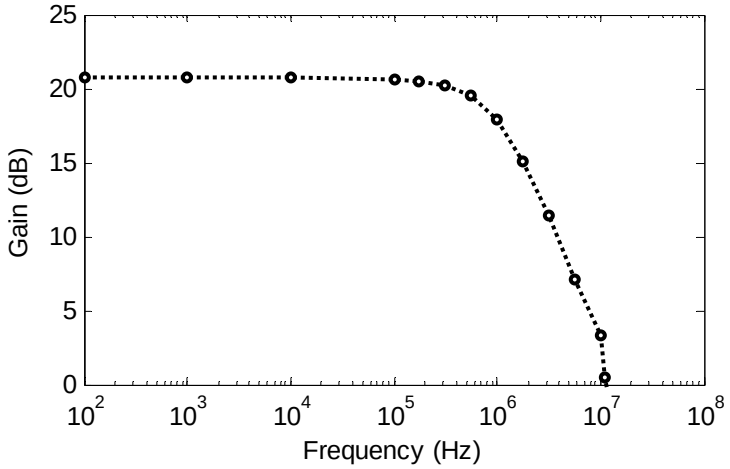

Figure 4.28 Measured closed-loop gain of UTA244 in a non-inverting amplifier configuration.

Figure 4.29, Figure 4.30, and Figure 4.31 show some experimental and simulated results for UTA244 in the unity-gain configuration. Figure 4.29 shows the DC input-output transfer characteristic. It is linear with unity gain when the input voltage is from -1.3 V to 1.4 V. Figure 4.30 shows the transient response to a pulse. The measured positive slew rate is about 7.6 V/μs, and the negative slew rate is about 7.4 V/μs. Figure 4.31 shows the transient response to a sine wave with the frequency of 250 kHz and the peak-to-peak amplitude of 2.6 V.

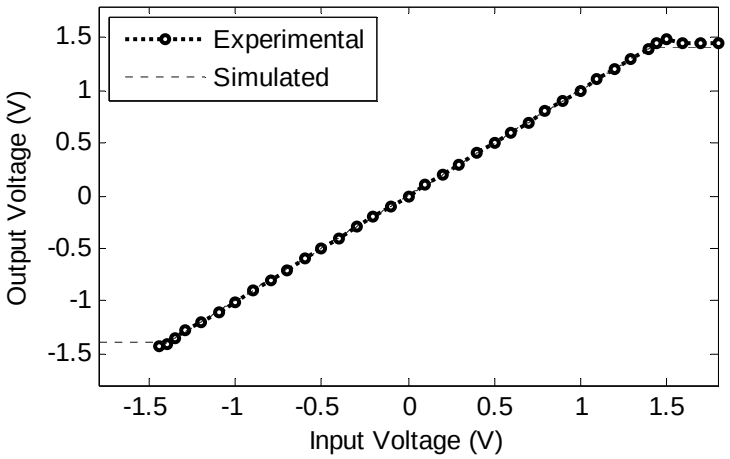

Figure 4.29 DC transfer curve of UTA244 in the unity-gain configuration.

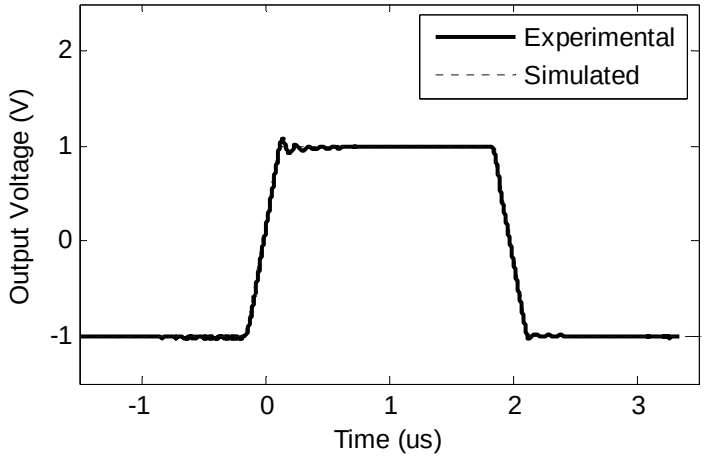

Figure 4.30 Transient response to a pulse of UTA244 in the unity-gain configuration.

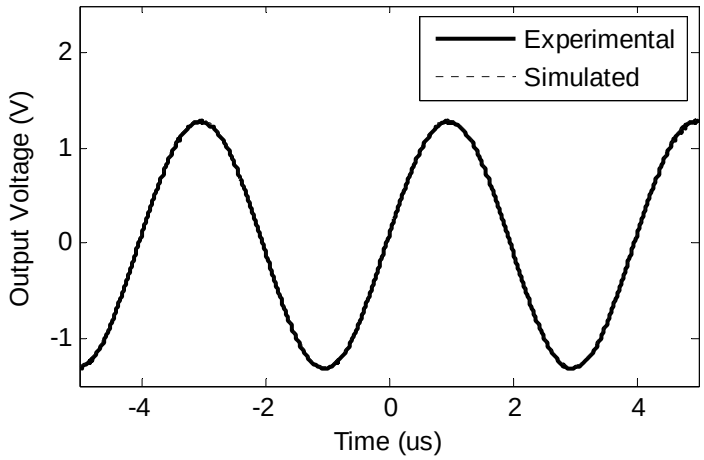

Figure 4.31 Transient response to a sine wave of UTA244 in the unity-gain configuration.

Figure 4.32 shows the measured offset voltage over the entire input common-mode voltage range. When the input voltage is greater than -0.2 V, the offset voltage is about -0.1 mV. In this range, the common-mode adapter circuit is not active. When the common-mode input voltage is less than -0.2 V and goes toward the negative supply rail, the absolute value of the offset voltage increase almost linearly. It reaches the maximum value of 3.9 mV. In this region, the common-mode adapter circuit is active, and it contributes an extra offset voltage of $\Delta(R_{LS}I_{LS})$. The level-shift current, I_{LS}, is a function of the common-mode input voltage. When the common-mode input voltage decreases and goes toward the negative supply rail, the level-shift current increases, and it introduces more offset voltage. Figure 4.33 shows the measured CMRR versus the common-mode input voltages. When the common-mode adapter is not active, the CMRR is about 100 dB; when the adapter circuit is starting to work, the CMRR begins to drop. The minimum value of the CMRR is about 47.2 dB.

As a summary, some performance aspects of UTA244 are given in Table 4.3.

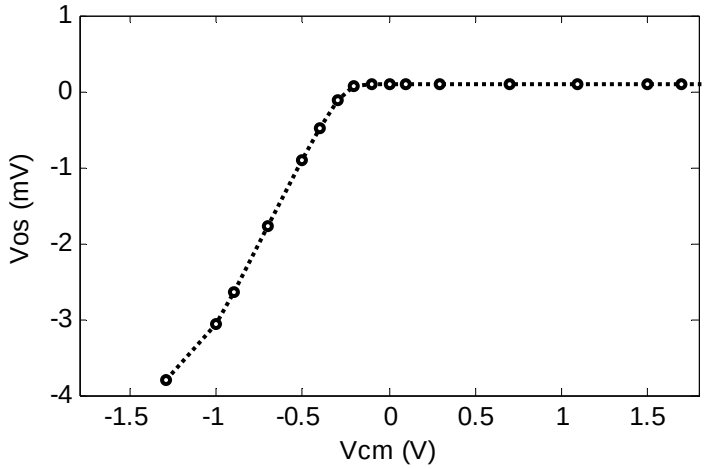

Figure 4.32 Measured offset voltage versus the common-mode input voltage for UTA244.

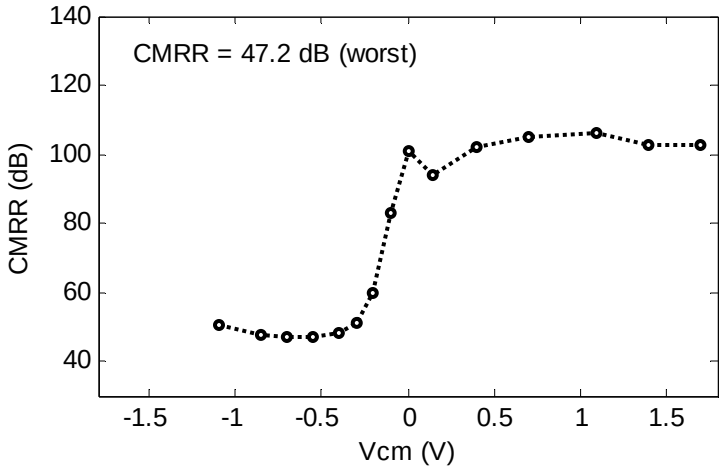

Figure 4.33 Measured CMRR versus the common-mode input voltage for UTA244.

Table 4.3 Performance Summary of UTA244.

Parameters	Value	Parameters	Value
$V_{SUP(\min)}$	2.4 V	*CMRR*	47.2 dB (min)
CMIR	V_{EE}+0.2V to V_{CC}+0.3V	$PSRR^+$, $PSRR^-$	95.2 dB, 92.5 dB
V_{OUT}	V_{EE}+0.1V to V_{CC}-0.1V	SR^+, SR^-	7.6 V/μs, 7.4 V/μs
I_{SUP}	470 μA to 517 μA	A_{DC}	105.6 dB
$I_{out\,(\max)}$	9.1 mA, -11.1 mA	*GBW*	11.8 MHz
V_{OS}	0.1 mV to 3.7 mV	φ_M	55°

4.4 OPA004: Two-Stage CMOS Op Amp with a Common-Mode Adapter Based on a Pseudo-Differential Pair

A two-stage CMOS op amp with the input stage in Figure 2.20 is designed. The overall op amp schematic is shown in Figure 4.34. This op amp is named OPA004. The op amp is designed with a 0.18 μm CMOS technology. The SPICE model parameters [61] are given in Appendix B. The threshold voltage of the NMOS transistor is about 0.48 V, and the threshold voltage of the PMOS transistor is about 0.45 V.

The bias circuit part provides three different bias voltages [9]. The input stage of OPA004 is discussed in Section 2.3.2. Transistors M_{18} and the diode connected M_{19} generate a reference voltage to bias M_{13}. The level-shift resistors, R_{LS1} and R_{LS2}, are 20 kΩ. The maximum level-shift current is limited by the current through M_{17}, which is about 10 μA. Because the W/L ratio of the level-shift transistors is 2.5 times of the W/L ratio of M_{14}, the maximum level-shift current is about 25 μA. So the maximum common-mode voltage it can shift is about 0.5 V. The class-A output stage is used in this op amp. The quiescent bias current for the output transistor M_{32} is about 50 μA. The Miller compensation is realized by capacitor C_C of 1.8 pF and M_C. M_C is in the deep triode region, and it acts as a resistor for the pole-zero cancellation [9].

Some simulations are performed for OPA004. The simulation setup and conditions are: the positive power voltage V_{CC} is +0.5 V; the negative power supply voltage V_{EE} is -0.5 V; the common-mode input voltage is biased at 0 V; the load is a 20 pF capacitor; the temperature is 25°C. The simulations in Section 4.4 and Section 4.5 are under these conditions if they are not specified.

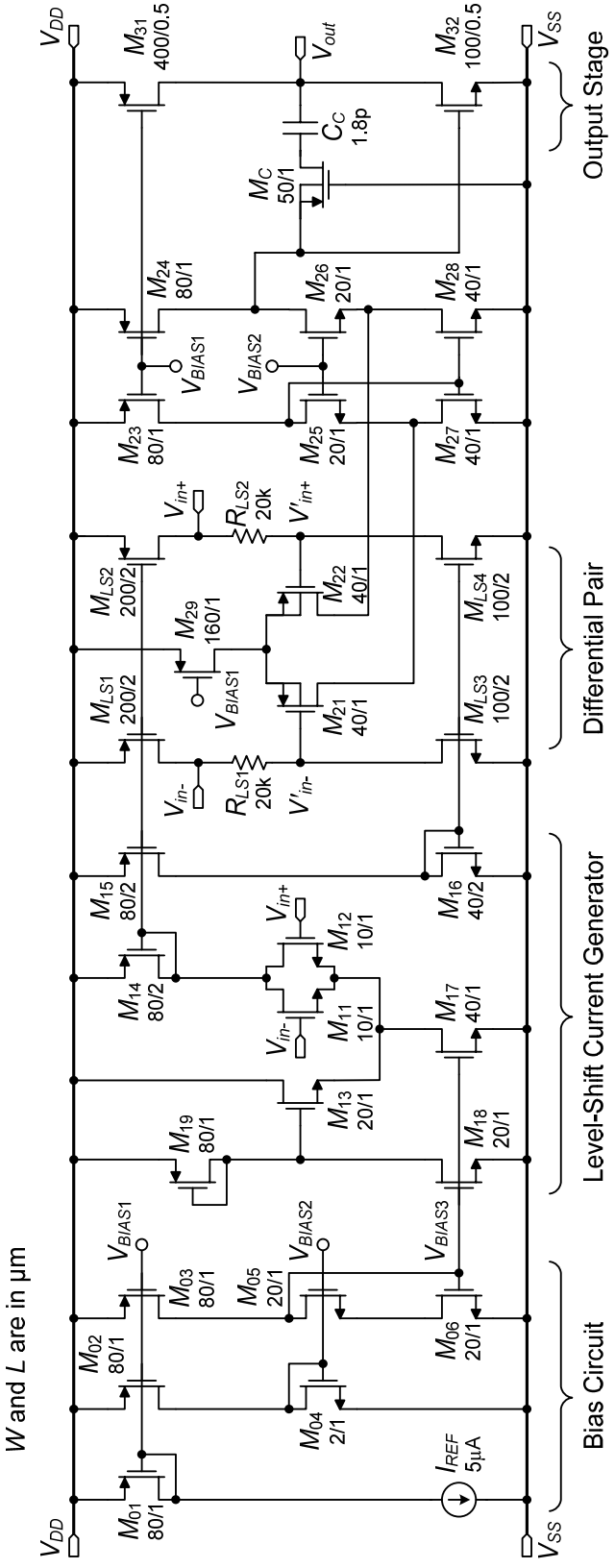

Figure 4.34 Complete circuit schematic of OPA004.

Figure 4.35 shows the open-loop frequency response of OPA004 for different common-mode input voltages. It shows the open-loop gain and phase shift are almost the same for different common-mode input voltages, 0 V and ±0.4 V. The low frequency gain is about 80 dB, the unity-gain frequency is about 6.1 MHz, and the phase margin is about 68˚.

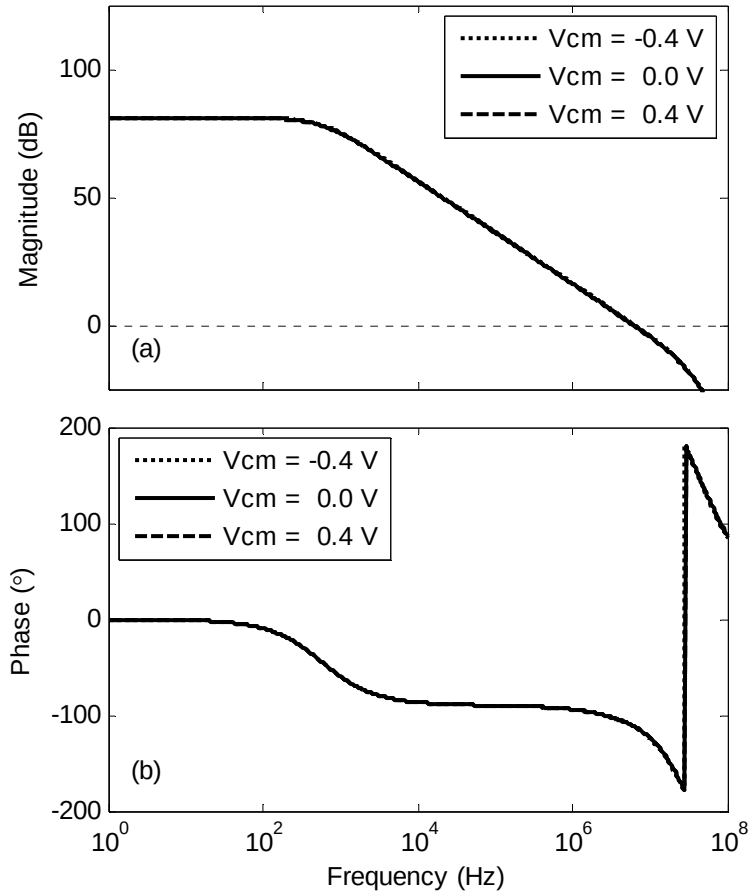

Figure 4.35 (a) Magnitude and (b) phase of the open-loop frequency response for OPA004 with different common-mode input voltages.

Figure 4.36 shows the simulated open-loop frequency response of OPA004 under different power-supply voltages, ±0.4V and ±0.5V. When the supply voltage is ±0.4 the open-loop gain is about 77.2 dB. There is about a 3 dB drop. The unity-gain

frequency decreases from 6.1 MHz to 4.7 MHz. When the supply voltage drops, some transistors work on the verge of the saturation region. Then output resistance transistors drops, which causes the gain drop.

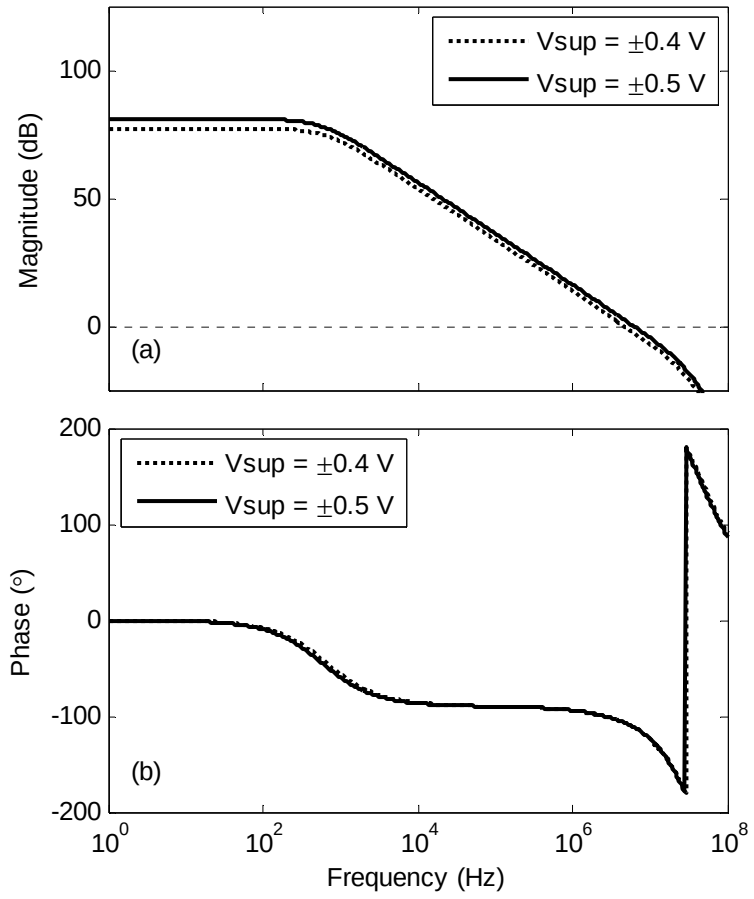

Figure 4.36 (a) Magnitude and (b) phase of the open-loop frequency response for OPA004 with different supply voltages.

Figure 4.37 shows the simulated DC input-output transfer curve of OPA004 in the unity-gain configuration. When the input voltage is from -0.45 V to 0.45 V, the transfer curve is linear and with unity gain. But when the input voltage is higher than 0.4 V, the level-shift current source transistors, M_{LS1} and M_{LS2}, are in the triode region.

In this region, performance aspects of the op amp like the input bias current, input resistance, and PSRR degrade significantly. So the upper limit of the CMIR is about $V_{DS(\text{sat})}$ below V_{DD}. Figure 4.38 shows simulated transient response to a pulse for OPA004 in the unity-gain configuration. The positive slew rate is about 2.1 V/μs, and the negative slew rate is about 3.1 V/μs.

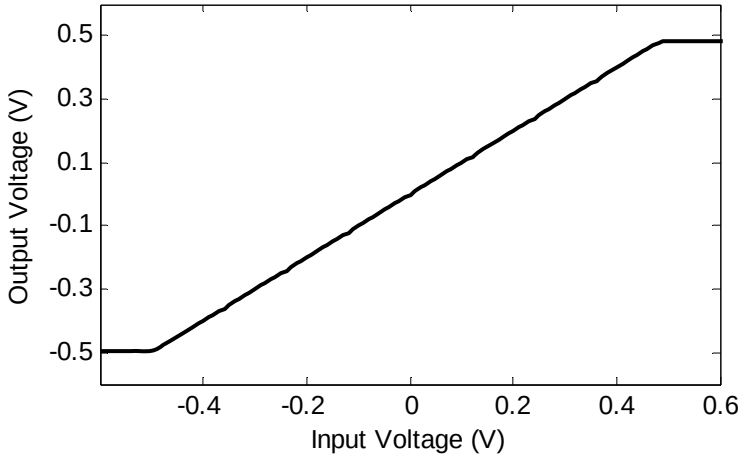

Figure 4.37 Simulated DC transfer curve of OPA004 in the unity-gain configuration.

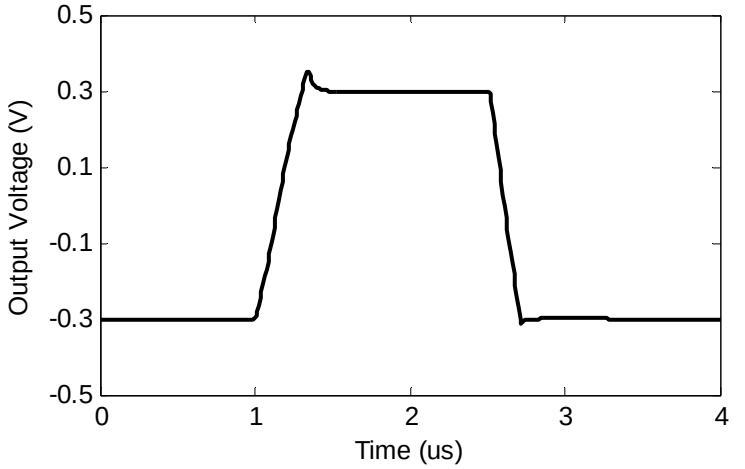

Figure 4.38 Simulated transient response to a pulse of OPA004 in the unity-gain configuration.

As a summary, some simulation results of OPA004 are given in Table 4.4. Because the offset voltage and CMRR are strongly dependent on the mismatch of the component in the op amp circuit, the simulation results are not given Table 4.4. In this table, f_u is the unity-grain frequency.

Table 4.4 Performance Summary of OPA004.

Parameters	Value	Parameters	Value
$V_{SUP(\min)}$	0.8 V	SR^+, SR^-	2.1 V/μs, 3.1 V/μs
$CMIR$	V_{SS}-0.2V to V_{DD}-0.1V	A_{DC}	80 dB
V_{OUT}	V_{SS}+0.05V to V_{DD}-0.05V	f_u	6.1 MHz
I_{SUP}	90 μA to 151 μA	φ_M	68.6°

4.5 OPA005: Two-Stage CMOS Op Amp with a Common-Mode Adapter Based on Current Subtraction

A two-stage CMOS op amp using the input stage in Figure 2.28 is designed in this section. The overall op amp schematic is shown in Figure 4.39. This op amp is named OPA005. The input stage of OPA005 is the rail-to-rail input stage with a single differential pair and a common-mode adapter based on current subtraction, which is discussed in Section 2.3.3. Transistor M_{17} and M_{18} are in cascode configuration, which are used to bias the drains of M_{11} and M_{12} at about $V_{DS(\text{sat})}$ above V_{SS}.

Some simulations are performed for OPA005. Figure 4.40 shows the open-loop frequency response of OPA005 for different common-mode voltages, 0V and ±0.4V. Obviously, the magnitude and phase are almost the same for different common-mode voltages. The low frequency open-loop gain is about 81 dB, the unity-gain frequency is about 6 MHz, and the phase margin is about 68˚.

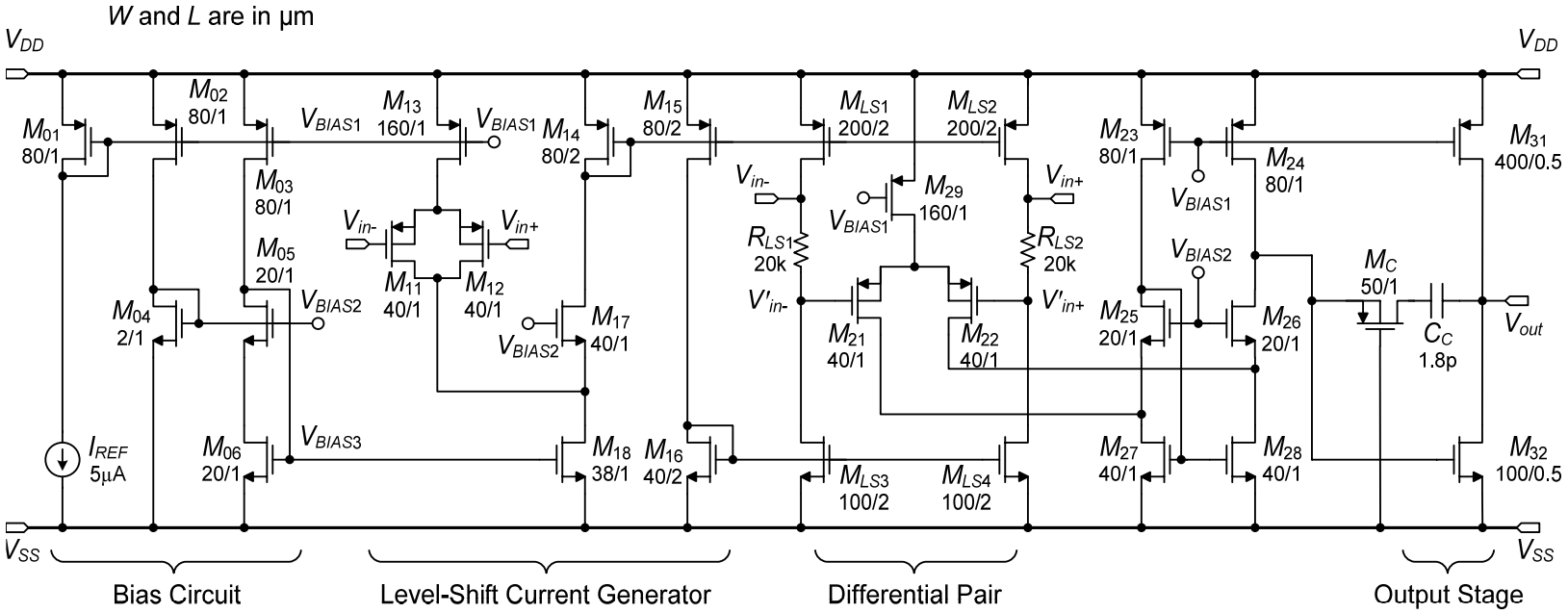

Figure 4.39 Complete circuit schematic of OPA005.

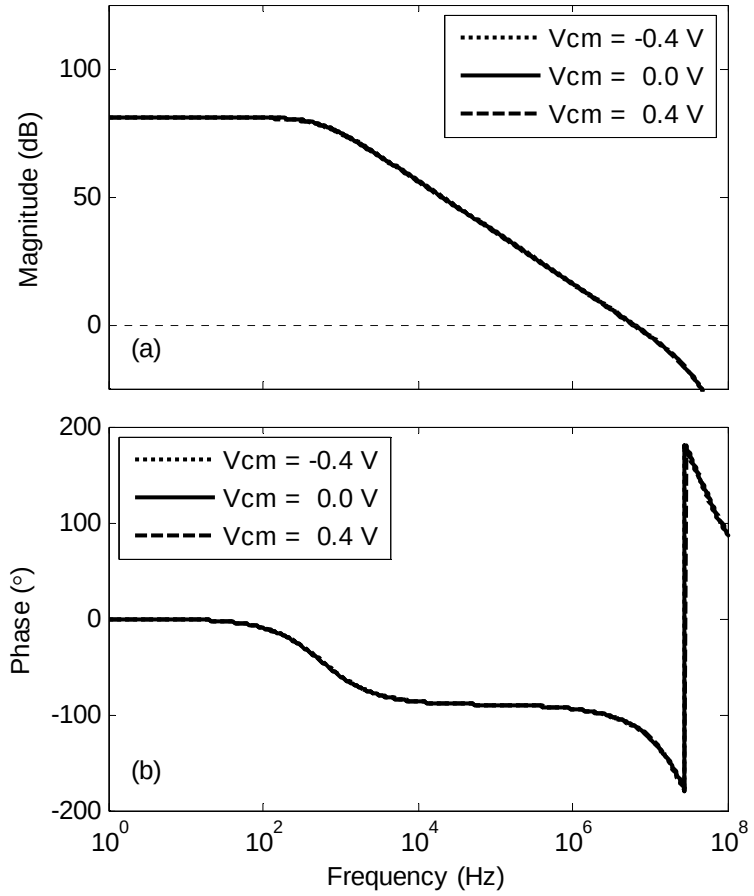

Figure 4.40 (a) Magnitude and (b) phase of the open-loop frequency response for OPA005 with different common-mode input voltages.

Figure 4.41 shows the open-loop frequency response of OPA004 under different power-supply voltages, ±0.4V and ±0.5V. When the power-supply voltage is ±0.4V, the open-loop gain drops from 81 dB to 74 dB, and the unity-gain frequency decreases from 6.3 MHz to 3.3 MHz.

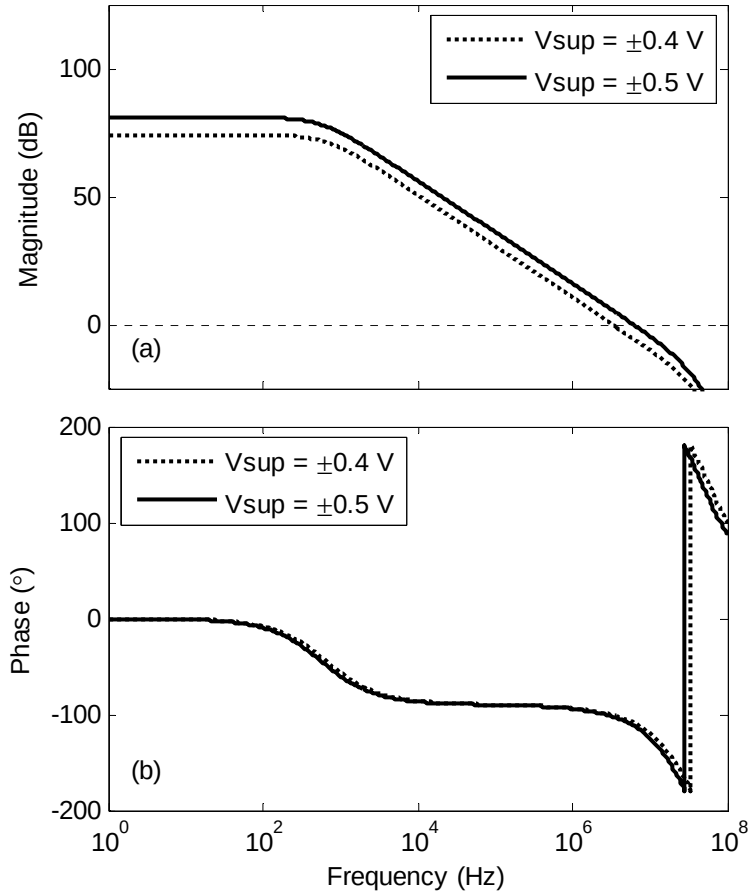

Figure 4.41 (a) Magnitude and (b) phase of the open-loop frequency response for OPA005 with different supply voltages.

Figure 4.42 shows the simulated DC input-output transfer curve of OPA005 in the unity-gain configuration. Both the input and the output can swing from rail to rail within 0.05 V. Figure 4.43 shows simulated transient response to a pulse of OPA005 in the unity-gain configuration. The simulated positive slew rate is about 1.7 V/μs, and the negative slew rate is about 3.2 V/μs.

As a summary, some simulation results of OPA005 are given in Table 4.5.

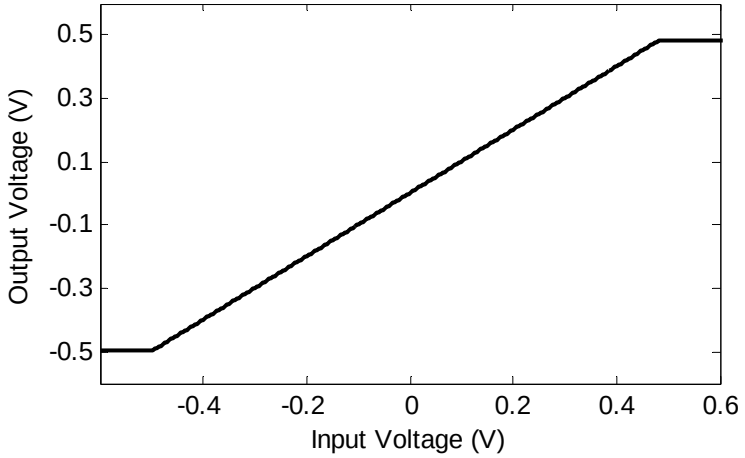

Figure 4.42 Simulated DC transfer curve of OPA005 in the unity-gain configuration.

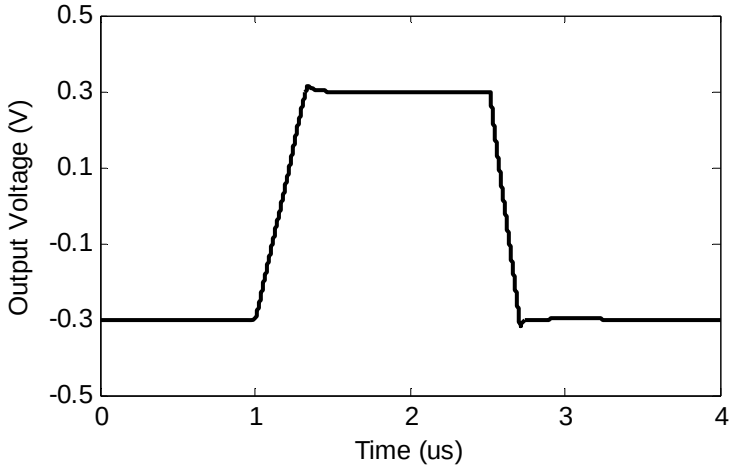

Figure 4.43 Simulated transient response to a pulse of OPA005 in the unity-gain configuration.

Table 4.5 Performance Summary of OPA005.

Parameters	Value	Parameters	Value
$V_{SUP(\min)}$	0.8 V	SR^+, SR^-	1.7 V/μs, 3.2 V/μs
CMIR	V_{SS}-0.2V to V_{DD}-0.1V	A_{DC}	81 dB
V_{OUT}	V_{SS}+0.05V to V_{DD}-0.05V	f_u	6.2 MHz
I_{SUP}	92 μA to 152 μA	φ_M	68.4°

4.6 Summary

Three different three-stage bipolar op amps and two different two-stage CMOS op amps have been designed. The simulation and chip test results are also given in this chapter.

Three three-stage bipolar op amps with the same intermediate and output stages but different input stages were discussed. The op amps of UTA242 and UTA243 have input stages based on complementary differential pairs. UTA242 has a constant-G_m complementary input stage. The constant transconductance is realized by means of making the total current through the pnp and npn pairs constant. UTA243 has constant-G_m complementary input stage with improved CMRR. The CMRR is improved by making the transition from pnp pair to npn pair gradually, i.e., increasing the transition region between the pnp and npn pairs. UTA244 has an input stage with a single differential pair and a common-mode adapter based on a pseudo-differential pair. The advantage of the op amp with a single differential pair is that the minimum power-supply voltage is about $V_{BE} + 2V_{CE(\text{sat})}$.

The designed two rail-to-rail two-stage CMOS op amps have input stages with a single differential pair and a common-mode adapter. The first CMOS op amp, OPA004, has an input stage with a common-mode adapter based on a pseudo-differential pair structure. The second CMOS op amp, OPA005, has an input stage with a common-mode adapter based on current subtraction.

CHAPTER 5

FUCTIONALITY ANALYSIS OF OPERATIONAL AMPLIFIERS

The performance of an op amp is determined by performance parameters [62] such as input offset voltage, common-mode rejection ratio, slew rate, open-loop gain, gain-bandwidth product, and phase margin. For different op amp designs, each design has its advantages and disadvantages. In other words, each design is only good at some certain aspects of performance, but not all of them. Assuming that each aspect of performance has the same importance, it is desirable to combine all the aspects into a single figure of merit to reflect the overall performance of each op amp. In this chapter, the General System Performance Theory (GSPT) [16, 63] is applied to characterize all performance aspects with one single parameter. A brief introduction to the GSPT is given in Section 5.1. Then the application of GSPT to functionality analysis and comparison of op amps is given in Section 5.2.

5.1 General System Performance Theory

The General Systems Performance Theory [16] is a systematic method for system performance analysis. It has been widely applied to human performance measurement and analysis [17, 64]. In [65], GSPT was used to measure education and training outcomes. In [66], it was applied on current reference circuits functionality analysis and comparison.

In the GSPT, the performance is defined as how well the system executes a specified function. Because a system may consist of more than one performance aspect, system performance has multidimensional properties. So the system performance is analyzed in a multidimensional space. Each dimension is called a dimension of performance (DOP) [16]. For each DOP, a metric is defined so that the value is always non-negative, and a large value always means better performance [16].

The performance of a system is interpreted as the available resource [16], and it is expressed as R_A for each DOP. The available resources determine the performance capacity envelop (PCE) as shown in Figure 5.1. In GSPT, a system is always analyzed with respect to a task. Each task is represented by a point in a multidimensional performance space. The task demand is the required resource to complete the task, and it is expressed as R_D for each DOP. If $R_D \leq R_A$ for each DOP, i.e., the task is located inside or on the PCE, the system is able to complete the task. If $R_D > R_A$ for any DOP, i.e., the task is located outside the PCE, the system fails to complete the task. In Figure 5.1, task *i* and task *j* are represented by points in a two-dimensional performance space. Task *i* is inside of the PCE, and the system can fulfill the task. Task *j* point is outside of the PCE, and the system cannot fulfill the task.

To apply the GSPT method, at first, the function associated with this potentially multifunctional system must be identified. Then the DOP needs to be determined for each aspect of performance. The performance can be a constant or varying quantity [66]. For the constant quantity case, the performance does not change, and the DOP is easy to define for this case [16, 63]. For the varying quantity case, the performance of

the system changes when a certain environmental parameter [66] changes. In [66], the functionality volume concept was proposed. The DOP of the varying quantity can be defined with the help of the functionality volume.

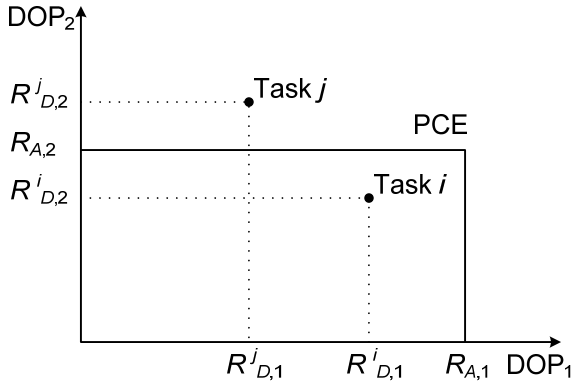

Figure 5.1 Representation of "success" and "fail" of a system in two-dimensional idealized system-task interface.

When the actual quantity changes because of a change in the environmental parameter, the actual performance is a curve in the performance-environment space (PES) [66], as shown in Figure 5.2 and Figure 5.3. The ideal performance curve and the actual performance curve never converge. There is always a non-zero area between these two curves. The area is defined as the functionality volume (FV) [66]. It stands for area for 2-D PES, and it only stands for volume for 3-D PES. The functionality volume represents the deviations between the actual performance and the ideal performance. It is the area of region 1 in Figure 5.2 or the sum of the area of region 1 and the area of region 3 in Figure 5.3. There is usually a difference between the task demand curve and the ideal performance curve. The area between these two curves is defined as the demand volume (DV) [66]. It is the sum of the area of region 1 and the area of region 2 in Figure 5.2 or Figure 5.3.

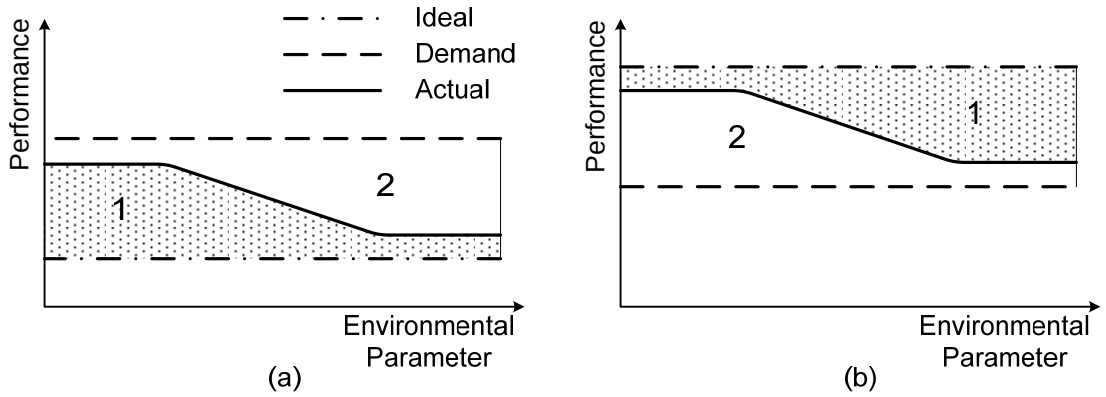

Figure 5.2 Performance versus an environmental parameter when task demands are met at all operating points. (a) Performance is the-lower-the-better case, and (b) performance is the-higher-the-better case.

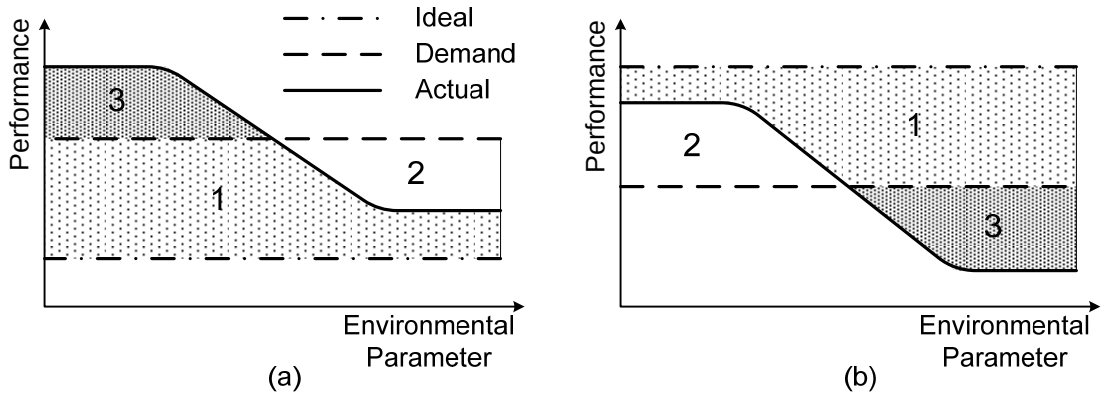

Figure 5.3 Performance versus an environmental parameter when task demands are not met at all operating points. (a) Performance is the-lower-the-better case, and (b) performance is the-higher-the-better case.

There are two different cases. The first one is task demands are met at all operating points as shown in Figure 5.2, and the second one is the task demands are not met at all operating points as shown in Figure 5.3.

If the task is completed at all operating points, the DOP is defined as the ratio of the demand volume to the functional volume. It should be pointed out that the "performance" and DOP are two different concepts in GSPT. The DOP is defined for

each performance aspect. The "performance" does not have to be the-higher-the-better; it can also be the-lower-the-better. Both cases are shown in Figure 5.2 and Figure 5.3.

If task demands are not met at all operating points, the concept of useful functional volume (UFV) [66] needs to be used. It is represented by area of region 1 in Figure 5.3. For this case, the DOP is defined as the ratio of useful functional volume to the functional volume. So the DOP of varying quantities can be defined by [66]

$$DOP = \begin{cases} DV/FV & \text{The task is completed at all operating point} \\ UFV/FV & \text{The task is not completed at all operating point} \end{cases} \tag{5.1}$$

The definition in (5.1) satisfies both requirements of the DOP metric. It can be interpreted as [66]

$$DOP \begin{cases} <1 & \text{The task demands are not satisfied} \\ =1 & \text{The task demands are satisfied exactly} \\ >1 & \text{The task demand are satisfied} \end{cases} \tag{5.2}$$

It should be mentioned that if the task demand is not satisfied at any operating point, the value of DOP is zero.

In order to convert all the DOPs into a single figure of merit, the concept of composite performance capacity (CPC) [16] can be used. The CPC is defined as

$$CPC = \prod_{i=1}^{n} DOP_i \tag{5.3}$$

where n is the total number of aspects of performance under consideration, and DOP_i is the ith DOP. Obviously, the higher the value of the CPC, the better the overall performance of the system.

5.2 Functionality Analysis of Op Amps

Three different three-stage bipolar op amps, UTA242, UTA243, and UTA244 designed in Chapter 4, are compared by using the GSPT in this section. In order to apply the GSPT to the comparison of op amps, it is necessary to identify the performance parameters associate with the potential multifunctional system. The three-stage op amps considered in this chapter have the same intermediate and output stages but different input stages. So only the performance parameters related to the input stage are considered here. The performance parameters chosen for comparison are the common-mode input range (*CMIR*), slew rate (*SR*), power-supply rejection ratio (*PSRR*), offset voltage (V_{OS}), common-mode rejection ratio (*CMRR*), and quiescent supply current (I_{SUP}).

5.2.1 Common-Mode Input Range

The common-mode input range specifies the range of the common-mode voltage over which normal operation is guaranteed. Assuming that the task demand of the magnitude of the CMIR is $V_{CC} - V_{EE}$, the DOP of the CMIR is defined as

$$DOP(CMIR) = \frac{|CMIR|}{V_{CC} - V_{EE}} = \frac{V_{CM(\max)} - V_{CM(\min)}}{V_{CC} - V_{EE}} \tag{5.4}$$

where $V_{CM(\max)}$ and $V_{CM(\min)}$ are the maximum and minimum values of the common-mode input voltage range, respectively. According to the definition in (5.4), the DOP of the CMIR is dimensionless. Here, V_{CC} equals 1.5 V, and V_{EE} equals -1.5 V. The measured CMIR and the corresponding DOP for UTA242, UTA243, and UTA244 are given in Table 5.1.

Table 5.1 CMIR and the Corresponding DOP.

	UTA242	UTA243	UTA244
CMIR	-1.8 V to 1.8 V	-1.8 V to 1.8 V	-1.3 V to 1.8 V
DOP(CMIR)	1.2	1.2	1.033

5.2.2 Slew Rate

The slew rate of an op amp is the maximum rate of change of the output voltage. For an op amp, the positive slew rate, SR^+, can be different from the negative slew rates, SR^-. Here the smaller value of the positive and negative slew rates is used to define the DOP. Assuming that the task demand of the slew rate is 3 V/μs, the DOP of the slew rate is defined as

$$DOP(SR) = \frac{SR \text{ in V/μs}}{3\text{V/μs}} \tag{5.5}$$

According to the definition in (5.5), the DOP of the slew rate is dimensionless. The measured slew rate and the corresponding DOP for UTA242, UTA243, and UTA244 are given in Table 5.2.

Table 5.2 Slew Rate and the Corresponding DOP.

	UTA242	UTA243	UTA244
SR^+ (V/μs)	4.2	3.8	7.6
SR^- (V/μs)	4.1	4.1	7.4
DOP(SR)	1.367	1.267	2.467

5.2.3 Power-Supply Rejection Ratio

In practice, the power supply voltages are not constant. The variations of the power supply voltages contribute to the output of the op amp. So there is a small-signal

gain from the power supplies to the output. The power supply rejection ratio is defined as the ratio of the open-loop gain of the op amp and the small-signal gain from the power supply to the output. The positive power-supply rejection ratio, $PSRR^+$, can be different from the negative power-supply rejection ratio, $PSRR^-$. Here the smaller value of $PSRR^+$ and $PSRR^-$ is used to define the DOP. Assuming that the task demand of the PSRR is 60 dB, the DOP of the PSRR is defined as

$$DOP(PSRR) = \frac{20\log_{10}(PSRR)}{60} = \frac{PSRR \text{ in dB}}{60} \tag{5.6}$$

The measured PSRR and the corresponding DOP for UTA242, UTA243, and UTA244 are given in Table 5.3.

Table 5.3 PSRR and the Corresponding DOP.

	UTA242	UTA243	UTA244
$PSRR^+$ (dB)	92.9	95.6	95.2
$PSRR^-$ (dB)	96.4	69.5	92.5
DOP(PSRR)	1.548	1.158	1.542

5.2.4 Input Offset Voltage

The input offset voltage is defined as the DC voltage that must be applied between the input terminals to force the output to be zero. For the rail-to-rail op amps, the offset voltage varies with different common-mode input voltages. So the offset voltage is a varying quantity, and the DOP definition according to (5.1) must be applied to this case. Since the offset voltage could be positive or negative, here the absolute value of the offset voltage, $|V_{OS}|$, is used to define the corresponding DOP. It can be represented as

$$\text{performance}\left(V_{OS}\right) = \left|V_{OS}\right| \tag{5.7}$$

For the absolute value of the offset voltage, the lower is the better. The ideal value is zero. The task demand is assumed to be 1.0 mV. Figure 5.4 shows the ideal, task demand, and actual performance of the absolute value of the offset voltage for UTA242, UTA243, and UTA244. The corresponding DOP of the offset voltage are shown in Figure 5.4.

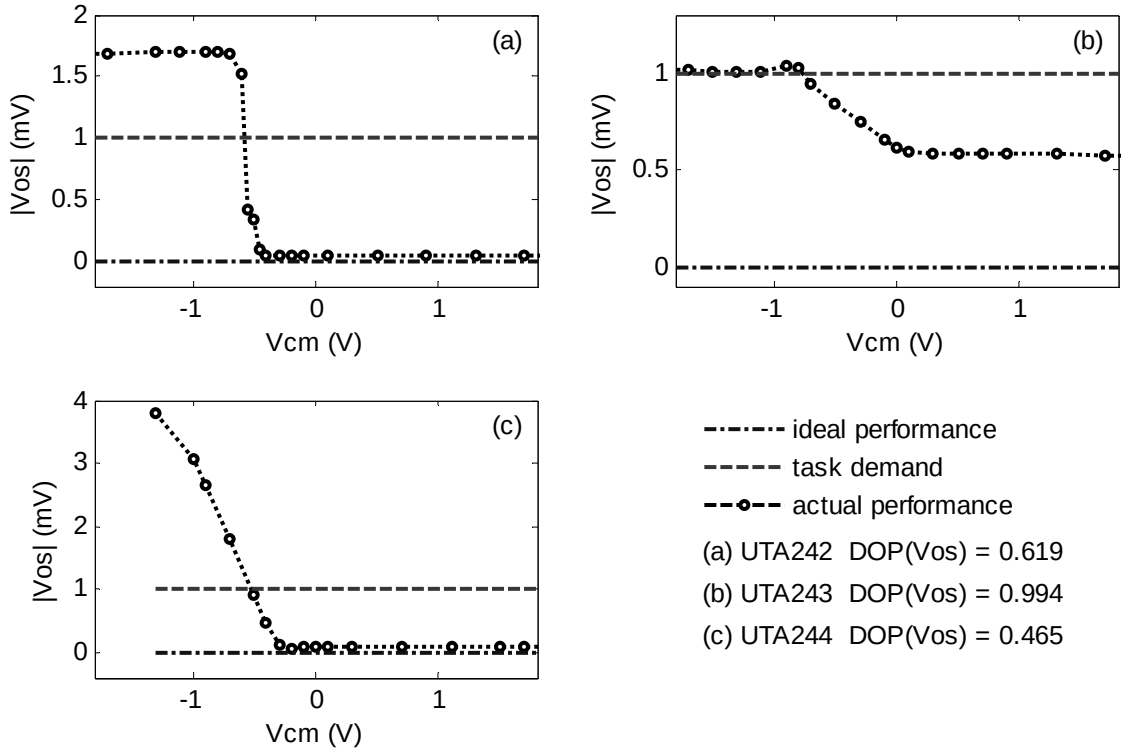

Figure 5.4 Ideal, task demand, and actual performance of the offset voltages for (a) UTA242, (b) UTA243, and (c) UTA244.

5.2.5 Common-Mode Rejection Ratio

The definition of CMRR is defined as the ratio of differential-mode gain to the common-mode gain. Usually, CMRR is a function of frequency. Here only the CMRR at DC is considered. The CMRR varies with the change of the common-mode input

voltage. The task demand for CMRR is assumed to be 80 dB. Since CMRR is the higher the better, the ideal value for CMRR is infinity, and the functional volume is also infinity. In order to solve this problem, a new aspect of performance can be defined as the reciprocal of the CMRR (in dB), which can be expressed as

$$\text{Performance}\left(CMRR\right) = \frac{1}{20\log_{10}\left(CMRR\right)} = \frac{1}{CMRR \text{ in dB}} \tag{5.8}$$

According to (5.8), the ideal value of the new performance aspect of the CMRR is zero, and the task demand is converted to 1/80. Figure 5.5 shows the ideal, task demand, and actual performances of the CMRR for UTA242, UTA243, and UTA244. The corresponding DOP of the CMRR are shown in Figure 5.5.

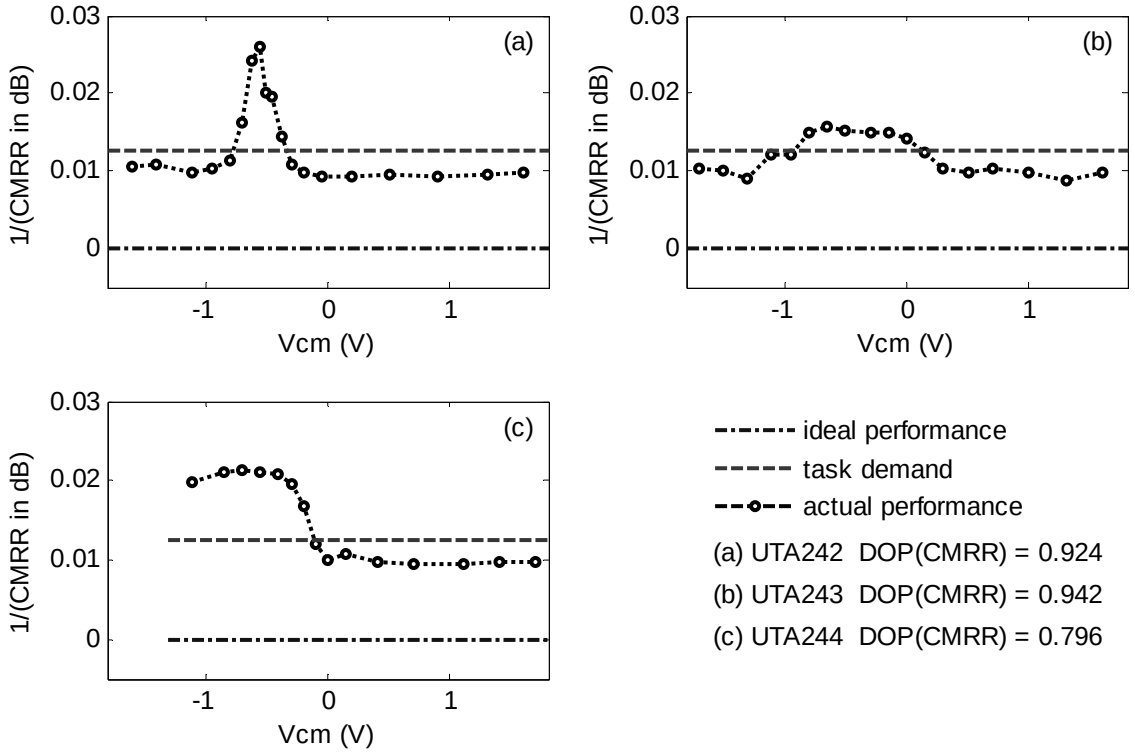

Figure 5.5 Ideal, task demand, and actual performance of the CMRR for (a) UTA242, (b) UTA243, and (c) UTA244.

5.2.6 Quiescent Supply Current

The quiescent supply current of the op amp is the supply current when the output current is zero. It is the smaller the better, and the ideal performance of the quiescent current is zero. The task demand of the quiescent supply current is assumed to be 1.0 mA. The supply current varies with different common-mode input voltages. Especially for UTA244, with different common mode input voltage, the level-shift current needed is different. Figure 5.6 shows the ideal, demand, and actual performance of the quiescent supply current for UTA242, UTA243, and UTA244. The corresponding DOP are shown in Figure 5.6.

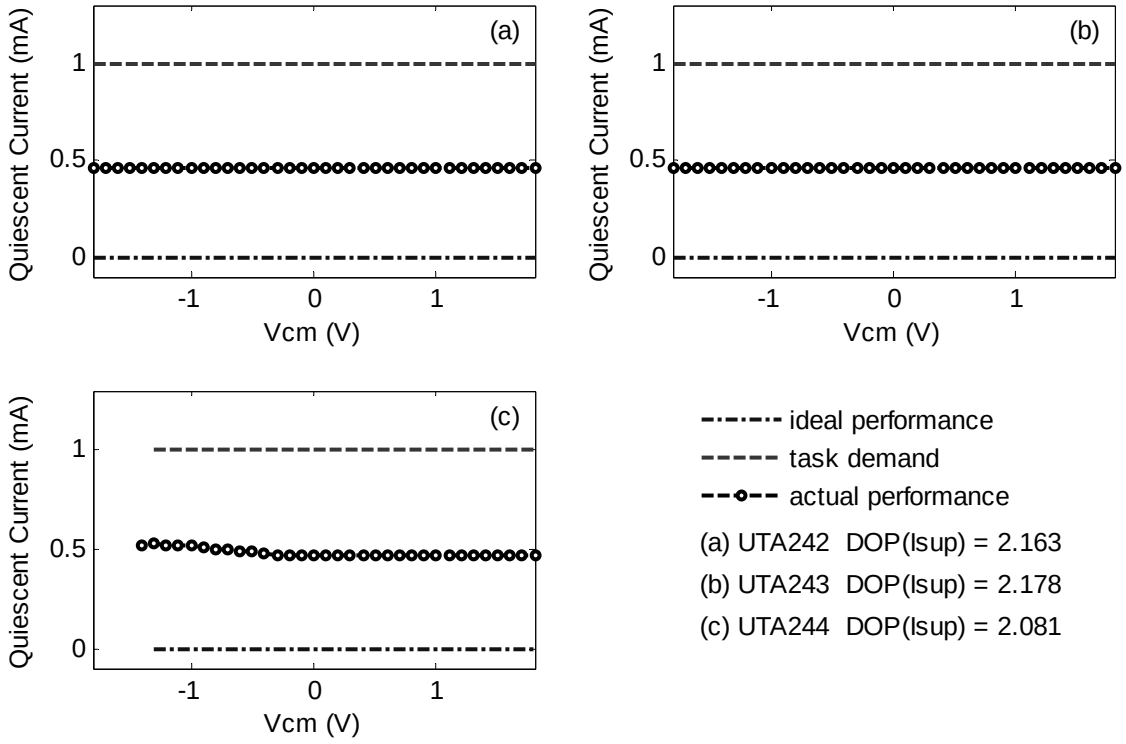

Figure 5.6 Ideal, task demand, and actual performance of the quiescent supply current for (a) UTA242, (b) UTA243, and (c) UTA244.

5.2.7 Composite Performance Capacity

So far the DOPs of the three op amps have been calculated. In order to get a single figure of merit, the CPC can be calculated according to (5.3). Equation (5.3) indicates that the higher the value of the CPC, the better the performance of the overall system. Table 5.4 gives the DOPs and CPCs of the designed three op amps. UTA243 has the highest value of the CPC, so UTA243 has the best overall performance.

Table 5.4 Functionality Comparison of Op Amps.

	UTA242	UTA243	UTA244
DOP(*CMIR*)	1.200	1.200	1.033
DOP(*SR*)	1.367	1.267	2.467
DOP(*PSRR*)	1.548	1.158	1.542
DOP(V_{OS})	0.619	0.994	0.465
DOP(*CMRR*)	0.924	0.942	0.796
DOP(I_{SUP})	2.163	2.178	2.081
CPC	3.142	3.591	3.027

5.3 Summary

In this chapter, the General System Performance Theory has been applied to compare the overall performance of the three bipolar rail-to-rail op amps. The beauty of applying the GSPT in op amp comparison is that a single figure of merit can be obtained. Since the three op amps have different input stages but the same intermediate stage and output stages, only the performance aspects related to the input stage are considered. The comparison result shows UTA 243, the op amp with CMRR-improved input stage, has the best overall performance.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

For low power-supply voltage, the rail-to-rail common-mode input range and output swing are desired for op amps. This dissertation investigated op amps with rail-to-rail input and output capability. The main goal of this dissertation is to design rail-to-rail constant-G_m input stages. The rail-to-rail input stage can be implemented by using the n-type and p-type differential pairs in parallel. The constant transconductance can be realized by making the sum of the current through the npn and pnp differential pairs constant for bipolar technology or making the sum of the square root of the current through the NMOS and PMOS differential pair constant. One drawback of the complementary input stage is that the required minimum supply voltage is about $2V_{BE} + 2V_{CE(\text{sat})}$ for the bipolar technology or $2V_{GS} + 2V_{DS(\text{sat})}$ for the CMOS technology. Another drawback is that the CMRR is poor during the transition region from p-type to n-type differential pairs. In this dissertation, a bipolar rail-to-rail input stage based on complementary differential pairs, which has better CMRR performance, was designed. The CMRR is improved by means of increasing the transition range between the p-type and n-type differential pairs.

The rail-to-rail input stage can also be implemented based on a single differential pair with a common-mode adapter. Since there is only one differential pair, the transconductance is constant as long as the tail current does not change. The advantage of this kind of input stages is that the required minimum power supply is about $V_{BE} + 2V_{CE(\text{sat})}$ for the bipolar technology or $V_{GS} + 2V_{DS(\text{sat})}$ for the CMOS technology.

Two new rail-to-rail input stages with a single differential pair and a common-mode adapter were presented. The first input stage is with a common-mode adapter based on a pseudo-differential pair structure; the second one is with a common-mode adapter based on current subtraction.

Three different three-stage rail-to-rail input and output bipolar op amps and two different two-stage rail-to-rail input and output CMOS op amps were designed. The designed bipolar op amps have different input stages but the same intermediate and output stages. These three bipolar op amp were fabricated, and the chip test results were given in this dissertation.

The performance of an op amp is indicated by specification parameters. One op amp may be good at some aspects but poor at others. The General System Performance Theory is a systematic method for system performance analysis. It combines all the performance aspects into a single figure of merit. In this dissertation, the General System Performance Theory was applied to compare the performance of the designed three different three-stage bipolar op amps. The result shows the op amp with CMRR improved complementary input stage has the best overall performance.

6.2 Future Work

Not all the op amp specification parameters were measured because of the lack of measurement equipments. Some parameters like harmonic distortion, noise, and phase noise were not measured in this dissertation.

This dissertation mainly focuses on the rail-to-rail constant-G_m input stage design. The overall performance of the op amps might not be optimized. The output stage for the three-stage bipolar op amps is a feedback-controlled class-AB Darlington output stage. The minimum supply voltage for this output stage is about $3V_{BE} + V_{CE(\text{sat})}$. The minimum supply voltage for the whole op amp is limited by the output stage. In order to reduce the minimum supply voltage, a new rail-to-rail class-AB output stage with lower minimum supply voltage needs to be designed.

One drawback of the rail-to-rail input stage is the poor CMRR, which is due to the offset voltage variation as a function of the common-mode input voltage. For a complementary input stage, the offset voltage can vary significantly during the transition between the n-type and p-type pairs. Though the device component mismatch is a random process, a statistical analysis can be investigated to find a good layout pattern to minimize the offset voltages and the variation of the offset voltage as a function of the common-mode input voltage.

APPENDIX A

BIPOLAR TRANSISTOR SPICE MODELS [24]

```
MODEL   QNPN   BJT      npn     = YES          pnp     = NO
IS      = 6.060E-18     BF      = 120.0        NF      = 1.000
VAF     = 156.0         IKF     = 3.040E-3     ISE     = 1.260E-15
NE      = 2.000         BR      = 3.000        NR      = 1.000
VAR     = 5.000         IKR     = 3.040E-2     ISC     = 6.060E-17
NC      = 1.000         RB      = 400.0        IRB     = 1.000E-3
RBM     = 30.0          RE      = 15.0         RC      = 22.5
CJE     = 3.0E-14       VJE     = 0.928        MJE     = 0.333
TF      = 1.769E-11     XTF     = 10.0         VTF     = 3.500
ITF     = 1.0E-3        PTF     = 25.0         CJC     = 1.800E-14
VJC     = 0.732         MJC     = 0.250        XCJC    = 1.0
TR      = 1.769E-9      CJS     = 5.000E-15    VJS     = 0.655
MJS     = 0.0           XTB     = 0.0          EG      = 1.126
XTI     = 4.0           KF      = 1.0E-9       AF      = 2.0
FC      = 0.5           TNOM    = 25           LATERAL = NO

MODEL   QPNP   BJT      npn     = NO           pnp     = YES
IS      = 2.6912E-18    BF      = 65.0         NF      = 1.000
VAF     = 52.0          IKF     = 1.350E-3     ISE     = 1.256E-15
NE      = 2.5           BR      = 4.0          NR      = 1.0
VAR     = 3.0           IKR     = 1.35E-2      ISC     = 2.691E-17
NC      = 1.00          RB      = 177.78       IRB     = 4.440E-4
RBM     = 13.33         RE      = 33.75        RC      = 22.5
CJE     = 3.0E-14       VJE     = 0.928        MJE     = 0.333
TF      = 1.990E-11     XTF     = 100.0        VTF     = 1.50
ITF     = 1.350E-3      PTF     = 30.0         CJC     = 3.000E-14
VJC     = 0.732         MJC     = 0.45         XCJC    = 1.0
TR      = 1.990E-9      CJS     = 5.000E-15    VJS     = 0.655
MJS     = 0.0           XTB     = 0.0          EG      = 1.126
XTI     = 4.0           KF      = 1.0E-9       AF      = 2.0
FC      = 0.5           TNOM    = 25           LATERAL = NO
```

APPENDIX B

CMOS TRANSISTOR SPICE MODELS [61]

```
MODEL NCH018 MOSFET
NOIMOD  = 1             AF      = 1.021         EF      = 0.874
KF      = 2.69E-28      TNOM    = 25            VERSION = 3.2
TOX     = 4.08E-09      TOXM    = 4.08E-9       XJ      = 1.60E-7
NCH     = 3.9000E+17    LLN     = 1.00          LWN     = 1.00
WLN     = 1.00          WWN     = 1.00          LINT    = 1.00E-8
LL      = 0.00          LW      = 0.00          LWL     = 0.00
WINT    = 1.00E-8       WL      = 0.00          WW      = 0.00
WWL     = 0.00          MOBMOD  = 1             BINUNIT = 2
XL      = -2E-8         XW      = 1E-6          WMLT    = 1
DWG     = 0.00          DWB     = 0.00          ACM     = 12
LDIF    = 9.00E-8       HDIF    = 2.00E-7       RSH     = 6.8
RD      = 0             RS      = 0             RSC     = 0
RDC     = 0             VTH0    = 0.4751247     K1      = 0.3998241
K2      = 6.352166E-2   K3      = 0.00          DVT0    = 0.00
DVT1    = 0.00          DVT2    = 0.00          DVT0W   = 0.00
DVT1W   = 0.00          DVT2W   = 0.00          NLX     = 0.00
W0      = 0.00          K3B     = 0.00          NGATE   = 0.00
VFB     = 99.00         VSAT    = 8.42922E4     UA      = -9.057631E-10
UB      = 2.760486E-18  UC      = 1.234253E-10  RDSW    = 170
PRWB    = 0.00          PRWG    = 0.00          WR      = 1.00
U0      = 0.04387662    A0      = 0.5262759     KETA    = -4.428695E-2
A1      = 0.00          A2      = 0.99          AGS     = -2.8363639E-2
B0      = 0.00          B1      = 0.00          VOFF    = -0.1246745
NFACTOR = 1.00          CIT     = 2.7566159E-4  CDSC    = 0.00
CDSCB   = 0.00          CDSCD   = 0.00          ETA0    = -2.9375E-4
ETAB    = 1.3875E-3     DSUB    = 0.00          PCLM    = 1.1025569
PDIBLC1 = 1.00E-6       PDIBLC2 = -6.146589E-3  PDIBLCB = 1.00E-2
DROUT   = 0.00          PSCBE1  = 4.00E8        PSCBE2  = 1.00E-6
PVAG    = 0.00          DELTA   = 1.00E-2       ALPHA0  = 0
ALPHA1  = 0.429         BETA0   = 11.59263      KT1     = -0.2268918
KT2     = -2.937242E-2  AT      = 2.00E4        UTE     = -2.1724229
UA1     = 1.2174139E-9  UB1     = -3.852224E-18 UC1     = -1.568814E-10
KT1L    = 0.00          PRT     = 0.00          CJ      = 1.000266E-6
MJ      = 0.3595262     PB      = 0.6882682     CJSW    = 2.040547E-13
MJSW    = 0.2003879     PBSW    = 0.6882682     CJSWG   = 3.340547E-13
```

```
MJSWG   = 0.43879       PBSWG   = 0.6882682     TPB     = 1.554306E-3
TPBSW   = 1.554306E-3   TCJ     = 1.040287E-3   TCJSW   = 6.45489E-4
JS      = 8.38E-6       JSW     = 1.60E-11      NJ      = 1.0
XTI     = 3.0           CGDO    = 3.4367E-10    CGSO    = 4.317E-10
CGBO    = 1.0E-13       CAPMOD  = 3             ELM     = 0
XPART   = 0             CF      = 0             TLEV    = 1
TLEVC   = 1             CALCACM = 1             NOFF    = 1.2
CLE     = 1             CLC     = 1.45E-8       DLC     = 4.6433E-8
LLC     = -0.123E-14    VOFFCV  = 0.1261        CGSL    = 6.6175E-10
CGDL    = 2.4366E-10    NMOS    = 1             PMOS    = 0
IDSMOD  = 8             VBM     = -3.0          EM      = 4.1E7
LVTH0   = 5.306376E-9   WVTH0   = 1.0620770E-9  PVTH0   = 5.1808260E-15
LK1     = 4.964413E-8   WK1     = 9.7659690E-8  PK1     = -6.472741E-15
LK2     = -2.388411E-8  WK2     = -4.2037990E-8 PK2     = 5.4169450E-15
LVSAT   = -2.0125E-4    WVSAT   = 1.4661819E-3  LUA     = 4.2158860E-18
WUA     = 4.675041E-16  PUA     = -5.258461E-23 LUB     = 5.4007650E-27
WUB     = -1.020856E-24 PUB     = 1.5842940E-33 LUC     = 4.2403960E-18
WUC     = -6.630735E-17 PUC     = -1.062770E-24 LU0     = 1.2834320E-9
WU0     = -5.211112E-9  PU0     = -3.156964E-16 LA0     = 8.2773920E-8
WA0     = 1.447255E-7   PA0     = -7.306591E-14 LKETA   = 3.2422730E-9
WKETA   = 2.458758E-8   PKETA   = -2.836800E-15 LAGS    = 1.1709090E-9
WAGS    = 8.430546E-8   PAGS    = -1.180276E-14 LVOFF   = -1.468027E-9
WVOFF   = 1.245329E-9   PVOFF   = -7.819310E-16 LCIT    = 1.0319570E-10
WCIT    = -3.764672E-11 PCIT    = 1.7317489E-17 LETA0   = 1.8112500E-10
LETAB   = -6.8425E-1    LPCLM   = 3.8132860E-8  WPCLM   = 5.1117520E-8
PPCLM   = 4.393024E-14  LPDIBLC2= 5.0605220E-9  WPDIBLC2= 2.1076341E-9
PPDIBLC2= -2.950686E-16 LKT1    = 5.1277220E-9  WKT1    = -2.576878E-9
PKT1    = -2.087376E-15 LKT2    = 6.0691700E-10 WKT2    = -1.65007E-9
PKT2    = -3.93619E-17  LUTE    = 8.3695030E-8  WUTE    = 9.0012740E-7
PUTE    = -1.336361E-13 LUA1    = 9.2209620E-19 WUA1    = 8.4305930E-18
PUA1    = -1.180283E-24 LUB1    = 4.3064910E-25 WUB1    = 3.2489980E-24
PUB1    = -4.814262E-31 LUC1    = 3.2866920E-17 WUC1    = 1.8689849E-16
PUC1    = -3.254285E-23 LVOFFCV = -0.0094E-6    LCGSL   = -0.3804E-16
LCGDL   = -0.175E-16
```

```
MODEL PCH018 MOSFET
NOIMOD  = 1             AF      = 1.369         EF      = 1.064
KF      = 5.77E-27      TNOM    = 25            VERSION = 3.2
TOX     = 4.08E-9       TOXM    = 4.08E-9       XJ      = 1.7000001E-7
NCH     = 3.90E17       LLN     = 1.00          LWN     = 1.00
WLN     = 1.00          WWN     = 1.00          LINT    = 1.4999999E-8
LL      = 0.00          LW      = 0.00          LWL     = 0.00
WINT    = 1.50E-8       WL      = 0.00          WW      = 0.00
WWL     = 0.00          MOBMOD  = 1             BINUNIT = 2
XL      = -2E-8         XW      = 1E-6          WMLT    = 1
DWG     = 0.00          DWB     = 0.00          ACM     = 12
LDIF    = 9.00E-08      HDIF    = 2.00E-07      RSH     = 7.2
RD      = 0             RS      = 0             RSC     = 0
RDC     = 0             VTH0    = -0.449372     K1      = 0.5178921
K2      = 4.280981E-2   K3      = 0.00          DVT0    = 0.00
DVT1    = 0.00          DVT2    = 0.00          DVT0W   = 0.00
DVT1W   = 0.00          DVT2W   = 0.00          NLX     = 0.00
W0      = 0.00          K3B     = 0.00          NGATE   = 0.00
VFB     = 99.0          VSAT    = 1.308125E5    UA      = 9.499295E-10
UB      = 4.958583E-19  UC      = -1.587904E-10 RDSW    = 530
PRWB    = 0.00          PRWG    = 0.00          WR      = 1.00
U0      = 0.009831898   A0      = 1.27343       KETA    = 1.500061E-2
A1      = 0.00          A2      = 0.40          AGS     = 2.0E-2
B0      = 0.00          B1      = 0.00          VOFF    = -0.1308178
NFACTOR = 1.00          CIT     = -6.280855E-5  CDSC    = 0.00
CDSCB   = 0.00          CDSCD   = 0.00          ETA0    = -4.687502E-4
ETAB    = 1.1367541E-3  DSUB    = 0.00          PCLM    = 0.91154
PDIBLC1 = 1.0E-6        PDIBLC2 = 7.96875E-3    PDIBLCB = 1.00E-2
DROUT   = 0.00          PSCBE1  = 3.50E8        PSCBE2  = 5.00E-7
PVAG    = 0.00          DELTA   = 1.00E-2       ALPHA0  = 0
ALPHA1  = 6.56          BETA0   = 22.67827      KT1     = -0.2368895
KT2     = -2.567999E-2  AT      = 1.00E4        UTE     = -0.7213691
UA1     = 1.224E-9      UB1     = -1.352532E-18 UC1     = 7.191495E-11
KT1L    = 0.00          PRT     = 0.00          CJ      = 1.121E-6
MJ      = 0.4476        PB      = 0.895226      CJSW    = 2.481E-13
MJSW    = 0.3683619     PBSW    = 0.895226      CJSWG   = 4.221E-13
```

```
MJSWG   = 0.3683619     PBSWG   = 0.895226      TPB     = 1.572025E-3
TPBSW   = 1.572025E-3   TCJ     = 9.739001E-4   TCJSW   = 4.130718E-4
JS      = 4.92E-6       JSW     = 9.00E-10      NJ      = 1.0
XTI     = 3.0           CGDO    = 3.53E-10      CGSO    = 3.56E-10
CGBO    = 1.0E-13       CAPMOD  = 3             ELM     = 0
XPART   = 0             CF      = 0             TLEV    = 1
TLEVC   = 1             CALCACM = 1             NOFF    = 0.75
CKAPPA  = 0.8           CLE     = 1             CLC     = 2.5E-10
VOFFCV  = 0.1894        CGSL    = 3.982E-10     CGDL    = 3.72E-10
DLC     = 5.75E-8       LLC     = -0.348E-14    PMOS    = 1
NMOS    = 0             IDSMOD  = 8             VBM     = -3.0
EM      = 4.1E7         NOIA    = 9.9E18        NOIB    = 2.4E3
NOIC    = 1.4E-12       LVTH0   = -8.06576E-9   WVTH0   = 1.0679620E-8
PVTH0   =-1.742597E-15  LK1     = 1.887120E-8   WK1     = 1.4451329E-7
PK1     =-2.057092E-14  LK2     = -6.758558E-9  WK2     = -5.283713E-8
PK2     = 8.796957E-15  LVSAT   = -3.656236E-4  LUA     = -1.785002E-16
WUA     = -7.679882E-16 PUA     = 1.845406E-22  LUB     = 1.373112E-25
WUB     = 4.379602E-25  PUB     = -1.528556E-31 LUC     = 1.958586E-17
WUC     = 2.9227921E-17 PUC     = -1.081963E-23 LU0     = -1.291645E-10
WU0     = -2.9276901E-9 PU0     = 3.0125661E-16 LA0     = 3.3696850E-9
WA0     = -5.001745E-7  PA0     = 1.2788430E-13 LKETA   = -5.831355E-10
WKETA   = 8.661148E-9   PKETA   =-2.4688039E-15 LVOFF   = 1.554266E-10
WVOFF   = 5.518163E-9   PVOFF   = -1.905712E-15 LCIT    = 1.18189E-10
WCIT    = 2.219781E-10  PCIT    = -8.554223E-17 LETA0   = 2.5593749E-10
LETAB   = -5.565394E-10 WETAB   = -5.903965E-10 PETAB   = 2.656785E-16
LPCLM   = 3.980698E-8   WPCLM   = -1.310087E-8  PPCLM   = 5.895399E-15
LPDIBLC2= 9.140624E-10  LKT1    = -2.463487E-9  WKT1    = 2.0141179E-8
PKT1    = -2.009008E-15 LKT2    = -7.622315E-11 WKT2    = 8.089046E-9
PKT2    = -1.558648E-15 LUTE    = 5.387008E-10  WUTE    = 1.2306521E-7
PUTE    = 1.059462E-14  LUB1    = 2.549208E-26  WUB1    = -2.575436E-25
PUB1    = 3.337843E-32  LUC1    = -7.869275E-18 WUC1    = -4.963781E-17
PUC1    = 1.019449E-23  LVOFFCV = -0.0172E-6    LCGSL   = -0.2830E-16
LCGDL   = -0.2324E-16
```

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BIOGRAPHICAL INFORMATION

Mingsheng Peng received his B.S. degree and M.S. degree in Physics from Jiangxi Normal University, Nanchang, China in 1994 and 1997, respectively. He received M.S. degree in Electrical Engineering from The University of Texas at Arlington (UTA) in 2002. In fall of 2002, he entered the Ph.D. program in Electrical Engineering Department at UTA. He joined the Analog IC Design Research Group, and worked under the guidance of Dr. W. Alan Davis and Dr. Ronald L. Carter in 2003. He received his Ph.D. degree in Electrical Engineering from UTA in 2007. His current research interests include analog, mixed-signal, and RF circuit design. He is a member of Tau Beta Pi.