MEASUREMENT AND MODELING OF 1/f NOISE IN MOSFET DEVICES WITH HIGH-κ MATERIAL AS THE GATE DIELECTRIC

by

TANVIR HASAN MORSHED

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2007

ACKNOWLEDGMENTS

All praises to Allah, the most merciful. Peace be upon Prophet Muhammad.

I would like to express my deepest respect for my advisor Professor Zeynep Çelik-Butler for her support and directions in this research and in times of need. It has been a remarkable experience to work with her, to learn and to flourish as a researcher. I am grateful to my advisor for her indispensable contributions in this research work.

I like to thank all my dissertation committee members; Dr. Donald Butler, Dr. Jung-Chih Chiao, Dr. Daniel Engels and Dr. Wiley Kirk for their precious time, advice and suggestions. I am especially thankful to Dr. Engels for his every effort to make my thesis a better written document as well as his insightful remarks. I appreciate Dr. Kirk for his discerning remarks on the experimental side of this work. I also like to thank Dr. Keith Green, Dr. Luigi Colombo and Dr. Ajit Shanware from Texas Instruments, for the devices used in this work and their valuable comments and suggestions. I like to express my gratitude to Semiconductor Research Corporation for the financial support.

I am grateful to Dr. Raymond Shoults for his kind favors in academic matters.

I am indebted to Dr. Aamer Mahmood and Dr. Mukti Rana for their support and encouragement. I like to thank all my friends, co-researchers and stuffs at NanoFab, especially Mazhar, Min, Siva, Shahriar, Shakhauat, Murali, Erkin, Vijay, Suraj and others. I thankfully acknowledge the excellent work environment we enjoy at the NanoFab.

I would like to especially mention the unconditional love and support from my wife Romana Zerin through our very difficult times, and the continuous encouragement from my parents Lt. Col. H. M. A. Gaffar (BU) and Hosne Ara Gaffar, my brother Tanjeer and my sisters Dr. Farzana and Farhana. I remember the blessings from my late grand father Abdul Karim Molla. I gratefully remember the cordial love from all our family members and friends in Dhaka and Toronto. This work was possible for me all because of that.

May Allah bless you all.

November 20, 2007

ABSTRACT

MEASUREMENT AND MODELING OF 1/f NOISE

IN MOSFET DEVICES WITH HIGH-κ

MATERIAL AS THE GATE

DIELECTRIC

Publication No. _____

Tanvir Hasan Morshed, PhD.

The University of Texas at Arlington, 2007

Supervising Professor: Dr. Zeynep Çelik-Butler

A new 1/f noise model has been developed for MOSFET devices with high-κ gate stack. To investigate the impacts of nitridation, MOSFETs with nitrided high-κ dielectric was used. These devices were provided by Texas Instruments, having four different interfacial layer thicknesses with a stack composition of SiON/HfSiON.

The dominant mechanism affecting the noise behavior of these devices was experimentally determined to be correlated number and mobility fluctuation. The impact of remote phonon scattering was investigated in the temperature range of 172K

to 300K. It has been observed that the mobility characteristics of these devices were significantly affected by remote phonon scattering. However, the impact of remote phonon scattering was not observed on the flicker noise characteristics. The new model was developed in the frame work of the original Unified Model incorporating two distinct features that distinguish high-κ gate stacks from SiO_2. The new model considers energy and spatial dependence of trap distribution in the dielectric, thus generates a more realistic trap profile. Furthermore, it incorporates the multi layered structure of the gate stack by considering tunneling of carriers through a double step cascaded barrier. The newly developed model is accordingly called MSUN (Multi Stack Unified Noise) Model, named after the original Unified Model.

MSUN Model has been successfully verified with data on MOSFETs having four different interfacial layer thicknesses, in the temperature range of 172K to 300K. The model predictions show very good agreement with data in the bias range of moderate to strong inversion. No specific impact due to nitridation was observed on these devices. The model has been successfully transformed into a compact form which is compatible with leading device simulation package used in the industry.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Aggressive downscaling of semiconductor devices has pushed the performance of SiO_2 to its limits as the ideal gate dielectric in CMOS technology. Introduction of high dielectric constant materials (referred to as high-k materials from here on) as the alternate dielectric for these MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistor) introduces some fundamental differences in the material properties and the structure of the gate stack. In addition, high-k incorporation affects some of the fundamental parameters of MOSFET devices, of which the carrier mobility degradation [1,2] and the low frequency noise behavior are of particular interest [3,4,5,6]. In this context, the Unified Model (the most successful flicker noise model developed for SiO_2 based MOSFET devices) shows significant discrepancies when applied to the analysis of noise in devices with high-k gate stacks. Flicker noise in semiconductor devices, characterized by $f^{-\delta}$ ($0.8<\delta<1.2$) in the lower frequency range (f<10kHz), is an important device performance criteria as it often sets the detection limits in device applications and its up-conversion affects higher frequency applications. Accurate prediction of flicker noise thus becomes an essential factor in device simulation. Most

notable of the discrepancies mentioned above is the variation in the extracted trap density values by different research groups even on the same material. Moreover, the extracted values show a dependence on the interfacial layer thickness (IL). IL is not a model parameter in the Unified Model. The semiconductor industry is in need of a flicker noise model that is capable of accurately predicting the low frequency noise in MOSFETs with high-k dielectric materials.

The objective of this work is to develop a physics-based, scalable and compact model for the flicker noise prediction of high-k MOSFET devices. This work focuses on identifying the physical origin of flicker noise in MOSFET devices having high-k materials as the gate dielectric by extensive analysis of experimental data and developing a physics-based accurate flicker noise model that is compatible with industry standard device simulators such as BSIM (Berkeley Short-Channel IGFET Model) and PSP (surface-potential-based model). Thus, in the absence of any existing flicker noise model for high-k gate stack MOSFET devices, this work addresses a significant deficiency in the low frequency noise research area and makes an important contribution in device modeling and characterization industry by providing an accurate flicker noise model compatible with industrial applications.

1.2 Scaling down of MOSFET devices and incorporation of high-κ materials

In order to facilitate faster device operations and higher on chip device integration, ITRS (International Technology Roadmap for Semiconductors) [7] has set out a very aggressive route for device scaling. As Moore's law predicted, there has been

an exponential growth in the number of devices integrated on a single chip over the last few decades with transistor densities doubling approximately every 18 months.

1.2.1 Role of SiO_2 in device scaling

One of the most important factors in achieving such a high rate of continued device integration is the role of SiO_2 as an excellent dielectric material in the CMOS process technology [8]. Thermally grown amorphous SiO_2 has some outstanding material and electrical properties which include a very high quality substrate-dielectric interface that is stable both electrically and thermodynamically. In addition to providing low interface densities (10^{10} cm^{-2}) as well as low defect charge densities ($10^{10}cm^{-2}eV^{-1}$), it results in very good electrical isolation between the channel and the gate with high breakdown fields (15 $MVcm^{-1}$). As a consequence of such significant reduction in device sizes, the gate oxide thickness has been proportionally decreased in order to achieve a reasonable threshold voltage. Currently, ultra thin (~13Å) SiO_2 as the gate dielectric is routinely obtained in the industry with dielectric properties sufficient to ensure proper device operations. Further reduction of SiO_2 thickness approaches to within two mono layers of the conduction channel, where the O_2 atoms can not have a full arrangement of O_2 neighbors and fail to form the full band gap compared to bulk SiO_2. Consequently, dual mono layer SiO_2 fails to retain the same desirable dielectric properties in ultra thin MOSFET devices, with a consequence of high leakage currents and thereby causing undesirable power dissipations. The semiconductor industry must use alternate materials to continue the performance gains predicted by Moore's law.

1.2.2 Principle of using high-k materials as the alternate gate dielectric

The effect of the device dimensions and oxide layer thickness on MOSFET performance can be better understood in terms of the relations between the channel current and applied bias voltages. From the basic theory of MOSFET operations, the expression for the channel current in the linear region (Equation 1.1) and the saturation region (Equation 1.2) can be given as:

$$I_d = (W/L)\mu C_{inv}\left(V_g - V_t - V_d/2\right)V_d \tag{1.1}$$

$$I_d = (W/L)\mu C_{inv}\left(V_g - V_t\right)^2/2 \tag{1.2}$$

Here, I_d is the channel current, W and L are width and length of the channel respectively, V_t is the threshold voltage, V_g and V_d are the voltages applied at the gate and the drain terminals respectively with respect to the source terminal. C_{inv} denotes the inverted channel capacitance, and μ is the carrier mobility.

As is made clear by these expressions, for both the linear region and the saturation region the channel current increases (resulting faster device response) with either an increase in C_{inv}, a decrease in channel length *L,* or a decrease in threshold voltage V_t. The dielectric thickness of the device has an inverse effect on both the inversion capacitance and the threshold voltage. Thus, decreasing the dielectric thickness increases the channel current. To make sure V_t is not affected by thermal energy fluctuations around room temperatures, V_t is maintained at a minimum value of 200mV.

Thicker dielectrics may be used to achieve the same drive current if they have higher dielectric constant. Considering any parallel plate capacitor, the relation between the channel capacitance and the dielectric thickness can be shown as:

$$C_{inv} = \kappa_{ox}\varepsilon_0 A/t_{ox} \tag{1.3}$$

Equation 1.3 directly shows the dependence of the device drive current on dielectric thickness and how it is related to dielectric constant of the material through C_{inv}. Here,

κ_{ox} and t_{ox} are the dielectric constant and the thickness of SiO_2 respectively, ε_0 is the permittivity of free space and A denotes the channel area. It is apparent from Eq. 1.3 that the same inversion capacitance C_{inv} and hence identical drive current I_d can be obtained using a thicker dielectric material with a physical thickness of $t_{high-\kappa}$ as well as a higher dielectric constant of $\varepsilon_{high-\kappa}$ following the relation

$$C_{inv} = \kappa_{high-\kappa}\varepsilon_0 \, A/t_{high-\kappa} \tag{1.4}$$

where,

$$\kappa_{high-\kappa}/t_{high-\kappa} = \kappa_{ox}/t_{ox} \tag{1.5}$$

The above relations provide the theoretical basis for using materials with higher dielectric constant to overcome the limitations imposed by physical thickness of the gate insulator. Figure 1.1 illustrates MOSFET devices with SiO_2 and high-k material stack as the gate dielectric.

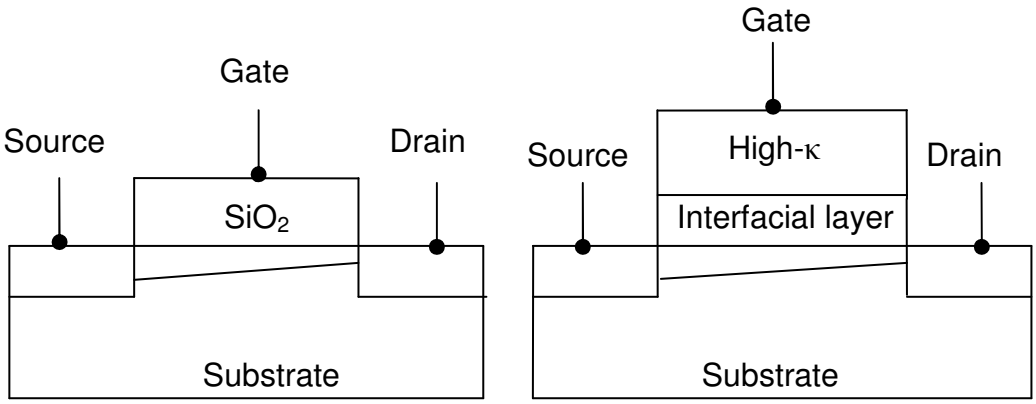


Figure 1.1 MOSFET devices with SiO_2 and high-k stack as the gate dielectric.

1.2.3 Selection of suitable high-k materials

The choice of the ideal dielectric requires fulfillment of some crucial properties and a systematic approach in the ideal dielectric selection process. Such a systematic consideration of dielectric properties includes [8]:

1. permittivity, band-gap and band offset between Si and dielectric conduction band (or valence band for p-type) edges.
2. thermodynamic stability
3. film morphology
4. interface quality
5. compatibility with materials used in current and future CMOS processes
6. process compatibility and
7. reliability

The significance of the above mentioned properties are briefly discussed here. Higher permittivity is required as a means to deposit dielectrics with higher physical thickness with the same current drive, as explained earlier. Large band gap ensures that the material has adequate insulating properties. A tradeoff should be under consideration at this point as permittivity and band gap show an inverse dependence on each other. The band offset between the dielectric and Si should be high, to ensure that the probability of tunneling into the dielectric from the conducting channel is low. The dielectric material needs to be thermodynamically stable, so that after deposition it does not react with the substrate and change the material properties. The resultant interface is expected to be low in interface states and defect states, to minimize Coulomb

interaction between carriers and charged interface traps which may lower the carrier mobility or increase the flicker noise in the device. Film morphology of the candidate dielectric is another important issue in the overall selection process. The dielectric is desired to be amorphous in nature as opposed to polycrystalline structures, as the grain boundaries in polycrystalline materials can act as current leakage paths and degrade the device performance. It is expected that the new dielectric material provides good performance with Si based gate materials and does not require special materials such as metal gates. Another important criteria in the dielectric selection process is its compatibility with the current and future fabrication process to ensure product quality, throughput and economic feasibility. The alternative material under consideration should also withstand the long term reliability benchmark test requirements of the industry to ensure product life.

Several high-κ compounds have been identified as promising candidates to replace SiO_2 as the gate dielectric [8, 9, 10]. Al_2O_3 from Group IIIA in the periodic table, shows excellent thermodynamic stability; however, the lower κ value does not show much promise for the long term solution, as smaller technologies in the future will require lower effective thickness of the dielectric and hence higher dielectric coefficient. La, Pr and Y based oxides from group III B have shown higher k values compared to Al_2O_3. However, the voltage shift associated with these materials lie in the range of 300 - 700 mV, suggesting a high fixed charge density (10^{12} cm^{-2}). Thermodynamic stability is another big concern for group III B materials, the materials react with Si substrate after deposition which is not desirable. TiO_2, ZrO_2 and HfO_2

from group IV B have shown very good overall performance, with the exception of Ti based oxides. Ti based oxides show reduced oxide limitations having many oxygen vacancies that can act as carrier traps and high leakage current paths. A system of materials, called the pseudo-binary alloys having the forms such as $(ZrO_2)_x(SiO_2)_{1-x}$ and $(HfO_2)_x(SiO_2)_{1-x}$, has emerged as a possible source of alternate dielectrics. This system enables retention of the desired characteristics of two different oxides and at the same time eliminates the undesired characteristics of the individual oxides.

1.2.4 Effect of N_2 incorporation

An important issue regarding the high-κ dielectric characteristics is the role of N_2 at the dielectric interface to improve the interface quality, which is explained in this section. Nitridation of gate dielectric materials is attractive as it provides advantages in terms of superior device performance when compared to MOSFETs with non-nitrided high-κ dielectric gate stack. The diffusion of Boron from highly doped gate region across the thin oxide to the lower doped channel area is reduced by N_2 incorporation; thus, it reduces the threshold voltage shift. Incorporation of N_2 also increases the dielectric constant compared to SiO_2 and helps to lower the leakage current [8]. The high-κ dielectric used in this work, HfSiON, has been reported to result in two orders of magnitude lower gate leakage current compared to SiO_2 [11]. Moreover, it shows good IV and CV stability under stress conditions with dielectric breakdown characteristics similar to that of SiO_2 [11] and high carrier mobility [12]. The interface trap density and the defect states introduced by nitridation have been well researched in the industry, revealing a strong correlation between nitrogen induced defects and

oxygen vacancies as well as interstitials in the high-κ gate stack [13]. The interface trap density is reported to be higher than that of SiO_2 but lower compared to other high-κ gate materials [14]. Moreover, the trap density was observed to be a function of distance into the dielectric in the case of nitrided gate dielectrics compared to a somewhat uniform trap density for non-nitrided ones [13]. Thus, N_2 incorporation shows a significant impact on the interface quality and the low frequency noise behavior of the MOSFET, as these greatly depend on carrier trapping at the interface and the associated scattering mechanisms [15].

1.2.5 Effects of incorporation of high-k materials

In general, incorporation of high-k materials largely lowers the leakage current through the dielectric and thereby lowers the power dissipation of the devices. Nevertheless, there are some undesirable consequences of using high-k materials in MOSFETs. The primary disadvantage of high-k is that they often reduce the device performance. Some of the commonly encountered effects associated with using high-k materials as the gate dielectric are:

1. Charge trapping in the dielectric
2. Threshold voltage instability
3. Dielectric breakdown
4. Lower carrier mobility
5. Higher flicker noise and
6. Effects of remote optical phonon scattering on device performance.

At this point, we need to elaborate the distinction of the anticipated effects of remote optical phonon scattering on device performance from the other undesirable effects. While the device may be subjected to some additional processing steps in order to alleviate the above mentioned shortcomings, the effect of remote phonon scattering on device performance remains an unavoidable consequence of the gate dielectric material having a higher electric permittivity, as both originate from the same physical property of the high-k materials. The high dielectric constant stems from the fact that the atomic bonds in high-k dielectrics are ionic in nature as opposed to hard atomic bonds such as in SiO_2. These so called soft bonds are flexible when subjected to electric fields that enable them to absorb higher electric fields compared to the rigid atomic bonds in SiO_2. The effect of this absorption is a higher dielectric constant. These flexible bonds also can respond to the oscillations caused by the optical phonons present in these materials, whereas the hard inflexible bonds in SiO_2 do not respond to such oscillations. When the interface plasmons or the electron cloud at the channel interface couple with this vibration of the atomic bonds, an additional scattering of the carriers in the conduction channel is introduced. This scattering is expected to further degrade the device performance [16]. As the rigid SiO_2 bonds do not couple with atomic vibrations caused by remote phonons, the carriers in conventional MOSFET devices are free from the effects of remote phonon scattering. To date, the impact of remote phonon scattering on the low frequency noise characteristics of MOSFET devices has not been investigated. The verification of the effect of remote phonon scattering on high-k MOSFETs thus becomes essential in this work. Any significant impact of such an

additional mechanism on the low frequency noise characteristics will necessitate a means to include the effect of remote phonon scattering in the formulation of the new noise model.

1.3 1/*f* Noise modeling

It has been the focus of research for many scientists and engineers to establish a unique theory to describe the 1/f noise in MOSFET devices, although a definite conclusion is not yet reached. In general the flicker noise models for MOSFETs can be classified as originating from two different schools of thought. In the number fluctuations models, or ΔN models, based on Mc.Whorter's [17] theory, it is assumed that fluctuations occur in the number of carriers in the channel as the carriers tunnel between the channel and the traps located in the dielectric. This fluctuation in the carrier number results in a fluctuation in the channel current which is responsible for the flicker noise. Thus, the ΔN models assume that 1/f noise in MOSFET devices is a surface phenomena that is directly related to the quality of the Si-SiO_2 interface and the SiO_2. On the other hand, the bulk mobility fluctuation models, or $\Delta\mu$ models, based on Hooge's theory [18] predict that the fluctuations in the channel current are a result of fluctuations in the carrier mobility through variation in the scattering cross section associated with the collision. This is believed to be originating from bulk phonon scattering from the substrate. Thus, $\Delta\mu$ models assume flicker noise is related to the total number of carriers in the channel. Instead of a surface origin of flicker noise as in ΔN models, $\Delta\mu$ models assume a volume origin in homogeneous semiconductors.

1.3.1 Flicker noise prediction with existing models

Both number fluctuation models and the bulk mobility fluctuation models have their advantages and disadvantages. The ΔN model is strongly supported by the random telegraph signal (RTS) measurements [19], although the presence of some additional noise components are not explained [20]. This model is also supported by Reimbold's formulation [21],valid over the bias range of weak inversion to strong inversion [20]. In Reimbold's model, McWhorter's model is further developed, taking into consideration all the capacitive components of small signal device model. The $\Delta\mu$ model, although showing better predictions for p-type devices in the strong inversion region, fails to explain the weak inversion mobility behavior. This model lacks from a strong theoretical definition of the noise coefficient α_H as well and thus remains an empirical model [20]. The so called Unified Model [22]; based on the correlated number and surface mobility fluctuations theory [22, 23]; shows a better agreement with the experimental data for both n and p type MOSFETs over a wide temperature range and thus has become the most successful theory adopted for low frequency noise modeling and analysis [20,24,25,26,27,28,29,30]. This model is derived from the number fluctuation theory, assuming that the carriers are trapped or detrapped by the traps in the dielectric. Therefore, along with the number of carriers in the channel, the number of trapped carriers also fluctuates. The fluctuation of the latter causes a fluctuation in the coulomb potential existing between the charged traps and the carriers in the channel, which in turn induces a correlated fluctuation in the mobility of the carriers at the channel interface. According to the Unified Model, this correlated number and mobility

fluctuation is responsible for the fluctuations in the drain current and hence the current noise spectrum S_{I_d}. The model is further modified according to Koga's [31] observation of Coulomb potential screening by higher density of channel carriers.

1.3.2 Application of Unified Model in noise prediction of high-k gate-stack MOSFETs

Although the Unified Model is the most successful low frequency 1/f noise model for the conventional gate dielectric devices, the extracted parameter values using this model show noticeable discrepancies when applied to devices using high-κ materials as the gate dielectric [32]. Most notable of them is the lack of agreement in the extracted trap density values by different research groups even for the same material. Furthermore, significant dependence on the interfacial layer thickness has been observed in the extracted trap density values, although interfacial layer thickness is not a model parameter in the original Unified Model.

1.3.3 Possible origins of the observed discrepancies

The original Unified Model was developed for conventional SiO_2 based MOSFET devices which differ from their high-κ gate stack counter parts both structurally and in material properties. In the former type, a single layer of SiO_2 is used as the gate dielectric material whereas the high-κ gate stack usually comprises of a single or multiple layers of high-κ materials over a thin interfacial layer (typically of SiO_2). SiO_2 is regarded as an ideal dielectric material as it provides a superior interface with Si substrate in terms of lower interfacial trap density as well as a much cleaner dielectric bulk. Compared to that, high-κ materials provide an interface with higher

interface trap density [33] and a bulk that is inherently phonon scattering prone due to its material properties having soft ionic bonds [16].

The processing of SiO_2 is a mature technology in the semiconductor industry and the trap profile in the SiO_2 is a thoroughly studied research topic [34, 35]. Unlike SiO_2, high-κ materials processing is still under development, with atomic layer deposition (ALD) being considered a promising process technology [36]. The estimated interface trap density by different research groups, which lacks an agreement with each other, are believed to represent an average value, as they appear to be dependent on the interfacial layer thickness as well as the process technology [32]. This disagreement in the extracted trap density, based on the original Unified Model, may be attributed to the fact that the original model accounts for only the noise contribution of the single layer of conventional dielectric material but not that of the high-κ layer, as this layer is absent in devices with SiO_2. Moreover, as the exact trap density profile for the high-κ materials is yet to be established, the trap profile model used for the high-κ layer needs to provide a great deal of flexibility to simulate realistic trap profiles. Energy dependence of trap density in SiO_2 based MOSFETs is well documented [37]. For high-k gate-stacks it has been reported that the effective trap density values inside the dielectric show spatial variation as well [13]. Thus, the use of a single valued trap density, as adopted in the original Unified Model, may prove to be inaccurate when applied to high-κ gate stack MOSFET devices.

1.3.4 Theoretical basis of the new model

The underlying mechanism affecting the low frequency noise characteristics of high-k MOSFETs used in this work was experimentally verified. Irrespective of temperature or interfacial layer thickness, the correlated number and surface mobility fluctuation model was determined as the dominant mechanism responsible for the observed noise behavior. Consequently, the new model was developed in the framework of the Unified Model based upon the same theory by implementing the above mentioned distinctive high-k features. The new model is named after the Unified Model as the MSUN (Multi Stack Unified Noise) Model [38, 39, 40].

1.3.5 Modifications in MSUN Model and implementation

First, the effect of remote phonon scattering was experimentally tested to identify any additional noise mechanisms originating from the high-k layer. No observable impact of remote phonon scattering was found on the flicker noise and its effect was not separately included in the MSUN Model. In this work, special attention was paid to the incorporation of the contribution of the high-κ layer in the total low frequency noise of the device, along with that of the interfacial layer. This was lacking in the original Unified Model. Tunneling of carriers through a double step cascaded barrier was considered instead of a single step, to incorporate the double layered structure of the gate stack, resulting in the required modification in the expression of $S_{\Delta N_t}\left(Hz^{-1}\right)$; the power spectral density resulting from the fluctuations of trapped charge carriers. Instead of using a single average experimental value, the trap density profiles for the interfacial layer as well as the high-κ layer were implemented using a more

flexible and comprehensive expression [34], which incorporates the dependence of the effective trap density on the energy and spatial distribution of traps, along with the band bending inside the dielectric.

1.3.6 MSUN Model performance verification

The theoretical model was experimentally verified on MOSFET devices having HfSiON as the high-k dielectric material on four different interfacial layer thicknesses of SiON. Verification of remote phonon scattering was done in the temperature range of 172K to 300K. Although the carrier mobility was affected by remote phonon scattering, the low frequency noise was not. The model predictions were found to be in very good agreement with the experimental data at all temperatures irrespective of interfacial layer thicknesses. The predicted current noise spectral density S_{I_d} at 1Hz showed very good agreement with the experimental data in the bias range of weak inversion to strong inversion. The extracted trap density values were observed to be consistent with respect to temperature or interfacial layer thicknesses. The working theoretical model verified with experimental data was transformed into a compact form to comply with industry requirements. The compact form was further expressed in various forms compatible with industry standard device simulation software packages.

1.4 Summary

The importance of this work is evident from the fact that, it represents research which deals with contemporary issues arising directly from the semiconductor industry, involving a novel technology, such as the incorporation of high-k materials for new generation of MOSFETs. The analysis of the technical complications posed by the inherent material properties of the high-k dielectric and the dynamics of the carrier tunneling in the multilayer gate-stack involve novel theories such as the effect of remote optical phonon scattering in high-k materials. The work involves verification of the theoretical predictions with massive amount of experimental data; taken on a meaningful array of samples using a customized experimental setup.

The key accomplishments of this work may be summarized as follows:

- In this work, we have developed the first ever physics-based compact flicker noise model for MOSFET devices with high-k dielectric materials. The lack of such model for prediction and analysis of low frequency noise with adequate accuracy is recognized as a large deficiency in the semiconductor noise research area. In this work, we have addressed that deficiency to its entirety. From a systematic analysis of the problem to the development of a new physics based model and its experimental verification, all the necessary steps were completed in this work. Finally, the model was expressed in an accurate compact form, and converted to formats compatible with leading device simulation packages in the industry, such as, PSP and BSIM.

- A systematic study on the failure of the Unified Model in flicker noise prediction of high-k dielectric MOSFETs was carried out and the possible origins of these failures were identified. Before this work, the fundamental discrepancies in the Unified Model predictions were reported. However a systematic study like this and identification of the root causes were lacking.
- The experimental verification of remote phonon scattering on the same samples were done considering two different aspects of device characteristics. The importance of this experimental findings lie in the fact that for the first time it has been established remote phonon scattering does not affect flicker noise characteristics, while its presence is confirmed through the observed effects on the mobility characteristics.
- Our experimental finding that the remote phonon scattering bears no effect on noise carries great significance from industrial application point of view. It indicates that the expected detrimental effects of phonon scattering on MOSFET characteristics need not be overly generalized. It may as well indicate to special application areas where high-k MOSFETs may be utilized more efficiently.
- A more realistic trap density profile is implemented in the new model showing exponential dependence on energy and spatial distribution of traps. This incorporation of energy and spatial dependence proves to be essential for modeling of noise in high-k dielectric MOSFETs.

- Multi layer structure of the gate dielectric was implemented by considering tunneling of carriers through a double step barrier. Thus, the dynamics of tunneling through stacked dielectric is incorporated in the model, which is essential in description of high-k MOSFET noise characteristics and lacking in the Unified Model.
- The crucial impact of the interfacial layer on the overall noise is very well explained by the MSUN Model. It also explains the interfacial layer dependence and variation in the extracted trap density values observed in the application of Unified Model on high-k MOSFETs. Tunneling of carriers through a single dielectric layer does not have the ability to take into account the variation in physical thicknesses of individual layer for the same effective physical thickness of the dielectric, which the MSUN Model is capable of.
- Physical thickness of each individual dielectric layer is taken into consideration, compared to assumption of infinitely thick dielectric in the Unified Model. Experimental verification shows, the interfacial layer dependence of flicker noise is correctly incorporated in this model, which was a major drawback in the application of the Unified Model.
- A physics based expression for the frequency exponent δ, of the noise spectrum $1/f^{\delta}$ has been obtained in MSUN Model. The resulting expression shows dependence on the trap density profile in the corresponding dielectric layer as well as on its material properties through the carrier tunneling coefficient. In contrast,

the frequency exponent in the Unified Model is always assumed to be 1, which has been experimentally proven wrong.

- The integrals $\int_{LL}^{UL} \frac{u^{\delta'}}{1+u^2} du$ representing the summation of noise in the dielectric were expressed in a compact form, within 1% of the actual integral. For noise predictions, this accuracy is quite satisfactory, as statistical nature of noise shows significant variation in successive measurements on the same sample. The main challenge in preserving the accuracy comes from the large range of values the integral limits can take (LL=10^{-10} to 10^{3} and UL=10^{-6} to 10^{23}) along with a range of values for δ' (-0.3 to 0.3).

The dissertation is organized in the following way. This chapter provides the background, goals and achievements of this work. The necessity of incorporation of high-k materials in scaled MOSFET devices and its consequences on the application of available flicker noise models on devices with high-k dielectrics are briefly explained. The fundamental factors contributing to the observed discrepancies are discussed and possible remedies are mentioned. The implementation of the newly proposed MSUN Model to high-k MOSFETs and the experimental verifications are also briefly discussed.

Chapter 2 provides the details of the experimental setup and procedures used in this work. The variable temperature measurement system as well as its measurement capabilities is discussed.

Chapter 3 provides a brief overview of the dominant flicker noise theories. Then a detailed derivation of the MSUN Model is given in the framework of the original Unified Model.

Chapter 4 explains the results obtained in this work. The verification of remote phonon scattering, identification of the dominant noise mechanism responsible for the observed noise behavior and comparison of the theory and experiment are presented along with experimental data on MOSFETs having four different interfacial layers in a wide temperature and bias range.

Chapter 5 evaluates the overall work considering the importance of the work from industrial application point of view, the goals set originally as the outcome of this work and the achievements made in meeting these goals.

Appendix A describes the Mathcad implementation of the theoretical model.

Appendix B presents the compact form of the MSUN Model and its derivation.

CHAPTER 2

NOISE MEASUREMENTS

2.1 Introduction

2.1.1 Flicker noise measurement

Flicker noise is a well established diagnostic tool for semiconductor device characterization and reliability prediction. Advantages of flicker noise measurements include its non destructive nature as well as ability to be performed on devices with small dimensions, which makes it particularly suitable for characterization of submicron MOSFET devices. The disadvantages of this measurement technique are possible electromagnetic interference from the environment, the sophistication of the experimental assembly and, as a consequence, the requirement of expertise skills to conduct the experimental procedures to acquire noise data.

In this work, flicker noise measurement have been performed on MOSFETs with four different interfacial layer thicknesses to determine the underlying physical mechanisms affecting the low frequency noise mechanism. Statistically meaningful amount of noise data has been acquired to experimentally validate the newly proposed noise model.

2.1.2 Variable temperature measurement

Variable temperature measurements provide a tool to evaluate carrier transport properties in semiconductor devices. A combination of several variable temperature procedures can be effectively used as a powerful characterization technique for the extraction of many temperature dependent device parameters. With the advent of high- κ based submicron MOSFETs, variable temperature measurements find an important application in the characterization of carrier mobility and low frequency noise characteristics of these devices. Remote optical phonon scattering is predicted to be a potential carrier scattering mechanism as an inherent property of high-κ dielectric materials. Temperature dependent nature of the phonon scattering mechanism is the key to this applicability of variable temperature measurements on high-k gate stack devices.

In this work, a variable temperature measurement setup has been built and used for the characterization of submicron high-κ gate MOSFET devices, incorporating the split CV and 1/f noise measurement procedures. The experimental validation of remote phonon scattering was done in the temperature range of 172K to 300K. Determination of any such additional underlying physical mechanism specific to these materials affecting the low frequency noise characteristics will require consideration in the noise formulation as well.

Two different aspects of device characteristics were considered for the investigation of remote phonon scattering effects:

1. Degradation of carrier mobility and
2. Low frequency noise characteristics.

2.2 The experimental setup

Providing a low noise ambient for the DUT is essential in this experiment, as low frequency noise measurements are sensitive to external electromagnetic interferences. To ensure precise control of temperature, good thermal isolation from the surrounding is required to minimize heat exchange by convection and conduction. For low temperature operations, controlling the humidity of the ambient of the DUT becomes an additional requirement, as condensation at lower temperatures can damage the device. The above mentioned requirements are fulfilled by placing the DUT inside a cryostat located in a metallic shielded chamber which minimizes the effect of noise from the surrounding. The cryostat is evacuated to thermally isolate the DUT from its surroundings as well as to minimize the humidity in the DUT ambient.

The following measurement facilities are utilized for characterization:

- DC measurements using a parameter analyzer
- Split CV measurements using a LCR meter and
- Low frequency noise measurements with a customized experimental setup

In this system we have used the cryostat Model RC-110 by CRYO Industries of America, Inc [41]. The cryostat was evacuated using an oil-sealed rotary pump. Welch DUOSEAL vacuum pump, Model 1376 [42] was used in this setup. The bias box was custom made and like the low noise pre amplifier it was low noise battery operated. Low noise preamplifier, Model 113, by EG&G Princeton Applied Research [43] was used in this setup. A HP 4284A LCR meter was utilized for the CV measurements, HP 4155B Parameter Analyzer measured the DC characteristics and the noise spectrum was

captured using a HP3562A Dynamic Signal Analyzer. A schematic diagram of the variable temperature measurement set up is shown in Figure 2.1.

Some of the special features of this setup are as follows:

- Less susceptibility to electromagnetic radiation
- Minimizing heat exchange and humidity
- Precise control of temperature
- Special switching method between the device terminals and the CV, DC and noise measurement setups to ensure device safety from electrostatic discharge effects.

The details of the experimental setup and its special features are available in the cited report [44] by Tanvir Hasan Morshed. The measurement procedures will be explained in latter sections in this chapter.

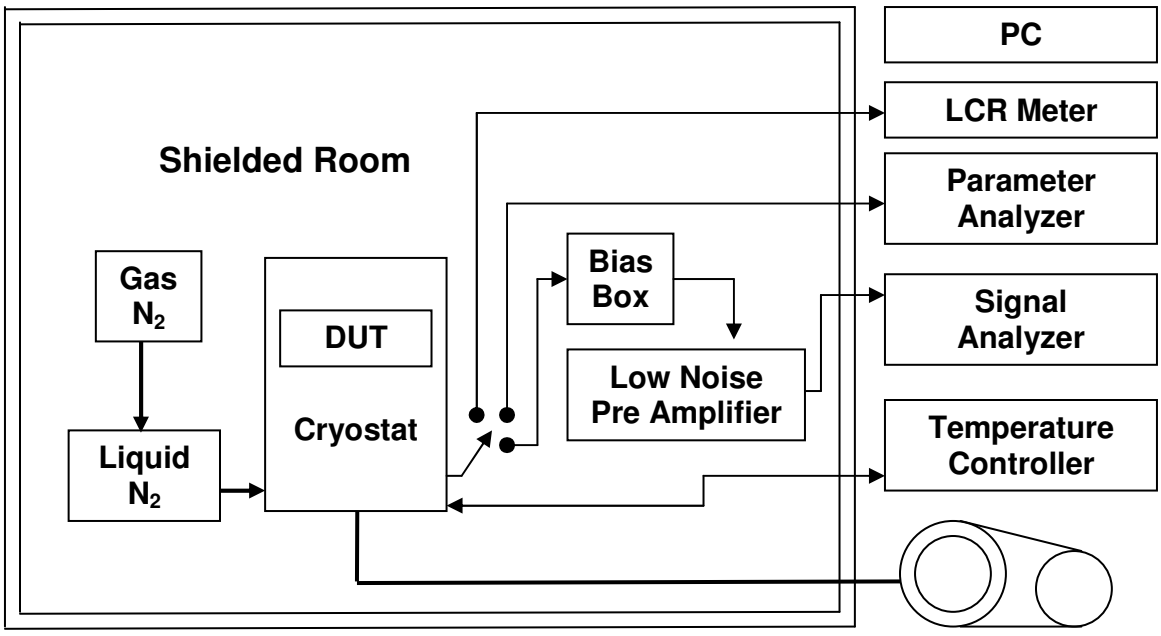


Figure 2.1 The schematic diagram of the variable temperature measurement setup.

2.3 Device specifications

The devices used in this work were provided by Texas Instruments. HfSiON was used as the high-κ gate dielectric material, with a uniform thickness of 3.0 nm on four different wafers. SiON was the interfacial layer (IL) between the dielectric layer and the silicon substrate with thicknesses of 0.8nm, 1.2nm, 1.5nm and 1.8nm; which resulted in effective oxide thicknesses (EOT) of 1.28nm, 1.33nm, 1.46nm and 1.66nm respectively. The lengths of these devices were chosen between 0.20μm and 0.25μm with a width of 10μm. Variable temperature flicker noise measurements were performed on these devices in the temperature range of 172K to 300K. For split CV measurements, larger devices with the dimensions of 10x10 μm^2 (LxW) were used in the same temperature range. Table 2.1 shows the devices used for variable temperature noise measurements.

Table 2.1 Devices used for flicker noise measurements

high-κ material	EOT (nm)	IL(nm)	Length(μm)	Width(μm)
HfSiON	1.24	0.8	0.20	10
HfSiON	1.33	1.0	0.20,0.25	10
HfSiON	1.46	1.5	0.20,0.25	10
HfSiON	1.66	1.8	0.14~0.25	10

2.4 Variable temperature measurement procedure

The experimental procedure was structured keeping in mind the differences in the material properties of high-k dielectrics from SiO_2 that might affect the flicker noise behavior of the devices. The first step was to verify the applicability of any existing flicker noise theory. This step was necessary to identify and establish the underlying physical mechanism that is responsible for the observed noise behavior. The correlated

number and mobility fluctuation model was given emphasis in this verification process for its applicability on both n and p type devices over a wide temperature range. The next step was to verify the effects of remote phonon scattering on these devices to incorporate any significant experimental findings in the formulation of the new noise model. As a part of this step, variable temperature split CV measurement was done to determine the carrier mobility for two purposes: (i) to use in fitting noise data to the predictions of the model, as carrier mobility is needed for the procedure and also (ii) to investigate the effects of remote phonon scattering on carrier mobility. Prior to noise and CV measurements, DC characteristics were taken to make sure the devices work properly in different operating regions of interest.

The overall procedure begins with locating the desired device on the wafer and a careful packaging of the device on a ceramic Leaded Chip Carrier (LDCC) [45] package. The device is then carefully bonded with an ultrasonic wire bonder. Prior to wire bonding a set of DC characteristics is recorded and the package leads are shorted. The bonded device is then mounted on the stage and connected to the wires extending to the ports at the base of the cryostat.

At the base of the cryostat, coaxial T connections were arranged in such a way that, a set of connection ports was always available connecting the device leads, parallel to the other set used for shorting the input ports. This is essential when dealing with nano-scale MOSFET devices, since electrostatic discharge (ESD) due to triboelectric charge formation on semiconductor devices is a well known phenomenon having detrimental effects on device life and performance. Sub-micron MOSFET devices are

especially sensitive to ESD, as charge buildup across the extremely thin dielectric results in very high electric fields and causes gate leakage or in severe cases gate dielectric breakdown. Shorting of the gate and substrate input leads together eliminates the possibility of charge buildup across the gate dielectric and ensures device safety. Thus, the provision of shorting the device inputs was required in any event of physically touching the setup, especially in switching between different experimental setups. To avoid electrostatic charging or discharging through the device or inducing charge on device surface, the operator should be carefully strapped to ground, as human body is very prone to electrostatic charge buildup by simple movements.

One set of ports of the T-connectors at the base of the cryostat is then shorted while the other set is available for any procedure specific setup. As the leads are shorted at the base of the cryostat in parallel, the shorting of the leads on the package can now be removed without harming the device.

After bonding the device, a careful examination of the DC characteristics is done to check for the threshold voltage shift and change in the gate leakage current, to make sure the device is not degraded due to bonding as well as the quality of the electronic contact of the bond is satisfactory. In case of device failure a new device is bonded and the procedure is repeated. The device is then mounted on the cryostat.

The desired temperature is set at the temperature controller, when the vacuum level goes down to 80 mTorr or lower. The PID coefficients are set accordingly. The buffer maintains 10 psi of pressure inside the Dewar when not in use, through its own regulators. As soon as liquid nitrogen flow is started to lower the sample temperature, the

pressure inside the Dewar also starts to fall gradually. The pressure inside the Dewar is used to transfer LN2 through the transfer line from the Dewar to the evaporation chamber. At the beginning, LN2 evaporates very fast even before reaching the evaporation chamber to cool off the transfer line all the way, which ends at the nozzle as shown in Figure 2.2.

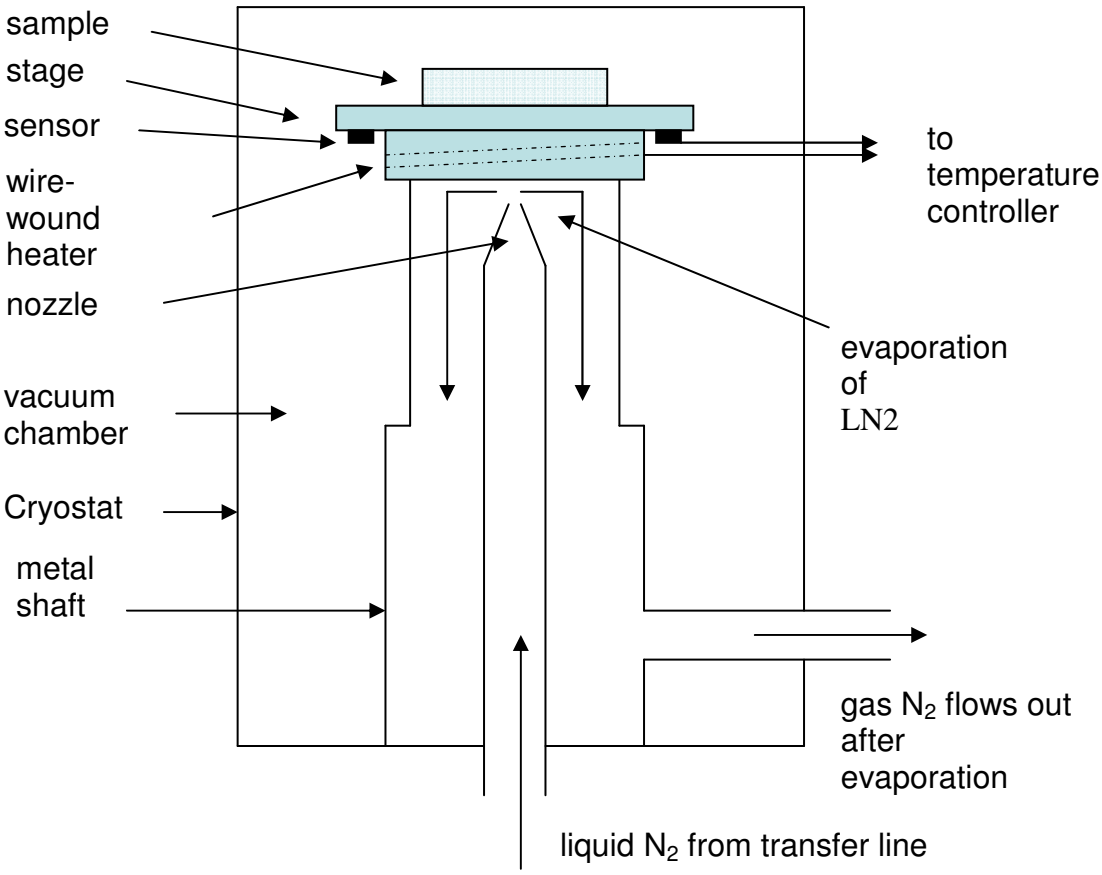


Figure 2.2 The cryogenic temperature setup comprises of two isolated chamber. The vacuum chamber where the sample is mounted maintains thermal isolation between the sample and the environment. In the evaporation chamber LN2 is evaporated to lower the temperature of the stage and the sample.

The evaporation chamber is completely isolated from the vacuum chamber. When the nozzle reaches cryogenic temperatures, LN2 passes through the nozzle tip and evaporates just underneath the stage where the sample is mounted. The evaporation of LN2 lowers down the stage temperature. As the sample maintains very good thermal contact with the stage, the sample temperature goes down as well. The gas N_2, as an outcome of the evaporation, flows out of the system which is not further recycled. When the pressure inside the Dewar goes down to about 4 psi, the gas nitrogen cylinder is turned on and the pressure inside the Dewar is kept constant using the regulator. A higher pressure causes shorter liquid nitrogen life time. A lower pressure is found difficult to maintain at a stable level, causing poor temperature control. The PID coefficient values can be fine tuned at this stage for precise control. A value of P=350, I=50 and D=0 was found a good setup for a temperature range of 300K down to 172K. The experimental procedures were started when the temperature was stable at the desired set point.

2.4.1 DC measurement procedure

The Force/Sense ports from the parameter analyzer HP 4155B were connected to the available ports in parallel to the shorted ones, eliminating the possibility of creating any potential difference across the connecting leads. The Force/Sense ports were set to be maintained at the same potential when idle. In this condition it was possible to safely open the shorted ports without risking the device to static electric charge development across the device inputs.

The basic device parameters such as lead currents I_d, I_s, I_g and I_{sub} as well as the terminal voltages were recorded. User defined functions to obtain the square root of

drain current $SQI_d\left(A^{1/2}\right) = I_d^{1/2}$ and its derivative with respect to gate terminal voltage $DSQI_d\left(A^{1/2}/V\right) = \frac{dSQI_d}{dV_g}$ were evaluated to determine the threshold voltage. The trans-conductance $g_m\left(A/V\right) = \frac{dI_d}{dV_g}$, channel conductance $g_d\left(A/V\right) = \frac{dI_d}{dV_d}$ and the sub threshold swing $S\left(Dec/V\right)$ of the device were also obtained. Details of the setup, extraction procedure and user defined function implementations can be found in the reference [46].

The experimental data acquired in the DC parameter extraction process are illustrated in the following figures.

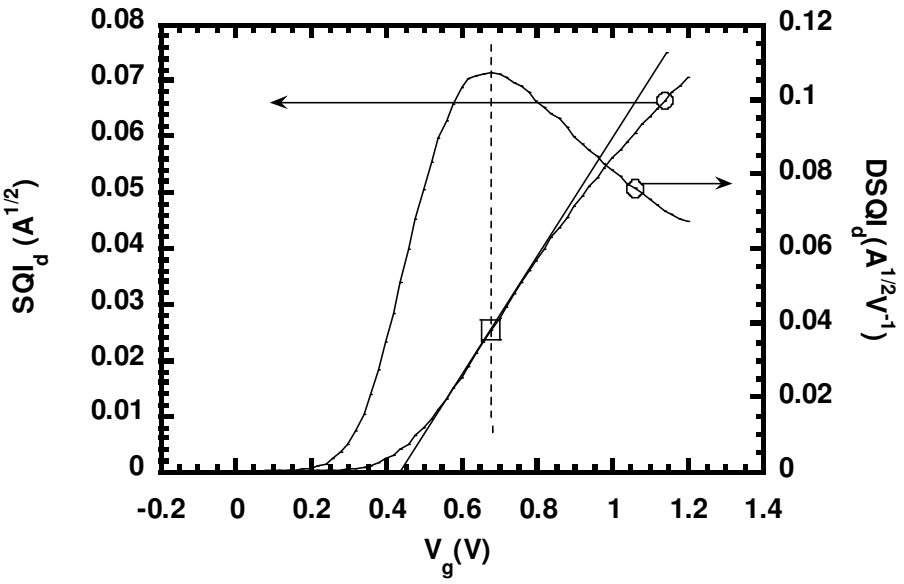


Figure 2.3 Extraction of threshold voltage $V_t\left(V\right)$ is shown here. A tangent is drawn on the curve SQI_d at V_g corresponding to the maxima of $DSQI_d$ (marked by the square on the vertical line). The tangent intersects the V_g axis at the threshold voltage V_t.

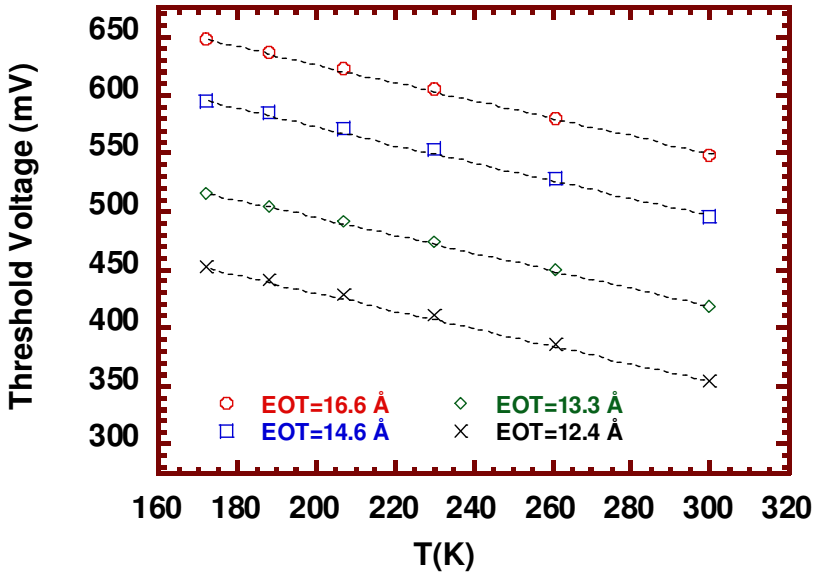


Figure 2.4 The extracted threshold voltage V_t is shown for four different interfacial layer thicknesses. A linear shift was observed in the threshold voltages irrespective of the interfacial layer thickness. The temperature dependence was observed to be identical for all devices.

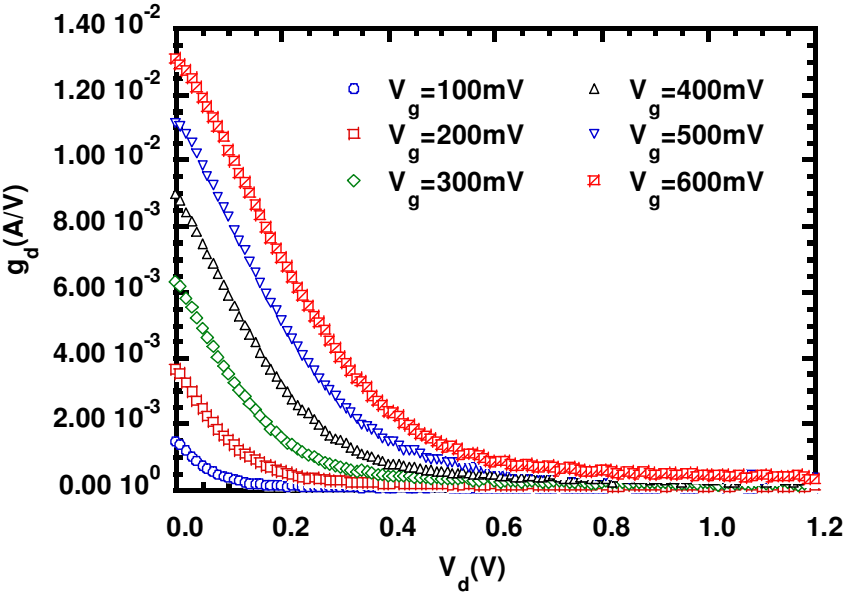


Figure 2.5 Channel conductance g_d as a function of drain voltage V_d for different values of gate voltage (V_g = 100mV to V_g = 600mV).

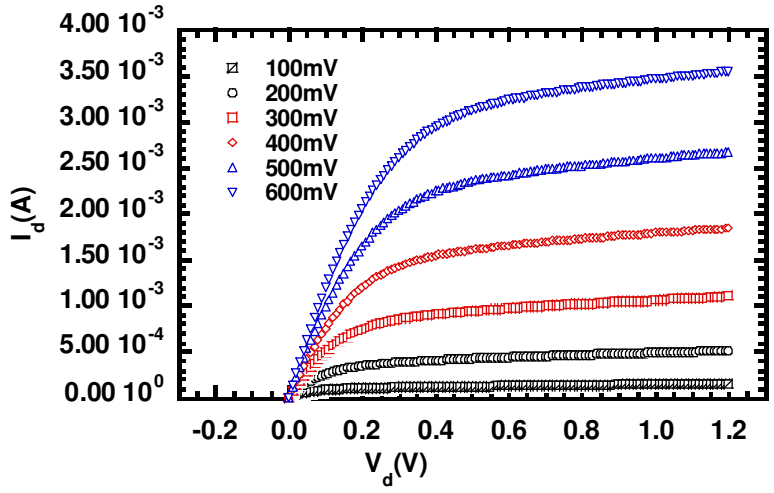


Figure 2.6 Channel current I_d as a function of V_d at different gate voltages in the range of V_g = 100mV to V_g = 600mV.

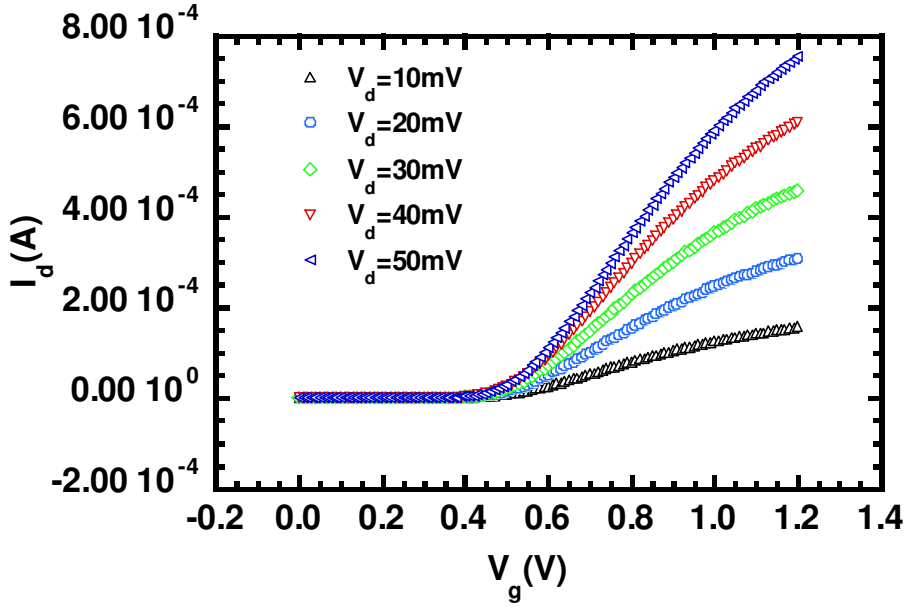


Figure 2.7 Drain current I_d as function of gate voltage V_g at different values of drain voltage (V_d = 10mV to V_d = 50mV).

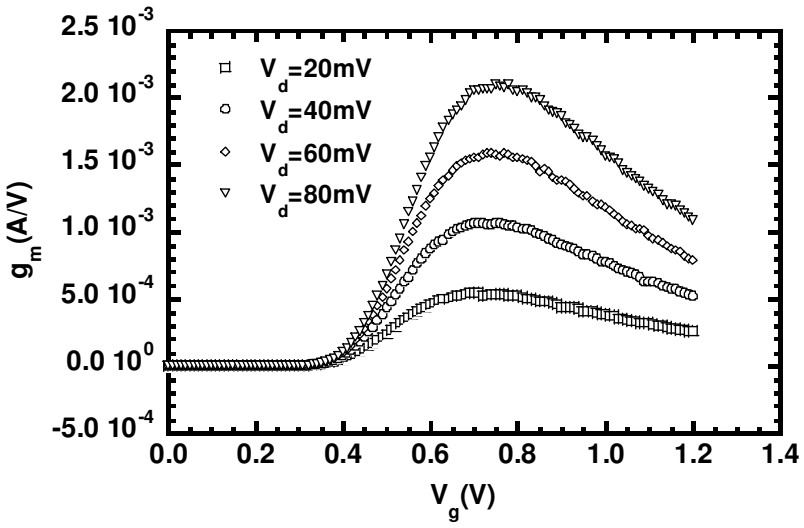


Figure 2.8 The trans-conductance g_m as a function of gate voltage V_g at different drain voltages V_d.

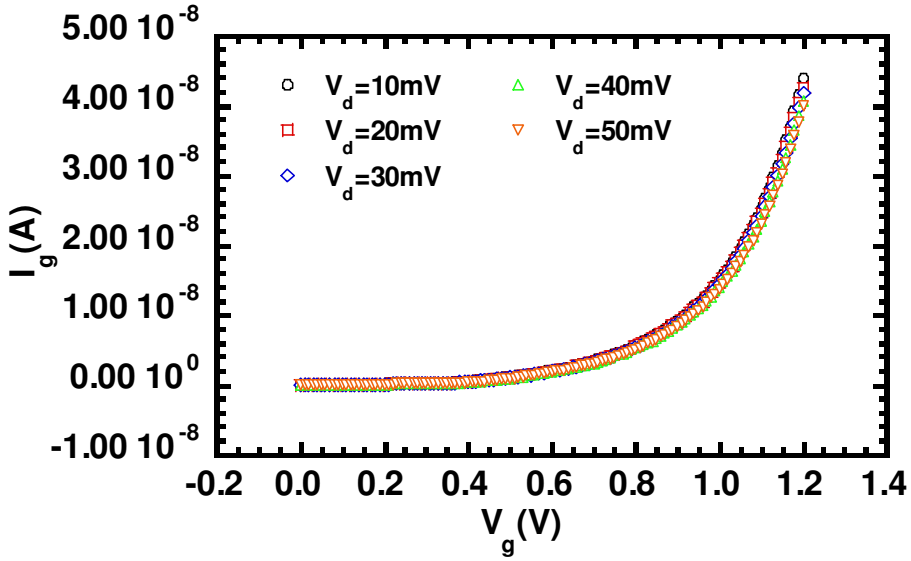


Figure 2.9 Gate leakage current I_g as a function of gate voltage V_g at different drain voltages (V_d = 10mV to V_d = 50mV). With the increase of V_g, the gate leakage current increased exponentially.

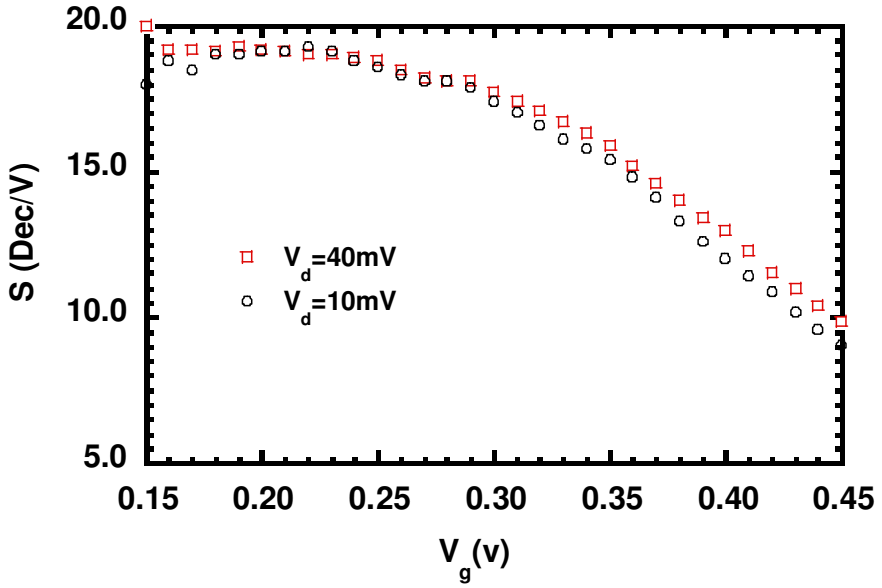


Figure 2.10 Sub-threshold swing *S* (Dec/V) shown as a function of gate voltage at drain voltages of V_d = 10mV and V_d = 40mV.

2.4.2 C-V measurement procedure

The C-V measurements were taken after the completion of DC parameter extraction. When idle, all the Force/Sense ports of the parameter analyzer are maintained at the same potential, as mentioned earlier. As a result, the ports can now be safely shorted using the parallel connections and the Force/Sense connections can be removed. The device was then connected to the LCR meter HP 4284A and the shorting wires in the parallel ports removed. For better estimation of the experimental data, an average of 8 measurements was taken. The operating frequency was chosen to be 1 MHz, to ensure the capacitance due to interface traps did not contribute to channel capacitance. As the channel capacitance was small (~1pf), parallel circuit mode (C_p-D) was selected. Both open and short corrections have been tested, no significant difference was observed in the

evaluated channel capacitance with or without these corrections. The high potential and high current ports were shorted together, as was done for the low potential and low current ports, as described in the operating instructions. To minimize the effects of stray capacitance, the shorting wires were kept as close to the dielectric leads as possible. The gate was connected to the high potential, the drain and source terminals were shorted and connected to the low potential ports. To remove the contribution from the bulk charges, the substrate terminal was connected to the system ground [47]. The details of the setup, theory and procedure can be found in an excellent report by Siva Prasad Devireddy [48]. The schematic of the setup is shown in Figure 2.11.

In C-V parameter extraction, first the channel capacitance is determined from the experimental data. The measured capacitance values are recorded and the stray capacitance measured from the sub-threshold region is subtracted to get the net channel capacitance C_{gc}. The capacitance values are then integrated with respect to V_g to obtain the total charge stored due to the channel capacitance.

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc}\left(V_g\right) dV_g \tag{2.1}$$

The corrected channel capacitance C_{gc} and the calculated inversion charge Q_{inv} are shown in Figure 2.12. Figures 2.13 and 2.14 show the effects of temperature.

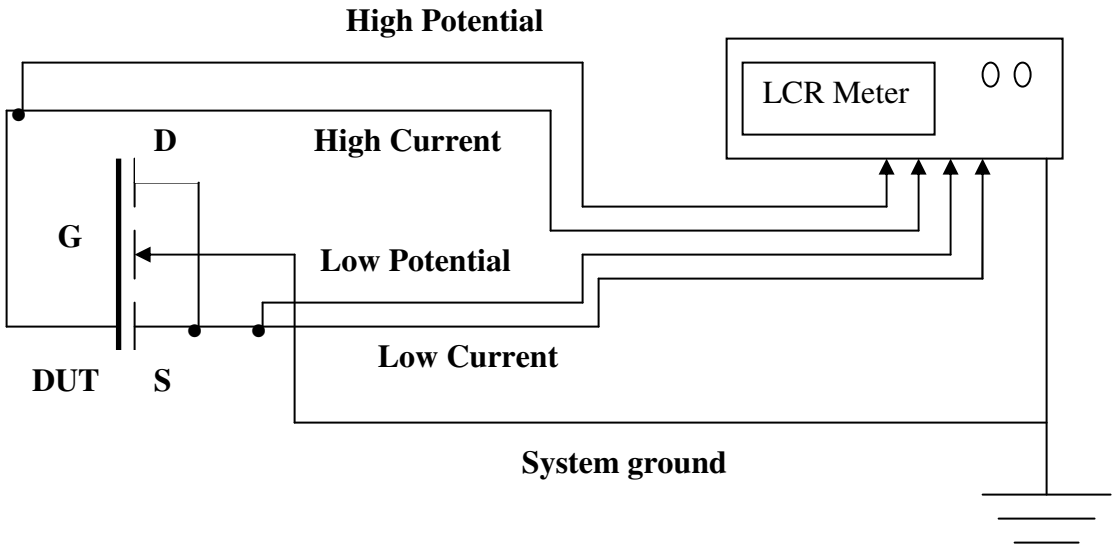


Figure 2.11 The schematic diagram of Split CV measurement.

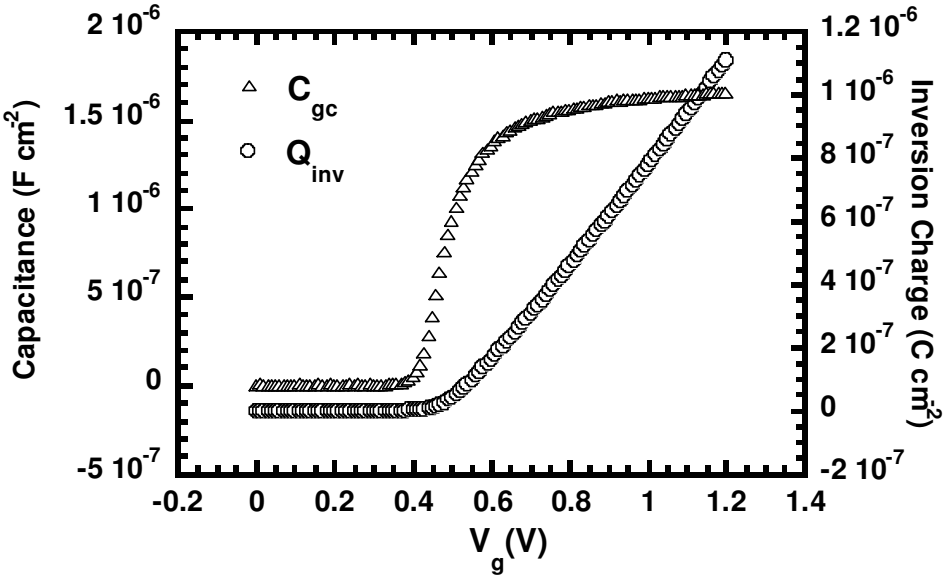


Figure 2.12 The channel capacitance C_{gc} is shown after correction. The calculated channel inversion charge Q_{inv} is also shown here.

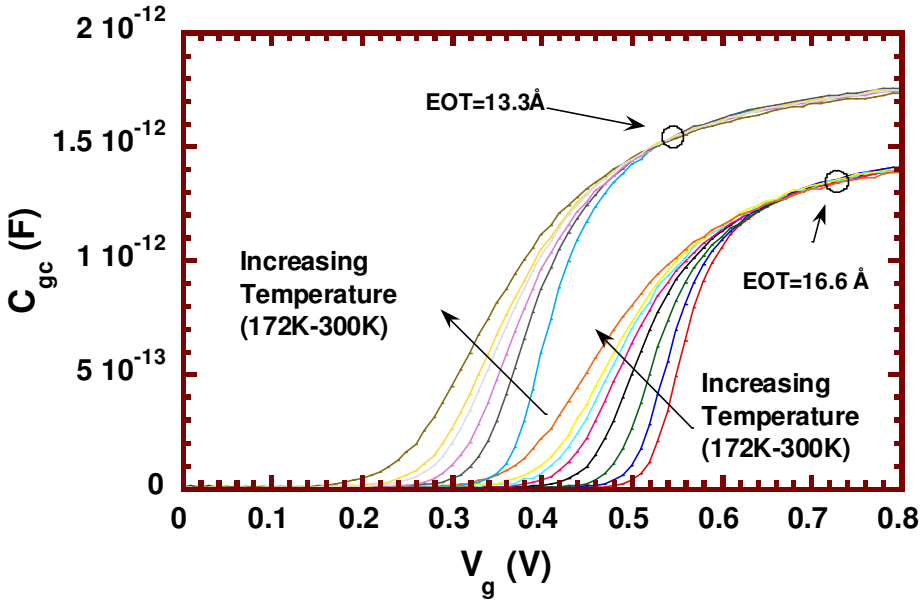


Figure 2.13 The channel capacitance C_{gc} is shown for two different interfacial layer thicknesses, with temperature as a parameter. At lower values of V_g ($\leq V_t$) significant impact of temperature was observed. As temperature decreases the C_{gc} increases more rapidly with increase in V_g. At higher V_g ($>V_t$), C_{gc} does not show dependence on temperature.

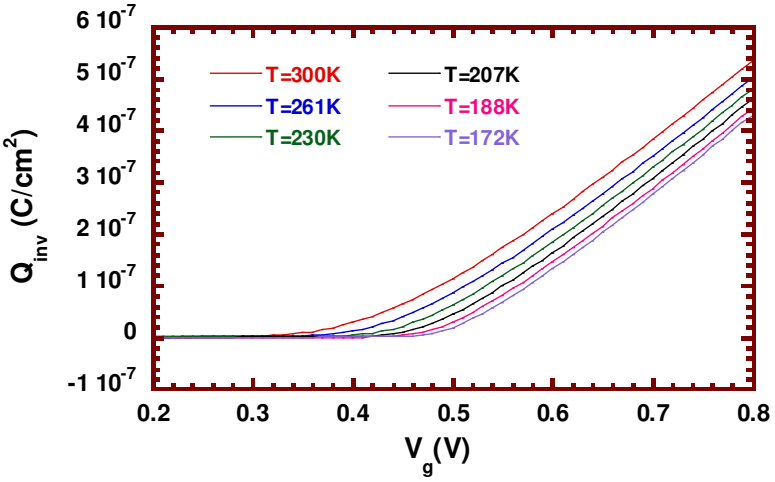


Figure 2.14 The channel inversion charge Q_{inv} is shown as a function of V_g at different temperatures. The effect of threshold voltage shift is reflected in higher inversion charge and smoother transition in the higher temperature region.

The DC data obtained earlier, combined with the CV data, are used to calculate the carrier mobility of the device [49] as:

$$\mu_{eff} = \frac{L}{W} \frac{I_d(V_g)}{V_d Q_{inv}(V_g)} \tag{2.2}$$

In ultra thin gate dielectric MOSFET devices, gate leakage is a prominent phenomenon which often leads to errors in extracted device parameters. If the effect of leakage on the drain current is not considered, the mobility values will be underestimated. The correction for the gate leakage current was done following the work of J. Koga [50], which introduces a modification in the channel conductance as $g_d(V_g) = (I_s(V_g) + I_d(V_g))/2V_d$.

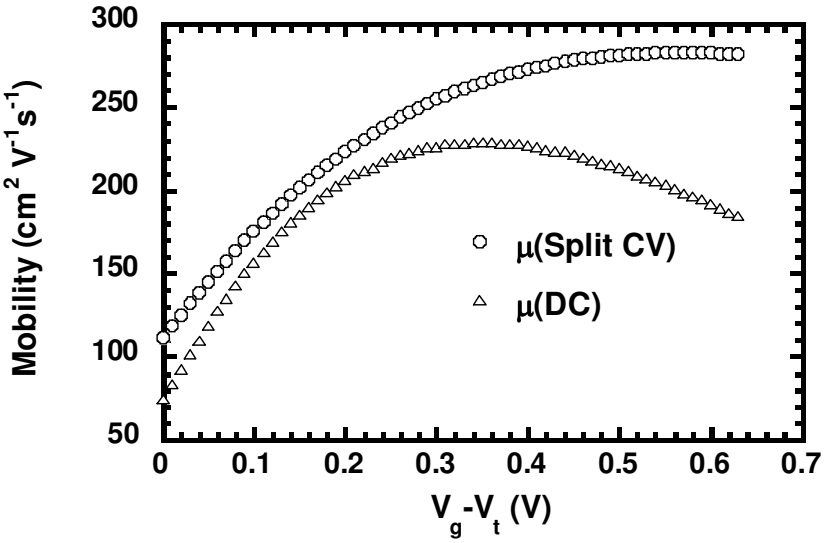


Figure 2.15 Comparison of carrier mobility calculated by DC measurements and split CV measurements. At lower gate over-drive voltage $(V_g - V_t)$ the mobility values differ because of erroneous inversion charge estimation by DC measurements. At higher gate over-drive voltages, DC measurements yield lower mobility values due to underestimation of the gate leakage current.

Comparison of mobility extracted by split CV measurements and that by DC measurements is shown in Figure 2.15, which reveals the effect of channel inversion charge estimation at lower values of V_g and that due to effects of leakage current at higher V_g. Figures 2.16 and 2.17 show the temperature and interfacial layer dependence of carrier mobility, respectively.

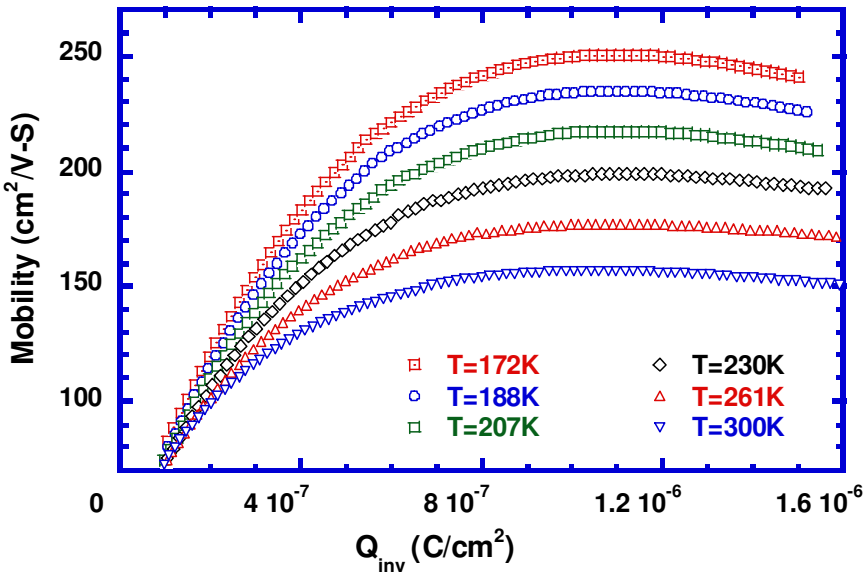


Figure 2.16 Comparison of carrier mobility calculated by the split CV measurements at different temperatures as a function of Q_{inv}. With the increase in temperature carrier mobility was observed to decrease.

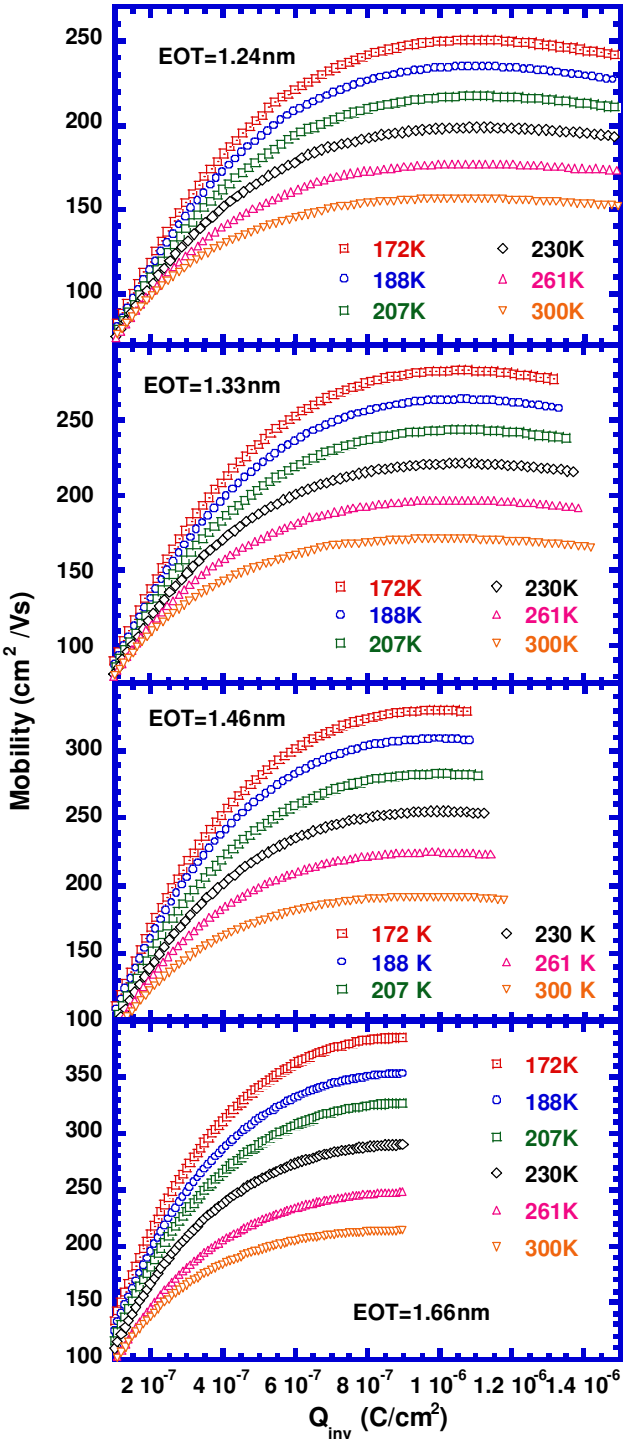


Figure 2.17 Comparison of carrier mobility determined by the split CV measurements for different interfacial layer thicknesses. An inverse dependence of mobility on interfacial layer thickness was observed.

2.4.3 1/f noise measurement procedure

Repeating the shorting procedure, the LCR meter was removed and the DC bias box was connected to the device inputs, followed by removal of the shorting wires. The bias box is used to set the quiescent points of the device at 100mV apart on the gate voltage axis, maintaining a constant 50mV at the drain terminal. The noise data was then acquired using Dynamic Signal Analyzer HP 3562A [51], which was optimally set by a customized computer program prior to each noise measurement. For better estimation of the noise data, 30 averages were used with up to 90% data overlapping. Log resolution was preferred over linear resolution in order to have more sampling points at lower frequency range, which is of particular interest in this experiment. The window type is constructed internally by the signal analyzer; each line in the log resolution is constructed from logarithmic combinations of linear resolution measurement lines. The frequency range was selected to be 1Hz to 100 kHz. To remove any DC offset from the amplifier output, the spectrum analyzer input was always selected to be AC coupled. For better estimation, the data was fitted to obtain the slope in the low frequency range (1Hz to 100Hz). The 1Hz data was used for subsequent noise analysis. The slope ($0.8 \leq \gamma \leq 1.2$) of the spectrum in the log-log scale indicated the validity of the 1/f nature of the device noise. The details of the optimum setup conditions for the signal analyzer can be found in the reference manual [51].

The low noise pre-amplifier preceding the signal analyzer is operated in differential mode to minimize the common mode noise. The inputs are always selected to be AC coupled. The band-pass filters are ideally set between DC to 300 kHz. As the AC

coupling is used at the input, in order to avoid building up of possible output offset voltage resulting from input offset current, the lower cutoff frequency is set to be 0.3 Hz. The gain of the pre amplifier is kept at 1000. The bias circuit for the low frequency noise measurement is shown in Figure 2.18.

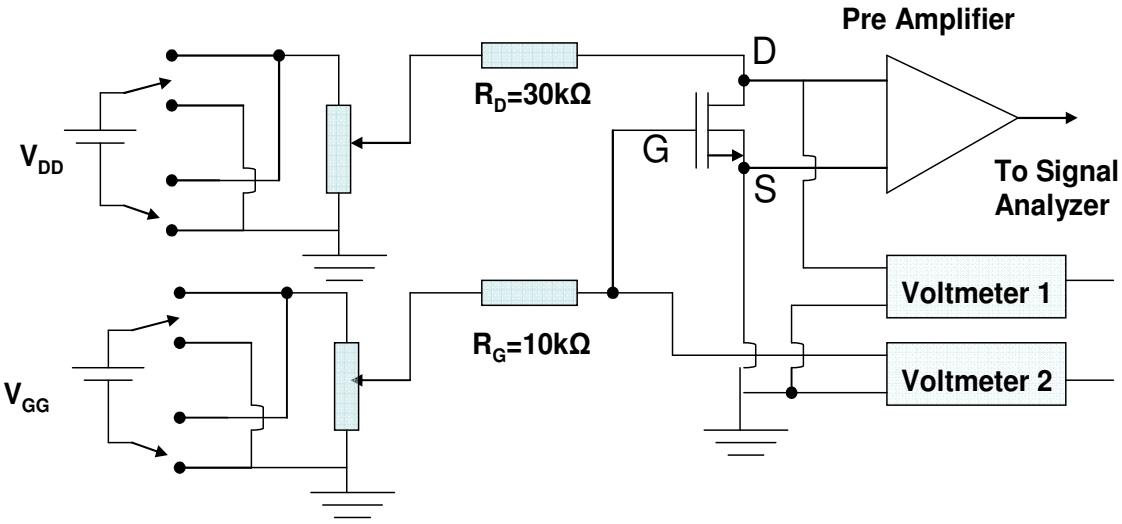


Figure 2.18 The MOSFET bias arrangement for low frequency noise measurements.

The noise data was obtained in two steps. As the background noise is sensitive to measurement setup, special care was taken to minimize it. The voltage noise spectrum $S_{V_d}\left(V^2/Hz\right)$ was obtained from drain and source terminals. The gate voltage was increased in steps of 100mV starting from the threshold voltage up to the device safety rating (1.2 V for the devices used in this investigation). In the first step, the gate voltage $\left(V_g\right)$ was set to the desired bias level, with the voltage across the channel $\left(V_{ds}\right)$ set to zero. The spectrum obtained was saved as the channel background noise at this particular gate bias level. Then V_{ds} was carefully increased to 50mV and the noise measurement

was repeated. The spectrum in the second step was treated as the total device noise at this particular gate bias level. The net noise from the channel was obtained by subtracting the background noise from the total noise in a similar fashion for each bias point of interest. For a better estimation of the experimental data, noise spectrum in the range of 1Hz to 100Hz was used for data fitting and the 1 Hz intercept point was obtained. This data was used for further calculations and comparisons. The noise spike from the line frequency at 60 Hz and its harmonics at 120, 180 Hz are discarded prior to data fitting. A typical voltage noise spectral density and the background noise are shown in Figure 2.19 with fitting of low frequency noise in 1Hz to 100Hz. Using the conductance values (g_d) obtained from the DC measurements, the current noise spectral density $S_{I_d}(A^2/Hz)$ was then calculated following the relation $S_{I_d} = (g_d)^2 S_{V_d}$. Figure 2.20 shows conversion of S_{V_d} into S_{I_d} for noise data at 1Hz. The effect of increasing the gate over-drive voltage on voltage noise spectral density S_{V_d} and that of interfacial layer thickness are depicted in Figures 2.21 and 2.22.

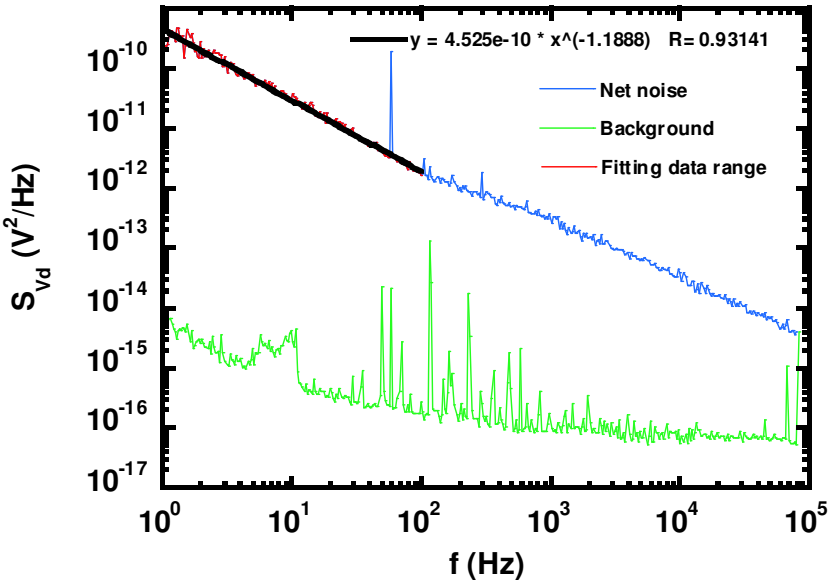


Figure 2.19 Typical 1/f voltage noise spectral density $S_{V_d}\left(V^2 Hz^{-1}\right)$ is shown with the background. The data range (highlighted) used for fitting and the fit equation is also shown. The 60Hz noise peak has been removed from the fitting data.

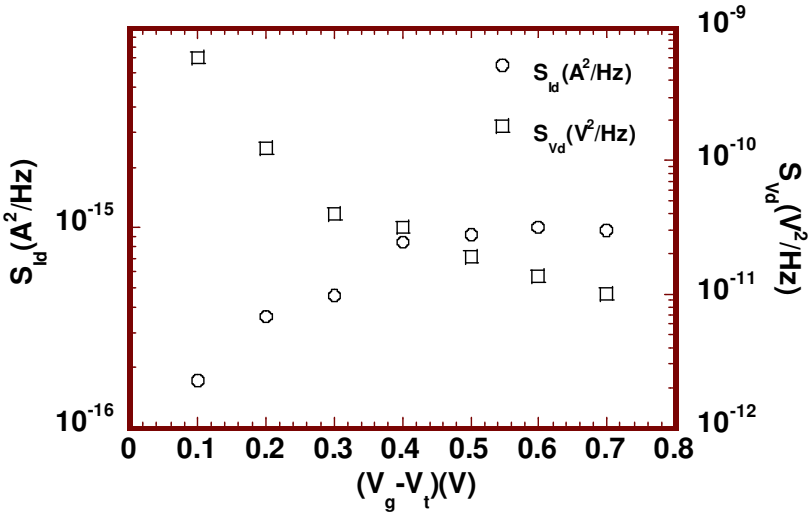


Figure 2.20 The current noise spectral density S_{I_d} is shown with the corresponding voltage noise spectral density S_{V_d}. The S_{V_d} at 1Hz intercept point and g_d have been used for the calculation of S_{I_d}.

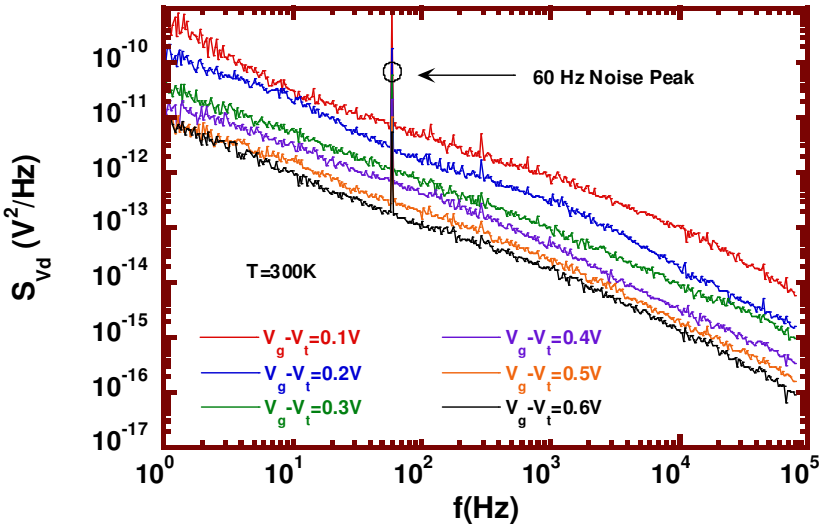


Figure 2.21 The voltage noise spectral density S_{V_d} is shown as a function of frequency at different gate over-drive voltages. Increasing the gate over-drive voltage decreased flicker noise.

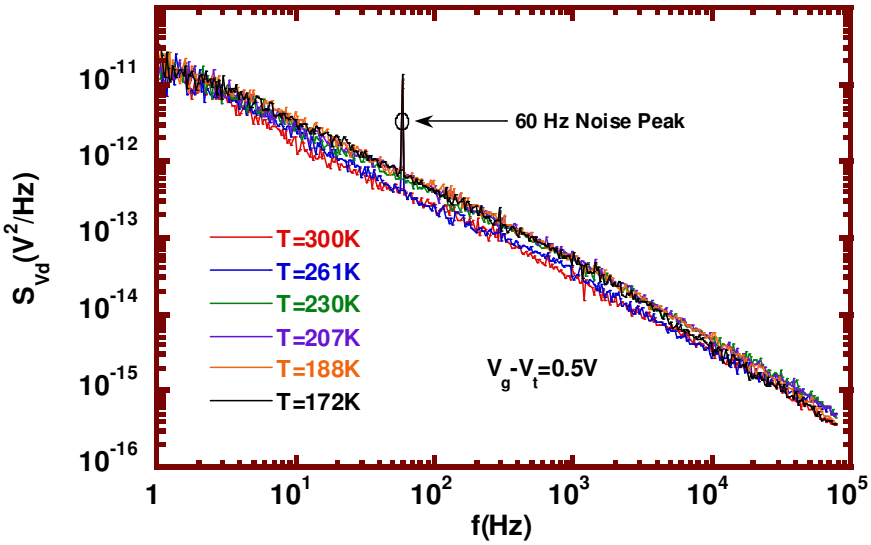


Figure 2.22 The voltage noise spectral density S_{V_d} is shown as a function of frequency at a fixed gate over-drive voltage at different temperatures. S_{V_d} does not show any noticeable dependence on temperature in the experimental range of 172K to 300K.

Many precautions were taken throughout the measurement procedure. The operator was strapped to ground reference to avoid static electric discharge. Proper shorting of the device input ports is also important. The bias box potentiometers were always set to zero before any changes were made to the circuit. As the sensitivity of the preamplifier is very high, any kind of switching was avoided after turning on the amplifier. To ensure this, the preamplifier was turned on as the last element in the whole setup and turned off as the first.

2.5 Summary

A variable temperature measurement setup was used in this experiment with the capability of DC, split-CV and 1/f noise measurements on high-k gate stack MOSFET devices in the temperature range of 172K to 300K. Taking into consideration the sensitivity of the nano-scale MOSFETs to static electric discharge, proper means of switching between different setups was provided by shorting the device inputs. The variable temperature feature enabled verification of the effects of remote phonon scattering on carrier mobility as well as flicker noise characteristics of the MOSFETs. The experimental data was also used for the validation of the newly proposed MSUN model.

CHAPTER 3

DEVELOPMENT OF MSUN MODEL

3.1 Introduction

The expressions for the newly proposed Multi Stack Unified Noise (MSUN) model is developed in this Chapter. First, the widely accepted flicker noise theories for MOSFET devices; i. the number fluctuation model and ii. the bulk mobility fluctuation model are briefly described. The correlated number and surface mobility fluctuation model, which is the most successful flicker noise model for both n and p channel MOSFETs derived from the classical number fluctuation theory, has been considered in this case. The noise formulation in the original Unified Model is then explored, which is based on the correlated number and mobility fluctuation model. The distinct features differentiating the high-k gate stacks from SiO_2 as the dielectric; namely, i. multi-layered gate dielectric structure and ii. energy and spatial dependence of trap distribution inside the dielectric are explained next. The Unified model is then extended into the newly proposed MSUN Model by implementing the above mentioned features.

3.2 The flicker noise theories for MOSFET devices

3.2.1 Carrier number and correlated mobility fluctuations

According to the number fluctuations theory, tunneling of carriers from the channel to the interface trap sites causes a fluctuation in the carrier numbers, which in

turn, causes the fluctuations in the drain current. The fluctuations in the interface traps δQ_t are related to the fluctuations in the flat-band voltage δV_{fb} as [52]:

$$\delta V_{fb} = -\delta Q_t / C'_{ox} \tag{3.1}$$

where $C'_{ox} = WLC_{ox}$, with L (cm) as the length, W(cm) the width and $C_{ox}\left(Fcm^{-2}\right)$ as the oxide capacitance per unit area.

As the occupied trap density also changes by the trapping of carriers, a fluctuation in the Coulomb potential between the carriers and the interface charges may cause a correlated fluctuation in the carrier mobility. Considering the number fluctuations along with the correlated mobility fluctuations, the fluctuations in the drain current can be shown as [52, 15]

$$\delta I_d = -g_m \delta V_{fb} \pm \alpha I_d \mu_{eff} \delta Q_{it} \tag{3.2}$$

where $g_m\left(A/V\right)$ is the trans-conductance, $\mu_{eff}\left(cm^2/Vs\right)$ is the effective mobility, $\alpha\left(Vs\right)$ is the screened scattering coefficient and $I_d\left(A\right)$ is the channel current. Thus, we can show in the strong inversion [52]:

$$\frac{\delta I_d}{I_d} = -\left(1 \mp \alpha\mu_{eff} \frac{I_d}{g_m}\frac{\delta Q_{it}}{\delta V_{fb}}\right)\left(\frac{g_m}{I_d}\right)\delta V_{fb} \tag{3.3}$$

From Eq. (3.1), $$\frac{\delta I_d}{I_d} = \left(1 \pm \alpha\mu_{eff} \frac{I_d}{g_m} C'_{ox}\right)\left(\frac{g_m}{I_d}\right)\delta V_{fb} \tag{3.4}$$

or, $$\frac{S_{I_d}}{I_d^2} = \left(1 \pm \alpha\mu_{eff} C'_{ox} \frac{I_d}{g_m}\right)^2 \left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \tag{3.5}$$

According to Eq. (3.5) S_{I_d}/I_d^2 shows variations similar to $(g_m/I_d)^2$ when plotted as a function of I_d. In modern day MOSFET devices (L < 0.35 μm), both N and P type, where the conduction occurs near the Si/dielectric interface, this behavior is clearly seen [52]. Eq. (3.5) is valid in nonlinear region of MOSFET operation as well [53]. The above expression can be utilized to experimentally determine if the MOSFET noise is following correlated number and surface mobility fluctuation theory.

3.2.2 Hooge mobility fluctuations

Hooge's theory predicts that, fluctuations in the drain current is caused by fluctuations in the bulk mobility of the carriers, which may find its origin in the variation of the collision capture cross section due to bulk phonon number fluctuations [52]. The normalized drain current noise in the Ohmic region can be shown as

$$\frac{S_{I_d}}{I_d^2} = \frac{\alpha_H}{fN} \tag{3.6}$$

where N is the number of carriers in the channel, f (Hz) is the frequency, α_H is the Hooge parameter. With L(cm) and W(cm) as the length and the width of the device we have $N = WLQ_{inv}/q$. In the linear region, as the inversion charge is not uniform along the channel, the normalized drain current spectral density can be shown as [54]:

$$\frac{S_{I_d}}{I_d^2} = \frac{q\alpha_H}{fWL^2}\int_0^L \frac{dx}{Q_{inv}(x)} \tag{3.7}$$

assuming $V_x = V_d(x/L)$, with a change of variable from x to V_x we can show

$$\frac{S_{I_d}}{I_d^2} = \frac{q\alpha_H}{fWL^2}\int_0^{V_d}\frac{W\mu_{eff}}{I_d}dV_x \tag{3.8}$$

which simplifies to

$$\frac{S_{I_d}}{I_d^2} = \frac{q\alpha_H\left\langle\mu_{eff}\right\rangle V_d}{fL^2 I_d} \tag{3.9}$$

Hooge's bulk mobility fluctuation theory fails to explain the noise behavior of MOSFET devices in weak inversion. Following Eq.(3.6) noise in this region should follow $1/N$ or following Eq.(3.9) it should be proportional to $1/I_d$, which predicts an exponential increase of normalized current noise spectral density S_{I_d}/I_d^2 in the sub-threshold region [54]. In most cases the noise predicted in this region is far less than the prediction of Eqs.(3.6) and (3.9) [20]. In general, in the surface mode operated MOSFETs, the Hooge model does not show a good agreement, although for bulk mode operated devices this model has been observed to provide better predictions. In 0.35 µm technology (L=0.35µm), P type devices were observed to obey mobility fluctuation model due to the buried architecture of the channel, where the device operates in bulk mode [52].

Hooge's constant α_H was originally believed to be applicable for all materials with a value $\approx 10^{-3}$. For Si α_H has been observed in the range of $5\text{x}10^{-6}$ to $2\text{x}10^{-3}$, α_H was not believed to be a constant anymore, rather it was assumed to vary from sample to sample depending on the material and device quality. Even though several theories have been suggested regarding the nature of α_H, none of them are well established to be

generally accepted. Hooge parameter is still considered as purely empirical and technology dependent.

3.3 Theoretical and experimental basis of the new model

As explained earlier, even though the Unified Model based on the correlated number and mobility fluctuation theory proves to be the most successful flicker noise model for devices with SiO_2, discrepancies are observed in the extracted high-k MOSFET parameters using this model. Noting the differences in the structure and the material properties between the high-k gate stack and SiO_2 as the dielectric, some related fundamental issues were investigated to lay the theoretical foundation of the new model, as will be discussed here. The effect of phonon scattering was experimentally found to be negligible; indicating no additional noise mechanism was required to be included in the new model. Correlated number and mobility fluctuation theory was experimentally validated to be the dominant noise mechanism responsible for the observed noise behavior. Consequently, the new model was developed on the framework of the original Unified Model, based on the same theory. The distinctions of the high-k gate stack from SiO_2 dielectric were identified, most significant among them being the multi layered structure of the gate stack and the distribution of traps inside the dielectric which is dependent on both carrier energy and tunneling distance from the interface. Thus, a single experimental value of trap density used in the Unified Model was replaced by a more flexible expression showing exponential dependence on energy and spatial distribution of traps as well as band bending in the dielectric. The multi stack gate structure was implemented by considering tunneling of carriers through a double step

cascaded barrier. The above implementation results in the necessary modifications in the spectral density expression due to fluctuations in the trapped carriers $S_{\Delta Nt}$, thus, incorporating the noise contribution from both the interfacial layer as well as the high-k layer.

The experimental verification of the dominant noise mechanism and the impact of remote optical phonon scattering are explained in detail in Chapter 4.

3.4 Development of the MSUN Model

3.4.1 The Unified Model

For a section of the channel with a length of $\Delta x(cm)$ and a width of $W(cm)$ as shown in Figure 3.1, the current can be expressed as $I_d = W\mu qNE_x$, where $\mu(cm^2V^{-1}s^{-1})$ is the carrier mobility, $q(C)$ is carrier charge and $N(cm^{-2})$ is the number of carriers per unit area. Interaction of carriers with the traps in the interface causes correlated fluctuations in the carrier number and carrier mobility. The resulting fluctuations in drain current $I_d(A)$ due to this correlated number and mobility fluctuations can be shown as [15,23]:

$$\frac{\delta I_d}{I_d} = -\left[\frac{1}{\Delta N}\frac{\delta \Delta N}{\delta \Delta N_t} \pm \frac{1}{\mu}\frac{\delta \mu}{\delta \Delta N_t}\right]\delta \Delta N_t \tag{3.10}$$

where $\Delta N = NW\Delta x$ and $\Delta N_t = N_t W\Delta x$ with $N_t(cm^{-2})$ as the occupied traps per unit area. The sign in front of the mobility term is to be taken as positive for repulsive-type traps and negative for attractive-type traps, i.e. depending on the nature of trap state in the oxide when filled and its interaction with the channel carriers.

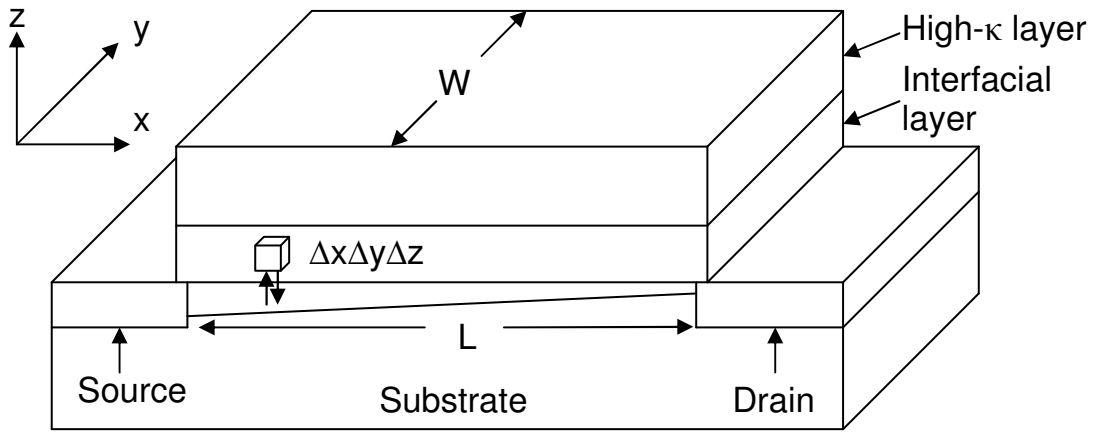


Figure 3.1. The schematic diagram of a MOSFET with high-k material as the gate stack with a channel length of L and width of W.

From Mathiessen's rule we can show that $\mu^{-1} = \mu_n^{-1} + \mu_{ox}^{-1}$, where $\mu_{ox}\left(cm^2V^{-1}s^{-1}\right)$ is the mobility limited by scattering by the charged oxide traps, $\mu_n\left(cm^2V^{-1}s^{-1}\right)$ is that by other scattering processes and $\mu\left(cm^2V^{-1}s^{-1}\right)$ is the resultant overall carrier mobility. With $\mu_{ox} = \left(\alpha N_t\right)^{-1}$, we have $\delta\mu/\delta\Delta N_t = -\alpha\mu^2/W\Delta x$, where the screened scattering coefficient $\alpha = \left(\mu_{co}N^{1/2}\right)^{-1}$, with $\mu_{co}\left(cmV^{-1}s^{-1}\right)$ as a fitting parameter [55].

For moderate to strong inversion, $\delta\Delta N/\delta\Delta N_t = 1$ [15]. The impact of the term $\delta\Delta N/\delta\Delta N_t$ on the flicker noise of MOSFETs in different operation regions are very well explained through Reimbold's model. In this model, McWhorter's number fluctuation theory is further extended and the small signal capacitive components of the device are

included. Conservation of charges in the MOSFET system governs that, any change in the fluctuation in the tapped charge Q_t should follow:

$$\delta Q_G + \delta Q_{it} + \delta Q_D + \delta Q_n + \delta Q_t = 0 \tag{3.11}$$

Here, δQ_G, δQ_{it}, δQ_D and $\delta Q_n = -q\delta N$ are fluctuations in the gate charge, interface trap charge, depletion charge and inversion charge respectively. Denoting the fluctuation in the surface potential (ϕ_s) as $\delta\phi_s$ we can show $\delta Q_G = -C_{ox}\delta\phi_s$, $\delta Q_{it} = -C_{it}\delta\phi_s$, $\delta Q_D = -C_D\delta\phi_s$, $\delta Q_n = -C_n\delta\phi_s$. C_{it} is the capacitance associated with the interface traps and $C_n = -(q/kT)Q_n = -\beta Q_n$, q is the electronic charge, k is the Boltzmann constant and T is the temperature. As fluctuations in the trapped carriers equal fluctuations in the occupied traps, we can show:

$$\delta\Delta N/\delta\Delta N_t = \delta Q_n/\delta Q_t = -\beta Q_n/(C_D + C_{ox} + C_{it} - \beta Q_n) \tag{3.12}$$

For weak inversion $|\beta Q_n| << C_{ox} + C_D + C_{it}$; $\delta\Delta N/\delta\Delta N_t = 1/(C_{ox} + C_D + C_{it})$ with a typical value of 10^{-10} [R]. For the strong inversion $|\beta Q_n| >> C_{ox} + C_D + C_{it}$; which results in $\delta\Delta N/\delta\Delta N_t \approx \beta Q_n/\beta Q_n = 1$.

The sign in front of the mobility fluctuations term in Eq. (3.10) is taken to be positive for repulsive traps (negatively charged when full) interacting with electrons in an n-MOSFET [15]. For donor type traps, loosing an electron puts the trap in positive charge state and gaining it back neutralizes the trap. Whereas, acceptor type traps are neutral when empty of an electron (analogously filled with a hole), trapping an electron puts it in negatively charge state (the hole recombines with the electron). For n channel

MOSFETs, experimental data shows presence of acceptor type charges in the dielectric interface [15]. This means tunneling of electrons in these traps results in an electrostatic repulsive force that increases with the number of trapping. The scattering of carriers associated with this repulsive force lowers the carrier mobility and increases the device noise. This increase in the device noise is reflected by the positive sign in front of the mobility fluctuation component. Thus:

$$\frac{\delta I_d}{I_d} = -\left[\frac{1}{N} + \alpha\mu\right]\frac{\delta \Delta N_t}{W \Delta x} \tag{3.13}$$

which gives

$$S_{\Delta I_d}(x,f) = \left[\frac{I_d}{\Delta N}(1+\alpha\mu N)\right]^2 S_{\Delta N_t}(x,f) \tag{3.14}$$

with

$$S_{\Delta N_t}(x,f) = \int_{E_v}^{E_c}\int_0^W \int_0^{T_{ox}} 4N_t(E,x,y,z)\Delta x f_t(1-f_t)\frac{\tau(E,x,y,z)}{1+\omega^2\tau(E,x,y,z)^2}dzdydE \tag{3.15}$$

where $N_t(E,x,y,z)$ is the trap distribution in the gate dielectric in $eV^{-1}\,cm^{-3}$, $\tau(E,x,y,z)$ is the trapping time constant, $f_t = \left[1+\exp(E-E_{fn})/kT\right]^{-1}$ is the trap occupancy function, $T_{ox}(cm)$ is the physical thickness of the dielectric, $\omega = 2\pi f$ with f as the signal frequency, $E_{fn}(eV)$ is the quasi Fermi level for electrons, $E_c(eV)$ and $E_v(eV)$ are the conduction and valence band edges, respectively. It is assumed that the probability of a carrier tunneling into the oxide decreases exponentially with the distance [15, 56]. Thus dielectric time constant $\tau = \tau_0 \exp(\gamma z)$ where $\tau_0(s)$ is the time constant at the interface

and $\gamma\left(cm^{-1}\right)$ is the attenuation coefficient given by WKB theory as $\gamma = \left(4\pi/h\right)\left(2m^{*}\Phi_{B}\right)^{1/2}$ in terms of Planck's constant $h\left(Js\right)$, $m^{*}\left(g\right)$ the electron effective mass in the dielectric and $\Phi_{B}\left(V\right)$ the barrier height [56].

Then using Eq. (3.14) and (3.15), the current noise spectral density expression can be given for the total length of the device $L\left(cm\right)$ as:

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{\Delta I_d}(x, f)\Delta x dx \tag{3.16}$$

3.4.2 Distinct features of high-k gate stack

3.4.2.1 The trap distribution function

The original Unified Model assumes uniform dielectric trap distribution with respect to both energy and distance from the interface. In the new model, a more realistic trap profile is implemented where the energy and spatial distribution of the traps are considered with a generalized expression appearing in Eq. (3.17). Figure 3.2 shows the energy and spatial distribution of traps that applies for the interfacial layer as well as the high-k layer.

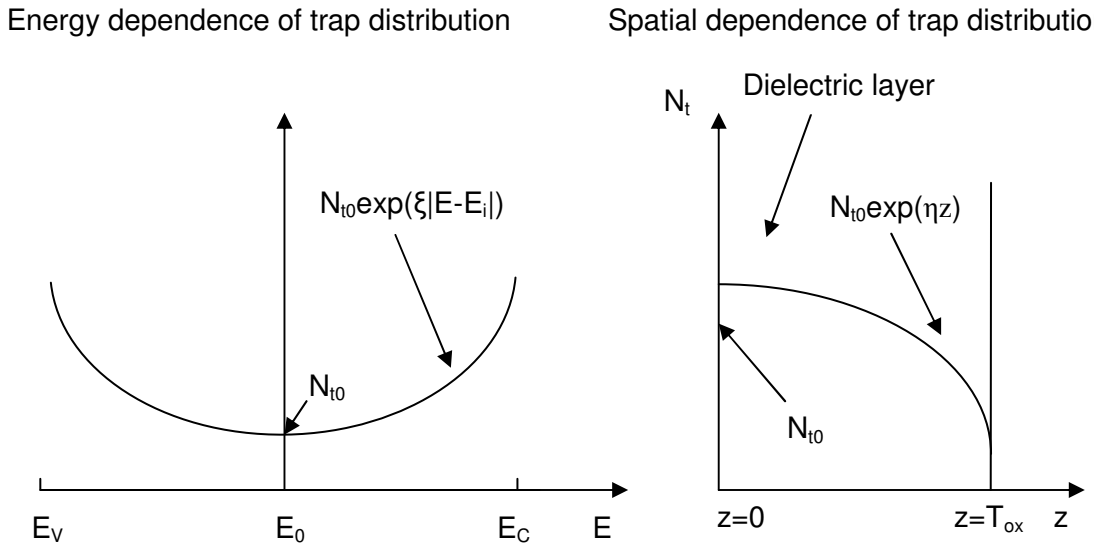


Figure 3.2. The variation in the trap density due to energy (with positive ξ) and spatial distribution of traps (η is assumed negative).

$$N_t(E,z) = N_{t0}\exp\left[\xi(E-E_i) + q\lambda\left(\frac{V_g - V_x}{T_{ox}}z\right) + \eta z\right] \tag{3.17}$$

The exponential energy distribution of traps – the first term in Eq. (3.17) - in the silicon dioxide is well-known [34, 35] and has been used in noise modeling before [34, 37]. The last term is the physical variation in the trap density with respect to distance into the dielectric. Although this is not very pronounced in SiO_2, stacked dielectric layers are expected to cause trap non-uniformity [13]. The amount of band-bending ($V_g - V_x$) also introduces non-uniformity in the trap density that the electron encounters as it tunnels into the dielectric. This is represented by the second term in Eq. (3.17) with the parameter $\lambda\left(eV^{-1}\right)$. Typically, $\xi = \lambda$ since the non-uniformity caused by the band-bending is artificially induced by the energy distribution of the traps. However, slightly

different values for λ have also been assumed in the past for SiO_2 traps [34]. Here, we have taken $\xi\left(eV^{-1}\right)$, $\lambda\left(eV^{-1}\right)$ and $\eta\left(cm^{-1}\right)$ as fitting parameters to verify the model with the measured noise data. $N_{t0}\left(cm^{-3}eV^{-1}\right)$ is the mid-gap trap density at the interface (z=0) and $V_x(V)$ is the voltage drop at position $x(cm)$ along the channel given by $V_x = V_d\left(x/L\right)$, in the region where gradual channel approximation is valid. For the experimental data presented in this paper the applied voltage at the drain terminal was V_d = 0.05V whereas the gate voltage $V_g(V)$ was incremented in steps of 0.1V starting from the threshold voltage $V_t(V)$. This ensures that the aforementioned expression for V_x is valid for all experimental data points. Furthermore, as the applied drain potential in this particular case is negligibly small, the channel was assumed to be uniform for noise evaluation by the model.

Considering that only the traps around the quasi-Fermi level for electrons participate actively [15, 56], the energy integral in Eq. (3.15) is solved as

$$\int_{E_v}^{E_c} N_t(E,z) f_t(1-f_t)dE \approx kTN_t\left(E_{fn},z\right) \tag{3.18}$$

where *k (J/K)* is the Boltzmann's constant and *T(K)* the temperature.

Defining, $f_t = \left[1+\exp\left(E-E_{fn}\right)/kT\right]^{-1}$ we have:

$$f_t(1-f_t) = \left[1+\exp\left(E-E_{fn}\right)/kT\right]^{-1}\left[1-\left[1+\exp\left(E-E_{fn}\right)/kT\right]^{-1}\right]$$

$$= \frac{1}{1+\exp\left(E-E_{fn}\right)/kT}\,\frac{\exp\left(E-E_{fn}\right)/kT}{1+\exp\left(E-E_{fn}\right)/kT}$$

$$= -kT\left[-\left[\exp\left(E-E_{fn}\right)/kT\right]^{-2}\right]\left[\exp\left(E-E_{fn}\right)/kT\right]\left[1/kT\right]$$

$$= -kT\frac{d}{dE}\left[\exp\left(E - E_{fn}\right)/kT\right]^{-1}$$

or, $$f_t\left(1 - f_t\right) = -kT\frac{df_t}{dE} \tag{3.19}$$

$$\int_{E_v}^{E_c} N_t\left(E,z\right) f_t\left(1 - f_t\right) dE = \int_{E_v}^{E_c} N_t\left(E,z\right)\left(-kT\frac{df_t}{dE}\right) dE$$

$$= -kT\int_{E_c}^{E_v} N_t\left(E,z\right) df_t$$

or, $$\int_{E_v}^{E_c} N_t\left(E,z\right) f_t\left(1 - f_t\right) dE = -kTN_t\left(E_{fn},z\right) \tag{3.20}$$

Substitution of N_t from the above expression into Eq. (3.15) gives

$$S_{\Delta N_t} = 4kTW\Delta x\int_0^{T_{ox}} N_{t0}\exp\left[\xi(E_{fn} - E_i) + q\lambda\left(\frac{V_g - V_x}{T_{ox}}\right)z + \eta z\right]\frac{\tau}{1+\omega^2\tau^2}\,dz \tag{3.21}$$

3.4.2.2 Multi layered gate stack

As opposed to a single layer of dielectric assumed in the Unified Model, multi layered structure of the gate-stack has been considered in the MSUN Model. The tunneling process for a double layered gate stack can be shown as depicted in Figure 3.3.

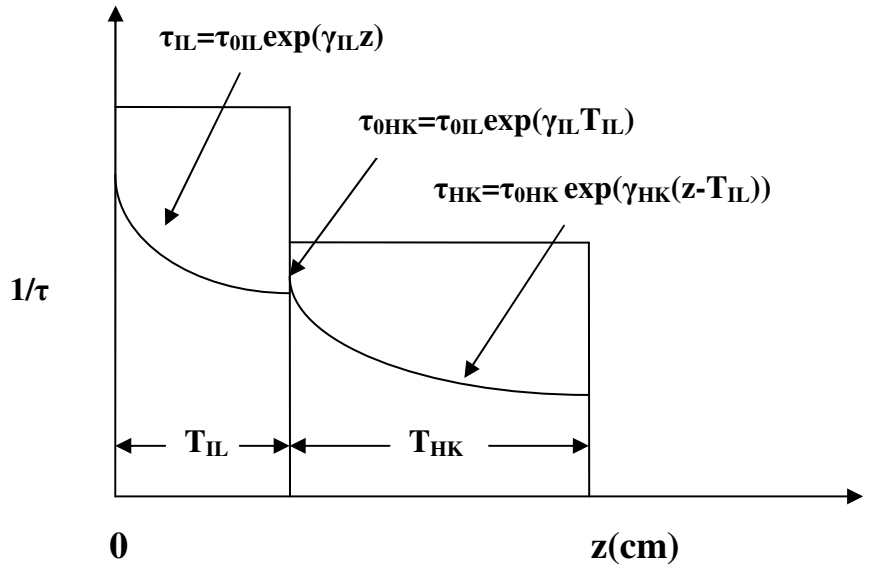


Figure 3.3. Tunneling of carriers through a double step cascaded energy barrier assumed to represent the stacked dielectric structure in the MSUN model.

In this case, quantum mechanical reflection at the step boundary has been neglected since for an IL of 1nm of SiO_2, the ratio of the forward traveling wave magnitude to that of the reflected one can be approximated as $\approx \exp(2\gamma_{IL} T_{IL})$ $\approx \exp(20) >> 1$. The trap density profile for the double layered gate stack along with Si band structure is shown in Figure 3.4. Active trap density profile for interfacial layer and the high-k layer are shown to be dependent on corresponding individual dielectric layer parameters.

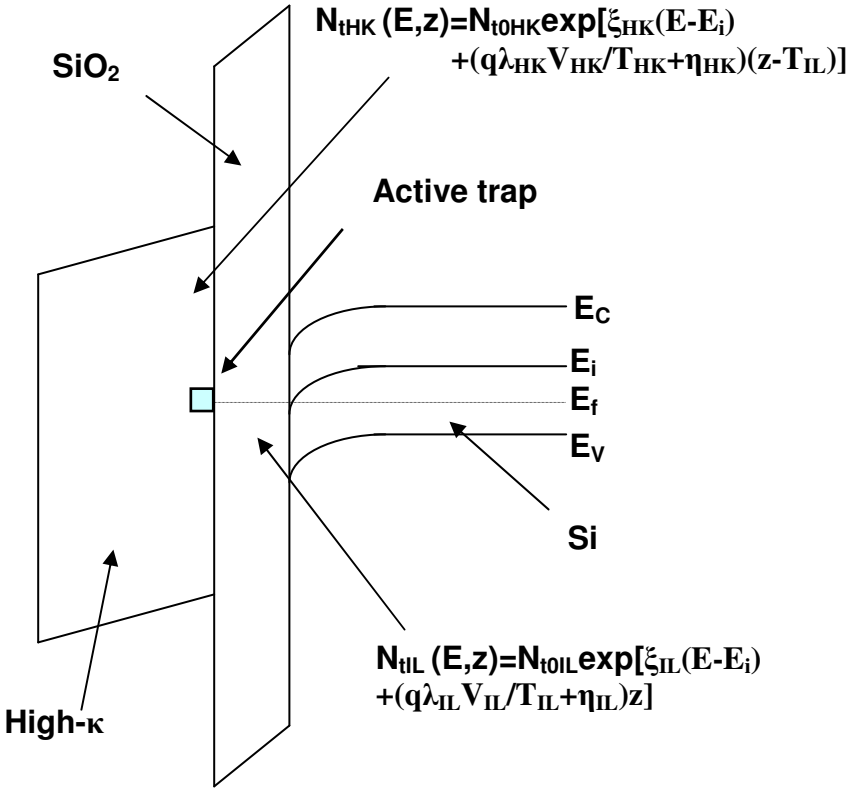


Figure 3.4. The exponential dependence of the trap distribution on the carrier energy and tunneling distance from the interface is shown here for the interfacial layer and the high-k layer.

The power spectral density of mean square fluctuations in trapped electron concentration can be shown as a summation of Lorentzians with weighted tunneling time constantans τ:

$$S_{\Delta N_t} = 4kTW\Delta x\int_0^{T_{IL}} N_{t0IL}\exp\left(\xi_{IL}(E_{fn}-E_i)+q\lambda_{IL}\frac{V_{IL}}{T_{IL}}z+\eta_{IL}z\right)\frac{\tau_{IL}}{1+\omega^2\tau_{IL}^{\,2}}dz$$
$$+4kTW\Delta x\int_{T_{IL}}^{T_{IL}+T_{HK}} N_{t0HK}\exp\left(\xi_{HK}(E_{fn}-E_i)+\left(q\lambda_{HK}\frac{V_{HK}}{T_{HK}}+\eta_{HK}\right)(z-T_{IL})\right)\frac{\tau_{HK}}{1+\omega^2\tau_{HK}^{\,2}}dz \quad (3.22)$$

The physical thicknesses of the IL and the high-κ layer are denoted by $T_{IL}(cm)$ and $T_{HK}(cm)$. The time constant for tunneling into the IL is $\tau_{IL} = \tau_{0IL}\exp(\gamma_{IL} z)$ where $\tau_{0IL}(s)$ is the time constant at the substrate/ IL interface, and $\gamma_{IL}(cm^{-1})$ is the attenuation coefficient in the IL. Similarly for the high-κ layer, $\tau_{HK} = \tau_{0HK}\exp(\gamma_{HK}(z - T_{IL}))$ where $\tau_{0HK} = \tau_{0IL}\exp(\gamma_{IL} T_{IL})$ is the time constant at the IL /high-κ interface and $\gamma_{HK}(cm^{-1})$ is the attenuation coefficient in the high-κ layer. $T_{IL_{eq}}(cm)$, $T_{HK_{eq}}(cm)$ and $T_{eq}(cm)$ are the equivalent oxide thicknesses (EOT) of the IL, the high-κ layer and the total gate stack, respectively. Since, in our case, IL is SiON instead of SiO_2, the EOT is different from the physical thickness. $V_{IL} = (V_g - V_x)T_{IL_{eq}}/T_{eq}$ and $V_{HK} = (V_g - V_x)T_{HK_{eq}}/T_{eq}$ are the potential drop in the IL and the high-κ layer, respectively.

Defining $\beta_{IL} = q\lambda_{IL}/T_{IL}$ and using $\tau_{IL}/\tau_{0IL} = \exp(\gamma_{IL} z)$; we have:

$$\exp(\beta_{IL} V_{IL} + \eta_{IL}) z = (\tau/\tau_{0IL})^{(\beta_{IL} V_{IL} + \eta_{IL})/\gamma_{IL}} \tag{3.23}$$

With a change of variable from z to τ using $d\tau/\tau = \gamma dz$ and following the above procedure for the high-κ part as well, we arrive at:

$$S_{\Delta N_t} = 4kTW\Delta x \left[\begin{array}{l} N_{t0IL}\exp[\xi_{IL}(E_{fn} - E_i)] \int_{\tau_{0IL}}^{\tau_{0IL}\exp(\gamma_{IL}T_{IL})} \left[\frac{\tau_{IL}}{\tau_{0IL}}\right]^{(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}} \frac{\tau_{IL}}{1+\omega^2\tau_{IL}^2} d\tau_{IL} \\ + N_{t0HK}\exp[\xi_{HK}(E_{fn} - E_i)] \int_{\tau_{0IL}\exp(\gamma_{IL}T_{IL})}^{\tau_{0IL}\exp(\gamma_{IL}T_{IL}+\gamma_{HK}T_{HK})} \left[\frac{\tau_{HK}}{\tau_{0HK}}\right]^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}} \frac{\tau_{HK}}{1+\omega^2\tau_{HK}^2} d\tau_{HK} \end{array} \right] \tag{3.24}$$

Here, $\exp(\beta_{HK} V_{HK} + \eta_{HK})(z - T_{IL}) = (\tau/\tau_{0HK})^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}$ and $\beta_{HK} = q\lambda_{HK}/T_{HK}$.

Converting the integration variables as $\omega\tau_{IL} = u_{IL}$ and $\omega\tau_{HK} = u_{HK}$; after simplification we have:

$$S_{\Delta N_t} = 4kTW\Delta x\left[\begin{array}{l}\dfrac{N_{t0IL}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}\tau_{0IL}^{(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}(2\pi f)^{1+(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}}\int_{2\pi f\tau_{0IL}}^{2\pi f\tau_{0IL}\exp(\gamma_{IL}T_{IL})}\dfrac{u_{IL}^{(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}}{1+u_{IL}^{2}}du_{IL} \\ +\dfrac{N_{t0HK}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}\tau_{0HK}^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}(2\pi f)^{1+(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}}\int_{2\pi f\tau_{0HK}}^{2\pi f\tau_{0HK}\exp(\gamma_{HK}T_{HK})}\dfrac{u_{HK}^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}}{1+u_{HK}^{2}}du_{HK}\end{array}\right] \tag{3.25}$$

The complete noise current spectral density expression can be given from Eqs. (3.14) and (3.16) after substitution of $S_{\Delta N_t}$ from Eq. (3.25) as:

$$S_{I_d}(f) = \frac{4kTI_d^{\,2}}{WL^2}\int_0^L\left(\alpha\mu_{eff}+\frac{1}{N(x)}\right)^2\left[\begin{array}{l}\dfrac{N_{t0IL}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}\tau_{0IL}^{(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}(2\pi f)^{1+(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}}\int_{2\pi f\tau_{0IL}}^{2\pi f\tau_{0IL}\exp(\gamma_{IL}T_{IL})}\dfrac{u_{IL}^{(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}}{1+u_{IL}^{2}}du_{IL} \\ +\dfrac{N_{t0HK}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}\tau_{0HK}^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}(2\pi f)^{1+(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}}\int_{2\pi f\tau_{0HK}}^{2\pi f\tau_{0HK}\exp(\gamma_{HK}T_{HK})}\dfrac{u_{HK}^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}}{1+u_{HK}^{2}}du_{HK}\end{array}\right]dx \tag{3.26}$$

where $N(x)\left(cm^{-2}\right)$ is the carrier density at position *x* from the source along the channel given by $N(x) = (1/q)\left[C_{ox}\left(V_g - V_t - V_x\right)\right]$ with $V_t(V)$ being the threshold voltage and $C_{ox}\left(Fcm^{-2}\right)$ the oxide capacitance per unit area.

3.5 Summary

The flicker noise expression for the MSUN Model has been derived. Correlated number and surface mobility fluctuation model has been taken as the physical mechanism responsible for the observed noise behavior. The MSUN Model has been developed in the framework of the original Unified Model based on the same theory. Two important modifications have been implemented in the MSUN model. A flexible

expression has been considered to model the trap densities inside the dielectrics. The active trap density is assumed to have an exponential dependence on band-gap energy and tunneling distance from the dielectric interface. It also includes the effects of band bending on trap density variation. The multi layered nature of the high-k gate stack has been implemented by considering tunneling of carriers through a double step cascaded barrier. The model is geometrically scalable; along with the length and the width of the devices the thickness of individual dielectric layers are kept as user defined parameters. Furthermore, the material properties of each layers such as effective carrier mass, dielectric constant and tunneling constant inside the dielectric are used as user defined parameters as well. Thus, MSUN model is capable of considering MOSFET devices with variable interfacial layer thicknesses and of various material compositions.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

In this chapter, analysis of the experimental data is presented along with comparison to the model predictions. To determine if remote phonon scattering needs to be included in flicker noise formulation for high-k gate dielectric MOSFETs, its effects are investigated on both carrier mobility characteristics and the low frequency noise mechanism, in variable temperature range of 172K to 300K. Next, the dominant flicker noise mechanism responsible for the observed noise behavior is determined from the experimental data following Ghibaudo's [52, 53] work. The newly developed flicker noise model is then used to extract the model parameters corresponding to both the interfacial and the high-k layers from the experimental noise and mobility data. Based on the observations, the role of the interfacial and the high-k layers on the flicker noise of these MOSFETs is explained; the extracted model parameters are presented and an interpretation of the extracted values is provided. The extracted trap density values are compared for devices with various interfacial layer thicknesses over a wide temperature range to verify the applicability of the new model. The actual excursion range of the

Fermi energy levels and the associated energy dependence of the active traps are also illustrated.

4.2 Experiments, results and discussions

4.2.1 The effect of phonon scattering

4.2.1.1 The effect of phonon scattering on mobility degradation

Split CV measurement was done in the temperature range of 172K to 300K to obtain the carrier mobility. Device dimensions were 10 μm x 10 μm in length and width with four different effective oxide thicknesses, as mentioned earlier. With the variation of temperature a linear shift in the threshold voltage was observed for all devices, which results largely from the variation of intrinsic carrier concentration $n_i(cm^{-3})$ with temperature. The shift was also observed to be fairly similar for all wafers, as the slopes of the curves in Figure 4.1 appear to be identical irrespective of the IL thickness.

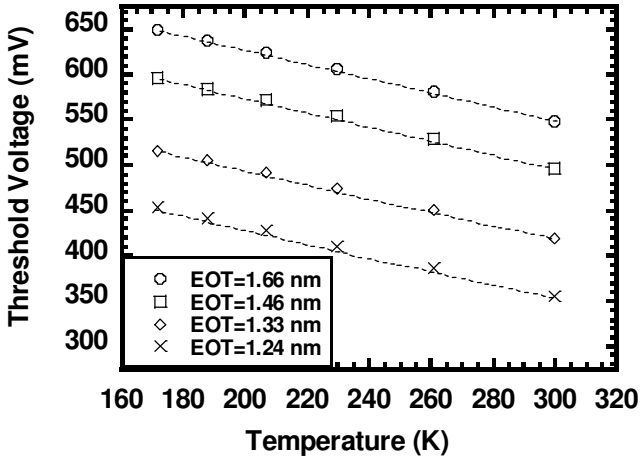


Figure 4.1 Threshold voltage shift with temperature for devices with different IL thickness.

To study the effect of interfacial layer thickness and temperature on the carrier mobility, we plotted mobility as a function of interfacial layer thickness with temperature as a parameter for different inversion charge concentrations (Q_{inv}). As seen in Figure 4.2, the thinner gate oxide devices show lower dependence on temperature, which is more pronounced at a lower inversion charge of $1x10^{-7}$ C/cm^2 compared to that at $9x10^{-7}$ C/cm^2. The difference in the observed temperature dependence can be attributed to the fact that the underlying scattering mechanism responsible for the mobility degradation is different at these two inversion charge concentrations.

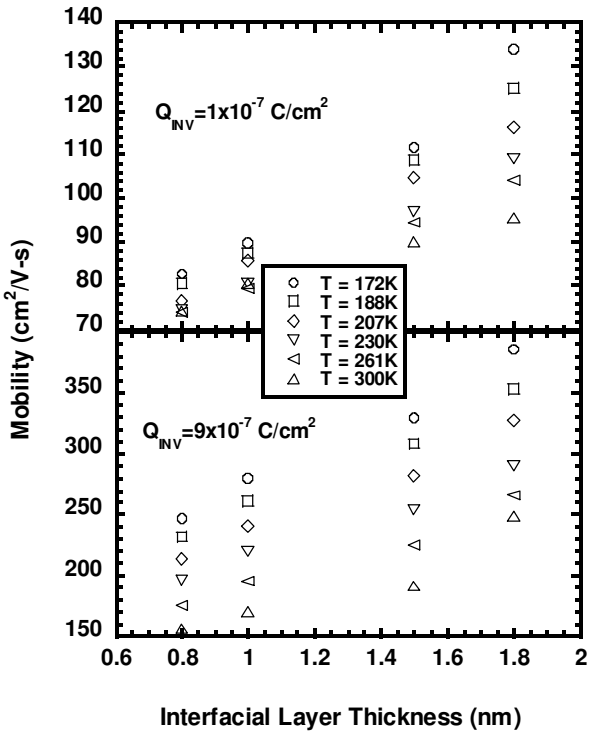


Figure 4.2 Comparison of mobility as a function of IL thickness with temperature as a parameter. The mobility values are calculated at an inversion charge concentration of $1x10^{-7}$ C/cm^2 and $9x10^{-7}$ C/cm^2.

A plot of mobility as a function of inversion charge as shown in Figure 4.3 reveals a linear increase in mobility at lower values of Q_{inv} which is limited primarily by Coulomb scattering. As the inversion charge increases, the Coulomb scattering potential is effectively screened by the increased charge concentration in the channel and the mobility behavior shifts away from this characteristic linear dependence on inversion charge. At high concentrations of inversion charge, mobility values are expected to decrease very sharply (E_{eff}^{-a} with a ~ 2.0-2.6), characterized as mobility limited by surface roughness scattering [57], which we do not see for these devices for the measured inversion charge concentration range. At moderate Q_{inv} where carrier mobility shows neither the linear dependence of Coulomb scattering; nor that of the surface roughness mechanism, where carrier mobility becomes flatter with respect to inversion charge as shown in Figure 4.3, phonon scattering is believed to be the dominant scattering mechanism responsible for the observed mobility behavior [57, 58].

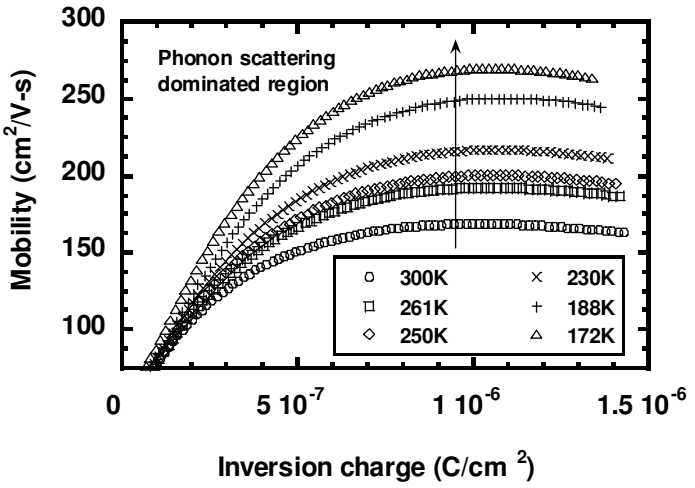


Figure 4.3 Mobility values are shown as a function of inversion charge. Q_{inv}~9x10^{-7} C/cm^2, LxW=10x10μm^2 and EOT=1.33nm.

To investigate what kind of phonon scattering is present in these devices, mobility was plotted as a function of temperature at an inversion charge concentration of $9x10^{-7}$ C/cm^2 where phonon scattering is believed to be the dominant scattering mechanism as discussed. An inverse temperature dependence was observed as shown in Figure 4.4. For the thicker gate oxide devices this dependence was ~T^{-1}, whereas the thinner gate oxide devices showed somewhat lower temperature dependence of T^{-a} (a ~ 0.8 – 0.9). According to the studies of Z. Ren [58] and N. Yasuda [59], this inverse temperature dependence suggests that, the carrier mobility is possibly affected by low energy (in the range of 10 meV – 20 meV) optical phonons as theoretically predicted and experimentally verified in their works, which also agrees with the theoretical predictions of M.V. Fischetti [60]. The lower temperature dependence of the thinner gate oxide devices may be explained by some additional Coulomb scattering component originating from above the thin interfacial layer, as predicted by J. Koga [61] for ultra-thin gate oxide devices with SiO_2 as the gate dielectric. The difference in the temperature dependence of phonons with different energies may also explain this deviation in the observed temperature dependence [59].

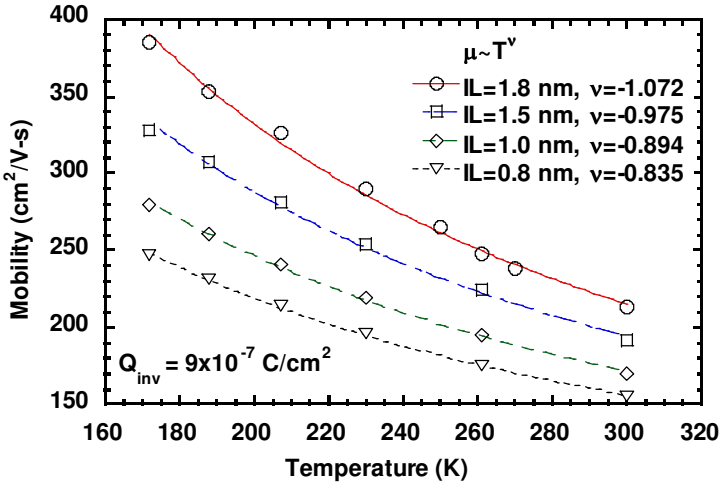


Figure 4.4 Dependence of mobility on temperature, in the phonon scattering dominated Q_{inv} region. As observed, $\mu \alpha T^{-\nu}$ with ν~1.072-0.834.

4.2.1.2. The effect of phonon scattering on 1/f noise

Normalized current noise spectral density measured at 1 Hz was plotted as a function of temperature, to study the effect of phonon scattering on the low frequency noise. Because of the difference in the length of the devices as well as the EOTs, the noise data was normalized with respect to both the drain current ($1/I_d^2$) and gate capacitance (C_{EOT}^2) [3]. As shown in Figure 4.5, the normalized noise curves corresponding to different gate overdrive voltages can easily be recognized which clearly shows the effect of gate voltage on noise data, but none of these curves show any noticeable dependence on temperature.

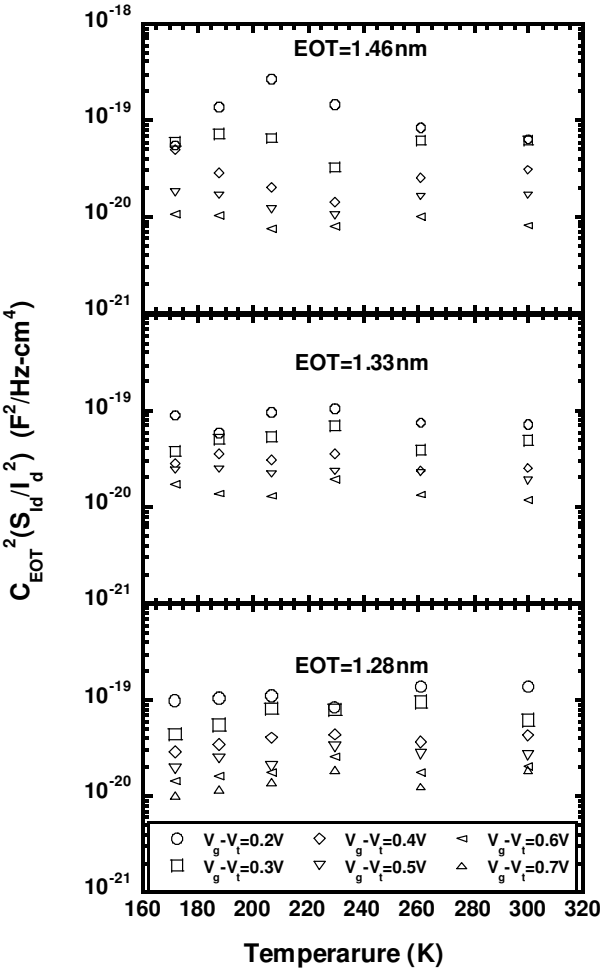


Figure 4.5 Comparison of normalized current noise spectral density $\left(C_{EOT}^2 \left(\frac{S_{I_d}}{I_d^2} \right) \left(F^2 Hz^{-1} cm^{-4} \right) \right)$ at 1 Hz as a function of temperature for devices with different IL thicknesses.

This indicates that, the low frequency noise behavior is not affected by any temperature sensitive processes that might be present in these devices. We conclude that even though phonon scattering has a significant effect on the carrier mobility, it does not

affect the low frequency 1/f noise characteristics of these devices. Upon this verification, the effect of phonon scattering is not included in the MSUN Model.

4.2.2 The dominant noise mechanism

According to the studies of Ghibaudo [52] it can be shown that, if the low frequency noise in the devices follows correlated number and mobility fluctuations theory, $\frac{S_{I_d}}{I_d^2}$ shows a dependence on $\left(\frac{g_m}{I_d}\right)^2$ following the relation:

$$\frac{S_{Id}}{I_d{}^2} = \left(1 + \frac{\alpha \mu_{eff} C_{ox} I_d}{g_m}\right)^2 \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} \tag{4.1}$$

Whereas if the dominant mechanism follows Hooge's bulk mobility fluctuations model, $\frac{S_{I_d}}{I_d^2}$ shows a dependence on $\frac{1}{I_d}$ following the relation:

$$\frac{S_{Id}}{I_d{}^2} = q^2 \alpha_H \langle \mu_{eff} \rangle \frac{V_d}{fL^2 I_d} \tag{4.2}$$

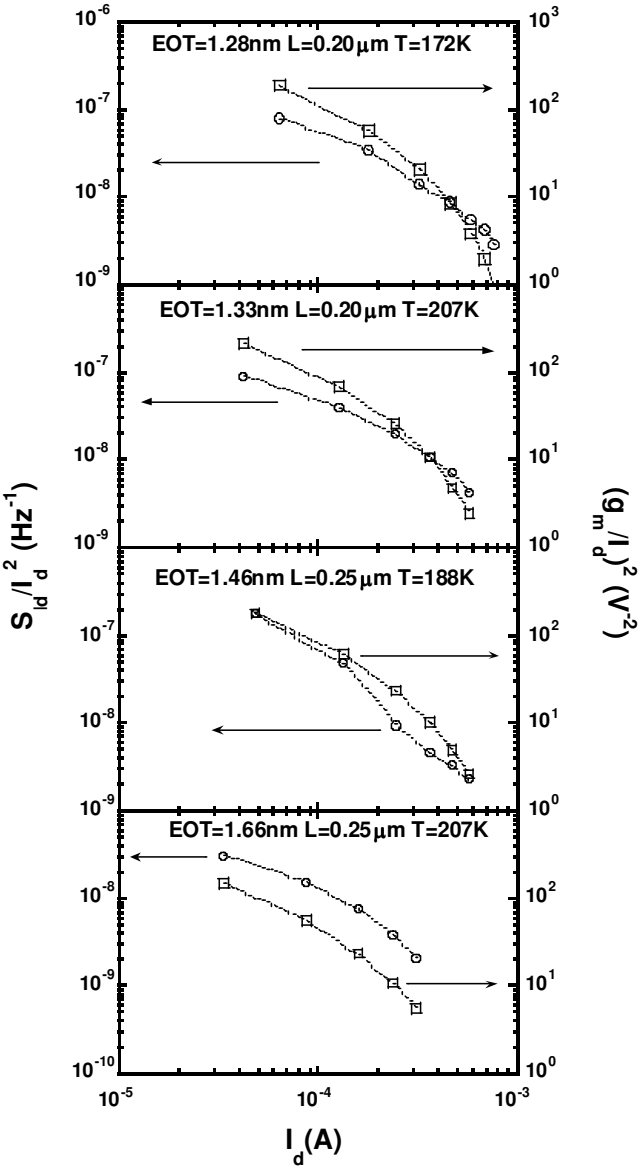


Figure 4.6 $\frac{S_{I_d}}{I_d^2}$ shows dependence on $\left(\frac{g_m}{I_d}\right)^2$ at all temperatures for devices with all four different IL thicknesses at frequency of 1 Hz.

As shown in Figure 4.6, for devices with different effective oxide thicknesses over the experimental temperature range, $\frac{S_{I_d}}{I_d^2}$ follows $\left(\frac{g_m}{I_d}\right)^2$, which experimentally

validates the correlated number and mobility fluctuations as the dominant mechanism responsible for the observed noise behavior. Upon this verification the Multi Stack Unified Noise Model has been based on the correlated number and mobility fluctuations theory.

4.2.3 The model parameters

Two important modifications have been made in the MSUN Model in order to incorporate the fundamental differences in the gate stack compared to that in conventional devices as modeled in the original Unified Model. As discussed earlier, tunneling through a double step barrier is considered instead of a single barrier, which incorporates the noise contribution of the high-κ layer along with that of the IL in the total noise expression, along with the single valued dielectric trap density being replaced with a comprehensive expression for both the oxide layers. The final expression of MSUN Model appears in Eq. (3.19) and the parameters extracted from the fitting to the experimental data using this expression are listed in Table 4.1.

Table 4.1: The list of extraction parameters used in the MSUN Model

High-k dielectric layer parameters		**Interfacial layer parameters**	
N_{t0HK}	**Mid-gap trap density at the IL-high-k interface**	N_{t0IL}	**Mid-gap trap density at the substrate-IL interface**
μ_{c0}	**Noise fitting parameter**	μ_{c0}	**Noise fitting parameter**
ξ_{HK}	**Band bending parameter at the interface corresponding to the high-k layer**	ξ_{IL}	**Band bending parameter at the interface corresponding to the IL**
η_{HK}	**Spatial trap distribution parameter for the high-k layer**	η_{IL}	**Spatial trap distribution parameter for the IL**
λ_{HK}	**Band bending parameter inside the high-k dielectric layer**	λ_{IL}	**Band bending parameter inside the IL**

4.2.3.1 The effective number of parameters

If we choose the IL trap density in the range of the published experimental values [15] (N_{t0IL} ~ 10^{16} $cm^{-3}eV^{-1}$), for the range of IL thicknesses used in this experiment (0.8nm to 1.8nm), the noise contribution from IL falls more than 2 orders of magnitude below the total noise exhibited by the devices in 1-100 Hz frequency range. For the thickest EOT device, a special phenomenon was observed. Traps further away from the semiconductor interface contribute noise to the lower end of the frequency spectrum, while traps at the interface are fast-states and contribute fluctuations to the higher frequencies. Consequently, as the IL gets thicker, the noise contribution from the high-κ layer increasingly shifts to the lower frequency range and at the same time higher frequency components get weaker since the noise contribution from the IL is relatively low. The summation of Lorentzians with weighted tunneling time constants [62] in Eq. (9) results in an interesting noise power spectral form for thick interfacial layers. S_{I_d} rolls off as $f^{-\delta}$ with $\delta = 0$ for $f < f_{c1}$, $\delta \approx 1$ for $f_{c1} < f < f_{c2}$ and $\delta \approx 2$ for $f > f_{c2}$, where, $f_{c2} = 1/(2\pi\tau_{0HK})$, and $f_{c1} = 1/(2\pi\tau_{0HK}\exp(\gamma_{HK}T_{HK}))$. The time constant at the high-κ interface is $\tau_{0HK} = \tau_{0IL}\exp(\gamma_{IL}T_{IL})$ while that at $z = T_{IL} + T_{HK}$ *is* given by $\tau_{HK} = \tau_{0HK}\exp(\gamma_{HK}T_{HK})$. For the devices with thinner interfacial layers (T_{IL} = 0.8nm, 1.0nm and 1.5nm) the characteristic corner frequencies were calculated as f_{c1} < 1Hz and f_{c2} > 100 Hz, as a result the noise contribution from the high-κ layer dominates in the range of $1Hz < f < 100Hz$. With γ_{IL}=0.982x10^8 cm^{-1} and γ_{HK}=0.538x10^8 cm^{-1}; for the devices with the thickest EOT (T_{IL} = 1.8nm) we have $\tau_{0HK} = \tau_{0IL}\exp(\gamma_{IL}T_{IL}) = 4.749\text{x}10^{-}$

^{3} s, which yields $f_{c2} = 1/(2\pi\tau_{0HK}) \approx 33.51\text{Hz}$ and $f_{c1} = 1/(2\pi\tau_{0HK}\exp(\gamma_{HK}T_{HK})) \approx 3.279\text{x}10^{-6}$ Hz. Therefore, in the frequency range of our interest (1Hz – 100Hz), even though the noise contribution in the lower frequencies comes from the high-κ layer, noise beyond f_{c2}=33.51Hz is contributed from the IL, which can result in from a higher trap density (N_{t0IL}) or a higher value of λ (and ξ) inside the IL near the high-κ/ IL interface compared to the bulk of the IL. The resulting spectrum is shown in Figure 4.7, which reveals the noise contribution from the IL does not affect the total noise significantly at lower frequencies (~1 Hz). As 1.8nm of IL is of little practical interest, this result may not be as significant from the application point of view.

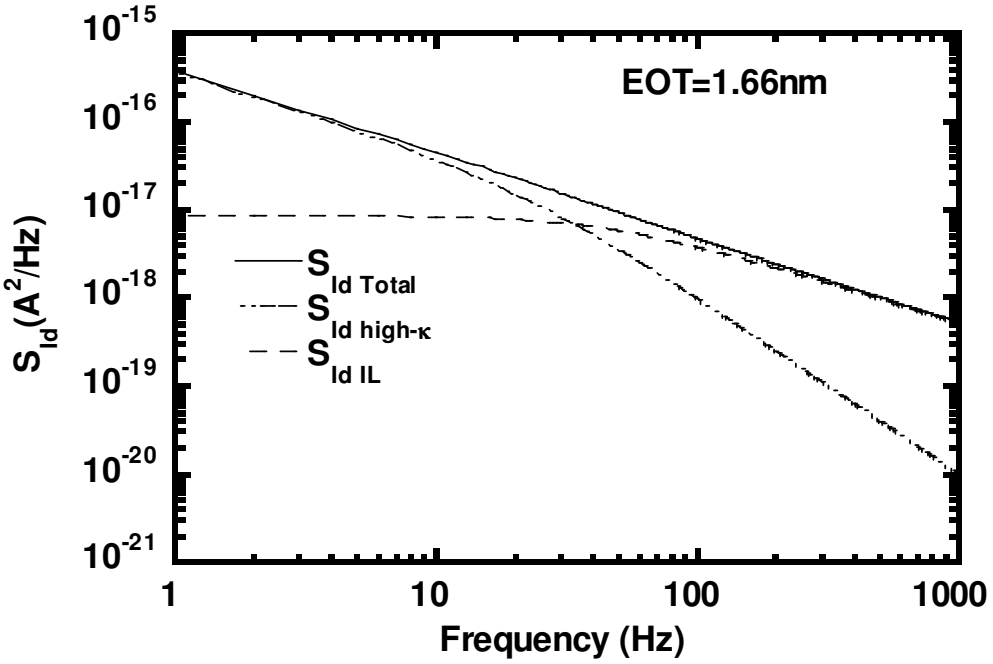


Figure 4.7 Contributions from the interfacial layer and the high-κ layer in the total S_{I_d} (A^2/Hz) for devices with T_{IL}=1.8nm.

To summarize, the IL parameters effectively do not play any role in the fitting to the experimental data. Furthermore, as the energy dependence parameters λ and ξ are set equal as described above, the number of effective fitting parameters reduce to 4.

4.2.3.2 Extraction of model parameters

The fitting parameters corresponding to the energy dependence (λ and ξ) and the spatial distribution of traps into the oxide layer (η) are extracted from the plot of frequency exponent (δ) as a function of gate voltage V_g at all temperatures for individual devices. As shown in the final form of the current noise spectral density S_{I_d} in (3.19), the frequency exponent δ can be shown as $\left[1+\left(\beta_{HK}V_{HK}+\eta_{HK}\right)/\gamma_{HK}\right]$, where $V_{HK}(V)=\left(V_g-V_x\right)T_{HK\,eq}/T_{eq}$ and $\beta_{HK}=q\,\lambda_{HK}/T_{HK}$. A linear fit of the frequency exponent, as depicted in Figure 4.8, can be shown as $\delta = aV_g + b\,\delta$. Evaluating the above equations λ, ξ and η can be extracted for individual devices, for the whole temperature range of 172K to 300K. As the noise is dominantly coming from the high-k layer, these parameters are assumed to represent the high-k layer. The extracted values of λ_{HK}, ξ_{HK} and η_{HK} are shown in Table 4.2.

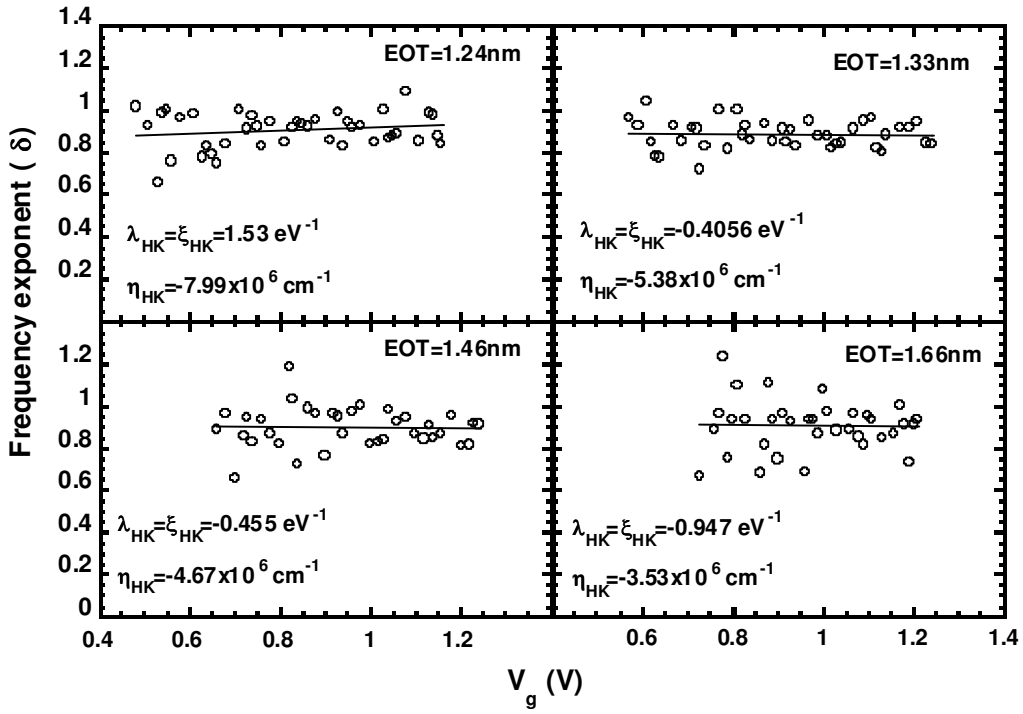


Figure 4.8 The experimental values of frequency exponent δ is plotted as a function of gate voltage for T = 172K - 300K. Linear fitting to the data is obtained for all four wafers. Using these fitting coefficients λ_{HK}, ξ_{HK} and η_{HK} parameters were calculated.

Once these values of λ_{HK}, ξ_{HK} and η_{HK} are determined, they are passed to the MSUN Model program and the noise current spectral density S_{I_d} at 1 Hz is calculated to find the best fit to the experimental data by freely varying N_{t0} and μ_{c0} parameters. For each temperature, average values of N_{t0} and μ_{c0} were determined by fitting the calculated S_{I_d} to the experimental data over the whole bias range using least square error (LSE) method. The average N_{t0} and μ_{c0} were used to calculate the current noise spectrum for each individual bias point from the MSUN Model program. Calculated

current noise spectral density was fitted to the experimental data as shown in Figure 4.9. Good agreement was observed over the temperature range of 172K to 300K for devices with different IL thicknesses.

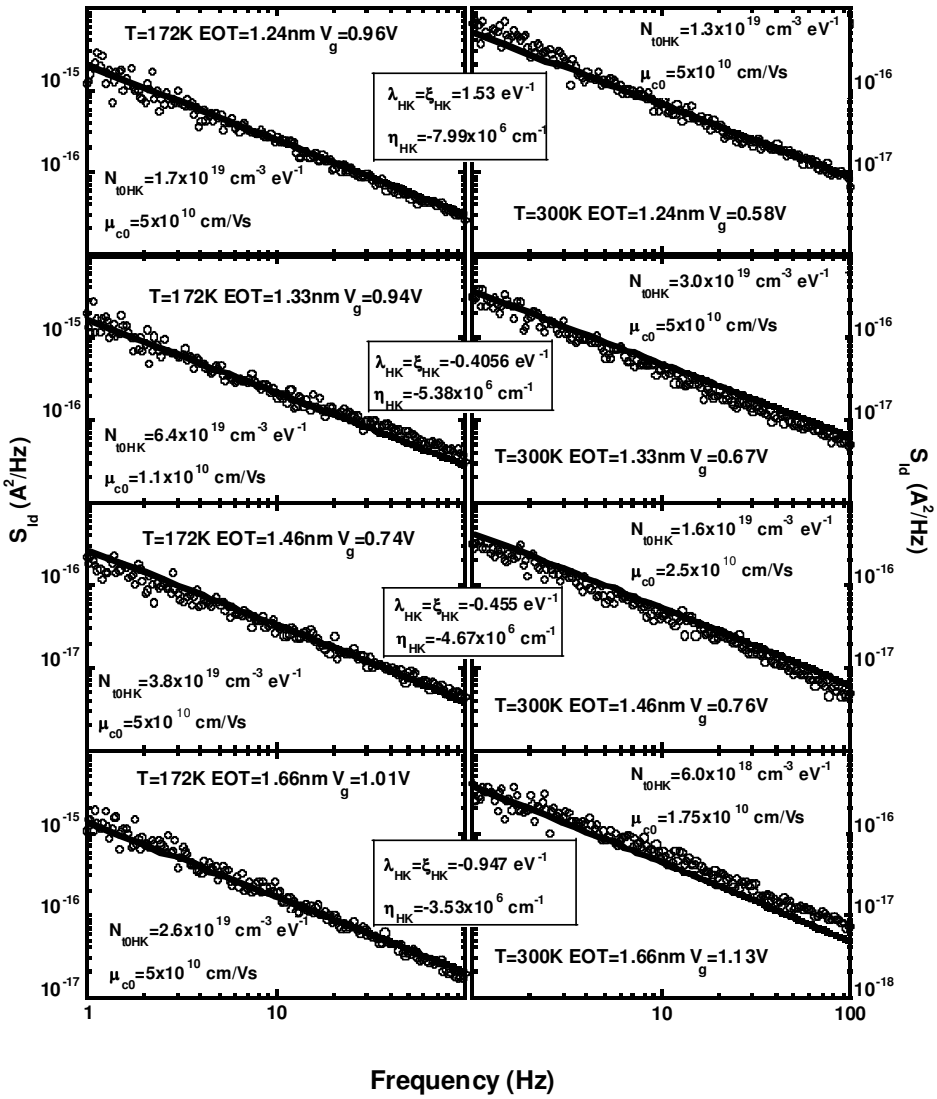


Figure 4.9 Comparison of current noise spectrum S_{I_d} calculated with MSUN Model to that obtained by experiment, shown at T=172K and T=300K. LxW=0.20x10μm^2. λ_{HK}, ξ_{HK} and η_{HK} values are the same for all temperatures for individual devices and correspond to the high-κ layer.

To investigate the bias dependence of the MSUN Model, the calculated S_{I_d} at 1 Hz was compared to the experimental values over the bias range of weak to strong inversion at all temperatures. Very good agreement between theory and experiment was observed over the entire experimental temperature range for different IL thicknesses, as shown in Figure 4.10.

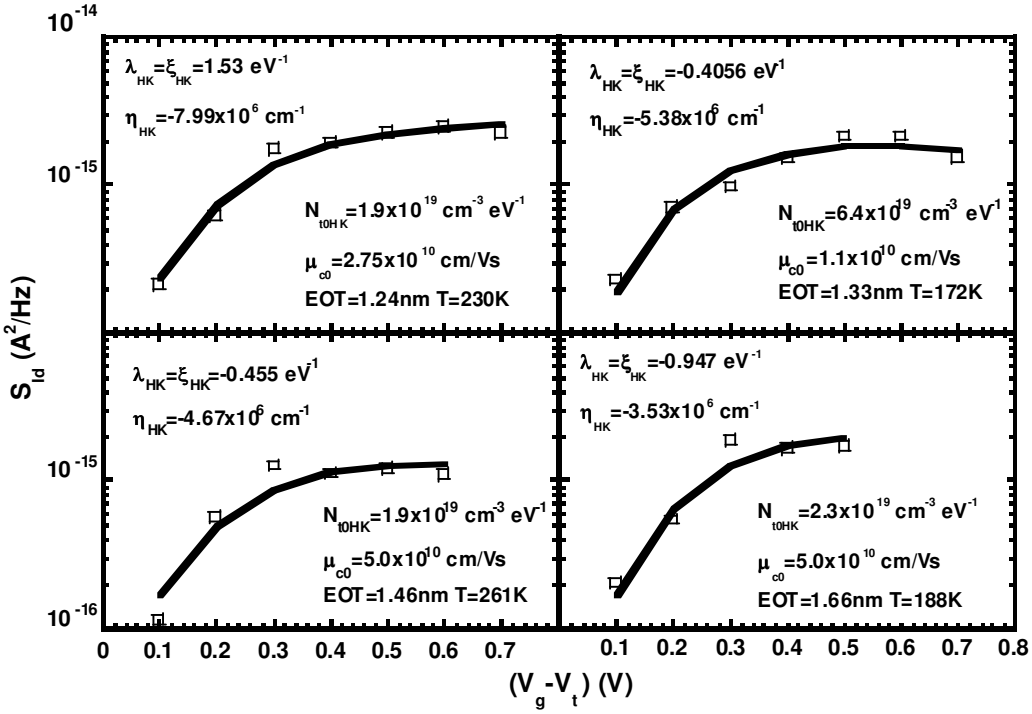


Figure 4.10 The current noise spectral density S_{I_d} (A^2/Hz) calculated at 1 Hz using MSUN Model is compared to experimental data. EOT = 1.28nm, 1.33nm, 1.46nm and 1.66nm from weak to strong inversion regions.

4.2.3.3 Extracted model parameters

The extracted parameters using the MSUN model are presented in Table 4.2 on devices with four different interfacial layer thicknesses in the temperature range of 172K

to 300K. Extracted N_{t0HK} values for different wafers show good agreement within experimental error limits, no noticeable dependence on IL thickness or temperature was observed as graphically depicted in Figure 4.11. Extracted μ_{c0} values lie in the range of $1x10^{10}$ cm/Vs to $5x10^{10}$ cm/Vs. In this range, the contribution from the mobility fluctuations are observed to be about 2 orders of magnitude lower than that from the number fluctuations component. Similar to extracted trap density values, the mobility fluctuation coefficient μ_{c0} shows consistency over the experimental temperature range irrespective of the IL thickness.

Table 4.2: The extracted parameters using the MSUN Model

EOT=1.28nm, $\lambda_{HK}=\xi_{HK}=1.53eV^{-1}$, $\eta_{HK}=-7.99x10^{-6}\,cm^{-1}$		
T(K)	**$N_{t0HK}(cm^{-3}\,eV^{-1})$**	**μ_{c0}(cm/Vs)**
172	**$1.7x10^{19}$**	**$5.0x10^{10}$**
188	**$1.8x10^{19}$**	**$5.0x10^{10}$**
207	**$1.7x10^{19}$**	**$3.0x10^{10}$**
230	**$1.9x10^{19}$**	**$2.75x10^{10}$**
261	**$1.4x10^{19}$**	**$5.0x10^{10}$**
300	**$1.3x10^{19}$**	**$5.0x10^{10}$**

EOT=1.33nm, $\lambda_{HK}=\xi_{HK}=-0.41eV^{-1}$, $\eta_{HK}=-5.38x10^{-6}\,cm^{-1}$		
T(K)	**N_{t0HK} ($cm^{-3}\,eV^{-1}$)**	**μ_{c0}(cm/Vs)**
172	**$6.4x10^{19}$**	**$1.1x10^{10}$**
188	**$5.8x10^{19}$**	**$1.25x10^{10}$**
207	**$5.6x10^{19}$**	**$4.5x10^{10}$**
230	**$5.9x10^{19}$**	**$3.5x10^{10}$**
261	**$3.7x10^{19}$**	**$4.0x10^{10}$**
300	**$3.0x10^{19}$**	**$4.0x10^{10}$**

EOT=1.46nm, $\lambda_{HK}=\xi_{HK}=-0.45eV^{-1}$, $\eta_{HK}=-4.67x10^{-6}\,cm^{-1}$		
T(K)	**$N_{t0HK}(cm^{-3}\,eV^{-1})$**	**μ_{c0}(cm/Vs)**
172	**$3.8x10^{19}$**	**$5.0x10^{10}$**
188	**$3.1x10^{19}$**	**$5.0x10^{10}$**
207	**$2.4x10^{19}$**	**$5.0x10^{10}$**
230	**$1.5x10^{19}$**	**$2.25x10^{10}$**
261	**$1.9x10^{19}$**	**$5.0x10^{10}$**
300	**$1.6x10^{19}$**	**$2.5x10^{10}$**

EOT=1.66nm, $\lambda_{HK}=\xi_{HK}=-0.95eV^{-1}$, $\eta_{HK}=-3.53x10^{-6}\,cm^{-1}$		
T(K)	**N_{t0HK} ($cm^{-3}\,eV^{-1}$)**	**μ_{c0}(cm/Vs)**
172	**$2.6x10^{19}$**	**$5.0x10^{10}$**
188	**$2.3x10^{19}$**	**$5.0x10^{10}$**
207	**$1.4x10^{19}$**	**$7.5x10^{10}$**
230	**$1.6x10^{19}$**	**$5.0x10^{10}$**
250	**$1.6x10^{19}$**	**$5.0x10^{10}$**
270	**$9.0x10^{18}$**	**$3.0x10^{10}$**
300	**$6.0x10^{18}$**	**$1.75x10^{10}$**

The extracted spatial trap distribution parameter η_{HK} showed negative values for all four wafers, which means as the carriers tunnel deeper into the high-κ layer, they experience a decrease in the effective trap density. The extracted values were close to each other and were comparable to the tunneling coefficient (γ) for high-κ materials.

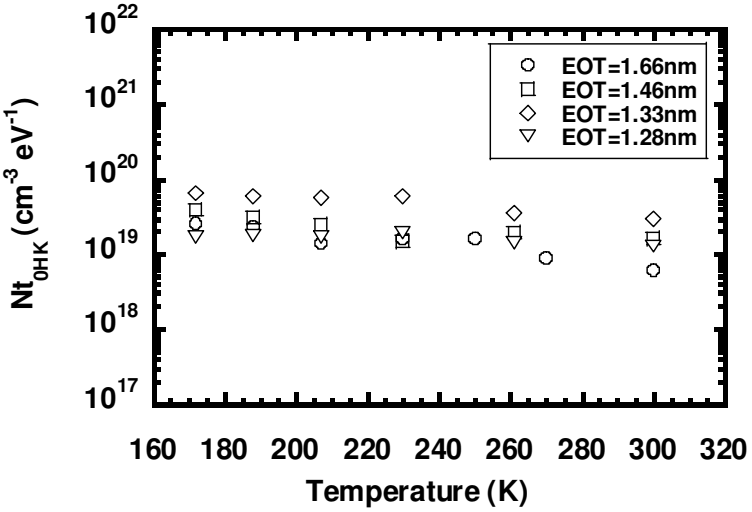


Figure 4.11 Extracted values of N_{t0HK} are plotted as a function of temperature for devices with different IL thicknesses.

The values of the energy dependence parameters λ_{HK} and ξ_{HK} are set equal, as the distribution in the trap density affected by band bending in the oxide is induced by the same energy dependence as due to the band bending at the interface. Both positive and negative values are observed, which means that with increase in the quasi Fermi level, the carriers experience both increase and decrease in effective trap density, which varies from device to device. The effect of the variation in the extracted values of energy

dependence parameters on the active trap density as probed by the Quasi Fermi level is more closely investigated in Figure 4.12.

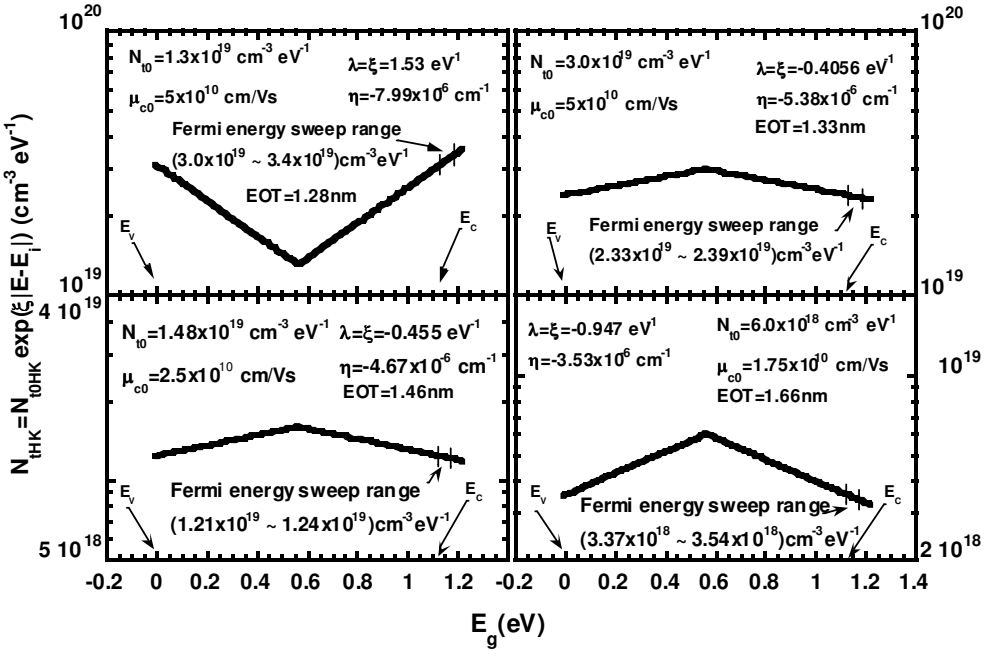


Figure 4.12 The extracted HfSiON trap distribution using the MSUN Model and the experimental data obtained for each IL thickness. Also imposed on each figure are the active trap levels probed by Quasi Fermi level.

The highlighted part of the solid line shows the actual excursion of the quasi Fermi level along the Si energy band. The range of active trap density values corresponding to this region is also shown on the figure. As it reveals, irrespective of the sign of the extracted energy dependence parameters, the active trap density values for different IL thicknesses were reasonably close. The trap distribution represented by the curve outside this region may not be an accurate reflection of the actual trap profile in the dielectric, as the experimental data corresponds to only the high lighted part of the

curve. At 300K, the active trap density was observed to show an inverse dependence on IL thickness, with the thinnest IL devices showing highest trap density.

4.2.4 Compact form of MSUN Model

The MSUN Model expressions were transformed into compact forms, so that the model could be incorporated in available device simulation packages used in the industry without increasing the computation time. Two leading device simulators have been considered for the incorporation of the MSUN Model. The BSIM Model [63] is well known as it has dominated the semiconductor industry over the decade. The surface potential based PSP Model [64], which is based on a more complex formulation, nevertheless facilitates smoother transitions between different MOSFET operating regions. Thus, for any kind of analysis which requires a derivative of the current with respect to the gate voltage, this model has become a better choice.

4.2.4.1 Compact form for the BSIM Model

The noise density according to the BSIM4.6.1 is given by the following expressions for the sub-threshold to strong inversion regions with usual notations [63].

$$S_{id,inv}(f) = \frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{oxe}\left(L_{eff} - 2.LINTNOI\right)^2 A_{bulk} f^{ef}.10^{10}}\left(NOIA.\log\left(\frac{N_0 + N^*}{N_l + N^*}\right) + NOIB\left(N_0 - N_l\right) + NOIC\left(N_0^2 - N_l^2\right)\right)$$

$$+ \frac{k_B TI_{ds}^2 \Delta L_{clm}}{W_{eff}\left(L_{eff} - 2.LINTNOI\right)^2 f^{ef}.10^{10}}\left(\frac{NOIA + NOIB.N_l + NOIC.N_l^2}{\left(N_l + N^*\right)^2}\right) \quad (4.3)$$

$$S_{id,subVt}(f) = \frac{k_B TI_{ds}^2 NOIA}{W_{eff} L_{eff} f^{ef}.10^{10}} \quad (4.4) \qquad S_{id}(f) = \frac{S_{id,inv}(f) x S_{id,subvt}(f)}{S_{id,subvt}(f) + S_{id,inv}(f)} \quad (4.5)$$

Here,

A_{bulk} = Parameter representing bulk charge effect considering effective length, width and applied bias

NOIA = Noise parameter A

NOIB = Noise parameter B

NOIC = Noise parameter C

N_0 = Charge density at source

N_l = Charge density at drain

$N^* = k_B T\left(C_{oxe} + C_D + C_{IT}\right)/q^2$

LINTNOI = Length reduction parameter offset

ΔL_{CLM} = Reduction due to channel length modulation

In terms of MSUN notations, *NOIA, NOIB* and *NOIC* in BSIM4 need to be expressed in the following way:

$$NOIA/(4x10^{10}f^{ef}) = (MSUN\_const\_IL + MSUN\_const\_HK)xA \tag{4.6}$$

$$NOIB/(4x10^{10}f^{ef}) = (MSUN\_const\_IL + MSUN\_const\_HK)xB \tag{4.7}$$

$$NOIC/(4x10^{10}f^{ef}) = (MSUN\_const\_IL + MSUN\_const\_HK)xC \tag{4.8}$$

where,

$$MSUN\_const\_IL = \frac{N_{t0IL}\exp\left[\xi_{HK}\left(E_F - E_i\right)\right]}{\gamma_{IL}\tau_{0IL}^{\frac{\beta'_{IL}}{\gamma_{IL}}}\left(2\pi f\right)^{1+\frac{\beta'_{IL}}{\gamma_{IL}}}}\int_{2\pi f\tau_{0IL}}^{2\pi f\tau_{0IL}\exp(\gamma_{IL}T_{IL})}\frac{u^{\frac{\beta'_{IL}}{\gamma_{IL}}}}{1+u^2}du \tag{4.9}$$

$$MSUN\_const\_HK = \frac{N_{t0HK}\exp\left[\xi_{HK}\left(E_F - E_i\right)\right]}{\gamma_{HK}\tau_{0HK}^{\frac{\beta'_{HK}}{\gamma_{HK}}}\left(2\pi f\right)^{1+\frac{\beta'_{HK}}{\gamma_{HK}}}}\int_{2\pi f\tau_{0HK}}^{2\pi f\tau_{0HK}\exp(\gamma_{HK}T_{HK})}\frac{u^{\frac{\beta'_{HK}}{\gamma_{HK}}}}{1+u^2}du \tag{4.10}$$

$A=1$, $B^2=4C$, $C=(\alpha\mu_{eff}R^{-1})^2$ and $R=-N/(N+N^*)$. $\beta'_{IL}=(q\lambda_{IL}V_{IL}/T_{IL})+\eta_{IL}$ and $\beta'_{HK}=(q\lambda_{HK}V_{HK}/T_{HK})+\eta_{HK}$.

4.2.4.2 Compact form for the PSP Model

In accordance with the surface potential based model, the noise expression in terms of PSP Model [64] parameters with usual notations can be expressed as:

$$S_{I_d1}(f)=\frac{2q^2\phi_t^2 I_d Y_1 \beta N_{t0HK}\left[\exp\left[\xi'_{HK}(\psi_m-\phi_f)\right]\right]}{\pi C_{ox}WLfN^*G_{vsat}}\left[(A-N^{*B}+N^{*2}C)\ln\left(\frac{N_m^*+\Delta N/2}{N_m^*-\Delta N/2}\right)+\Delta N\left(B+C\left(N_m^*-2N^*\right)\right)\right]$$
$$+\frac{2kTI_d^2 Y_1 N_{t0HK}\left[\exp\left[\xi'_{HK}(\psi_{sat}-\phi_f)\right]\right]}{\pi WLf}(1-G_{\Delta L})\left[\frac{A+B\left(N_m^*-\Delta N/2\right)+C\left(N_m^*-\Delta N/2\right)^2}{\left(N_m^*-\Delta N/2\right)^2}\right] \tag{4.11}$$

$$S_{I_d2}(f)=\frac{2q^2\phi_t^2 I_d Y_2 \beta N_{t0IL}\left[\exp\left[\xi'_{IL}(\psi_m-\phi_f)\right]\right]}{\pi C_{ox}WLfN^*G_{vsat}}\left[(A-N^{*B}+N^{*2}C)\ln\left(\frac{N_m^*+\Delta N/2}{N_m^*-\Delta N/2}\right)+\Delta N\left(B+C\left(N_m^*-2N^*\right)\right)\right]$$
$$+\frac{2kTI_d^2 Y_2 N_{t0IL}\left[\exp\left[\xi'_{IL}(\psi_{sat}-\phi_f)\right]\right]}{\pi WLf}(1-G_{\Delta L})\left[\frac{A+B\left(N_m^*-\Delta N/2\right)+C\left(N_m^*-\Delta N/2\right)^2}{\left(N_m^*-\Delta N/2\right)^2}\right] \tag{4.12}$$

Total noise spectrum $S_{I_d}(f)=S_{I_d1}(f)+S_{I_d2}(f)$ (4.13)

where,

$\phi_t=k_BT/q$

ψ_m = Mid value of the surface potential

ϕ_f = Fermi potential

G_{vsat} = Parameter representing effect of channel length modulation and velocity saturation

β = Parameter representing zero field mobility, channel aspect ratio, oxide capacitance and operating temperature

$$N^* = \frac{C_{ox}}{q}\alpha_m\phi_t$$

α_m = Linearization coefficient

$$\Delta N = \frac{C_{ox}}{q}\alpha_m\Delta\psi$$

$\Delta\psi$ = Surface potential difference between drain and source terminal

$$N_m^* = \frac{C_{ox}}{q}q_{im}^*$$

q_{im}^* = Mid-point inversion charge, considering body effect and poly depletion effect at operational temperature

ψ_{sat} = Channel potential where gradual channel approximation breaks down

$G_{\Delta L}$ = Parameter representing the channel length modulation effect

$$Y_1 = \frac{1}{\gamma_{HK}\left(2\pi f\tau_{0HK}\right)^{\beta_{HK}'/\gamma_{HK}}}\int_{2\pi f\tau_{0HK}}^{2\pi f\tau_{0HK}\exp(\gamma_{HK}T_{HK})}\frac{u^{\beta_{HK}'/\gamma_{HK}}}{1+u^2}du$$

$$Y_2 = \frac{1}{\gamma_{IL}\left(2\pi f\tau_{0IL}\right)^{\beta_{IL}'/\gamma_{IL}}}\int_{2\pi f\tau_{0IL}}^{2\pi f\tau_{0IL}\exp(\gamma_{IL}T_{IL})}\frac{u^{\beta_{IL}'/\gamma_{IL}}}{1+u^2}du$$

$A=1$, $B^2=4.C$, $C=(\alpha\mu_{eff}R^{-1})^2$, $R=-N/(N+N^*)$ and $\xi_{HK}' = q\xi_{HK}$.

The compact form of the MSUN Model for BSIM and PSP Model can found in the cited reference [65]. The compact form of the integrals corresponding to the dielectric layers is discussed in the next section.

4.2.5 Compact form of the integrals into the dielectric

To make the theoretically verified model compatible with industry standard simulation packages, the integrals into the dielectric layers as appearing in Eq. 3.25, need to be expressed in compact form. As the interfacial layer has 5 different parameters affecting the integral with the high-k layer having 7, preserving the accuracy of the compact form over the considered range of the integral limits (10^{-6} to 10^{21}) becomes quite challenging. In the compact form, the interfacial layer thickness was considered in the range of 0.7nm (where SiO_2 approaches its atomic dimensions) to 1.8nm (beyond this limit use of high-k is not necessary). The high-k layer was considered with more flexible choice of materials and physical thicknesses. The range of high-k thickness was considered in the range of 0.8 nm to 5nm with tunneling coefficients in the range of $0.2\text{x}10^{-8}$ cm^{-1} to $1\text{x}10^{-8}$ cm^{-1}. The frequency exponent δ (the frequency exponent in $1/f^{\delta}$ spectral form) was considered in the range of 0.7 to 1.3.

To preserve the accuracy of the integral, the curve representing the integral as a function of ($2\pi f\tau$) was divided into 6 different parts, with δ' as the parameter, where $\delta' = \delta - 1$. The best matching compact closed form expressions were obtained for each region by comparing the standard error with the actual integral for 30 predefined closed form expressions.

The derivation of the compact form of the integral is explained in detail in Appendix B. The comparison between the actual integral and the compact form is shown in Figure 4.13. The calculated error is shown in Figure 4.14.

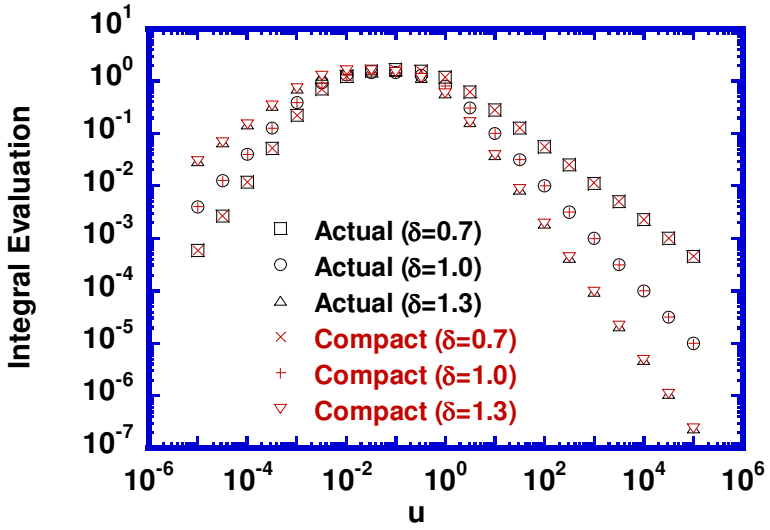


Figure 4.13 Comparison between the actual integral and the values obtained using the compact form. Very good agreement was achieved.

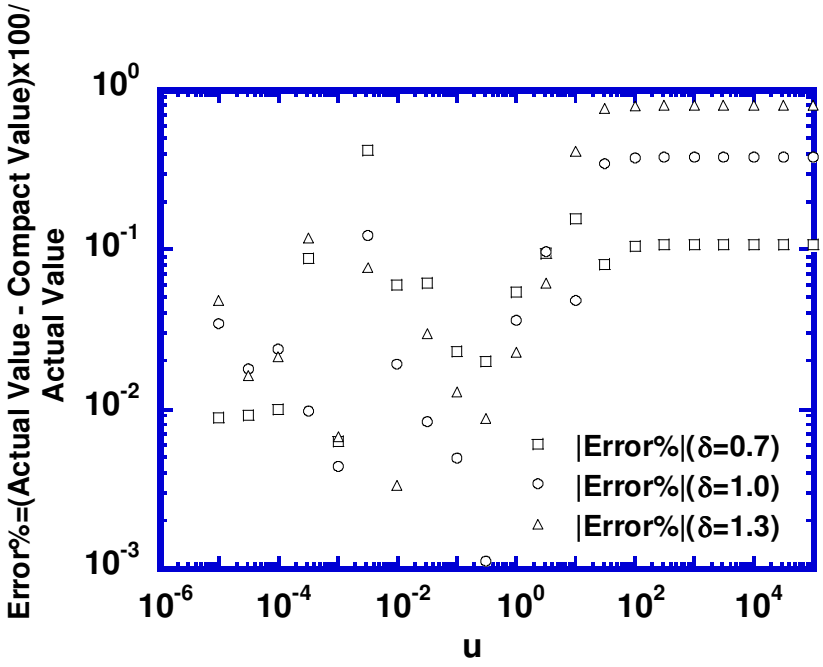


Figure 4.14 The error between the actual integral and the compact form is shown for 3 different values of frequency exponent δ. In all cases the error was below 1%.

4.3. Summary

The quantitative predictions of the newly developed MSUN Model are experimentally verified. The variable temperature mobility data revealed significant impact of remote optical phonon scattering on the carrier mobility in high-k MOSFETs. The noise data was not affected by any temperature sensitive processes. This observation confirmed that no additional noise mechanism arising from the remote phonon scattering is present in these devices. Consequently, the impact of remote phonon scattering was not separately included in the MSUN Model. The correlated number and mobility fluctuation model was experimentally verified as the dominant noise mechanism responsible for the observed noise characteristics. Therefore, the MSUN model was developed in the framework of the Unified Model.

Two distinct high-k features were implemented in the MSUN Model; the stacked nature of the dielectric and a more realistic flexible trap density profile dependent on both the tunneling distance and energy of the carriers. The tunneling of carriers through multiple dielectric layers successfully explained the observed interfacial layer dependence of noise data using Unified Model. The observed differences in the extracted trap density values for the same materials are also explained by the energy and spatial dependence of trap distribution, as the extracted values of mid-gap trap densities did not show significant variation with respect to interfacial layer thickness or temperature.

The observed consistency in the extracted N_{t0HK} suggests that the IL dependence of the trap profile is properly incorporated in the MSUN Model. Thus, a major drawback in the application of the original Unified Model to MOSFETs with high-κ dielectric has

been successfully overcome in the MSUN Model. Furthermore, the extracted trap distribution was self-consistent over the experimental temperature range of 172K to 300K and the bias range of moderate to strong inversion. The new model also provides better understanding of the impact of different dielectric layers on the noise magnitude and frequency range, which is not possible with the original Unified Model considering a single dielectric layer.

CHAPTER 5

CONCLUSIONS

A physics based compact flicker noise model has been developed for MOSFET devices with high-k materials as the gate dielectric. The reported discrepancies observed in the application of the original Unified Noise Model to high-k gate dielectric MOSFETs are studied. The origin of these discrepancies is identified. Possible remedies are suggested. The effect of remote optical phonon scattering and the dominant scattering mechanisms are experimentally verified. A flexible trap density profile, showing exponential dependence on band-gap energy and tunneling distance of the carriers is implemented in the newly developed Multi Stack Unified Noise (MSUN) Model. As evident from the name, multiple layered nature of the gate dielectric is also incorporated in this model. The quantitative predictions of the new model are experimentally verified. The model is transformed into a compact form to make it compatible with industry standard simulation packages PSP (Surface-Potential-Based Model) and the BSIM (Berkeley Short-Channel IGFET Model).

The variable temperature mobility data revealed significant impact of remote optical phonon scattering on carrier mobility in high-k MOSFETs. However, the variable temperature noise data did not show any dependence on temperature. This observation confirmed that no additional noise mechanism arising from remote phonon

scattering is present in these devices, as tunneling considered in this model is temperature insensitive. As a result, the impact of remote phonon scattering was not separately included in the MSUN Model. This is an important observation as it indicates that the so-called detrimental effects of high-k materials on device performance do not need to be overly generalized. It may as well shed some light on which application areas these devices can be utilized more efficiently.

The correlated number and mobility fluctuation model was experimentally verified as the dominant noise mechanism in these devices. Noise data obtained on MOSFETs with four different interfacial layer thicknesses supported this observation. The correlated number and mobility fluctuation theory has been successfully implemented in the Unified Model and tested in the industry over the time. Therefore, the new model is developed in the framework of this original model and named after it.

The experimental verification of the correlated number and mobility fluctuation and the absence of any additional noise generating mechanism indicate that, the theoretical basis of the Unified Model is correct but not adequate to describe the noise behavior of high-k MOSFET devices. Thus, it further indicates that, the possible causes of the model failure may be from the lack of incorporation of necessary high-k features in the Unified Model. Two such important features of the high-k gate stack that distinguish it from SiO_2 and are not properly incorporated in the Unified Model are identified. These are: (1) the multi layered structure of the gate stack and (2) the energy and spatial dependence of trap densities in the dielectrics. Unified Model assumes a

single layer of SiO_2 as the dielectric and a uniform trap density value throughout the dielectric and with respect to the band-gap energy.

The multi layered structure of the gate stack, implemented by considering tunneling of carriers through a double step barrier, made a key improvement. The resulting expression for $S_{\Delta N_t}$ included the flicker noise contribution from the high-k layer in to the total noise of the device, along with that from the interfacial layer. In the original Unified Model noise contribution from the single SiO_2 layer was considered. Analysis of the experimental data indicates that incorporation of this multi layered structure is key to explaining the interfacial layer dependence of the noise data, as observed in the extracted parameters using the Unified Model. It has been successfully explained in this work that thin interfacial layers does not have any direct contribution in the total device noise. However, the interfacial layer thickness effectively determines the tunneling distance between the channel and the traps in the high-k/ interfacial layer interface, and thus it impacts the total noise magnitude even for the same high-k interface trap densities. As the Unified Model considers noise contribution from only a single dielectric layer, this model is not capable of correct evaluation of the noise contribution from individual dielectric layers of the high-k stack. For devices with the same effective oxide thickness comprised of various physical thicknesses of the interfacial and high-k layers, the Unified Model would predict identical noise performance. The actual device noise may significantly vary from the Unified Model prediction, as evident from the reported discrepancies in the literature. The device noise in this case can be correctly predicted with the MSUN Model as demonstrated on

MOSFETs with various interfacial layer thicknesses over the experimental temperature and bias range.

The trap density model considered in the MSUN Model assumes an exponential dependence of the active trap density values on the energy and spatial distribution of traps. Experimental data taken on MOSFETs with SiO_2 dielectric supporting these assumptions are available in the literature. The impact of this flexible trap profile on noise modeling is observed on the experimental noise data. As the actual excursion of the Fermi energy is small with varying temperature and bias, compared to the total Si band-gap, the energy dependence observed in this range is not very significant irrespective of the sign and value of the extracted energy dependence parameters. However, the impact of these parameters becomes evident when the active trap densities are compared to the mid-gap trap densities. As the devices are operated in the moderate to strong inversion region, the Fermi energy excursion is dominantly around or above the conduction band edge, in which case the energy deviation from the mid-gap becomes significant compared to the total Si band-gap. As observed in the model parameters extracted from the experimental data, the resultant active trap density values closely replicated the low frequency noise from devices with various interfacial layers in a wide range of test conditions. The extracted mid-gap trap density values did not show much variation with temperature or interfacial layer thickness, as expected. However, the calculated parameters outside the excursion range of the Fermi energy level may not be an accurate representation of the actual device parameters, as the experimental data does not belong to those regions.

The energy dependence parameters ξ and λ were observed to be positive for the thicker dielectrics. For the thinnest interfacial layer of 0.8nm these parameters were negative. This difference may be attributed to that fact that, in this range of physical thickness the interfacial layer actually reaches the atomic dimensions, in which case the constituent atoms may not have a full arrangement with the neighboring atoms. Properties of such thin dielectric layers thus can differ from that in fully grown films. The negative values of the spatial distribution parameter η indicate that trap distribution decreases with distance away from the interface. This is a simple manifestation of the fact that, the bulk of the dielectric contains less defect states compared to the interface, as expected.

The observed consistency in the extracted N_{t0HK} with respect to interfacial layer thickness suggests that the IL dependence of the trap profile is properly incorporated in the MSUN Model. Thus, a major drawback in the application of the original Unified Model to MOSFETs with high-κ material as the gate dielectric has been successfully explained in the MSUN Model. Furthermore, the extracted trap distribution values were shown to be consistent over the experimental temperature range of 172K to 300K and the bias range of weak to strong inversion.

Upon verification of the MSUN Model with experimental noise data, the noise expression was transformed into a compact form. As the noise data measured in this work were obtained applying a negligible voltage at the drain terminal, the variation of channel potential, surface potential and carrier density along the channel was neglected in the compact form for the PSP Model. For the BSIM Model, the noise formulation

takes care of the variation of the charge along the channel. The integrals into the dielectrics were eliminated by using closed formed expressions to evaluate the integrals in different dielectric layer thicknesses and compositions. For lower (< 0.1) values of integral limits $2\pi f\tau_{0IL}\exp(\gamma_{IL}T_{IL})$ and $2\pi f\tau_{0HK}\exp(\gamma_{HK}T_{HK})$, corresponding to lower frequencies and/or thinner dielectric, the error between the integral and the compact form was well below 1%. When the integral limits approach the value of 1, the error starts to increase and approaches 1%. However, over the specified range of dielectric properties and the frequency exponent ($T_{IL} \sim 0.7nm - 1.8nm$, $T_{HK} \sim 0.7nm - 5nm$, $\gamma_{HK} \sim 0.2x10^{8} - 1x10^{8}\,cm^{-1}$ and δ~-0.7 to -1.3) the compact form never exceeds the error of 1%. For prediction of noise data this accuracy is satisfactory, taking into consideration the statistical nature of measured noise. For technical complications of the simulator coding, the noise formulation and the compact form was handed over to Compact Modeling Council, as advised by the SRC industrial liaisons. At 45 nm technology node, several companies such as Intel Corporation are already incorporating high-k materials on MOSFET devices. In that respect, the developed model is expected to play an instrumental role in analysis and modeling of flicker noise in next generation MOSFETs with high-k dielectric materials.

As extension to this work, flicker noise modeling can be done on MOSFET devices with smaller dimensions. Compared to larger dimension devices, the low frequency noise in these devices are more Lorentzian like as opposed to well defined 1/f noise characteristics. Moreover, the low frequency noise on different samples shows higher deviation from device to device compared to their larger counterparts. The

dominance of certain trap or trap groups with specific time constants instead of a uniformly distributed trap time constants throughout the dielectric is responsible for this kind of behavior. Characteristics of individual traps or dominant cluster of traps can be studied by Random Telegraph Signal measurements. Based on that, statistical modeling of flicker noise can be suggested for MOSFET devices of smaller dimensions. Another good prospect is to investigate the possibility of relating flicker noise characteristics to device reliability issues. Using 'percolation theory', change in the behavior of defects in the dielectric over specified length of time can be predicted for different stress conditions. Good agreements between experimental data and predictions have been reported [66]. The possibility of correlating the predicted change in the dielectric defect characteristics due to degradation over time and the corresponding deviation in the flicker noise behavior can be a very interesting study and might become an applicable device reliability tool.

APPENDIX A

MATHCAD IMPLEMENTATION OF MSUN MODEL

Two Mathcad files were used to evaluate the flicker noise spectrum by the MSUN Model (1) “LowFrequencyNoiseModel” and (2) “SurfacePotentialCalculation”. The first one contained the fundamental quantities required for the noise evaluation, operating condition dependent parameters (bias and temperature), device physical dimensions and material property parameters, the extracted model parameters and the MSUN Model equations.

For the evaluation of the noise spectrum, the bias dependent parameters were obtained from the DC and CV measurements. The parameters related to energy and spatial distribution of traps, namely ξ_{HK}, λ_{HK} and η_{HK}, were obtained from the experimental values of frequency exponent δ as explained in Chapter 4. For ξ_{IL}, λ_{IL} and η_{IL}, experimental values obtained from SiO_2 were used. N_{t0HK} and μ_{c0} were determined by fitting the MSUN Model to the experimental noise data at 1Hz; freely varying N_{t0HK} and μ_{c0}. Microsoft Excel was used for this experimental data fitting. Best fit values were determined by minimizing the root mean squared error between the data and the model for different combinations of N_{t0HK} and μ_{c0}. N_{t0IL} was assumed to be two orders of magnitude lower than N_{t0HK}, as explained in the main text. Once the required parameter values are obtained, they are passed to the model file; the noise spectrum is evaluated using the MSUN Model expressions.

For noise spectrum evaluation, determination of the channel surface potential was required. This was done by another Mathcad file called ‘SurfacePotentialCalculation’. To evaluate the channel surface potential, a guess value is provided as an initial step. Then, the actual value is solved from the total charge equation, using inversion charge N_{Inv} from CV measurements.

Here, both the files are shown with experimental data obtained on the MOSFET with the thickest interfacial layer of 1.8nm at operating temperature of 172K.

" LowFrequencyNoiseModel"

Fundamental quantities:

$eV := 1.602 \cdot 10^{-19}\,joule$ Electronvolt

$nm := 10^{-9}\,m$ Nano meter

$q := 1.6021 \cdot 10^{-19} \cdot C$ Electronic charge

$h := 6.6262 10^{-34} \cdot J \cdot s$ Planck constant

$\varepsilon_{Si} := 11.8$ Dielectric constant of Si

$\varepsilon_{HfSiON} := 13$ Dielectric constant of HfSiON

$\varepsilon_{SiON} := 9.28$ Dielectric constant of SiON

$\varepsilon_{SiO2} := 3.9$ Dielectric constant of SiO_2

$\varepsilon_0 := 8.8542 10^{-12} \cdot F \cdot m^{-1}$ Vacuum permittivity

$k_B := 8.617 \cdot 10^{-5} \cdot eV \cdot K^{-1}$ Boltzmann constant

$meV := eV \cdot 10^{-3}$ Milli electronvolt

Temperature dependent Parameters:

$n_i := 143.84\,cm^{-3}$ Intrinsic carrier concentration

$E_i := 0.575\,eV$ Intrinsic energy level

$E_g := 1.154\,eV$ Si energy band gap

Parameters related to operating conditions:

$T := 172\,K$ Operating temperature

$V_d := 50\,mV$ Drain voltage with respect to source

$V_g := 1.21\,V$ Gate voltage with respect to source

$N := 5.14 \cdot 10^{12} cm^{-2}$ Inversion charge concentration

$\mu := 382.7575 \cdot \frac{cm^2}{V \cdot s}$ Carrier mobility

$\phi_{ss} := 1.1474\,V$ Surface potential

$I_d := 5.85 \times 10^{-4} A$ Channel current

$V_t := 0.71\,V$ Threshold voltage

Parameters related to physical dimensions and material properties of the device:

$Na := 1.573 \cdot 10^{17} cm^{-3}$	Doping concentration of substrate
$L := 0.2 \cdot 10^{-6} m$	Channel length
$W := 10^{-5} m$	Channel width
$T_{HK} := 3.0\ nm$	Physical thickness of high-k layer
$T_{IL} := 1.8 \cdot nm$	Physical thickness of interfacial layer
$T_{hk} := T_{HK} \cdot \frac{\varepsilon_{SiO2}}{\varepsilon_{HfSiON}}$	Effective thickness of high-k layer
$T_{il} := T_{IL} \cdot \frac{\varepsilon_{SiO2}}{\varepsilon_{SiON}}$	Effective thickness of interfacial layer
$T_{eq} := T_{il} + T_{hk}$	Effective thickness of the dielectric stack
$\gamma_{il} := 9.82 \times 10^{7} \cdot cm^{-1}$	Tunneling coefficient in the interfacial layer
$\gamma_{hk} := 5.38 \times 10^{7} \cdot cm^{-1}$	Tunneling coefficient in the high-k layer
$\tau_{0il} := 10^{-10} s$	Time constant at the interfacial layer/substrate interface
$\tau_{0hk} := \tau_{0il} \cdot \exp(\gamma_{il} \cdot T_{IL})$	Time constant at the high-k/interfacial layer interface
$V_{hk}(x) := \left(V_g - V_d \cdot \frac{x}{L}\right) \cdot \frac{T_{hk}}{T_{eq}}$	Voltage drop across the high-k layer at position x along the channel
$V_{il}(x) := \left(V_g - V_d \cdot \frac{L}{L}\right) \cdot \frac{T_{il}}{T_{eq}}$	Voltage drop across the interfacial layer at position x along the channel
$\phi_{HfSiON} := \frac{1}{q}(1.5eV)$	Band offset of HfSiON with Si
$\phi_{SiON} := \frac{1}{q}(2.5eV)$	Band offset of SiON with Si
$\phi_P := \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{Na}{n_i}\right)$	$=(E_i-E_f)/q$
$\phi_{th} := 2 \cdot \phi_P$	Threshold voltage
$Efs := E_i + q(-\phi_P + \phi_{ss})$	Fermi energy level at the surface

Extracted parameters and derived parameters:

$\lambda_{hk} := -0.947\,eV^{-1}$ Band bending parameter in the high-k layer

$\eta_{hk} := -3.53 \cdot 10^{6} cm^{-1}$ Spatial trap distribution parameter in the high-k

$\xi_{hk} := \lambda_{hk}$ Parameter representing energy dependence of traps in the high-k layer

$\beta_{hk} := \left(\frac{q \cdot \lambda_{hk}}{T_{HK}}\right)$ Derived parameter for high-k layer

$\lambda_{il} := \lambda_{hk}$ Band bending parameter in the interfacial layer

$\eta_{il} := \eta_{hk}$ Spatial trap distribution parameter in the interfacial layer

$\xi_{il} := 9.1 eV^{-1}$ Parameter representing energy dependence of traps in the interfacial layer

$\beta_{il} := \left(\frac{q \cdot \lambda_{il}}{T_{IL}}\right)$ Derived parameter for interfacial layer

$\mu_{c0} := 50 \cdot 10^{9} \frac{cm}{V \cdot s}$ Mobility fluctuation coefficient

$N_{til0} := 2.453 \times 10^{17} \cdot cm^{-3} \cdot eV^{-1}$ Mid-gap trap density value at the Substrate/interfacial layer interface

$N_{thk0} := 100\, N_{til0}$ Mid-gap trap density value at the interfacial layer/high-k interface

$N_{til} := N_{til0} \cdot \exp\left[\xi_{il} \cdot \left(Efs - E_i\right)\right]$ Energy dependent part of active trap density for the interfacial layer

$N_{thk} := N_{thk0} \cdot \exp\left[\xi_{hk} \cdot \left(Efs - E_i\right)\right]$ Energy dependent part of active trap density for the high-k layer

$\alpha := \frac{1}{\left(\mu_{c0} \cdot \sqrt{N}\right)}$ Screened scattering coefficient

Length dependent parameters, not used for these measurements:

$C_{ox} := \frac{\varepsilon_{SiO2} \cdot \varepsilon_0}{T_{eq}}$ Oxide capacitance (SiO_2)

$K_s := \frac{1}{C_{ox}} \cdot \sqrt{2 \cdot \varepsilon_0 \cdot \varepsilon_{Si} \cdot q \cdot Na}$ Parameter used to define parameter 'a'

$g := 1 - \frac{1}{1.744 + 0.8364 \frac{\phi_{th}}{V}}$ Parameter used to define parameter 'a'

$a := 1 + \frac{1}{2} \cdot g \cdot K_s \cdot \frac{1}{\sqrt{\phi_{th}}}$ Parameter used for linearization of inversion charge with position and V_d

$N1(x) := \frac{C_{ox} \cdot \left(V_g - V_t - a \cdot V_d \cdot \frac{x}{L}\right)}{q}$ Channel charge linearly dependent on position along the channel with V_d

MSUN Model Expressions:

Summation of noise spectral components from the high-k layer used for T_{IL}>1.0nm:

$$N_{Thk}(x,f) := \int_0^{T_{HK}} N_{thk}\cdot\left[\exp\left[\left[\frac{q\cdot\lambda_{hk}\cdot\left(V_g - V_d\right)}{T_{HK}}\cdot\frac{T_{hk}}{T_{eq}} + \eta_{hk}\right]\cdot z\right]\cdot\frac{\tau_{0hk}\cdot\exp\left(\gamma_{hk}\cdot z\right)}{1+\left[2\pi\cdot f\cdot\left(\tau_{0hk}\cdot\exp\left(\gamma_{hk}\cdot z\right)\right)\right]^2}\right] dz$$

Summation of noise spectral components from the interfacial layer used for T_{IL}>1.0nm:

$$N_{Til}(x,f) := \int_0^{T_{IL}} N_{til}\cdot\left[\exp\left[\left[\frac{q\cdot\lambda_{il}\cdot\left(V_g - V_d\right)}{T_{IL}}\cdot\frac{T_{il}}{T_{eq}} + \eta_{il}\right]\cdot z\right]\cdot\frac{\tau_{0il}\cdot\exp\left(\gamma_{il}\cdot z\right)}{1+\left[2\pi\cdot f\cdot\left(\tau_{0il}\cdot\exp\left(\gamma_{il}\cdot z\right)\right)\right]^2}\right] dz$$

$\beta_{hk1}(x) := \beta_{hk}\cdot V_{hk}(x) + \eta_{hk}$ $\beta_{il1}(x) := \beta_{il}\cdot V_{il}(x) + \eta_{il}$ <= Simplifying parameters

Summation of noise spectral components from the high-k layer used for T_{IL}=<1.0nm:

$$N_{Thk1}(x,f) := \frac{N_{thk}}{\gamma_{hk}\cdot\left(\tau_{0hk}\right)^{\frac{\beta_{hk1}(x)}{\gamma_{hk}}}\cdot\left(2\cdot\pi\cdot f\right)^{1+\frac{\beta_{hk1}(x)}{\gamma_{hk}}}}\cdot\int_{2\cdot\pi\cdot f\cdot\tau_{0hk}}^{2\cdot\pi\cdot f\cdot\tau_{0hk}\cdot\exp\left(\gamma_{hk}\cdot T_{HK}\right)}\frac{u^{\frac{\beta_{hk1}(x)}{\gamma_{hk}}}}{1+u^2} du$$

Summation of noise spectral components from the interfacial layer used for T_{IL}=<1.0nm:

$$N_{Til1}(x,f) := \frac{N_{til}}{\gamma_{il}\cdot\left(\tau_{0il}\right)^{\frac{\beta_{il1}(x)}{\gamma_{il}}}\cdot\left(2\cdot\pi\cdot f\right)^{1+\frac{\beta_{il1}(x)}{\gamma_{il}}}}\cdot\int_{2\cdot\pi\cdot f\cdot\tau_{0il}}^{2\cdot\pi\cdot f\cdot\tau_{0il}\cdot\exp\left(\gamma_{il}\cdot T_{IL}\right)}\frac{u^{\frac{\beta_{il1}(x)}{\gamma_{il}}}}{1+u^2} du$$

Total current noise spectral density considering gradual channel:

$$S_{Id}(f) := \frac{4k_B \cdot T \cdot I_d^{\,2}}{W \cdot L^{\,2}} \cdot \int_0^L \left(\alpha \cdot \mu + \frac{1}{N}\right)^2 \cdot \left[\left(N_{Til}(x,f)\right) + \left(N_{Thk}(x,f)\right)\right] dx$$

Total current noise spectral density considering uniform channel:

$x := L$

$$S_{Id1}(f) := \frac{4k_B \cdot T \cdot I_d^{\,2}}{W \cdot L} \cdot \left[\left(\alpha \cdot \mu + \frac{1}{N}\right)^2 \cdot \left[\left(N_{Til}(x,f)\right) + \left(N_{Thk}(x,f)\right)\right]\right]$$

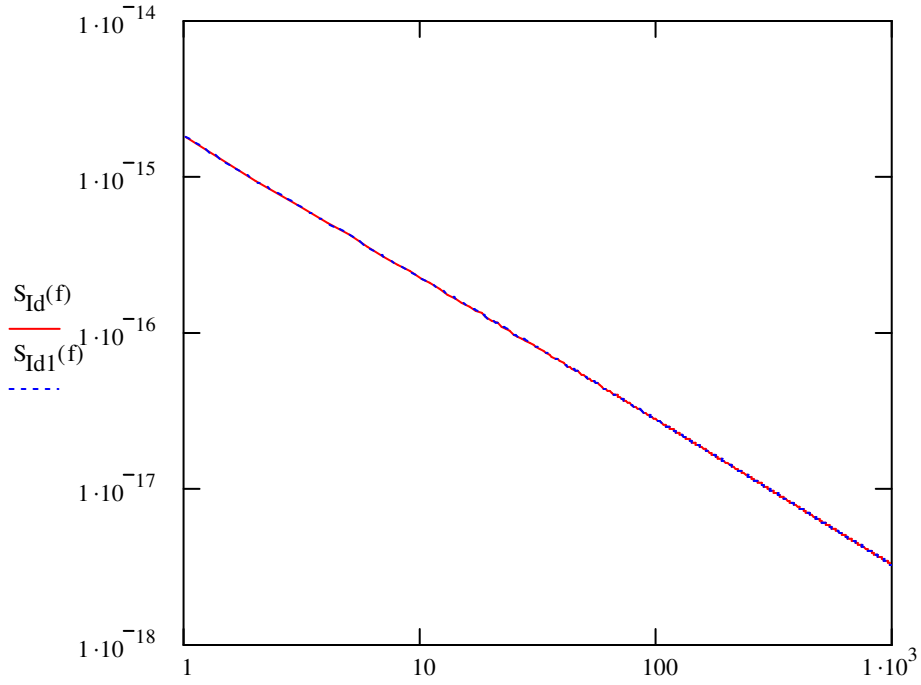
$N_{t1}(x,f) := \left(N_{Til}(x,f)\right) + \left(N_{Thk}(x,f)\right)$

$N_t(x,f) := \left(N_{Thk}(x,f)\right)$

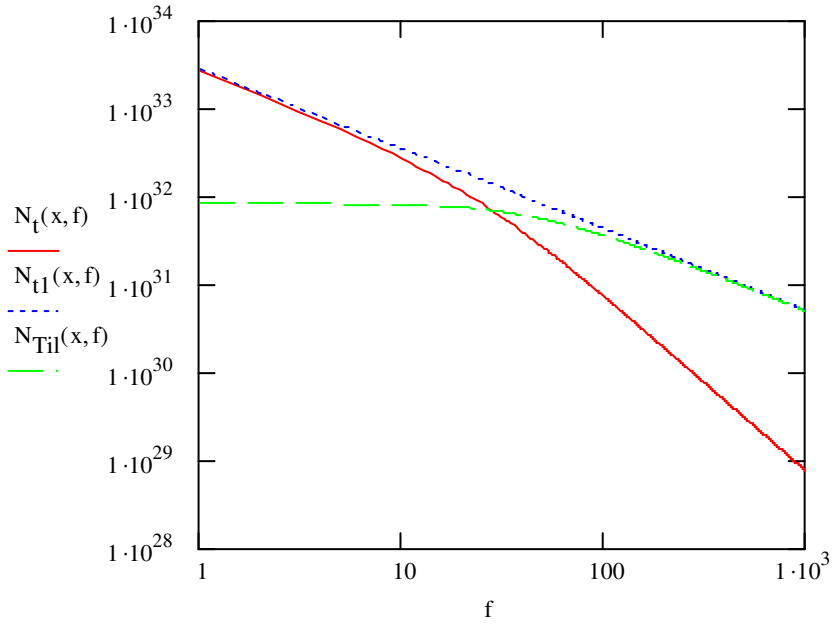
Variables defined to observe the impact of interfacial and high-k layers

$f := 1Hz, 2Hz .. 1000Hz$

Defining noise frequency range



Length dependence of S_{Id} is compared for uniform channel approximation and uniform channel evaluation.



Noise contribution from different layers and resultant effect for T_{IL}=1.8nm

f =
1
2
3

$N_{t1}(x,f)$ =
2.756·10^33
1.479·10^33
1.028·10^33

$N_t(x,f)$ =
2.675·10^33
1.398·10^33
9.465·10^32

$\frac{S_{Id1}(f)}{10^{-16}}$ =
17.549
9.418
6.543

$\frac{S_{Id}(f)}{10^{-16}}$ =
17.549
9.418
6.543

"SurfacePotentialCalculation"

Parameters: Device specific and relating to operating conditions

$Na := 1.573 \cdot 10^{17} cm^{-3}$ Substrate doping concentration

$ni := 1.438 \cdot 10^{2} cm^{-3}$ Intrinsic carrier concentration

$N_{inv} := 5.14 \cdot 10^{12} cm^{-2}$ Inversion charge density

$T := 172\,K$ Experimental temperature

Fundamental quantities

$eV := 1.602 \cdot 10^{-19} joule$ Electronvolt

$q := 1.6 \cdot 10^{-19} C$ Electronic charge

$\varepsilon_{si} := 11.7 \cdot 8.85 \cdot 10^{-14} F\,cm^{-1}$ Permittivity of Si

$k := 8.62 \cdot 10^{-5} eV \cdot K^{-1}$ Boltzmann constant

$vt := \frac{k \cdot T}{q}$ Thermal potential

$LD := \left(\frac{\varepsilon_{si} \cdot vt}{q \cdot Na} \right)^{0.5}$ Debye length

The total charge equation in a MOS CAP:

$$\left[2^{0.5} \cdot \varepsilon_{si} \cdot \left(\frac{vt}{q \cdot LD} \right) \cdot \left[\left[\frac{\psi_s}{vt} + e^{\left(\frac{-\psi_s}{vt} \right)} - 1 \right] + \left(\frac{ni}{Na} \right)^2 \cdot \left[e^{\left(\frac{q \cdot \psi_s}{k \cdot T} \right)} - 1 \right] \right]^{0.5} \right] - Na \cdot \left(\frac{2 \cdot \varepsilon_{si} \cdot \psi_s}{q \cdot Na} \right)^{0.5} - N_{inv} = 0$$

$\psi_s := 1.136\,V$ ←Surface potential - Initial guess value (chosen close to actual solution)

$$root\left[\left[2^{.5} \cdot \varepsilon_{si} \cdot \left(\frac{vt}{q \cdot LD} \right) \cdot \left[\left[\frac{\psi_s}{vt} + e^{\left(\frac{-\psi_s}{vt} \right)} - 1 \right] + \left(\frac{ni}{Na} \right)^2 \cdot \left[e^{\left(\frac{\psi_s}{vt} \right)} - 1 \right] \right]^{0.5} - Na \cdot \left(\frac{2 \cdot \varepsilon_{si} \cdot \psi_s}{q \cdot Na} \right)^{0.5} - N_{inv}, \psi_s \right] = 1.136V$$

This part is to check if the obtained root value for surface potential is valid.

$$\frac{\psi_s}{vt} = 76.524 \qquad e^{\left(\frac{-\psi_s}{vt}\right)} - 1 = -1 \qquad \left[\frac{\psi_s}{vt} + \left[e^{\left(\frac{-\psi_s}{vt}\right)} - 1\right]\right] = 75.524$$

$$e^{\left(\frac{\psi_s}{vt}\right)} = 1.714 \times 10^{33} \qquad e^{\left(\frac{\psi_s}{vt}\right)} - 1 = 1.714 \times 10^{33} \qquad \left(\frac{ni}{Na}\right)^2 \cdot \left[e^{\left(\frac{\psi_s}{vt}\right)} - 1\right] = 1.433 \times 10^3$$

$$\left[\left[\frac{\psi_s}{vt} + \left[e^{\left(\frac{-\psi_s}{vt}\right)} - 1\right]\right] + \left(\frac{ni}{Na}\right)^2 \cdot \left[e^{\left(\frac{\psi_s}{vt}\right)} - 1\right]\right] = 1.508 \times 10^3$$

$$\left[\left[\frac{\psi_s}{vt} + \left[e^{\left(\frac{-\psi_s}{vt}\right)} - 1\right]\right] + \left(\frac{ni}{Na}\right)^2 \cdot \left[e^{\left(\frac{\psi_s}{vt}\right)} - 1\right]\right]^{0.5} = 38.838$$

N_{Inv} value calculated substituting back the surface potential.

$$N_{Total} := 2^{.5} \cdot \varepsilon_{si} \cdot \left(\frac{vt}{q \cdot LD}\right) \cdot \left[\left[\frac{\psi_s}{vt} + \left[e^{\left(\frac{-\psi_s}{vt}\right)} - 1\right]\right] + \left(\frac{ni}{Na}\right)^2 \cdot \left[e^{\left(\frac{\psi_s}{vt}\right)} - 1\right]\right]^{0.5}$$

$$N_{Depl} := Na \cdot \left(\frac{2 \cdot \varepsilon_{si} \cdot \psi_s}{q \cdot Na}\right)^{0.5}$$

$$N_{Inv} := N_{Total} - N_{Depl}$$

$$N_{Inv} = 5.231 \times 10^{16} \frac{1}{m^2}$$

APPENDIX B

DERIVATION OF THE COMPACT FORM FOR THE INTEGRALS

B.1 Introduction

According to the MSUN Model, the final expression of the current noise spectral density S_{I_d} can be shown as [38, 39]:

$$S_{I_d}(f) = \frac{4kTI_d^{\,2}}{WL^2}\int_0^L \left(\alpha\mu_{eff} + \frac{1}{N(x)}\right)^2 \left[\frac{N_{t0IL}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}\tau_{0IL}^{\,(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}(2\pi f)^{1+(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}} \int_{2\pi f\tau_{0IL}}^{2\pi f\tau_{0IL}\exp(\gamma_{IL}T_{IL})} \frac{u_{IL}^{\,(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}}{1+u_{IL}^{\,2}}du_{IL} \right.$$
$$\left. + \frac{N_{t0HK}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}\tau_{0HK}^{\,(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}(2\pi f)^{1+(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}} \int_{2\pi f\tau_{0HK}}^{2\pi f\tau_{0HK}\exp(\gamma_{HK}T_{HK})} \frac{u_{HK}^{\,(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}}{1+u_{HK}^{\,2}}du_{HK} \right] dx$$

(B.1)

The integrals appearing in the above expression need to be transformed into a compact form in order to incorporate the model in industry standard device simulation programs like BSIM or PSP. The main challenge in doing so comes from the fact that, the integral for the interfacial layer has 5 parameters, where as that for the high-k layer has 7. Expressing integral functions in compact form with that many parameters, while maintaining the integration limits of 10^{-6} - 10^{21}, requires careful manipulations.

B.2. Simplification of the integral

To simplify the evaluation of integrals, β'_{HK}/γ_{HK} and β'_{IL}/γ_{IL} are generalized as δ' with values in the range of 0.3 to -0.3, resulting in a frequency exponent in the range of δ = 0.7 to δ = 1.3.

Here, $$\beta'_{HK} = \beta_{HK}V_{HK} + \eta_{HK}, \tag{B.2}$$

$$\beta'_{IL} = \beta_{IL}V_{IL} + \eta_{IL} \tag{B.3}$$

and $$\delta' = \delta - 1 \tag{B.4}$$

and δ is the flicker noise exponent for the spectral form ~ $1/f^{\delta}$.

The lower limit of the high-k layer integral $2\pi f\tau_{0HK}$ is generalized as *LL* (lower limit) in the range of 10^{-6} (assuming $f_{(min)}$ = 1Hz, γ_{IL} = 1x10^8 cm^{-1}, minimum T_{IL} = 0.8nm, $2\pi f\tau_{0HK(\min)} \approx$ 1.62x10^{-6}) to 10^2 (assuming $f_{(max)}$ = 1kHz, γ_{IL} = 1x10^8 cm^{-1}, maximum T_{IL} = 1.8nm and $2\pi f\tau_{0HK(\max)} \approx 30$). $\exp(\gamma_{HK}T_{HK})$ is generalized as a single parameter U_{HK} and the upper limit is generalized as $UL = LLxU_{HK}$. U_{HK} is allowed to vary in the range of 4.05 (with $\gamma_{HK(\min)}$ = 0.2x10^8 cm^{-1} and minimum T_{HK} = 0.7nm) to 5.18x10^{21} (with $\gamma_{HK(\max)}$ = 1x10^8 cm^{-1} and maximum T_{HK} = 5.0nm).

For the high-k layer, the integral in the generalized form can be shown as:

$$\int_{LL}^{UL}\frac{u^{\delta'}}{1+u^2}du=\int_0^{UL}\frac{u^{\delta'}}{1+u^2}du-\int_0^{LL}\frac{u^{\delta'}}{1+u^2}du \tag{B.5}$$

$$LL=2\pi f\tau_{0HK} \tag{B.6}$$

with $$\delta'=\beta'_{HK}/\gamma_{HK} \tag{B.7}$$

and $$\int_0^{UL}\frac{u^{\delta'}}{1+u^2}du=\int_0^{LLxU_{HK}}\frac{u^{\delta'}}{1+u^2}du \tag{B.8}$$

For the interfacial layer, the integral in the generalized form can be shown as:

$$\int_{2\pi f\tau_{0IL}}^{LL}\frac{u^{\delta'}}{1+u^2}du=\int_0^{LL}\frac{u^{\delta'}}{1+u^2}du-\int_0^{2\pi f\tau_{0IL}}\frac{u^{\delta'}}{1+u^2}du \tag{B.9}$$

with $$\delta'=\beta'_{IL}/\gamma_{IL} \tag{B.10}$$

Considering a minimum interfacial layer thickness of 0.8nm (when it approaches the atomic limits) and a tunneling coefficient of γ_{IL} = 1x10^8 cm^{-1}, we have

$\exp(\gamma_{IL}T_{IL}) \approx 10^4$, and the second term becomes at least two orders of magnitude smaller than the former. The total integral from the IL can be approximated as:

$$\int_{2\pi f\tau_{0IL}}^{LL} \frac{u^{\delta'}}{1+u^2}du = \int_0^{LL} \frac{u^{\delta'}}{1+u^2}du \tag{B.11}$$

Evaluating the integrals in this fashion results in a single compact form as a function of *LL* (with 0 as the lower limit) with δ' as a parameter. In addition, this also allows the use of the same functional codes to evaluate all three integrals $\int_0^{LLxU_{HK}} \frac{u^{\delta'}}{1+u^2}du$ and $\int_0^{LL} \frac{u^{\delta'}}{1+u^2}du$ with $\delta' = \beta'_{HK}/\gamma_{HK}$, and $\int_0^{LL} \frac{u^{\delta'}}{1+u^2}du$ with $\delta' = \beta'_{IL}/\gamma_{IL}$.

B.3 Compact expressions

The form of the compact expression is expected to vary with the behavior of the integrand in different regions over the total range of the integral limit *LL*. The integrand in the range of 10^{-5} to 10^5 is shown in Figure B.1. As we move away from u=1, the integrand changes monotonically with logarithm of u. In the immediate vicinity of u=1 ($10^{-2} < u < 10^2$), the variation of the integrand with u is more complicated. Observing the nature of the integrand, the total range of *LL* is subdivided into six different regions in each of which $\int_0^{LL} \frac{u^{\delta'}}{1+u^2}du$ is expressed as a function of *LL* with δ' as a parameter in compact form.

Region1: $10^{-6} \le LL < 10^{-2}$ and $-0.3 \le \delta' \le 0.3$

Region2: $10^{-2} \le LL < 10^{-1}$ and $-0.3 \le \delta' \le 0.3$

Region3: $10^{-1} \le LL < 10^{0}$ and $-0.3 \le \delta' \le 0.3$

Region4: $10^{0} \le LL < 10^{1}$ and $-0.3 \le \delta' \le 0.3$

Region5: $10^{1} \le LL < 10^{2}$ and $-0.3 \le \delta' \le 0.3$

Region6: $10^{2} \le LL < 10^{4}$ and $-0.3 \le \delta' \le 0.3$

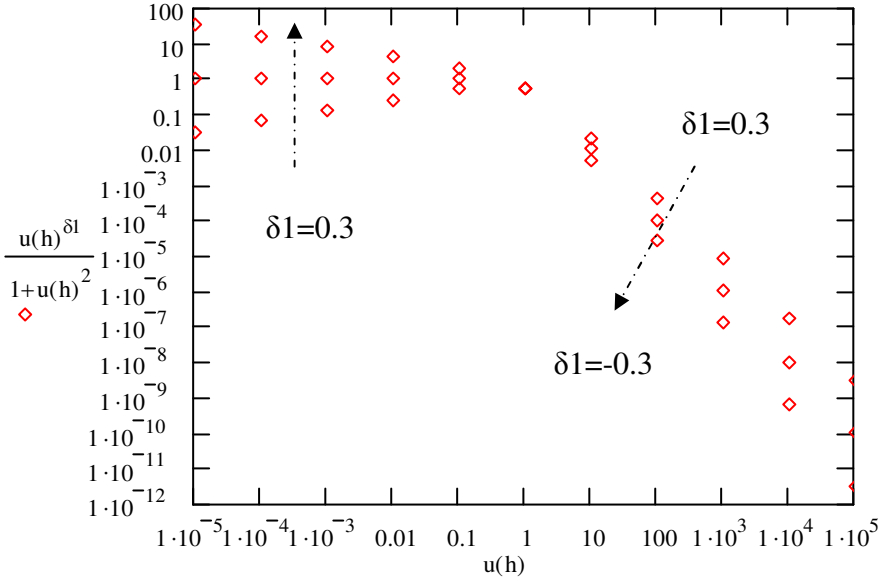


Figure B.1 The integrand $u^{\delta'}/\left(1+u^{2}\right)$ as a function of u, here represented by u(h). The integrand is shown for δ'=-0.3, δ'=0 and δ'=0.3. δ1 in Mathcad represents δ'.

Compact forms were obtained for individual regions and were verified with the actual integral in Mathcad. In Mathcad, representations of actual quantities are made as follows:

LL ➔ LL(h)

δ' ➔ δ1

$$\int_0^{LL} \frac{u^{\delta'}}{1+u^2}\,du \rightarrow Int(\delta 1, h)$$

The functions are implemented in Mathcad for all regions as follows:

Defining, $$LL(h) = 10^h \tag{B.12}$$

and $$Int(\delta 1, h) = \int_0^{LL(h)} \frac{u^{\delta 1}}{1+u^2}\,du \tag{B.13}$$

here, *h* is a variable to generate desired order of *LL*.

B.3.1 Compact expression for Region 1

In this region, we can simplify the integral as (assuming $u^2 << 1$)

$$\int_0^{LL} \frac{u^{\delta'}}{1+u^2}\,du \approx \int_0^{LL} \frac{u^{\delta'}}{1}\,du = \left[\frac{u^{\delta'+1}}{\delta'+1}\right]_0^{LL} = \frac{LL^{\delta'+1}}{\delta'+1} \tag{B.14}$$

In Mathcad, the compact form corresponding to region 1 is defined as:

$$func1(\delta 1, h) = \frac{LL(h)^{\delta 1+1}}{\delta 1+1} \tag{B.15}$$

Comparison of the compact form with the actual integral is shown in Figure B.2 The absolute error is shown in Figure B.3.

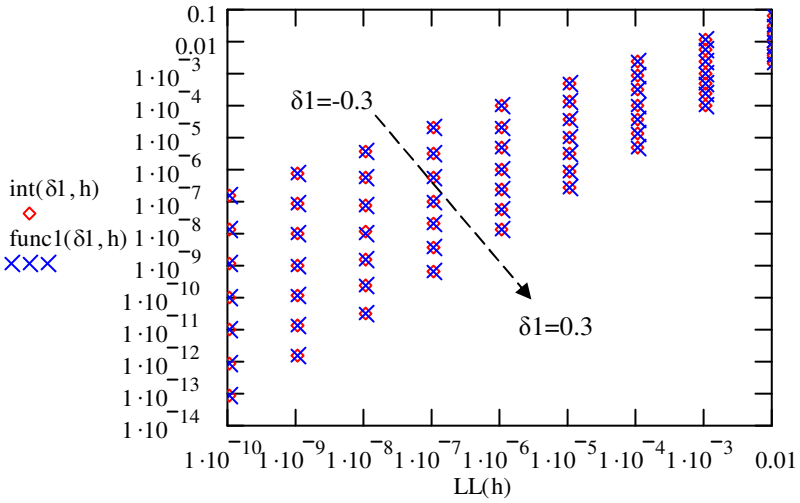


Figure B.2 Comparison of region 1 compact expression *func1(δ1,h)* and actual integration int(δ1,h), with *LL=LL(h)* and *δ*1=0.3 to -0.3, in steps of 0.1.

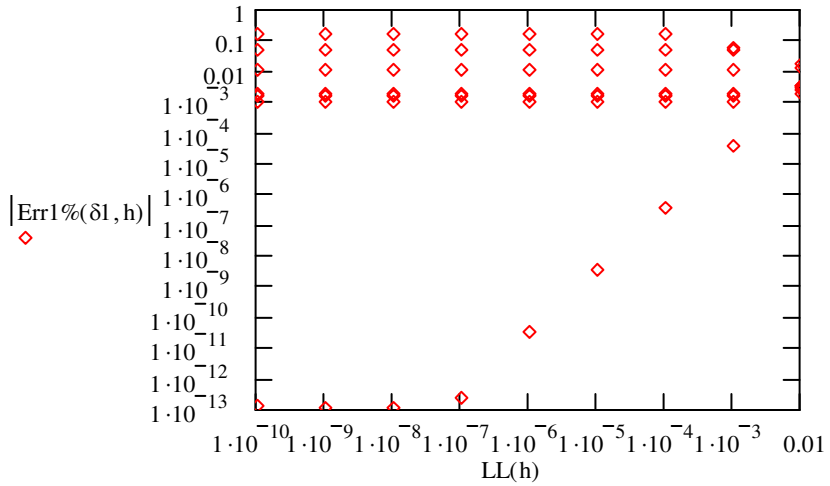


Figure B.3 The error between the compact expression and the actual integration in region 1.

B.3.2 Compact expression for Region 2

The compact form was obtained for region 2 by using curve fitting. Actual integral values were obtained in the range of $LL=10^{-2}$ to 10^{-1} for individual values of $\delta'=0.3$ to -0.3 in steps of 0.1. The best fitting functional form was obtained using the software CurveExpert, which compares more than 30 predefined functions and sorts them according to standard error.

The Hoerl model was found as the best fitting function for δ' in the range of -0.3 to 0.3 for this region with the functional form of:

$$y = ab^x x^c \tag{B.16}$$

The coefficients *a, b* and *c* for individual δ' values are obtained and expressed as functions of δ' by curve fitting. The compact form of the integral for region 2 is implemented in Mathcad as:

$a \rightarrow a2(\delta 1)$

$b \rightarrow b2(\delta 1)$

$c \rightarrow c2(\delta 1)$

$y \rightarrow func2(\delta 1,h)$

$$func2(\delta 1,h) = a2(\delta 1)\, b2(\delta 1)^{LL(h)} LL(h)^{c2(\delta 1)} \tag{B.17}$$

The functional forms for $a2(\delta)$, $b2(\delta)$ and $c2(\delta)$ as well as the coefficients are provided in Table B1. The compact form and the actual integral is compared in Figure B.4 with the error in Figure B.5.

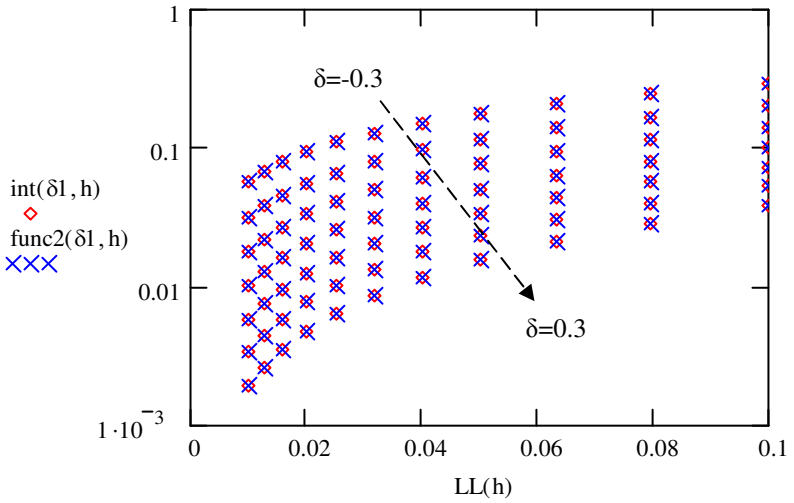


Figure B.4 Comparison of region 2 compact expression *func2(δ1,h)* and actual integration int(δ1,h), with *LL=LL(h)* and *δ*1=0.3 to -0.3, in steps of 0.1.

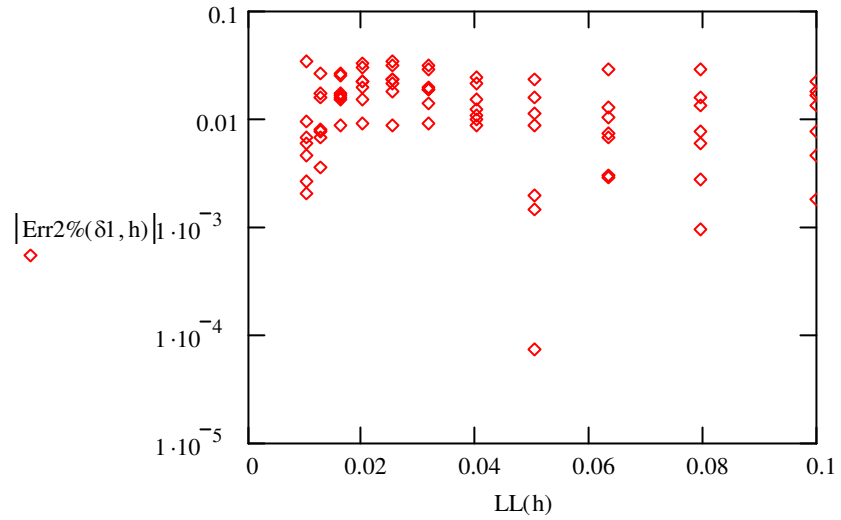


Figure B.5 The error between the compact expression and the actual integration in region 2.

For regions 3, 4, 5 and 6, the same procedure is followed. Thus, for these regions, only the obtained compact forms and the results will be discussed.

B.3.3 Compact expression for Region 3

Actual integral values were obtained in the range of LL=10^{-1} to 10^{-0} for individual values of δ'=0.3 to -0.3 in steps of 0.1. In this region, 6th order Polynomial function was found to give the minimal error. The functional form is:

$$y = a + bx + cx^2 + dx^3 + ex^4 + fx^5 + gx^6 \tag{B.18}$$

The coefficients *a, b, c, d, e, f* and g for individual δ' values are obtained and expressed as functions of δ' by curve fitting. The compact form of the integral for region 3 is implemented in Mathcad as:

a ➔ $a3(\delta 1)$

b ➔ $b3(\delta 1)$

upto

g ➔ $g3(\delta 1)$

y ➔ $func3(\delta 1,h)$

$$func3(\delta 1,h) = a3(\delta 1) + b3(\delta 1)LL(h) + c3(\delta 1)LL(h)^2 + d3(\delta 1)LL(h)^3 + e3(\delta 1)LL(h)^4 + f3(\delta 1)LL(h)^5 + g3(\delta 1)LL(h)^6 \tag{B.19}$$

a3(δ), b3(δ), c3(δ), d3(δ), e3(δ, f3(δ)) and *g3(δ)* function types along with the corresponding coefficients are provided in Table B1.

The compact form is compared with the actual integral in Figure B.6 with the error in Figure B.7.

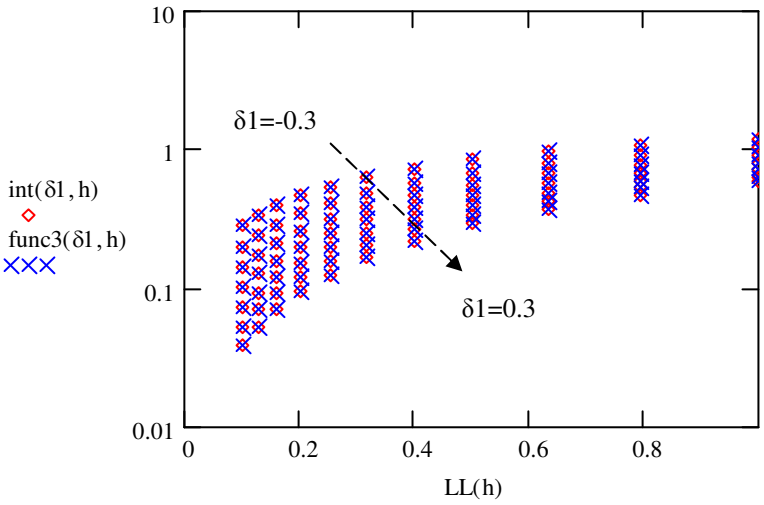


Figure B.6 Comparison of region 3 compact expression *func3(δ1,h)* and actual integration int(δ1,h), with *LL=LL(h)* and *δ*1=0.3 to -0.3, in steps of 0.1.

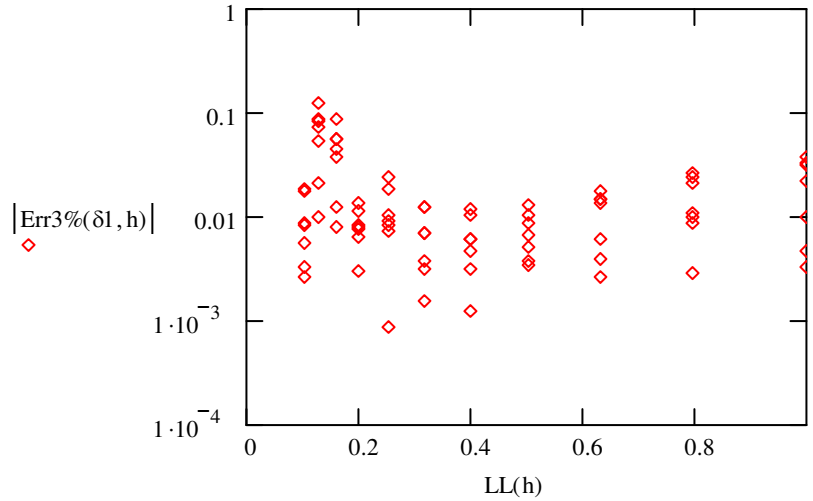


Figure B.7 The error between the compact expression and the actual integration in region 3.

B.3.4 Compact expression for Region 4

Actual integral values were obtained in the range of $LL=10^0$ to 10^1 for individual values of δ'=0.3 to -0.3 in steps of 0.1. In this case, MMF function was found to give the best results. The functional form of MMF function is:

$$y = \left(ab + cx^d\right) / \left(b + x^d\right) \tag{B.20}$$

The coefficients *a, b*, *c* and *d* for individual δ' values are obtained and expressed as functions of δ' by curve fitting. The compact form of the integral for region 4 is implemented in Mathcad as:

$a \rightarrow a4(\delta 1)$

$b \rightarrow b4(\delta 1)$

$c \rightarrow c4(\delta 1)$

$d \rightarrow d4(\delta 1)$

$y \rightarrow func4(\delta 1, h)$

$$func4(\delta 1, h) = \left(a4(\delta 1)b4(\delta 1) + c4(\delta 1)LL(h)^{d4(\delta 1)}\right) / \left(b4(\delta 1) + LL(h)^{d4(\delta 1)}\right) \tag{B.21}$$

Function types of $a4(\delta 1)$, $b4(\delta 1)$, $c4(\delta 1)$ and $d4(\delta 1)$ along with the corresponding coefficients are provided in Table B1.

The compact form is compared with the actual integral in Figure B.8 with the error in Figure B.9.

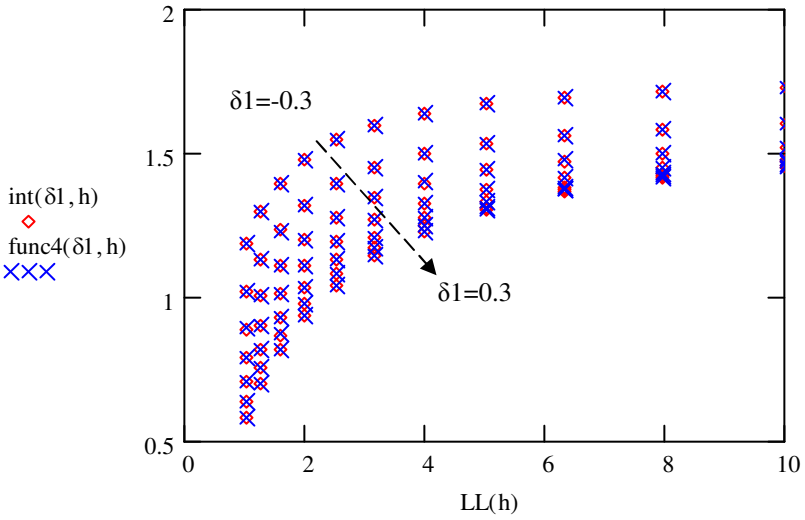


Figure B.8 Comparison of region 4 compact expression *func4(δ1,h)* and actual integration int(δ1,h), with *LL=LL(h)* and *δ*1=0.3 to -0.3, in steps of 0.1.

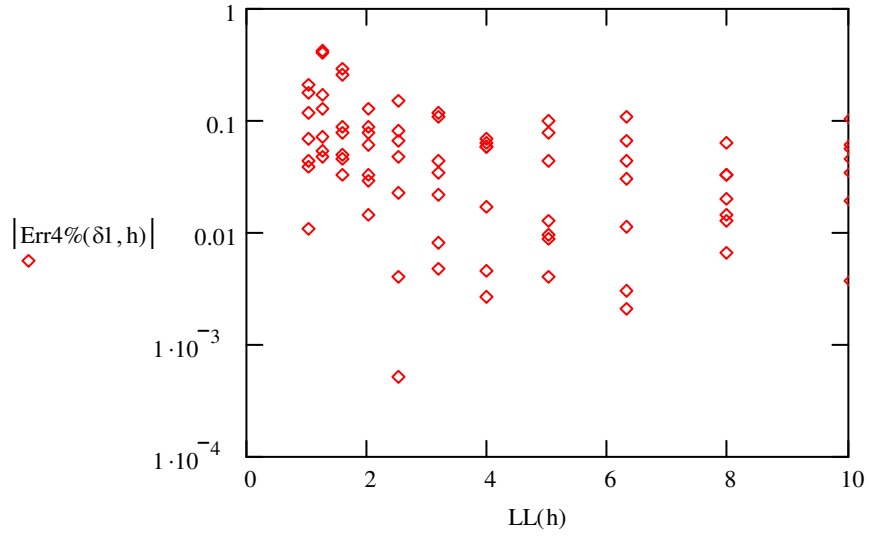


Figure B.9 Error between compact expression and actual integration in region 4.

B.3.5 Compact expression for Region 5

Actual integral values were obtained in the range of $LL=10^1$ to 10^2 for individual values of δ' =0.3 to -0.3 in steps of 0.1. In this case, Modified Hoerl function was found to give the best results. The functional form of Modified Hoerl function is:

$$y = ab^{\frac{1}{x}}x^c \tag{B.22}$$

The coefficients *a, b* and *c* for individual δ' values are obtained and expressed as functions of δ' by curve fitting. The compact form of the integral for region 5 is implemented in Mathcad as:

$a \rightarrow a5(\delta 1)$

$b \rightarrow b5(\delta 1)$

$c \rightarrow c5(\delta 1)$

$y \rightarrow func5(\delta 1,h)$

$$func5(\delta 1, h) = a5(\delta 1)b5(\delta 1)^{\frac{1}{LL(h)}}LL(h)^{c5(\delta 1)} \tag{B.23}$$

Function types of $a5(\delta 1)$, $b5(\delta 1)$, and $c5(\delta 1)$ along with the corresponding coefficients are provided in Table B1.

The compact form is compared with the actual integral in Figure B.10 with the error in Figure B.11.

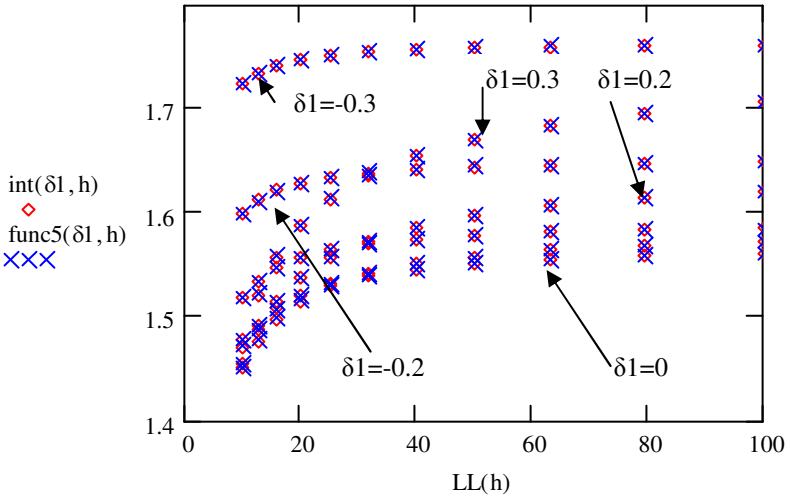


Figure B.10 Comparison of region 5 compact expression *func5(δ1,h)* and actual integration int(δ1,h), with *LL=LL(h)* and *δ*1=0.3 to -0.3, in steps of 0.1.

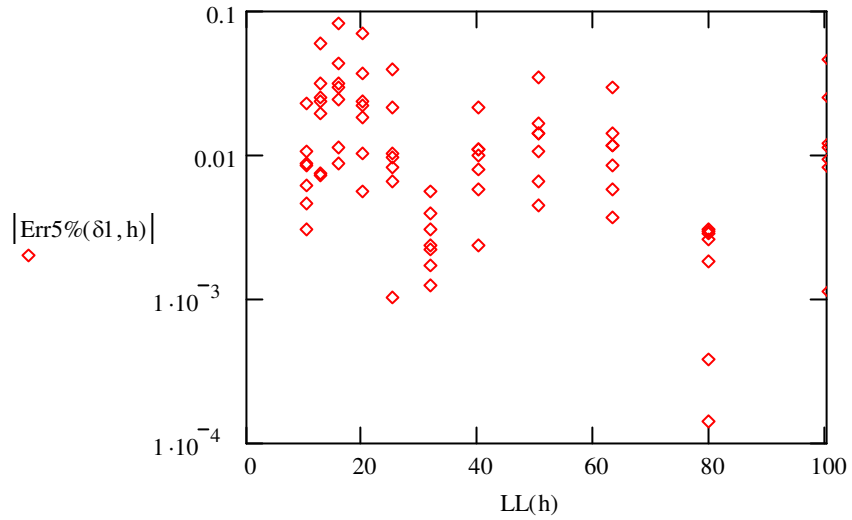


Figure B.11 The error between the compact expression and the actual integration in region 5.

B.3.6 Compact expression for Region 6

Actual integral values were obtained in the range of $LL=10^2$ to 10^4 for individual values of $\delta'=0.3$ to -0.3 in steps of 0.1. Modified Hoerl function was

observed to give the best fit values for this region. The functional form of Modified Hoerl function is:

$$y = ab^{\frac{1}{x}} x^{c} \tag{B.24}$$

The coefficients *a, b* and *c* for individual δ' values are obtained and expressed as functions of δ' by curve fitting. The compact form of the integral for region 6 is implemented in Mathcad as:

$a \rightarrow a6(\delta 1)$

$b \rightarrow b6(\delta 1)$

$c \rightarrow c6(\delta 1)$

$y \rightarrow func6(\delta 1, h)$

$$func6(\delta 1, h) = a6(\delta 1) b6(\delta 1)^{\frac{1}{LL(h)}} LL(h)^{c6(\delta 1)} \tag{B.25}$$

Function types of $a6(\delta 1)$, $b6(\delta 1)$, and $c6(\delta 1)$ along with the corresponding coefficients are provided in Table B1.The comparison of the compact form with the actual integral is shown in Figure B.12 with the error in Figure B.13.

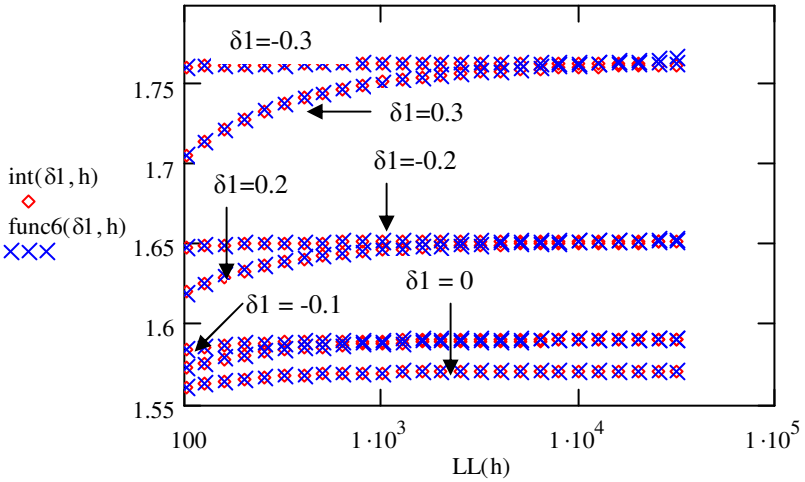


Figure B.12 Comparison of region 6 compact expression *func6(δ1,h)* and actual integration int(δ1,h), with *LL=LL(h)* and *δ*1=0.3 to -0.3, in steps of 0.1.

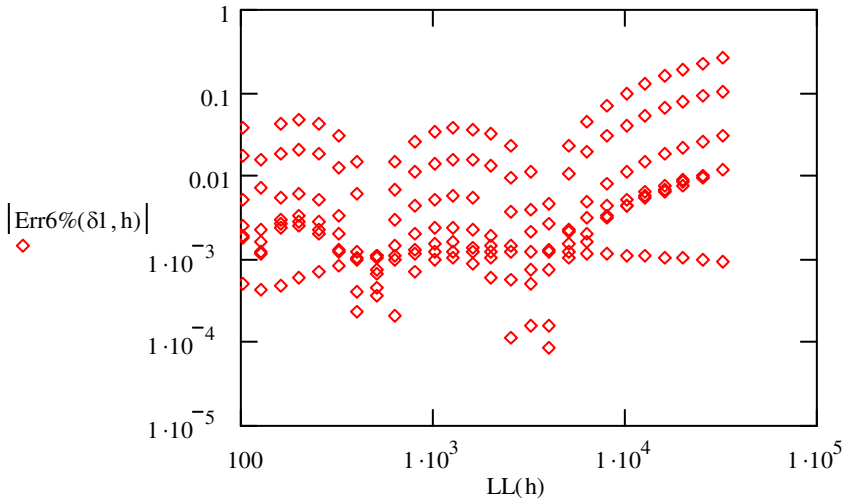


Figure B.13 The error between the actual and the compact integral in region 6.

For the integral values beyond $LL = 10^4$, $func6(\delta, h)$ evaluated at $LL(h) = 6309$ is used, denoted as *func6_lim(δ,h)*. 6309 is the maximum value of *LL(h)* for the data

values used to arrive at the expression of $func6(\delta, h)$. Using a value of $LL(h)=10^4$ will give essentially the same result.

B.3.7 Evaluation of the integral

The evaluation of the integral $\int_0^{LL} \frac{u^{\delta'}}{1+u^2} du$ is carried out according to the following algorithm using *if* condition:

$$cal\_LL(\delta,h) = \begin{cases} func1(\delta 1, h) \text{ if } 10^{-6} \le LL(h) < 10^{-2} \\ func2(\delta 1, h) \text{ if } 10^{-2} \le LL(h) < 10^{-1} \\ func3(\delta 1, h) \text{ if } 10^{-1} \le LL(h) < 10^{0} \\ func4(\delta 1, h) \text{ if } 10^{0} \le LL(h) < 10^{1} \\ func5(\delta 1, h) \text{ if } 10^{1} \le LL(h) < 10^{2} \\ func6(\delta 1, h) \text{ if } 10^{2} \le LL(h) < 6300 \\ func6\_lim(\delta 1, h) \text{ if } 6300 \le LL(h) \end{cases}$$

The evaluation of the integral $\int_0^{UL} \frac{u^{\delta'}}{1+u^2} du$, where $UL=LL \times U_{HK}$ and $U_{HK} = \exp(\gamma_{HK} T_{HK})$, is carried out according to the following algorithm using *if* condition:

$$cal\_UL(\delta 1,h,HK) = \begin{cases} H\_func1(HK, \delta 1, h) \text{ if } 10^{-6} \le LL(h) \times U_{HK} < 10^{-2} \\ H\_func2(HK, \delta 1, h) \text{ if } 10^{-2} \le LL(h) \times U_{HK} < 10^{-1} \\ H\_func3(HK, \delta 1, h) \text{ if } 10^{-1} \le LL(h) \times U_{HK} < 10^{0} \\ H\_func4(HK, \delta 1, h) \text{ if } 10^{0} \le LL(h) \times U_{HK} < 10^{1} \end{cases}$$

$$H\_func5(HK,\delta 1,h) \text{ if } 10^1 \le LL(h)\text{x}U_{HK} < 10^2$$

$$H\_func6(HK,\delta 1,h) \text{ if } 10^2 \le LL(h)\text{x}U_{HK} < 6300$$

$$H\_func6\_lim(HK,\delta 1,h) \text{ if } 6300 \le LL(h)\text{x}U_{HK}$$

To calculate *cal_UL(*δ1*,h,HK*), identical functions are used with *LL(h)* replaced with *LL(h)*xV_{HK} and renaming the functions as *H_func* instead of *func* followed by the corresponding region number, as can be seen in the definitions in the previous condition blocks.

The integral $\int_{LL}^{UL} \frac{u^{\delta'}}{1+u^2} du$ is now evaluated as

$$cal\_Int(\delta 1,h,HK) = cal\_UL(\delta 1,h,HK) - cal\_LL(\delta 1,h) \quad \text{(B.26)}$$

The calculated integral *cal_Int(*δ1*,h,HK)* is compared below to the actual integral *Int(*δ1*,h,HK)* for a high-k layer thickness of 1nm with γ_{HK} of 0.2x108 $cm^{-1}$and δ'=-0.3. Figure B.14 shows the comparison of the calculated and the actual integration. Corresponding *cal_UL(*δ*,h,HK)* and *cal_LL(*δ*,h)* are shown in Figure B.15 for the same range. Figure B.16 shows the error between the estimated and the calculated integrals.

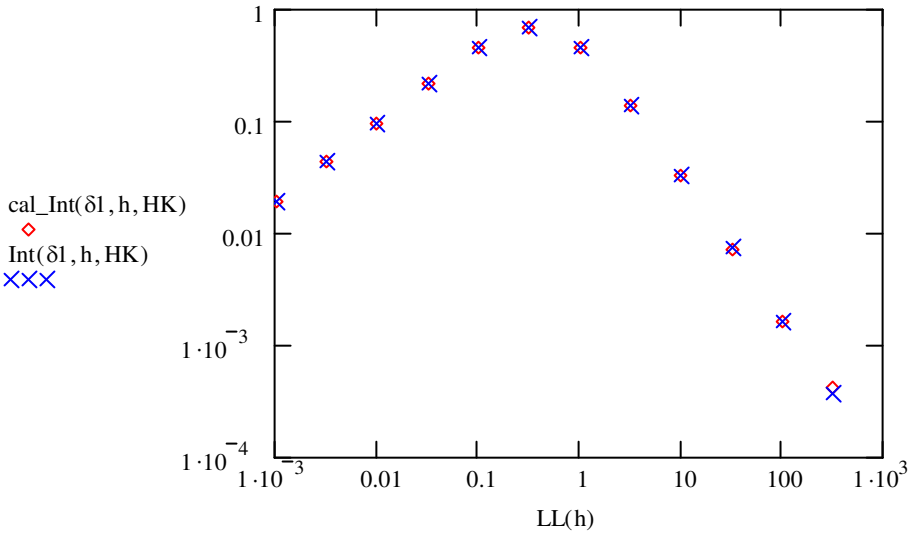


Figure B.14 Comparison between calculated integral *cal_Int(δ1,h,HK)* and actual integral *Int(δ1,h,HK)* shows a difference at higher values of *LL(h)*.

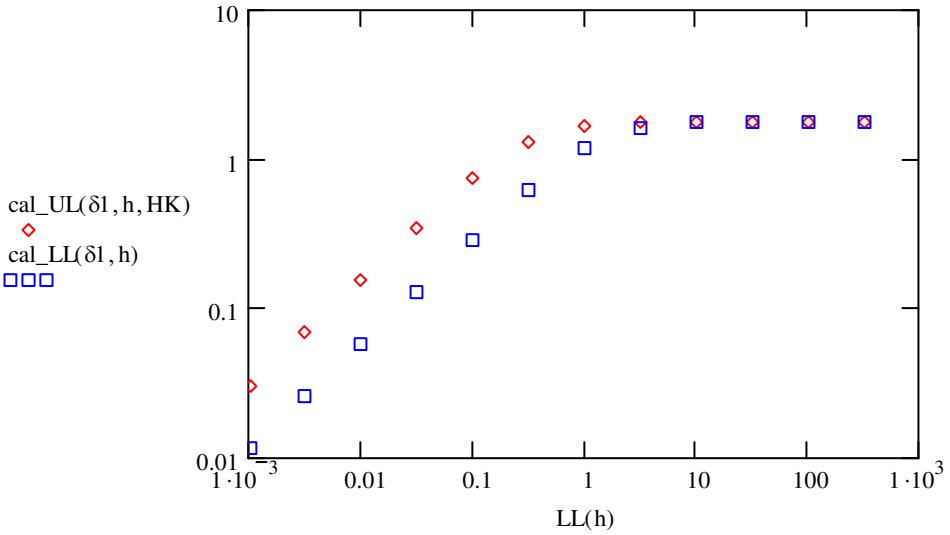


Figure B.15 Comparison between *cal_UL(δ1,h,HK)* and *cal_LL(δ1,h)*. At lower values of *LL(h)* [*LL(h)*<1], *cal_UL(δ1,h,HK)* is significantly higher than *cal_LL(δ,h)*. At higher values of *LL(h)* [*LL(h)*>10], *cal_UL(δ1,h,HK)* approaches *cal_LL(δ1,h)* very closely, which gives rise to error in *cal_UL(δ1,h,HK)*-*cal_LL(δ1,h)*.

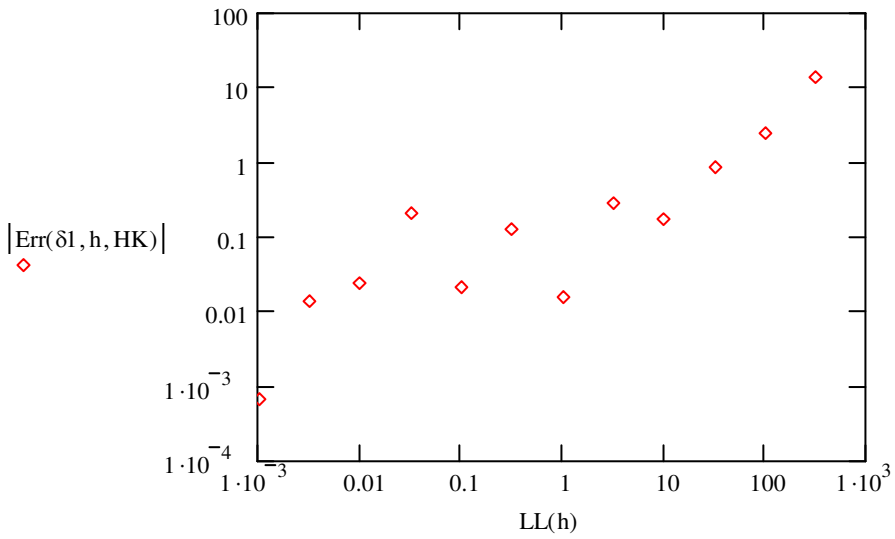


Figure B.16 The error between the calculated and the actual integral shows lower values at lower *LL(h)*. The error increases at higher values of *LL(h)* where *cal_UL(δ1,h,HK)* approaches *cal_LL(δ1,h)*.

To overcome this problem of increase in error beyond LL>10, the integral is evaluated in the higher *LL(h)* region based on the following observations. It has been observed that the actual integral beyond *LL(h)*=10 rolls off with a slope of 1-δ'. Furthermore, for U_{HK} > 450 and *LL(h)*>10, the upper limit of the integral UL(=U_{HK} x *LL*) becomes so large (>*4500*) that the integral $\int_0^{UL} \frac{u^{\delta'}}{1+u^2} du$ becomes saturated. Further increase in U_{HK} thus does not have any impact on $\int_0^{UL} \frac{u^{\delta'}}{1+u^2} du$, or the total integral for the high-k $\int_{LL}^{UL} \frac{u^{\delta'}}{1+u^2} du$ according to Eq. B.5.

The values for the integral are generated in this range of *LL(h)* (>10) for these two cases as discussed below. We have observed that *cal_Int(*δ1*,h,HK)* can calculate the integral values within an error of 1% up to *LL(h)*=10, beyond which the error increases with *LL(h)*. Therefore, we use *cal_Int(*δ1*,h,HK)* to evaluate the integral at *LL(h)* =10 for U_{HK} < 450 which is termed as *cal_base(*δ1*,h,h1,HK)*. Using this value as the *LL(h)*=10 intercept, the subsequent integral values are calculated as a function of *LL(h)* using the known slope of -1. The integral in this range is given by the function *eval_Int1(*δ1*,h,HK)*. For U_{HK} > 450, where U_{HK} does not have any effect on the integral beyond *LL(h)*=10, we generate the integral values as a function of δ denoted by *const(*δ1*)* and calculate the subsequent values from the known slope of δ' -1. To fine tune the values of *const(*δ1*)* another polynomial function *corr(*δ1*)* is used. The integral in this range is given by the function *eval_Int2(*δ1*,h,HK).*

Functions used for *LL(h)*>10 and U_{HK} <450:

We define, *LL(h1)*=10 (a fixed value) (B.27)

$$cal\_base(\delta 1,h,h1,HK) = \begin{cases} H\_func5(\delta 1,h1,HK) - low\_base(\delta 1,h1) & \text{if } 10 \le U_{HK} \times LL(h1) < 100 \\ H\_func6(\delta 1,h1,HK) - low\_base(\delta 1,h1) & \text{if } 100 \le U_{HK} \times s(h1) < 6300 \\ H\_func6\_lim(\delta 1,h1,HK) - low\_base(\delta 1,h1) & \text{if } 6300 \le U_{HK} \times s(h1) \end{cases}$$

$low\_base(\delta 1,h1)$ = $func5(\delta 1,h)$ evaluated at $LL(h)=s(h1)=10$

(B.28)

$H\_func5(\delta 1,h1,HK)$ = $H\_func5(\delta 1,h,HK)$ evaluated at $LL(h)=s(h1)=10$

(B.29)

$H\_func6(\delta 1,h1,HK)$ = $H\_func6(\delta 1,h,HK)$ evaluated at $LL(h)=s(h1)=10$

(B.30)

$H\_func6\_lim(\delta 1,h1,HK)$= $H\_func6\_lim(\delta 1,h,HK)$ evaluated at

$LL(h)=LL(h1)=10$ (B.31)

$$eval\_Int1(\delta 1,h,HK) = 10^{\log((cal\_base(\delta 1,h,h1,HK)))+slope(\delta 1)\log\left(\frac{LL(h)}{10}\right)} \quad \text{(B.32)}$$

where, $slope(\delta 1) = \delta 1 - 1$ (B.33)

Functions used for LL(h)>10 and V_{HK}>450:

$$func(h,\delta 1) = 10^{slope(\delta 1)\log(LL(h))} \quad \text{(B.34)}$$

$$const(\delta 1) = ac + bc\delta 1 + cc\delta 1^2 + dc\delta 1^3 + ec\delta 1^4 \quad \text{(B.35)}$$

$$corr(\delta 1) = ad + bd\delta 1 + cd\delta 1^2 + dd\delta 1^3 + ed\delta 1^4 \quad \text{(B.36)}$$

$eval\_Int2(\delta 1,h,HK)$ = $func(h,\delta 1)\ const(\delta 1)\ corr(\delta 1)$ (B.37)

Finally the compact expression for the integral in all cases considered above is given by:

$Cal\_Integral(\delta 1,h,HK)$ = $cal\_Int(\delta 1,h,HK)$ if $LL(h)<10$

$eval\_Int1(\delta 1,h,HK)$ if $LL(h)\geq 10$ and $U_{HK}<450$

$eval\_Int2(\delta 1,h,HK)$ if $LL(h)\geq 10$ and $U_{HK}>450$

The compact form is compared to the actual integral in Figures B.17, B.18 and B.19. Figures B.20, B.21 and B.22 compare *cal_UL(δ1,h,HK)* and *cal_LL(δ1,h)*. The error between the actual integrals and the compact form predictions are given in Figures B.23, B.24 and B.25.

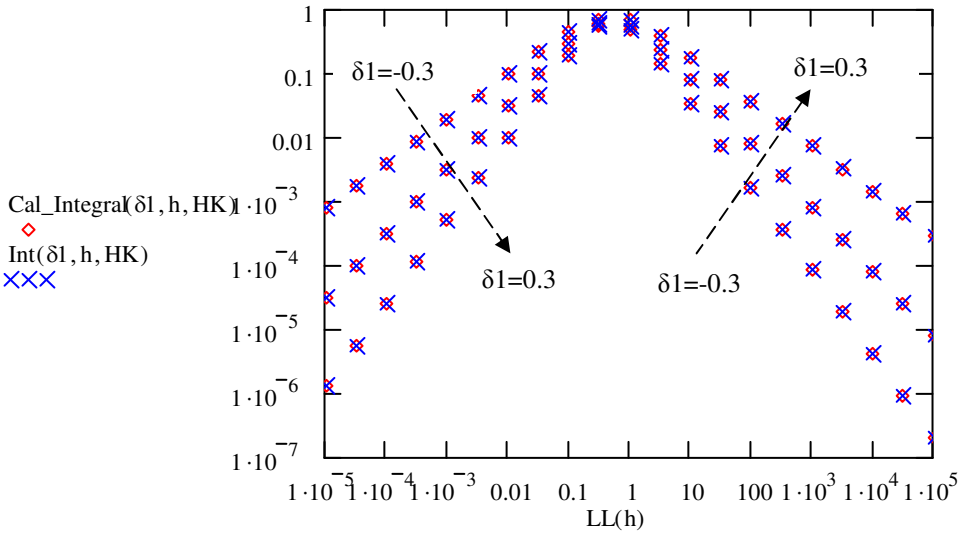


Figure B.17 Comparison between the actual integral *Int(δ1, h, HK)* and the final compact form *Cal_Integral(δ1,h,HK)* for high-k thickness of 0.7nm with γ_{HK} =0.2x10^{8} cm^{-1}. U_{HK} (=*exp*($\gamma_{HK}T_{HK}$))has a value of 4.05. Three different values of *δ1* (-0.3, 0 and 0.3) are used.

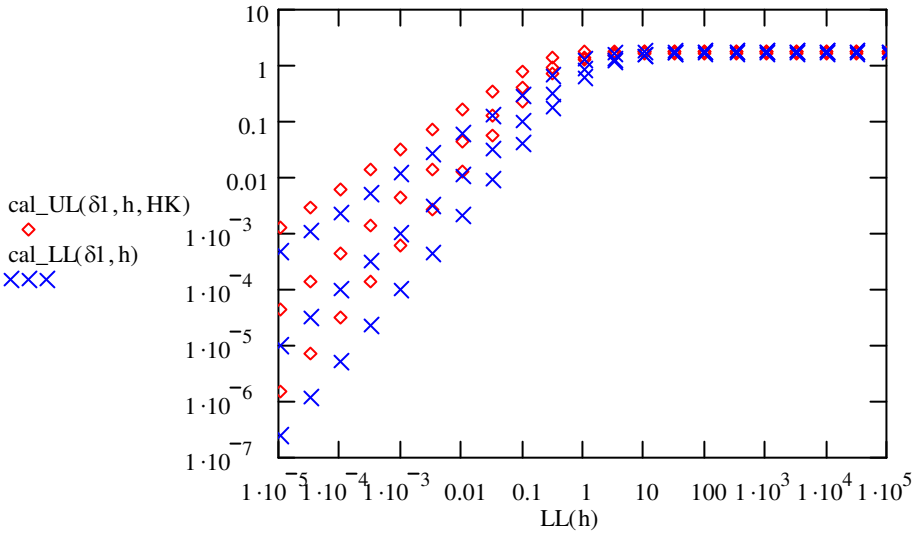


Figure B.18 Comparison between *cal_UL(δ1,h,HK)* and *cal_LL(δ1,h)*. *cal_UL(δ1,h,HK)* is close to *cal_LL(δ1,h)* due to a small U_{HK}=4.05. This explains why the integral values decreases at high end of *LL(h)* as well.

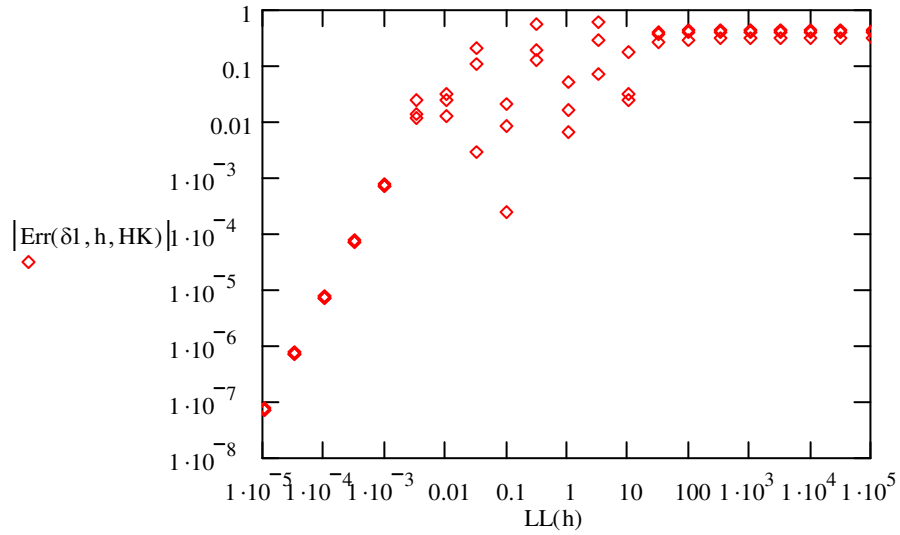


Figure B.19 The absolute error in the estimation of the compact form for small values of U_{HK} is illustrated here which is well within 1% of the actual integral.

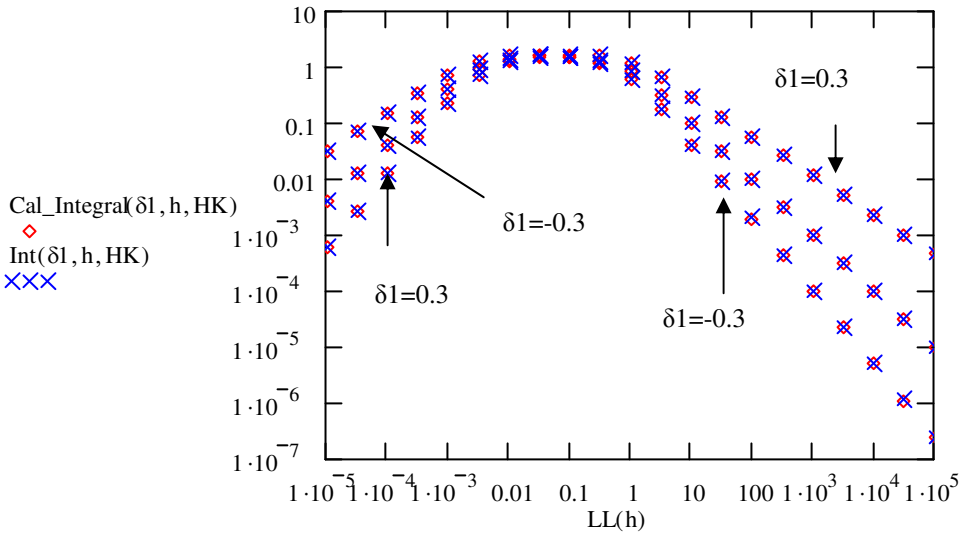


Figure B.20 Comparison between the actual integral *Int(*δ1*, h, HK)* and the final compact form *Cal_Integral(*δ1*,h,HK)* for high-k thickness of 3nm with γ_{HK} =0.2x10^{8} cm^{-1}. U_{HK} (=*exp*($\gamma_{HK}T_{HK}$)) has a value of 403.429. Three different values of δ1 (-0.3, 0 and 0.3) are used.

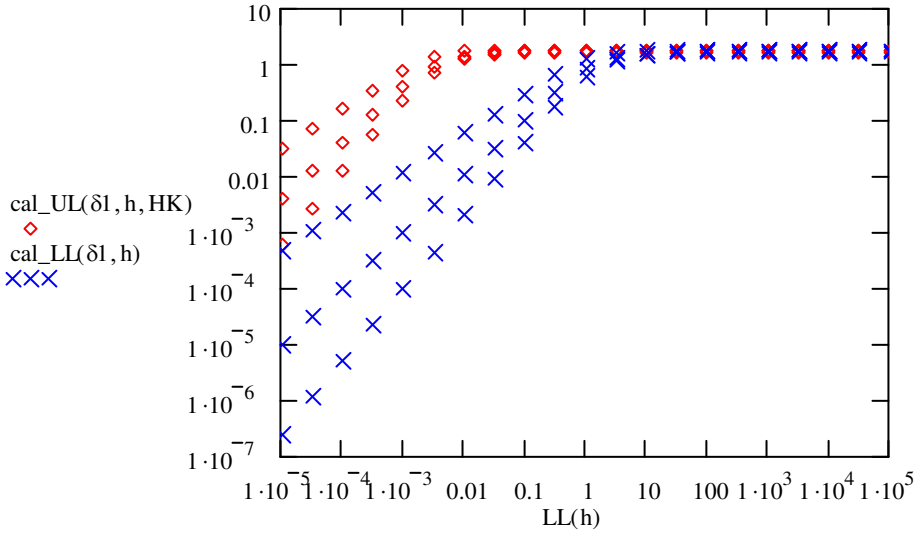


Figure B.21 Comparison between *cal_UL(*δ1*,h,HK)* and *cal_LL(*δ1*,h)*. *cal_UL(*δ1*,h,HK)* has a wider separation from *cal_LL(*δ1*,h)* due to a higher U_{HK}=403.429. As a result the pick in the integral values widens at the mid values of *LL(h)*.

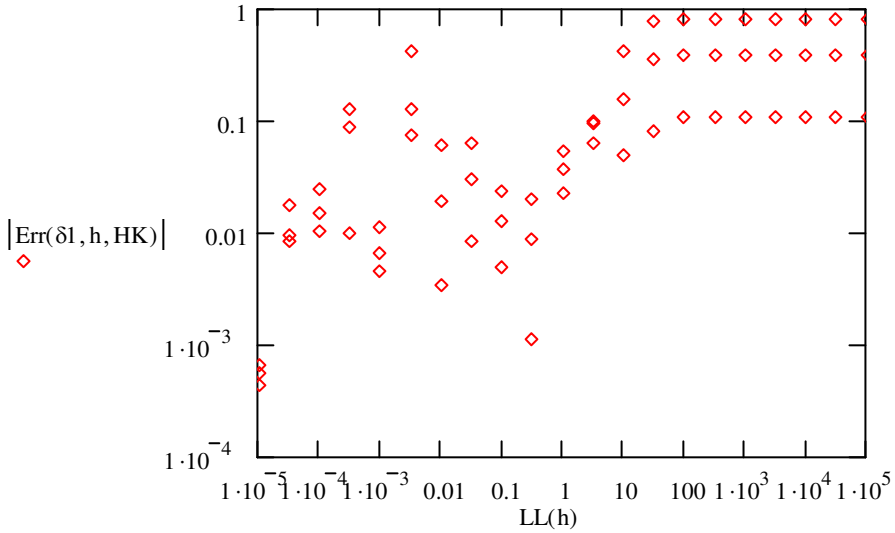


Figure B.22 The absolute error in the estimation of the compact form for moderate values of U_{HK} is illustrated here which is within 1% of the actual integral.

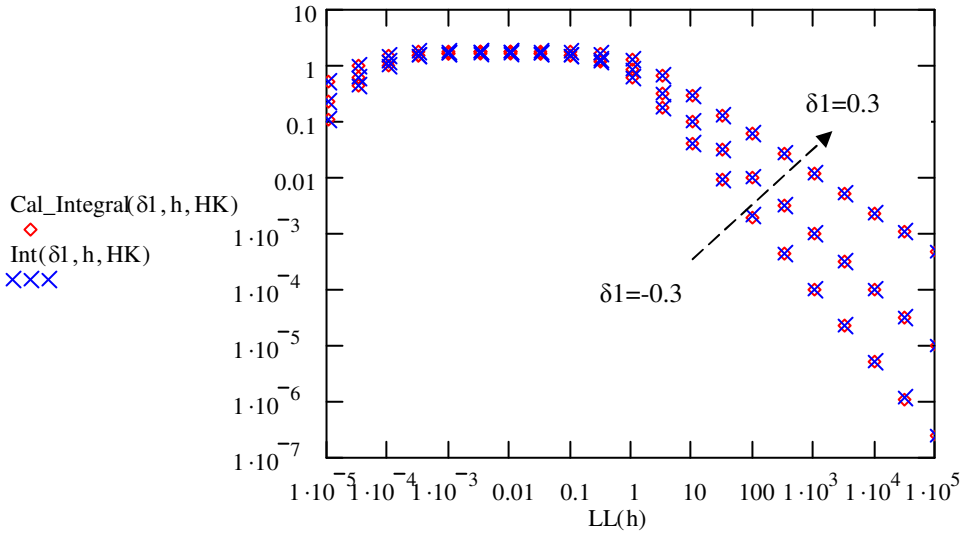


Figure B.23 Comparison between the actual integral *Int(δ1, h, HK)* and the final compact form *Cal_Integral*(*δ*1,*h*,*HK*) for high-k thickness of 5nm with γ_{HK} =0.2x10^8 cm^{-1}. U_{HK} (=$exp(\gamma_{HK})T_{HK}$) has a value of 2.203x10^4. Three different values of *δ*1 (0.3,0 and -0.3) are used.

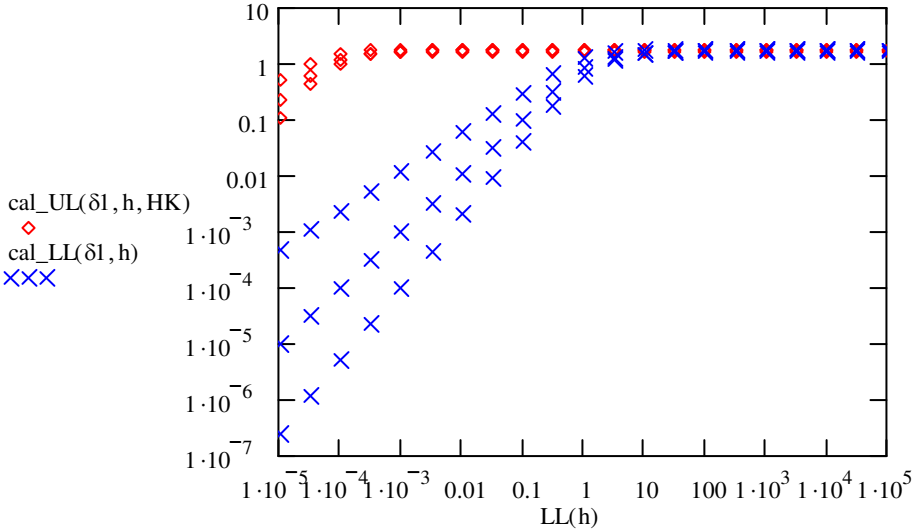


Figure B.24 Comparison between *cal_UL(δ1,h,HK)* and *cal_LL(δ1,h)*. *cal_UL(δ1,h,HK)* has a still wider separation from *cal_LL(δ1,h)* as U_{HK}=2.203x10^4. As a result the pick in the integral values further widens below the mid values of *LL(h)*.

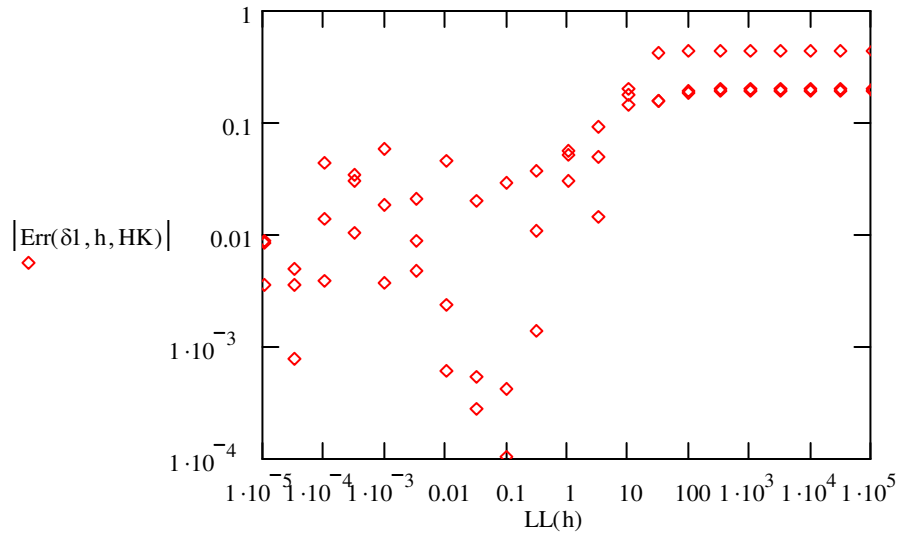


Figure B.25 The absolute error in the estimation of the compact form for higher values of U_{HK} is illustrated here. The error in case is still within 1% of the actual integral.

B.4 List of all the coefficients used in this work

The coefficients used in defining all the functions are listed in this section. The functions are categorized as appears in each region. Each coefficient name has two numbers. First number represents the function number, same as the region number, and appears also in each group in the first column. The second number signifies the coefficient number (*italicized*).

Table B1 Coefficients of the piecewise compact expressions

func2: list of co-efficients							
	1	2	3	4	5	6	Type
a2	0.990631	0.993914					Rational
b2	0.937227	-0.03748	-0.01482	-0.04912	0.353313		4th Order Polynomial
c2	1.001182	1.000393	0.002126	-0.00115	-0.02981	0.051413	5th Order Polynomial

func3: list of co-efficients							
	1	2	3	4	5	6	Type
a3	0.000175	-0.05597	0.237416	-0.50635	0.894246	-1.06559	5th Order Polynomial
b3	0.996464	-3.30581	4.782229	-4.18853	2.533656	-0.76142	5th Order Polynomial
c3	0.028957	6.582207	-15.1348	16.32367	-10.8668	2.550179	5th Order Polynomial
d3	-0.44732	-9.60891	28.47278	-35.3668	24.58974		4th Order Polynomial
e3	0.229087	9.878608	-31.9016	42.39337	-30.6174		4th Order Polynomial
f3	-0.00265	-5.8828	19.40628	-26.7562	19.7944		4th Order Polynomial
g3	-0.01929	1.481365	-4.89793	6.898379	-5.18499		4th Order Polynomial

func4: list of co-efficients							
	1	2	3	4	5		Type
a4	-0.15113	-1.08467	2.248277	0.515716	-20.7306		4th Order Polynomial
b4	0.818802	0.77518	1.725867	1.169509	-16.0894		4th Order Polynomial

c4	1.552768	-0.08737	1.653067	-0.31987	2.939761		4th Order Polynomial
d4	1.207738	-0.71601	0.641232	0.583059	-8.59915		4th Order Polynomial

func5: list of co-efficients							
	1	2	3	4	5	6	Type
a5	1.574887	-0.16206	1.359836	-1.0173	0.874898	-1.37038	5th Order Polynomial
b5	0.511924	-0.83727	0.075661	0.732455	-0.07534	-0.60364	5th Order Polynomial
c5	-0.0005	0.018281	0.063111	0.085259	0.052513	0.004906	5th Order Polynomial

func6: list of co-efficients							
	1	2	3	4	5	6	Type
a6	1.570838	-0.01542	1.840882	-0.28242	1.476943	-1.2425	5th Order Polynomial
b6	0.527276	-1.66433	-0.92114	4.348269	4.662585	-6.16009	5th Order Polynomial
c6	-0.00017	0.001103	0.006507	0.018697	0.037995	0.044935	5th Order Polynomial

const : list of co-efficients							
	ac	bc	cc	dc	ec		Type
	0.99774	0.980833	0.938258	0.916667	0.719697		4th Order Polynomial

const : list of co-efficients							
	ad	bd	cd	dd	ed		Type
	1.000333	0.013972	0.0275	0.061111	0.166667		4th Order Polynomial

B.5 Conclusions

The compact form of the integrals appearing in the MSUN final expression for S_{I_d} as shown in Eq. B.1, has been successfully obtained for the expected MOSFET dimensions and operating frequency range. The compact form is able to predict the actual integral for an interfacial layer of SiO_2 in the range of 0.8nm to 1.8nm. The high-k thickness range is from 0.7nm to 5nm with a tunneling coefficient of γ_{HK} within the

range of $0.2x10^{8}$ cm^{-1} to $1x10^{8}$ cm^{-1}. The noise frequency range is 1Hz to 1000Hz. The actual capability of the compact form is well above the specified range of operations. It has been demonstrated that the accuracy for this range is within 1% of the actual integral. As noise measurement is a statistical estimation of many data points, it can result in values varying somewhat from time to time on the same device at similar experimental conditions. The specified accuracy for the resultant compact model is well below this variation.

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BIOGRAPHICAL INFORMATION

Tanvir Hasan Morshed was born in Khulna, Bangladesh. He received his B.Sc. (1997) and M.Sc. (1999) degrees in Applied Physics and Electronics, from the University of Dhaka, Bangladesh. He completed the Masters degree in Electrical Engineering from the University of Texas at Arlington, USA, in December 2002. He pursued the Ph.D. degree in Electrical Engineering in December 2007, from the University of Texas at Arlington, USA.

His dissertation focused on measurement and modeling of 1/f noise in high-κ gate dielectric MOSFETs. He is interested in continuing research in device characterization and modeling.