DIFFUSION-FREE BACK CONTACT SOLAR CELLS ON S-PASSIVATED SI(100) SUBSTRATES

by

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ABSTRACT

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A diffusion-free back contact solar cell is proposed in this work. The textured front-side of this cell is coated with ~100 nm thermal SiO_2 to enhance the light trapping meanwhile reduce the surface recombination velocity (SRV). The back-side of this cell is finger-patterned, using a diffusion-free junction as its emitter region and Al-Si alloy as its base contact. The diffusion-free junction is made by a Schottky contact between low work-function metal aluminum (Al) and sulfur (S)-passivated p-type Si(100) surface.

Solution-based S passivation is one of the experimental realizations of the "valence-mending concept". Previously developed MBE (molecular bean epitaxy) selenium (Se) passivation is not used due to its time-consuming process and high energy input. Following the concept, passivation of Si(100) surface by Group VI

elements such as S and Se terminates the dangling bonds and releases the strained bonds and dimer bonds, thus significantly reduces the surface states. Quantification of surface states or interface states is introduced through the nano-CMOS devices. Removal of surface states enables an almost ideal barrier height after metal contact. This is one of the methods achieving the high Schottky barrier.

Al on S-passivated p-type Si(100) surface yields an extremely high Schottky barrier of 1.1 eV, about 0.2 eV higher than the corresponding ideal barrier height. This discrepancy is accounted by S-Si dipole moment on the surface. Calculations using Fermi statistics discloses that the barrier height of 1.1 eV causes the degenerate inversion on Si surface, making this Schottky junction electrically behave like a diffused p-n junction. Eventually this junction as a field-induced junction free of any diffusion is integrated in the fabrication of the proposed back contact solar cells. High work-function metal Platinum (Pt) and nickel (Ni) on S-passivated n-type Si(100) are also investigated, but the yielding barrier heights are not high enough to create degenerate inversion on Si surface.

Due to many limiting factors such as surface passivation quality, SRV, bulk minority-carrier lifetime, etc., for the fabricated solar cells, the measured low conversion efficiency (η) of ~1% should be a reasonable value. The future work is proposed to further improve the cells performance.

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CHAPTER 1

INTRODUCTION

1.1 Fossil fuels

Current global energy consumption is about 13 TW [1-3]. Over 80% of it comes from the combustion of fossil fuels, which are oil, coal, and natural gas. The renewable energy consumption accounts only 2%, almost 40 times less than the fossil fuels. This is illustrated in Figure1.1. With continuing depletion of fossil fuels and their price considerably rising in the future, the other energy sources supposed to be renewable will be brought more attention to the future energy supply.

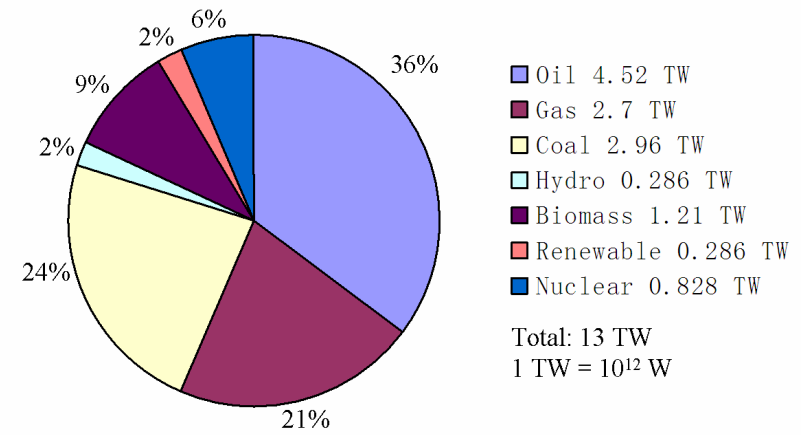


Figure 1.1 Mean global energy consumption, 1998. Data reproduced from Lewis [3].

From the environmental point of view, the combustion of fossil fuels releases a large amount of CO_2, one of the greenhouse gases, into the atmosphere. Today, about 2×10^{13} kg of CO_2 is released every year mainly by burning of fossil fuels [4-6]. The

concentration of CO_2 in the atmosphere has increased from a pre-industrial level of ~280 ppm to present ~360 ppm [6-8] (ppm = parts per million). The concentration of CO_2 above 450 ppm will cause major climatic changes. With current consumption rate of the fossil fuels and assuming the fossil fuels are only energy sources for future increase of global energy demand, the concentration of CO_2 will climb to a dangerous level of 750 ppm by 2050 [3]. At this level, the planet earth could very quickly become a less habitable place to live. Hence the carbon-free clean energy sources need to play a more important role than fossil fuels in the future energy supply. And these energy sources would also be sufficient and affordable in the future like fossil fuels at present.

1.2 Renewable energy sources

By 2050, the global energy demand will hit ~30 TW [3,9]. Renewable energy sources such as wind, tides, biomass, and geothermal heat, etc, can only sustain fractions of this demand because the maximum power supplied by each of them is limited, less than 5 TW [1-3]. In comparison with above energy sources, the solar energy is sufficient enough because the incident solar power on the earth is at a level of 10^5 TW and the estimated exploitable solar power can be 600 TW, which itself can sustain decades of global energy supply. This indicates that the solar energy might be an only candidate to meet the future fast-growing energy demand.

1.3 Perspective of solar energy

At present, the PV (photovoltaic) industry has grown into a multi-billion dollar business. The solar power provided by the PV industry has surpassed 1 GW since 2004 and is expected to reach 3 GW by 2010. The market has been growing at a double-digit

rate of 20-40% annually over recent years [10]. However, the price of PV modules still remains high in last few years, about $4.0-4.8/Wp (watt peak) [10,11]. The PV industry is now still struggling with improving conversion efficiency and decreasing the price of commercial PV modules.

1.4 Bulk Si-based PV modules

Current PV modules are dominated by the bulk silicon (Si)-based modules including mono-crystalline modules and multi-crystalline modules, which comprise approximately 85% of all worldwide PV modules market. Despite the possible lower cost of emerging modules based on thin-film technologies [12-15] (less material, higher theoretical efficiency), the bulk Si-based modules will still dominate the PV industry for at least the next 15 years due to their higher conversion efficiency and greater durability [14].

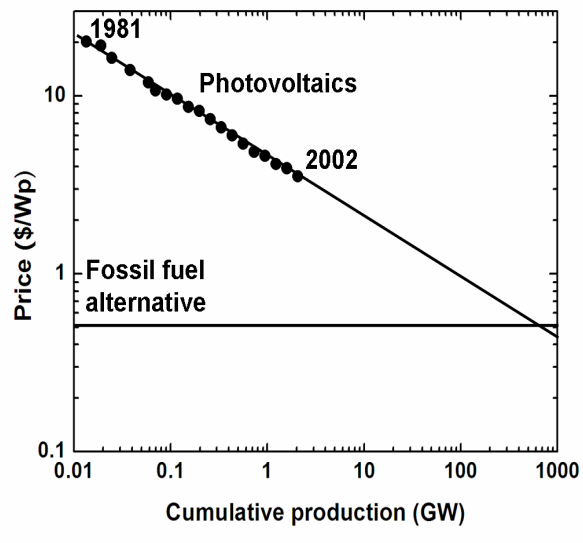


Figure 1.2 The learning curve of bulk Si-based photovoltaic. Data reproduced from Green [16].

Figure 1.2 shows the learning curve of bulk-Si based photovoltaic. This curve demonstrates a 20% reduction of module price with every doubling in accumulated volume production. If the same growth rate is maintained, a further increase of the cumulative production by a factor of 100 will lead to cost equality with fossil fuels. This means that the PV manufactures would be able to generate electricity cheaper than any other options [16].

1.5 Materials issue for bulk Si-based PV modules

Major concern for bulk Si-based PV modules (mono-, multi-, and small portion of ribbons [17,18]) is the availability of good quality feedstock materials and, consequently, cheap Si substrates. The thinner substrate or the less material used for solar cell design can further decrease the modules price. The optimum thickness of thin substrate has to comply with two aspects, one-without scarifying much conversion efficiency and the other-without causing wafer warping after high temperature treatments [19,20].

Using thin Si substrates with high quality opens another route to make highly-efficient back contact solar cells if the lifetime (τ) or diffusion length of the minority carriers can go extremely high, for example $\tau > 1$ms for Sunpower's cells. The only drawback of the back contact solar cells is the cost accumulation due to the complication of the fabrication process and the required high quality Si substrate. Besides these, the back-contact solar cells possess some unique advantages in comparison with the conventional (front junction) solar cells. These will be presented in Chapter 2, the structures of back contact solar cells.

CHAPTER 2

STRUCTURES OF BACK CONTACT SOLAR CELLS

A basic design concept of the solar cells is introduced through a typical structure of the conventional solar cells. With this understanding, three historical types of structures of back contact solar cells are demonstrated. The difference between the conventional solar cells and the back contact solar cells is how to position the metal contacts for the emitter region and the back-surface field (BSF), which are usually formed by diffusion processes involving the high energy input.

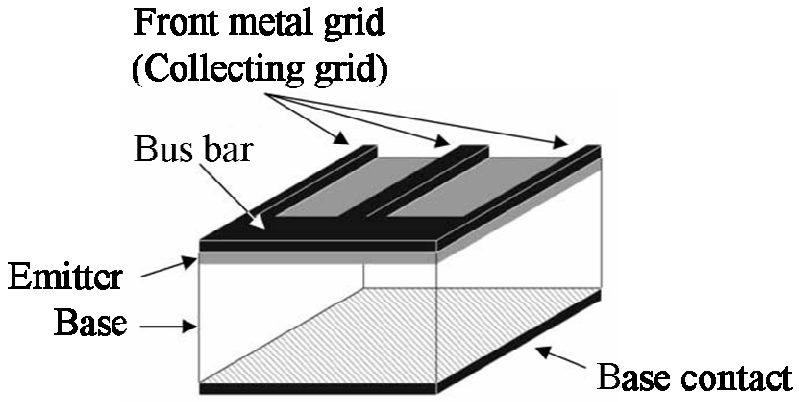


Figure 2.1 A typical structure of the conventional solar cells. Figure reproduced from Kerschaver [21].

2.1 A typical structure of the conventional solar cells

Figure 2.1 shows a typical structure of the conventional solar cells. The Si base is the main part of the mechanical structure. The emitter is a region with diffused p-n junction, located near the front surface. The metal grid on the emitter region is to

effectively collect the minority carriers generated from the junction and the base region. The design of the metal grid is a trade-off between optical losses by high shading area and resistive losses by low metal covering. The busbars are relatively wide and are used as solder pads for external connection. The rear surface has a highly doped back-surface field (n^+-n or p^+-p junction), which is fully covered by metals to reduce the contact resistance. The back-surface field is not only to form an ohmic contact on the back but also decrease the surface recombination velocity (SRV), thus reducing the loss of minority carriers at the rear surface.

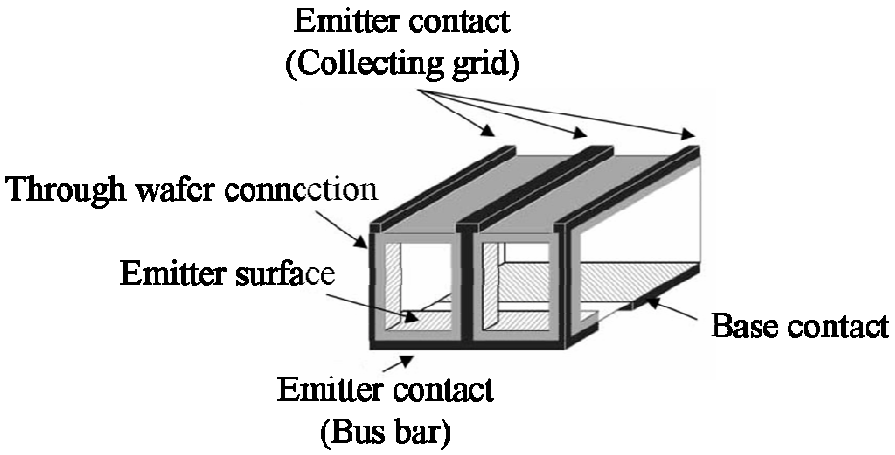


Figure 2.2 Metallization wrap-through solar cell structure. Figure reproduced from Kerschaver [21].

2.2 The structures of back contact solar cells

2.2.1. Metallization wrap-through (MWT) solar cell structure [22,23]

The concept of metallization wrap-through (MWT) structure is most closely linked to the conventional solar cell structure. In these cells, the emitter is still located near the front surface with metal grid covered, but the wide busbars are moved from the

front surface to the rear surface, which is shown in Figure 2.2. The metal grid on the front surface is connected through a number of openings in the substrate to the busbars. By doing this, the shading area on the front surface can be significantly reduced, causing low optical losses.

2.2.2. Emitter wrap-through (MWT) solar cell structure [24-26]

Unlike metallization wrap-through structure, the emitter wrap-through (EWT) structure has the front surface free of any metallization. The emitter contact grid and base contact grid are separately patterned on the rear surface. The emitter near the front surface is still connected by a number of openings in the substrate.

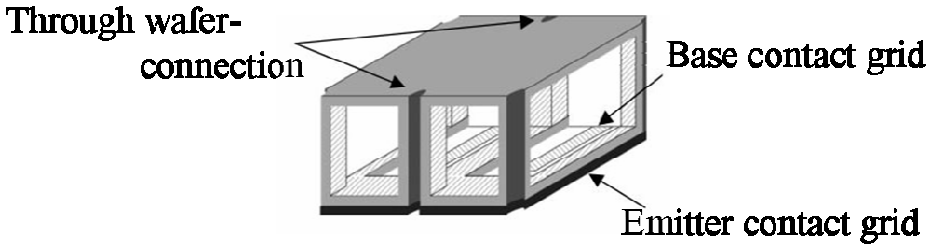


Figure 2.3 Emitter wrap-through solar cell structure. Figure reproduced from Kerschaver [21].

The openings mentioned in both MWT and EWT cell structures have a diffused p-n junction wall, serving as part of the emitter region. The inner side of these openings is filled with annealed metal paste. Because of this, the generated carriers can be easily separated by internal built-in potential and collected by metal contacts. The bulk minority-carrier lifetime is not an issue here for both designs.

2.2.3. Back junction solar cell structure [27-30]

For the back junction cell structure, the emitter is no longer located near the front surface. The emitter together with the back-surface field is placed on the rear surface, as shown in Figure 2.4. This design requires a high quality Si substrate with bulk minority-carrier lifetime as high as possible, > 1 ms for Sunpower's back contact solar cell. For Sunpower's solar cell, its conversion efficiency has been achieved above 20%, but its production cost is accumulated by using high quality Si substrate. Moreover, the diffused junctions used in its cell design need a high energy input.

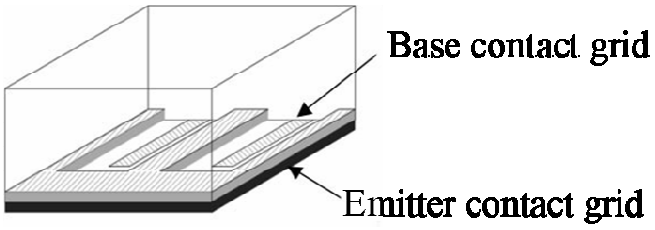


Figure 2.4 Back junction solar cell structure. Figure reproduced from Kerschaver [21].

2.2.4. The proposed diffusion-free back contact solar cell

The proposed diffusion-free back-contact solar cell is similar to the back junction solar cell where the diffused p-n junction is replaced by the Schottky junction free of any diffusion. This Schottky junction is field-induced by extremely high Schottky barrier of 1.1 eV between cheap metal Al and low cost wet-chemically sulfur (S)-passivated p-type Si(100) surface [31]. The barrier height of 1.1 eV causes the degenerate inversion on Si surface, making this type of Schottky junction electrically

behave like a p-n junction. The attempt of this work is to design and test this new cell structure and then come up with the strategies to improve the conversion efficiency that will be mentioned in the future work (see Chapter 8.5).

2.2.5. Advantages of back contact solar cells [32]

In comparison with the conventional solar cells, the back contact solar cells possess some unique advantages listed as below.

1. No shading of the illuminated surface (front surface) since there is no metal grid or contact structure on the illuminated surface.
2. The metal contacts, all of which are on the rear surface, may cover nearly the entire surface and may be made as thick as desired. This means that the series resistance of the contacts may be as small as desired.
3. The current flows normal to the surface in the junction regions, rather than parallel to the surface as in a conventional solar cell. That means the sheet resistance of junction regions is no longer a constraint and the voltage drop in these regions is negligible.

CHAPTER 3

PRINCPLES OF SCHOTTKY DIODES AND SOLAR CELLS

The most important parts of this work are focused on Schottky diodes and solar cells. Researching Schottky diodes is to find a way to achieve extremely high Schottky barrier, which can cause degenerate inversion on Si surface, making this Schottky junction electrically behave like a diffused p-n junction that is eventually integrated in the fabrication of the proposed back contact solar cell. Attempts have been done on both n-type Si substrate and p-type Si substrate. Therefore, the principles of Schottky diodes and solar cells are briefly reviewed in this chapter as far as these are helpful to understand the mechanisms of these two devices.

3.1 Principles of Schottky diodes [33]

3.1.1. Ideal Schottky contacts

Schottky diodes are made from the contact between metal and semiconductor. When a metal contacts with a semiconductor, a barrier will be formed at the metal-semiconductor interface. Ideally, the barrier is determined by the metal work-function and the electron affinity of the semiconductor in accordance with Mott-Schottky theory. The metal work-function $q\phi_m$ is the energy difference between the vacuum level and Fermi level, and the electron affinity of the semiconductor $q\chi$ is measured from the bottom of the conductance band E_C to the vacuum level. They are denoted in Figure 3.1 (a) and 3.2 (a) where the metal and semiconductor are separated.

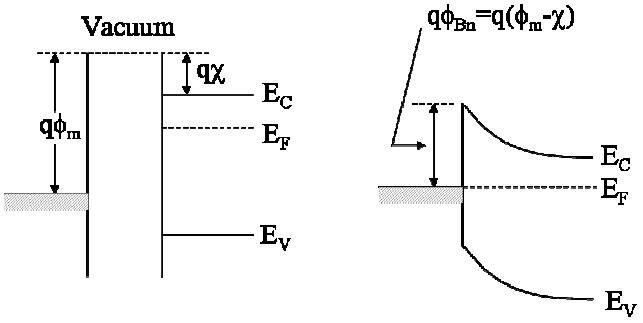
For the contact between metal and *n*-type semiconductor shown in Figure 3.1 (b), the barrier is given by

$$q\phi_{Bn} = q(\phi_m - \chi) \tag{3. 1}$$

For the contact between metal and *p*-type semiconductor shown in Figure 3.2 (b), the barrier is given by

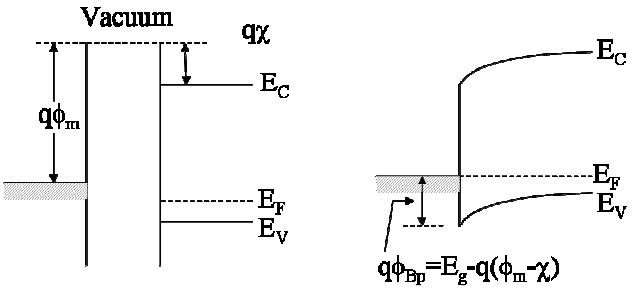
$$q\phi_{Bp} = E_g - q(\phi_m - \chi) \tag{3. 2}$$

where the E_g is the band gap of the semiconductor.



(a) (b)

Figure 3.1 Energy-band diagrams of metal on a n-type semiconductor, (a) no contact and (b) after contact.



(a) (b)

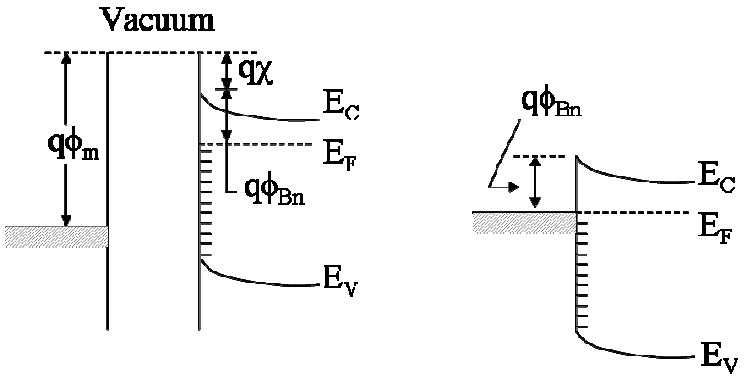
Figure 3.2 Energy-band diagrams of metal on a p-type semiconductor, (a) no contact and (b) after contact.

3.1.2. Surface states

Semiconductor surface property is much different from its bulk. The surface is a discontinuity of its bulk lattice, possessing a large amount of defects contributing to the surface states [34]. The surface states pin Fermi level, causing a surface potential even without a metal contact. This is illustrated in Figure 3.3 (a) for a n-type semiconductor. After metal contact, the ideal barrier height is adjusted by D_{it}, the density of interface traps originated from the surface states. This is empirically expressed by Equation 3.3,

$$q\phi_{Bn} = q(\phi_m - \chi) - \delta(D_{it}) \qquad (3.3)$$

where δ is the adjustment of the ideal barrier height by the density of interface traps. One of the methods quantifying the D_{it} is introduced in Chapter 5. The point here is that the existence of surface states makes ideal barrier height deviating from the Mott-Schottky theory.



(a) (b)

Figure 3.3 Energy-band diagrams of metal on a n-type semiconductor with surface states, (a) no contact and (b) after contact.

3.1.3. Determination of Schottky barrier

3.1.3.1 Capacitance-voltage measurement

Metal-semiconductor contact under a non-equilibrium condition, external voltage applied, the boundary condition of the Poisson equation is changed to give another solution of space charge Q_{sc} as below

$$Q_{sc} = \sqrt{2q\varepsilon_s N_D (V_{bi} - V - \frac{kT}{q})} \qquad \text{C/cm}^2 \qquad (3.4)$$

where q is electron's charge, ε_s is semiconductor permittivity, N_D is donor impurity density for a n-type semiconductor, V_{bi} is the built-in potential, k is Boltzmann constant, and T is absolute temperature.

The differential of space charge to voltage gives the depletion layer capacitance C per unit area, which is given by

$$C = \frac{|\partial Q_{sc}|}{\partial V} = \sqrt{\frac{q\varepsilon_s N_D}{2(V_{bi} - V - \frac{kT}{q})}} \qquad \text{F/cm}^2 \qquad (3.5)$$

Equation 3.5 can be rewritten in the form of

$$\frac{1}{C^2} = \frac{2(V_{bi} - V - kT/q)}{q\varepsilon_s N_D} \qquad (3.6)$$

Plotting of $1/C^2$ versus V yields a straight line, by which the intercept on the voltage axis is the built-in potential V_{bi} (or ϕ_s surface potential or band-bending, in another name) and the slope is used to calculate the donor impurity density N_D. With the extracted donor impurity density, the difference between conduction band E_C and Fermi level E_F is determined. The barrier height is the sum of the built-in potential V_{bi} and the

difference between E_C and E_F if the small amount of kT/q is neglected. The same criteria can be used to determine the barrier height for a metal on a p-type semiconductor where the difference between E_F and valance band E_V needs to be determined by the extracted acceptor impurity density N_A from $1/C^2$-V characteristics.

3.1.3.2 Current-voltage measurement

The current transport in metal-semiconductor contacts is mainly due to majority carriers, in contrast to p-n junctions where the minority carriers are responsible. This current transport characteristic can be explained by thermionic emission theory. It assumes that the transport of the electrons from the semiconductor to the metal is from the electrons over the potential barrier (V_{bi}), which is shown in Figure 3.4, the first transportation process, and the electron transport from metal to semiconductor has to overcome the Schottky barrier (ϕ_{Bn} for n-type).

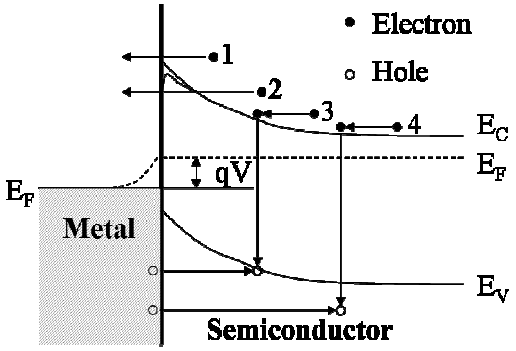


Figure 3.4 Four basic transport processes under forward bias for a n-type semiconductor. 1: Thermionic emission, 2: Tunneling, 3: Recombination in space-charge region, 4: Hole injection from the metal to the semiconductor.

The current density from semiconductor to metal is given by

$$J_{s\to m} = A^* T^2 \exp(\frac{-q\phi_{Bn}}{kT}) \exp(\frac{qV}{kT}) \qquad (3.7)$$

The current density from metal to semiconductor is given by

$$J_{m\to s} = -A^* T^2 \exp(\frac{-q\phi_{Bn}}{kT}) \tag{3. 8}$$

The total current density is

$$J = A^* T^2 \exp(\frac{-q\phi_{Bn}}{kT})[\exp(\frac{qV}{kT}) - 1] = J_s[\exp(\frac{qV}{kT}) - 1] \tag{3. 9}$$

where J_s or $A^*T^2\exp(-q\phi_{Bn}/kT)$ is the saturation current density. The A^* in Equation 3.7, 3.8, and 3.9 is Richardson constant. In the field range of 10^4-2×10^5 V/cm, A^* remains essentially at a constant value of ~110 A/cm^2/K^2 for electrons and ~30 A/cm^2/K^2 for holes. These values are used for fitting of current-voltage curves shown in Chapter 6 (p-type Schottky diodes) and Chapter 7 (n-type Schottky diodes) to extract the barrier height.

For a heavily doped semiconductor or for operation at low temperatures, the tunneling current may become the dominant transport process. Because of this, the expression for $J_{s\to m}$ as shown in Equation 3.7 and $J_{m\to s}$ as shown in Equation 3.8 have to be modified. Together with considering the series resistance R_s and the contact area S, Equation 3.9 can be rewritten as

$$I = A^* S T^2 \exp(\frac{-q\phi_{Bn}}{kT})\left\{\exp[\frac{q(V - IR_s)}{nkT}] - 1\right\} \tag{3. 10}$$

where I is total current and n is ideality factor defined as

$$n = \frac{q}{kT}\frac{\partial V}{\partial(\ln J)} \tag{3. 11}$$

The ideality factor, n, is very close to unity at low dopings and high temperatures.

3.1.3.3 Activation energy measurement

The principal advantage of Schottky barrier determination by means of activation energy measurement is that no assumption of electrically active area is required. This feature is particularly important in the investigation of novel or unusual metal-semiconductor interfaces.

If Equation 3.9 is multiplied by S_e, the electrically active area, and the forward current I_F is considered, the following equation can be obtained

$$In(\frac{I_F}{T^2}) = In(S_e A^*) - \frac{q(\phi_{Bn} - V_F)}{kT} \qquad (3.\ 12)$$

where V_F is the applied forward voltage and $q(\phi_{Bn}-V_F)$ is the activation energy. Over a limited range of temperature (e.g., 273 K < T < 373 K), the value of A^* and ϕ_{Bn} are essentially temperature-independent. Thus for a given forward bias V_F, the slope of a plot of In (I_F/T^2) versus 1/T yields the barrier height ϕ_{Bn}.

3.2 Principles of solar cells [33]

Solar cells are devices, where solar radiation is directly converted into electricity. The conversion process is based on the photovoltaic (PV) effect which was first observed by Becquerel in 1839 [35]. Figure 3.5 shows a schematic cross-section of a conventional solar cell, and its energy-band diagram in the emitter region is shown in Figure 3.6 (a). Figure 3.6 (b) shows the energy-band diagram for a solar cell with its emitter region based on the Schottky junction. The mechanism of carriers' generation and separation for both cells is same except for the junction type.

Under irradiation, a photon with energy less than E_g, the band gap of the semiconductor, makes no contribution to cell power-output. A photon with energy greater than E_g contributes an energy E_g to cell output, the excess over E_g is wasted as heat. Most of the charge carriers are generated from the depletion region, and then separated by built-in electrical field and eventually collected by the corresponding metal contacts. A few portions of minority carriers generated from the base region can diffuse to the emitter collecting contacts if they are not recombined with holes in the bulk.

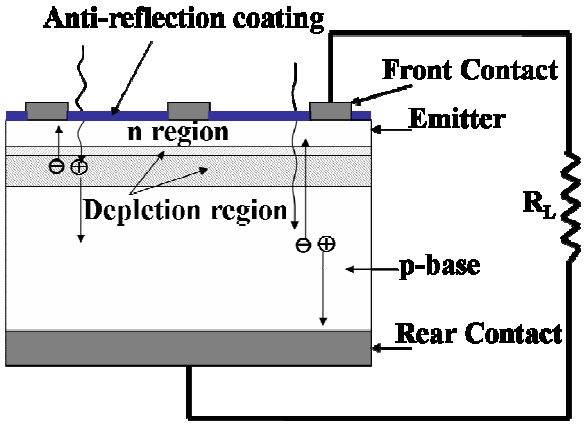
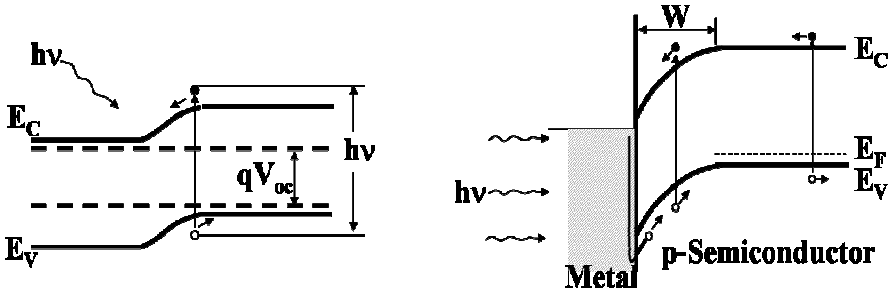


Figure 3.5 A schematic cross-section of a conventional solar cell.



(a) (b)

Figure 3.6 Energy-band diagrams of a solar cell using either a p-n junction (a) or a Schottky junction (b) as its emitter region under irradiation.

The idealized equivalent circuit of a solar cell is shown in Figure 3.7, where constant-current source is in parallel with the junction. The I-V characteristic of a solar cell is given by

$$I = I_s(e^{\frac{qV}{nkT}} - 1) - I_L \qquad (3.\ 13)$$

The photo current, $I_{L,}$ results from the excitation of excess carriers by solar radiation. I_s is the diode saturation current. It has different expression between p-n junction diodes and Schottky diodes.

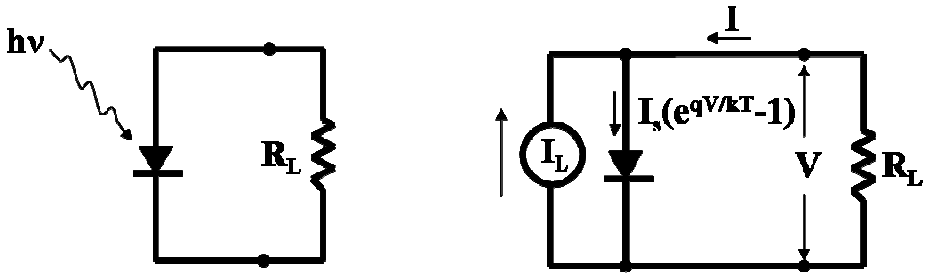


Figure 3.7 The idealized equivalent circuit of a solar cell.

3.2.1. Fundamental parameters of solar cells

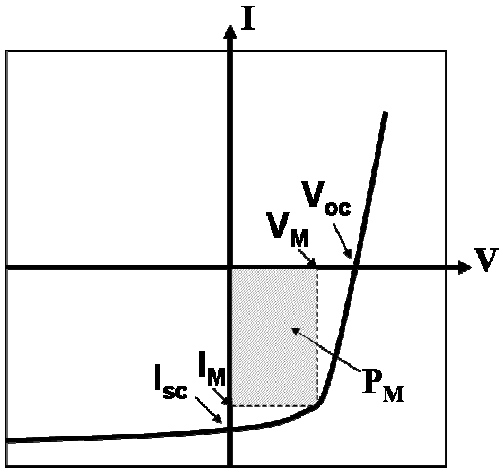


Figure 3.8 Current-voltage characteristic of a solar cell under irradiation.

The performance of a solar cell can be simply described using three parameters that are short circuit current I_{sc}, open circuit voltage V_{oc}, and fill factor FF. Figure 3.8 shows a typical current-voltage (I-V) characteristic of a solar cell under irradiation.

3.2.1.1 Short-circuit current I_{sc}

Ideally, the short-circuit current I_{sc} or the light-generated current I_L can be obtained from the integration of the solar spectrum with photon energy [36] shown in Equation 3.14,

$$I_L(E_g) = qA \int_{h\nu=E_g}^{\infty} (dn_{ph} / dh\nu) d(h\nu) \qquad (3.\ 14)$$

where q is electron's charge, A the active emitter area, $dn_{ph}/dh\nu$ corresponds to the solar spectrum, and $h\nu$ is the photo energy.

Experimentally, the short-circuit current is obtained when the load is at a short circuit (V_{out} =0). It is usually lower than the light-generated current due to the series resistance R_s, mainly resulting from the bulk resistance of the semiconductor, the possible resistive emitter region and the contact resistance from both the emitter and the base.

3.2.1.2 Open-circuit voltage V_{oc}

When the load is at an open circuit (I_{out} =0), the corresponding V_{out} is so called the open circuit voltage V_{oc}. In the ideal case, V_{oc} can be expressed by

$$V_{oc} = \frac{kT}{q} In(\frac{I_L}{I_s} + 1) \qquad (3.\ 15)$$

Hence for a given I_L, the open-circuit voltage increases logarithmically with decreasing saturation current I_s.

3.2.1.3 Fill factor FF

With reference to Figure 3.8, the fill factor FF is defined by

$$FF = \frac{V_M I_M}{V_{oc} I_{sc}} \tag{3.16}$$

where V_M and I_M are the voltage and current corresponding to the maximum output power P_M under illuminated I-V curve, which is the rectangular area shown in Figure 3.8. The fill factor could be extremely low in a practical cell assuming a high carrier recombination and the possible losses in series resistance and shunt resistance. The shunt resistance is originated from the current leakage across the junction [37].

3.2.2. Conversion efficiency η

The conversion efficiency η is technically defined by

$$\eta = \frac{I_M V_M}{P_{in}} = \frac{FF \cdot I_{sc} V_{oc}}{P_{in}} \tag{3. 17}$$

$$P_{in} = \int_0^\infty P(\lambda) d\lambda \tag{3. 18}$$

where P_{in} is the power of the incident light and $P(\lambda)$ is the solar power density at wavelength λ [38]. The conversion efficiency given by a real solar cell is usually much lower than the ideal one due to many factors causing efficiency losses.

The fundamental efficiency losses include the loss by long wavelength photons of the solar spectrum [39], loss by excess energy of the photons, voltage factor qV_{oc}/E_g

that is limited by unavoidable intrinsic Auger recombination [40], and the fill factor FF that is limited by the maximum value of 0.89 for an ideal solar cell.

The most common technological factors influencing the cell efficiency are loss by reflection, loss by metal coverage, loss by incomplete absorption, and the collection efficiency limited by recombination in the bulk and at the surfaces.

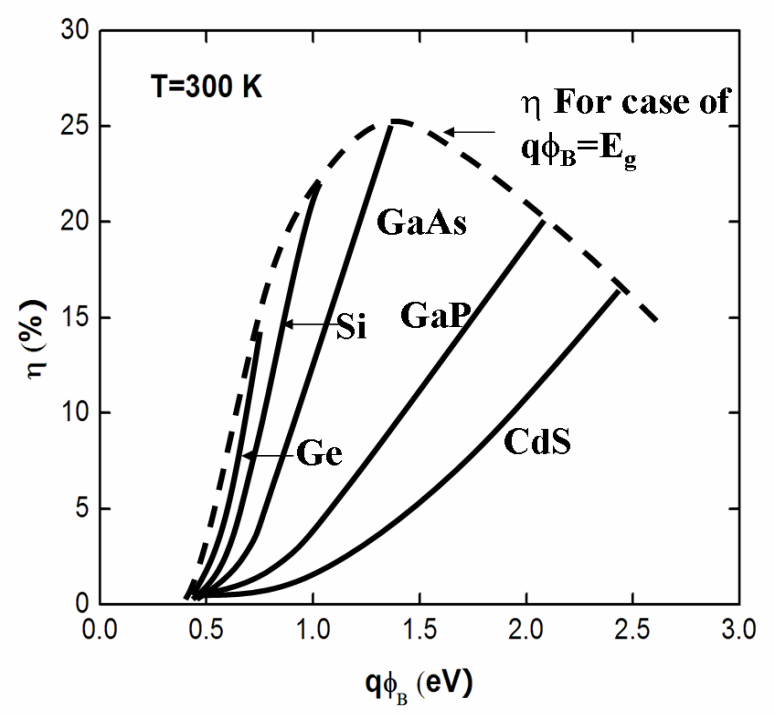


Figure 3.9 Conversion efficiency vs barrier height for the solar cells built on the Schottky junction. The envelope shows maximum efficiency calculated for $q\phi_B = E_g$. Data reproduced from Pulfrey and McOuat [41].

This work investigates a diffusion-free back contact solar cell, in which the diffusion-free junction is actually field-induced by an extremely high Schottky barrier. For this type of solar cell, despite the efficiency losses mentioned above the conversion efficiency is mainly dependent on the Schottky barrier height ϕ_B. The relationship

between them is depicted in Figure 3.9. For Si-based solar cells, the maximum efficiency is ~22% at $q\phi_B = E_g$ and it drops quickly with decreasing of the barrier height.

CHAPTER 4

SI(100) SURFACE PASSIVATION

4.1 Si(100) surface structure

Si surface is a discontinuity of its bulk lattice, full of a large amount of defects. Among them, the dangling bonds are the main contribution to the surface states. The surface states become the interface states after a foreign material is deposited on the surface. The density of interface states is related to the surface atomic density. For Si(100) surface, the surface atomic density is $6.78\times10^{14}/cm^2$. Because of this, the interface-state density is usually measured at a high level once the surface is not pre-treated by a passivation step. With the best passivation method using thermal SiO_2, it can be reduced to a low level of $\sim10^9$ ev^{-1}/cm^2. For nano-CMOS technology, due to down-scaling issues [42], the high-κ material has to replace SiO_2 as gate dielectric. This change will raise the interface-state density to a high level of $\sim10^{12}$ eV^{-1}/cm^2. Reduction of the interface-state density is demonstrated in Chapter 5 through nano-CMOS devices where the Si(100) surface is passivated by a monolayer of selenium (Se). For metal-semiconductor contacts (Schottky contacts), the interface states pin Fermi level, making the Schottky barrier more or less independent on the metal work function and electron affinity of the semiconductor. Is there any way to make Fermi level unpinned by the surface states or interface states? Before answering this, let's first look at the atomic structure of Si(100) surface.

Figure 4.1 shows the original atomic structure of Si(100) surface from (110) point of view. Each Si atom contributes two dangling bonds. This configuration possesses a very high surface energy, which can be reduced by experiencing a surface reconstruction. Figure 4.2 shows Si(100) configuration after reconstruction in ultrahigh vacuum. Surface reconstruction results in the reduction of dangling bonds and appearance of dimer bonds and strained bonds between neighboring atoms [43]. Both dimer bonds and strained bonds will again contribute comparative amount of surface states. Hydrogen (H) as passivation atom can only passivate dangling bonds and leaves dimer bonds and strained bonds unreleased because of its smaller atomic size than Si atom and the less bond strength once it bonds with Si. A new method using Group VI elements as passivation atom is given in next section.

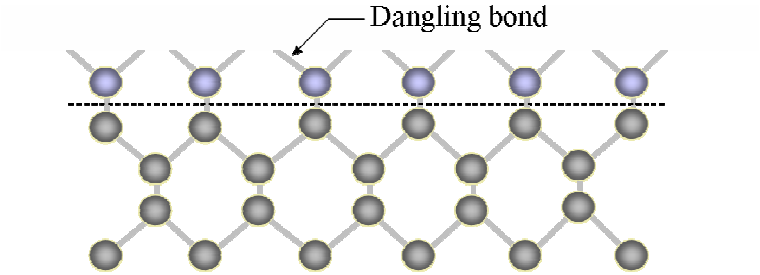


Figure 4.1 The original atomic structure of a clean Si (100) surface from (110) point of view.

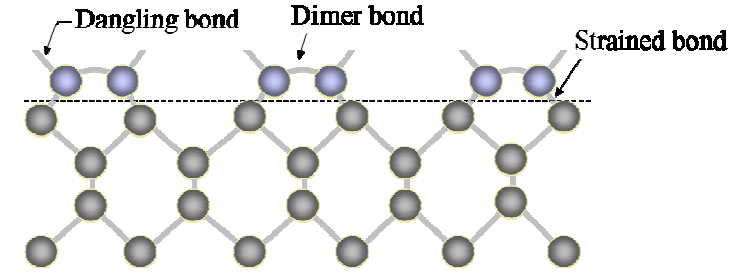


Figure 4.2 The atomic stricture of a clean Si(100) surface after reconstruction in ultrahigh vacuum [43] from (110) point of view.

4.2 "Valence-mending concept"

The idea of Si surface passivation by proper elements has been studied more than three decades. The most important aspect of the surface passivation is considering the valence difference between the surface atom and the foreign atom. In 1991, Kaxiras [44] proposed the "valence-mending concept" to passivate the Si (100) surface. As proposed, the most appropriate passivating elements on Si(100) surface would be Group VI element with six valence electrons such as oxygen (O), sulfur (S), selenium (Se), and terillium (Te). These elements tend to form structures with twofold coordination and sp^3 bonding hybrids, precisely a requirement for the restoration of a strained Si(100) surface. In this work, the element O is not selected because it can easily diffuse into Si to form SiO_2 in tenth of angstrom. This will deviate the monolayer passivation concept. Table 4.1 compares the covalent and atomic radius of Si with S, Se, and Te. Table 4.2 summarizes the bonding parameters of bulk phases of S/Se in comparison with that of the bulk Si(100) and the restored Si(100) by S/Se. Among these, Se is predicted to be the best candidate because it has basically same covalent and atomic radius comparing with Si. The bonding parameters between Se and Si also match Si lattice. The element Te is the worst candidate because its bond length is ~22% higher than Si (data not shown). Some of our fabricated CMOS devices also use Te passivation, but results from this type of devices are not shown. The focus of this chapter is on Se and S passivation.

Table 4.1 Covalent and atomic radius of Si and group VI elements.

	Si	Se	S	Te
Covalent Radius (Å)	1.17	1.17	1.04	1.37
Atomic Radius (Å)	1.18	1.16	1.06	1.42

Table 4.2 The bonding parameters of bulk phases of S/Se in comparison with that of the bulk Si(100) and restored Si (100) surface by S/Se.

	Bond length(Å)	Bond angle(degrees)
Monoclinic Se	2.34	105.5
Rhombohedral S	2.06	102.2
Diamond Si (100)	2.35	109.4
Restored Si (100):S	2.24	118.4
Restored Si (100):Se	2.34	110.2

Figure 4.3 shows the atomic structure of Si(100) surface after Se/S pasivation. Se/S passivation terminates the dangling bonds and relaxes the dimer bonds and strained bonds, resulting in a perfect bulk lattice termination on the surface. Because of this, the surface states are significantly reduced.

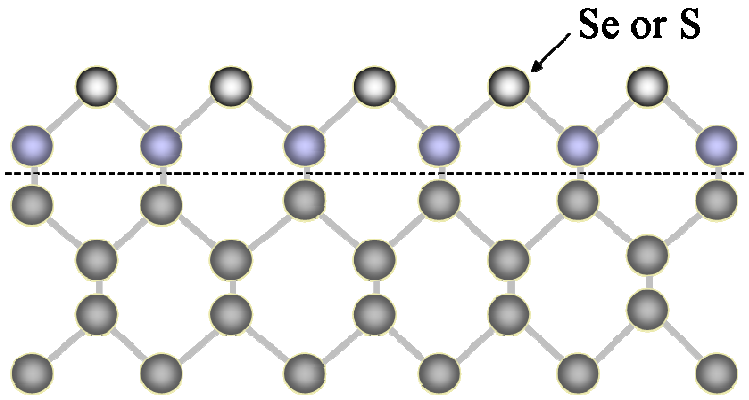


Figure 4.3 Atomic structure of the Si(100) surface after Se/S passivation.

Two passivation methods have been developed for Si(100) surface to realize this "valence-mending concept". One is MBE (molecular beam epitaxy) Se passivation performed in ultrahigh vacuum involving several high temperature steps [45], and the

other is wet-chemical S passivation performed in an aqueous solution [46]. The quality of S passivation is not good as Se passivation.

In reality, a clean passivated surface is unable to hold once the surface is exposed to the atmosphere due to the adsorbents that can further reduce the surface energy [47]. The oxygen can even penetrate the Se/S passivating layer and react with Si, causing somewhat of damages on the passivating layer. In order to maximize the benefits from Se/S-passivated surface, another needed layer should be in-situ grown on the passivated surface such as the high-κ gate dielectric for nano-CMOS devices and metal layer for Schottky diodes. It was found that even for an ex-situ grown layer, the interface also expresses better electrical performances than the control samples without Se/S passivation.

4.3 MBE Se passivation [45]

Se passivation is realized in a MBE system, by which a monolayer of Se is passivated on Si(100). The Si wafer is first rinsed in de-ionized (DI) water for 2 minutes and then immediately dipped into 2% hydrofluoride acid (HF) for 35 seconds to remove the native oxide. After this step, the Si(100) surface is actually hydrogen terminated. The wafer is subsequently dried by nitrogen (N_2) and loaded into the MBE transfer line, which will be pre-vacuumed to the base pressure. The base pressure of the MBE chamber is maintained at ultrahigh vacuum (~10^{-10} Torr). The Si wafer is first annealed at 600°C for 25 minutes. This step is to remove the adsorbents and passivated H atoms. After that the wafer is transferred to the Si source chamber. A Si buffer layer of 100~1000 Å is grown at 600°C to create an atomically flat Si(100) surface and then

annealed at 800°C for 1 hour. At this point, a sharp 2×1 surface reconstruction is indicated by a reflection high-energy electron diffraction (RHEED) pattern shown in Figure 4.4 (a).

The wafer is then transferred to the Se source chamber for Se passivation. The Se source temperature is 224°C and the holding substrate for Si wafer is kept at 300°C during the passivation. Se passivation starts once the shutter is open. The in-situ gas residual analyzer (RGA) monitors the Se growth. The shutter is immediately closed once a strong RGA Se signal is observed. It takes 60 seconds from shutter opening to shutter closing. The strong RGA Se signal means no more Se stacking on the surface. Over 60 seconds the RHEED pattern still remains with 1×1 surface reconstruction, which is shown in Figure 4.4 (b), suggesting the Se passivation is self-limited monolayer growth process. After Se growth, Si wafer stays inside the MBE chamber till it cools down to room temperature for loading out. If needed, it can be transferred to another chamber for an in-situ material deposition such as metal deposition.

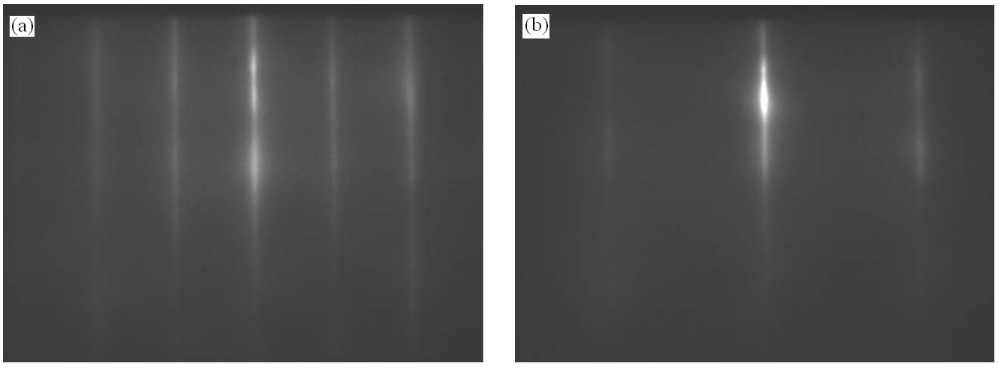


Figure 4.4 RHEED patterns of bare Si (100) with 2×1 surface reconstruction (a) and Se-passivated Si (100) with 1×1 surface reconstruction (b).

4.4 Solution-based S passivation [46]

Solution-based passivation has been successfully applied to GaAs(100) and Ge(100) substrates and different S- and Se-containing solutions are known to impart a greater or lesser degree of passivity to GaAs and Ge substrates [48-50]. However, solution passivation of Si(100) substrates has not been reported in the literature. The key to the success of passivation from a solution is its ability to remove native oxide from the semiconductor surface.

The idea is to add an etchant for SiO_2, ammonium hydroxide [NH_4OH] [51], to a solution containing a passivant for Si(100), ammonium sulfide [$(NH_4)_2S$] [52]. The choice of the etchant ensures that it does not react with the passivant in the solution. Native or thermal oxide on Si(100) is removed in the solution to expose a fresh and clean surface, which is immediately passivated by S in the same solution.

The Si(100) wafers are first cleaned with 2% HF for 30 seconds. A 20-Å SiO_2 layer was grown by ozone oxidation at 500°C. The wafers were then dipped in a mixture of $(NH_4)_2S$ and NH_4OH at 60°C for 20 minutes for passivation. By growing the thin oxide layer and then etching it in-situ in the solution, this process has the inherent advantage of removing carbon along with other contaminants.

A closely monolayer S-passivated Si(100) surface has not been characterized by any physical tool such as positron annihilation auger electron spectroscopy (PAES), which has been successfully applied in the investigation of Se-passivated Si(100) surface [53]. Instead, electrical current-voltage characteristics (I-V) are used to evaluate S-passivated Si(100) surface.

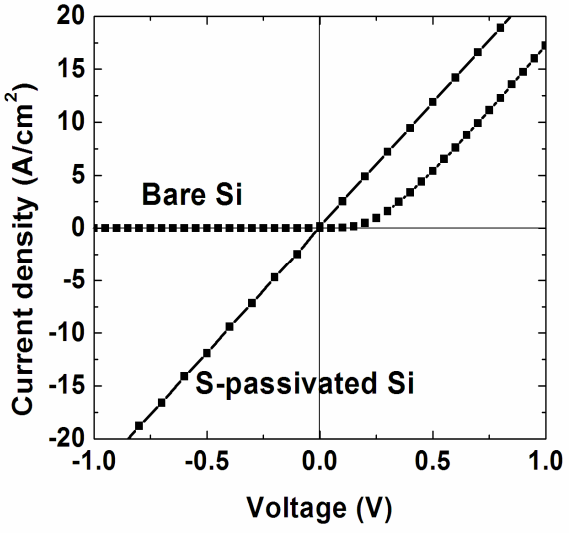


Figure 4.5 Current-voltage characteristics (I-V) for Al on S-passivated and bare n-type Si(100) where the resistivity is 1-20 Ω-cm.

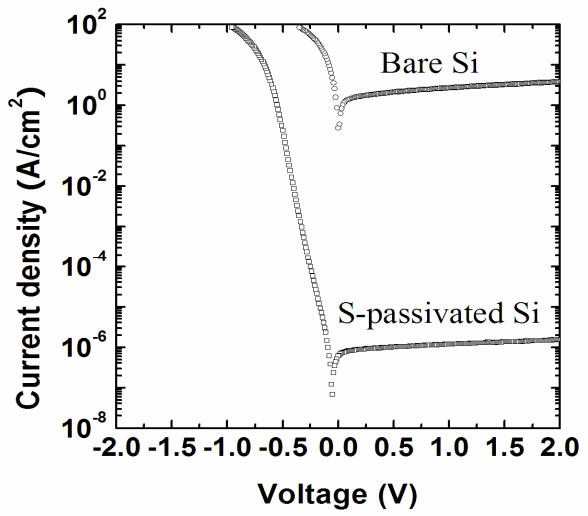


Figure 4.6 Current-voltage characteristics (I-V) for Al on S-passivated and bare p-type Si(100) where the resistivity is 0.2-0.3 Ω-cm.

As indicated by Chapter 3, if the surface states or interface states are significantly reduced, the metal-semiconductor contacts should give a closely ideal barrier height that is only dependent on the metal work-function and electron affinity of

the semiconductor. For example, aluminum (Al) contacts with S-passivated Si, the closely ideal barrier heights of low 0.25 eV for n-type Si and high 0.89 eV for p-type Si should be given assuming the Al work-function is 4.28 eV [54] and Si electron affinity is 4.05 eV. Therefore, the measured I-V for Al on S-passivated Si should show more ohmic behavior for n-type Si and deeper rectification for p-type Si if comparing with Al on bare Si without S passivation. This point has been confirmed by the measured I-V, which is demonstrated in Figure 4.5 and Figure 4.6.

A method quantifying interface states is introduced in Chapter 5 through nano-CMOS devices. The fabricated devices with monolayer Se preparing Si(100) surface shows a better interface property, indicated by a reduction of density of interface traps (D_{it}) comparing with control devices without using Se passivation.

CHAPTER 5

QUANTIFICATION OF INTERFACE STATES THROUGH NANO-CMOS DEVICES

CMOS is an abbreviation of complementary metal-oxide-semiconductor. It serves as gate part between source and drain in the MOSFET (metal-oxide-semiconductor field effect transistor) for the channel current control. The schematic structures of MOSFET and CMOS are shown in Figure 5.1. Nano-CMOS devices require the gate dielectric with an equivalent oxide thickness (EOT) of less than 10-Å [42]. Conventional SiO_2-based dielectrics with such a thickness will cause a severe leakage current due to the tunneling effect, which can be avoided by replacing SiO_2 with a comparatively thicker high-κ dielectric. The concern for using high-κ dielectric is the arising of interface states between high-κ dielectric and Si surface. A high density of interface states pins the interface Fermi level, and thus the threshold voltage of the device.

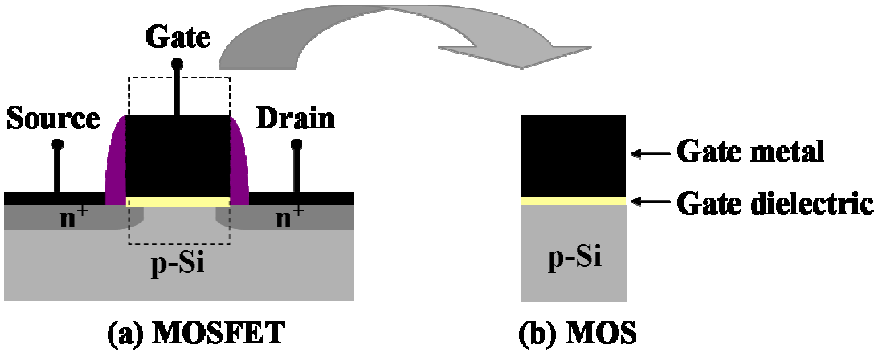


Figure 5.1 Schematic structures of (a) MOSFET and (b) CMOS.

Interface states arise from the dangling bonds at the high-k/Si interface and, unfortunately, are an inherent feature of any dielectric/semiconductor interface. The interface between thermal SiO_2 and Si(100) represents the best dielectric/semiconductor interface with an interface-state density (D_{it}) in the low 10^{10} eV^{-1}/cm^2 range. The interface-state density for high-κ on Si is usually in the level above 10^{12} eV^{-1}/cm^2. One method to reduce the interface states is to use monolayer of Se passivating Si(100) surface before the growth of high-κ dielectric. Passivation of Si(100) by monolayer of Se terminates most of the dangling bonds and electrically minimizes the surface states on Si(100). In addition, Se-passivated Si(100) surface expresses a better stability than hydrogen (H)-passivated surface and it suppresses the oxygen diffusion to form SiO_2, causing an interfacial layer between high-κ dielectric and Si [55]. Figure 5.2 shows the HRTEM cross-section of HfO_2 formed by oxidizing 4-nm Hf layer at 300°C in 1 atm O_2 on Se-passivated Si(100) and non-passivated Si(100) [56]. The observed thinner interfacial layer for Se-passivated sample clearly indicates this suppression action.

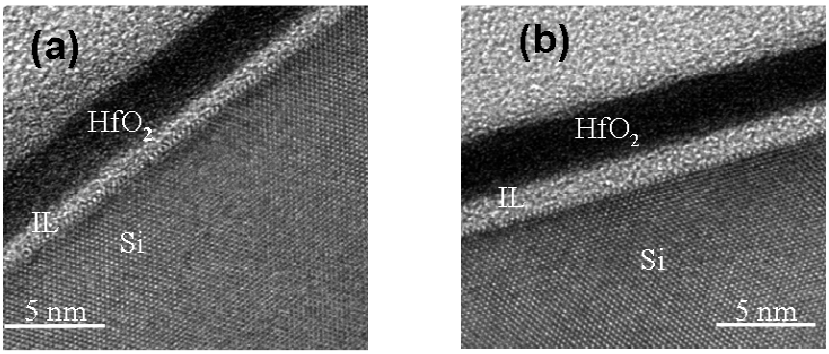


Figure 5.2 HRTEM cross-section of HfO_2 formed by oxidizing a 4-nm Hf layer at 300°C in 1 atm O_2 on (a) Se-passivated Si(100) and (b) non-passivated Si(100) [56].

The objective of this chapter is to utilize nano-CMOS devices to demonstrate the reduction of interface states between high-κ dielectric and Se-passivated Si(100). A delicate experiment is designed for this purpose [57].

5.1 Experimental

Previously mentioned HfO_2 is formed by oxidizing a thin ex-situ grown Hf layer. It means that the growth of Hf layer is after air exposure of MBE Se-passivated sample. The air-exposed Se-passivated surface will be contaminated by the adsorbents, thus degrading the passivation quality. Figure 5.3 shows the HRTEM cross-section of a Se-passivated sample after air exposure. A ~10-Å adsorbents layer is observed [47].

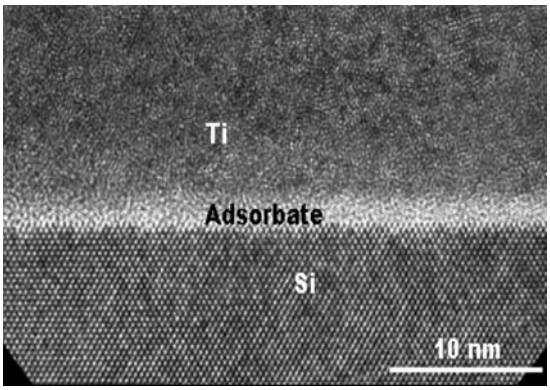


Figure 5.3 HRTEM cross-section of Se-passivated sample after air exposure. The grown Ti layer is to make the contrast [47].

In order to eliminate the adsorbents layer, a 20-Å Al layer instead of Hf is in-situ grown on the Se-passivated surface without breaking the vacuum. Using Al is due to the availability of Al source in MBE chamber. The thin Al layer is then ozone-oxidized at 400°C for 10 minutes and 20 minutes respectively to form Al_2O_3. Lastly, a

700-Å Ti layer is deposited by electron beam evaporation and circular dots for gate electrodes are fabricated with a lift-off process. The same process for control samples without Se passivation is simultaneously conducted for comparison.

5.2 Zero interfacial layer

To demonstrate the removal of absorbents layer by an in-situ deposition process, two wafers are prepared. One Si wafer was prepared as described above, with Se passivation and in-situ deposition of 100-Å Al. The second wafer was prepared in a similar manner, except that after Se passivation and before Al deposition, the wafer was taken out of MBE and exposed to the atmosphere for 10 days before MBE Al deposition. Figure 5.4 (a) shows the HRTEM cross-section of the wafer with ex-situ grown 100-Å Al. An amorphous interfacial layer of 1.5-nm is observed between Al and Si. When Al is deposited in-situ on Si without breaking vacuum, TEM exhibits an atomically sharp interface free of any interfacial layer shown in Figure 5.4 (b). This suggests that a high vacuum in-situ process is required if zero interfacial layer is needed for sub-10 Å EOT.

Figure 5.5 shows the HRTEM cross-section a 38-Å Al_2O_3 layer on Se passivated Si(100) surface. The Al_2O_3 layer was obtained by oxidizing a 20-Å in-situ Al layer in UV ozone at 400^{o}C for 10 minutes. The Al_2O_3/Se/Si interface is clearly exempt of any interfacial layer, with an atomic abruptness. In comparison, the previously ex-situ formed HfO_2 always gives an interfacial layer ranging between 10-20 Å.

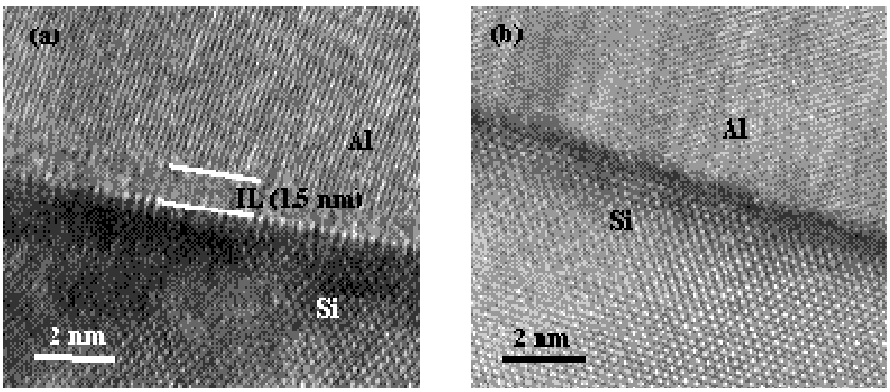


Figure 5.4 HRTEM cross-sections of two different Al/Si interfaces. A 100-Å Al layer is deposited after air exposure of the sample for 10 days (a) and in situ without breaking vacuum (b) [57].

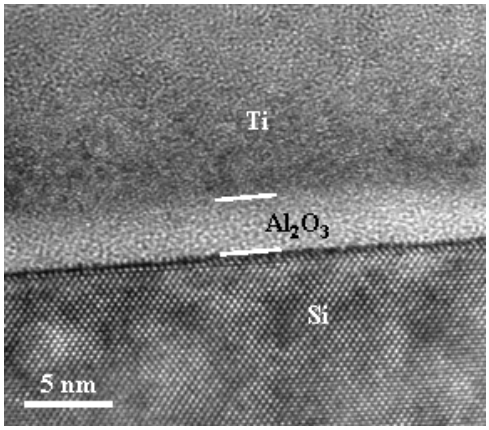


Figure 5.5 HETEM cross-section of a 38 Å Al_2O_3 layer on Se passivated Si(100) surface. The Al_2O_3 layer is obtained by oxidizing a 20-Å in-situ Al layer in UV ozone at 400^{o}C for 10 minutes [57].

5.3 Interface-state density extracted from normalized C-V and G-V

Figure 5.6 shows the measured and normalized C-V and G-V curves at 1 MHz for a CMOS device with integration of Se passivation and in-situ formed Al_2O_3. The Al_2O_3 is formed by ozone-oxidation of an in-situ 20-Å Al layer at 400°C for 10

minutes. The CMOS device structure is shown in Figure 5.7 (a). Figure 5.7 (b) shows the equivalent circuit of this device.

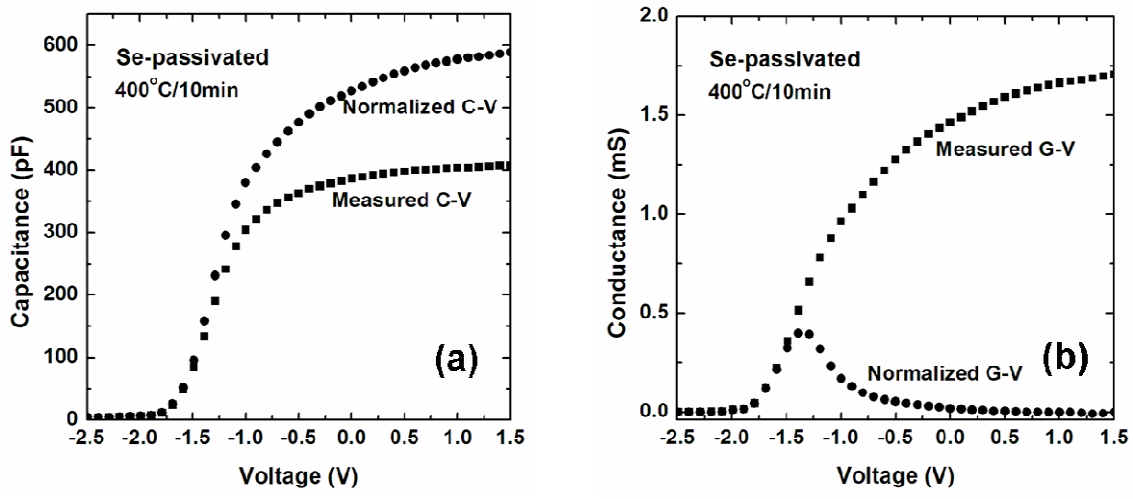


Figure 5.6 The measured and normalized C-V (a) and G-V (b) for a CMOS device with in-situ formed Al_2O_3 on Se-passivated Si(100). The Al_2O_3 is formed by UV ozone oxidation of a 20-Å Al layer at 400°C for10 minutes.

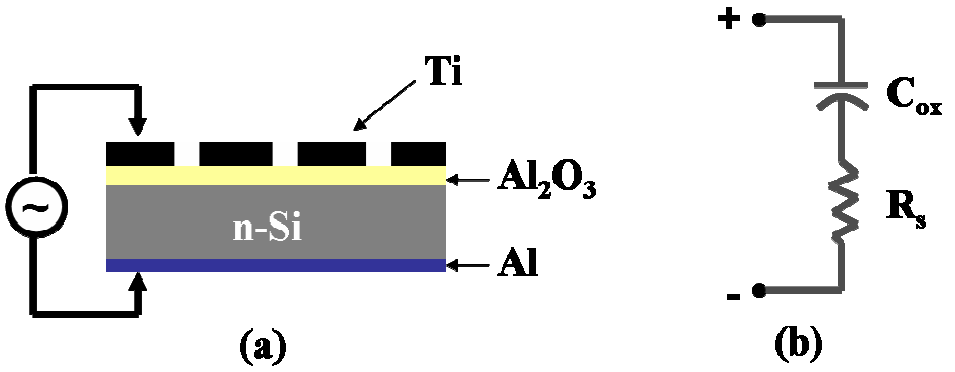


Figure 5.7 A schematic CMOS structure (a) with in-situ grown Al_2O_3 on Se-passivated Si(100) and its equivalent circuit (b), where the C_{ox} is the oxide capacitance and R_s is the series resistance.

The normalized C-V and G-V curves are that taking out the effects from the series resistance and frequency referred from Maiti's work [58]. Related equations are listed as below,

$$Y_{ma} = \left| G_{ma} + j\omega C_{ma} \right|, R_s = \mathrm{Re}\, l(1/Y_{ma}) \qquad (5.1)$$

where Y_{ma} is the admittance across the dielectric stack when the MOS capacitor is biased into strong accumulation, G_{ma} corresponds to strong accumulated capacitance C_{ma}, and series resistance R_s is the real part of impedance $Z_{ma}=1/Y_{ma}$,

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{(a^2 + \omega^2 C_m^2)},\ G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{(a^2 + \omega^2 C_m^2)} \qquad (5.2)$$

where C_c and G_c are the corrected capacitance and conductance corresponding to measured C_m and G_m, respectively, ω is angular frequency, and a is defined by Equation 5.3 as below.

$$a = G_m - (G_m^2 + \omega^2 C_m^2)R_s \qquad (5.3)$$

Calculation of interface-state density D_{it} was referred from Lu's work [59] by Equation 5.4,

$$D_{it} = \frac{(2/qA)(G_{\max}/\omega)}{[(G_{\max}/\omega C_{axx})^2 + (1 - C_m/C_{acc})^2]} \qquad (5.4)$$

where q is electron's charge, A is area of electrode dot, C_m corresponds to G_{max} that is the peak value of the corrected conductance curve, and C_{acc} is strongly accumulated capacitance.

Using the normalized C-V and G-V curves together with the Equation 5.4, the interface-state density near mid gap level [60] can be calculated. Figure 5.8 shows the comparison of extracted interface-state density between control samples and Se-passivated samples where the Al_2O_3 is formed by ozone oxidation of in-situ 20-Å Al at 400°C for 10 minutes and 20 minutes, respectively. A monolayer of Se passivation gives a reduction in interface-state density by about 5 times as compared to control samples. It is worth noting that no forming gas annealing is performed on these samples, which could further reduce the interface-state density.

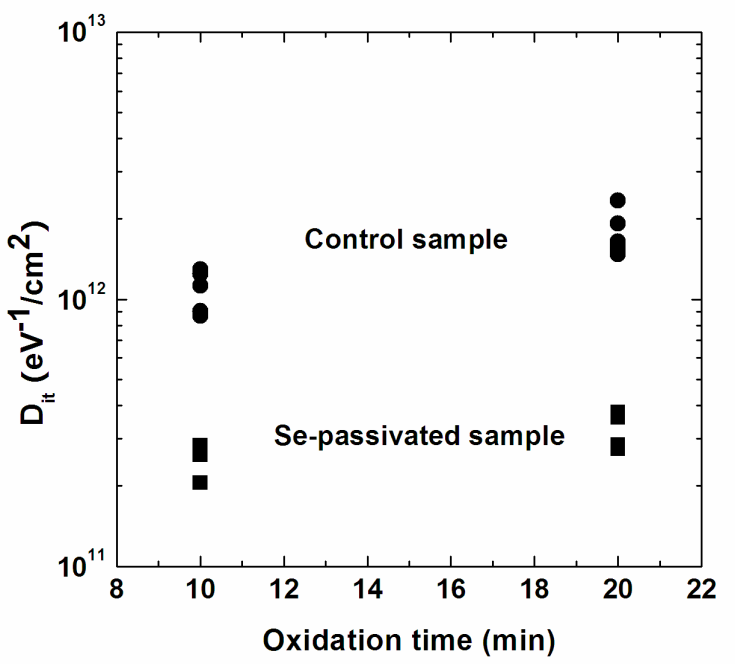


Figure 5.8 Interface-state density extracted from normalized C-V and G-V. The Al_2O_3 layers are obtained after oxidation of in-situ 20-Å Al in UV ozone at 400°C for 10 minutes and 20 minutes. Se passivation provides a reduction in interface states by about 5 times.

5.4 C-V hysteresis

C-V hysteresis from forward bias to reverse bias is an indication of gate dielectric quality. The less hysteresis in C-V sweeping curve means less bulk defects density in dielectric layer. Figure 5.9 shows the measured C-V hysteresis at 1 MHz for control and Se-passivated samples where the Al_2O_3 layer is formed by ozone oxidation of in-situ 20-Å Al at 400°C for 10 minutes and 20 minutes, respectively. The monolayer Se-passivated samples give C-V hysteresis above 2 times lower than control samples. This indicates Al_2O_3 on Se-passivated Si(100) surface has a lower bulk defects density than on bare Si(100) surface. More fundamentally, surface preparation by Se monolayer could change the way Al_2O_3 is formed on Si(100).

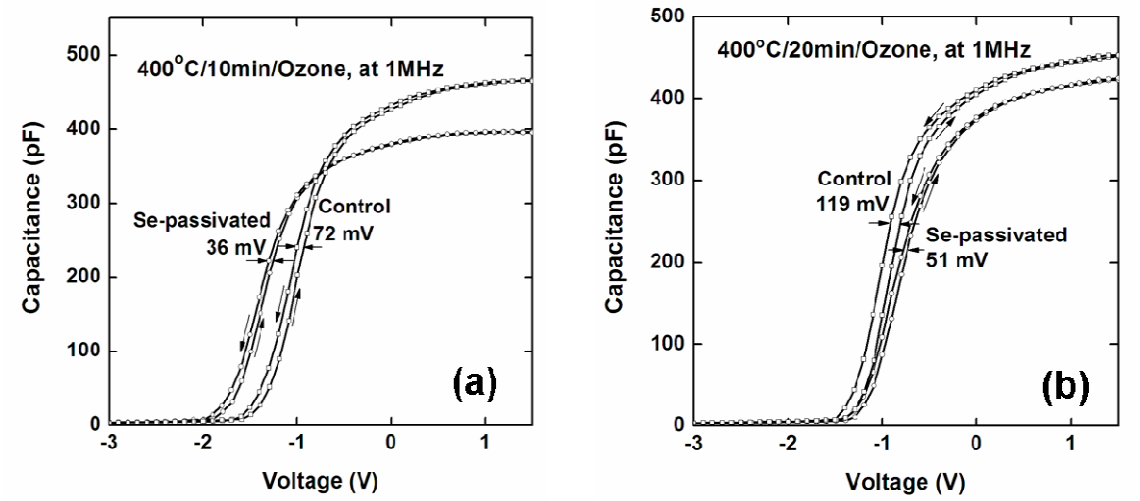


Figure 5.9 C-V hysteresis at 1 MHz for Se-passivated samples and control samples. The Al_2O_3 layer is obtained by oxidizing an in-situ 20-Å Al in UV ozone at 400°C for 10 minutes and 20 minutes, respectively.

5.5 Summary

Through nano-CMOS devices, a quantified method is introduced to calculate the interface-state density. This method utilizes the normalized C-V and G-V curves that are calculated from the measured C-V and G-V curves by taking out the effects from series resistance and frequency. The extracted interface-state density for Se-passivated samples is 5 times lower than control samples without Se passivation. It means that the monolayer Se passivation on Si(100) improve the interface quality. The C-V hysteresis for Se-passivated samples is 2 times lower than the control samples without Se passivation, indicating the lower bulk defects in Al_2O_3 dielectric formed on Se-passivated surface.

CHAPTER 6

HIGH SCHOTTKY BARRIER ON P-TYPE SI(100)

Using "Valence-mending concept" to passivate Si(100) surface has been introduced in Chapter 4. This concept is experimentally realized by two methods, one is self-limited and well controlled MBE monolayer Se passivation, and the other is solution-based and closely a monolayer S passivation. The MBE Se-passivated Si(100) surface also expresses a better thermalstability than solution-based S passivation. However, MBE Se passivation involves a high energy input. If this is not an issue for research investigation, its time-consuming work will be a roadblock for a short-cycle experiment that needs to be repeated frequently. Solution-based S passivation, even though it is a less controlled process, can satisfy this need. This is why the solution-based S passivation is developed and used in most of our experiments especially in achieving high Schottky barrier and finally making diffusion-free back contact solar cells.

Other methods attempting to achieve high Schottky barrier, such as deep surface cleaning [61], hydrogen passivation [62,63], ion implantation [64], growth of thin Si oxide [65], and silicidation of interface [66-68], have been tried by many groups. Among these, the highest Schottky barrier to date is 0.96 eV for iridium silicide on n-type Si [66] and 0.94 eV for lead on hydrogen-passivated p-type Si [62]. Both of them are unable to make degenerate inversion on Si surface for solar cell use.

The proposed method using S passivating Si(100) surface is to reduce the surface states, making an almost ideal barrier height after metal contact. If this is true, some of the metal/Si contacts can produce extremely high Schottky barriers. According to Mott-Schottky theory, for a p-type Si the low work-function metals are needed, instead the high work-function metals for an n-type Si.

Table 6.1 Ideal barrier heights and given barrier heights for some regularly used metals on Si [33].

		Ag	Al	Au	Cr	Ni	Pt	Ti	W
	ϕ_M (eV)	4.26	4.28	5.10	4.50	5.15	5.65	4.33	4.55
n-Si	Ideal ϕ_{Bn} (eV)	0.21	0.23	**1.05**	**0.45**	**1.10**	**1.60**	0.28	0.50
	ϕ_{Bn} (eV)	0.78	0.72	0.80	0.61	0.61	0.90	0.50	0.67
p-Si	Ideal ϕ_{Bp} (eV)	**0.91**	**0.89**	0.07	0.67	0.02	-0.48	0.84	0.62
	ϕ_{Bp} (eV)	0.54	0.58	0.34	0.50	0.51		0.61	0.45

Table 6.1 summarizes the work-function of some regularly used metals in the laboratory, the ideal barrier heights and the given barrier heights [33] for these metals on Si. For p-type Si, metals such as silver (Ag) and aluminum (Al) are good candidates because of their low work-functions. But the ideal barrier heights for these two metals on p-type Si are not high enough to create the degenerate inversion on Si surface. In reality, experimentally obtained barrier height between Al and S-passivated p-type Si(100) is ~0.2 eV larger than the ideal barrier height of 0.89 eV, causing a degenerate inversion on Si(100) surface which will be explained in section 6. 5.

6.1 Experimental

P-type boron doped Si(100) wafers with doping concentration of low 10^{17} cm^{-3} were used in the experiment. Some wafers were first cleaned in HF and then oxidized in ozone to form a 2-nm oxide layer. The oxide layer was stripped and the wafers were

wet-chemically passivated with S in an aqueous solution of $(NH_4)_2S$ [46]. Other wafers were cleaned in HF but without S passivation as control samples. Low work-function Al electrodes with a diameter of 216 μm and thickness of ~100 nm were formed by e-beam evaporation through a shadow mask on both S-passivated and control samples. Al was also used for blank back contact. Figure 6.1 shows the Schottky-contact structure of Al on S-passivated p-type Si(100) that contains multiple identical single diodes. The large area of the back contact made possible the characterization of the front Al/Si diodes with a negligible effect from the Schottky behavior of the back contact. Capacitance-voltage (C-V), current-voltage (I-V) and temperature-dependent I-V characterizations were performed on these Al/S-passivated p-type Si(100) diodes.

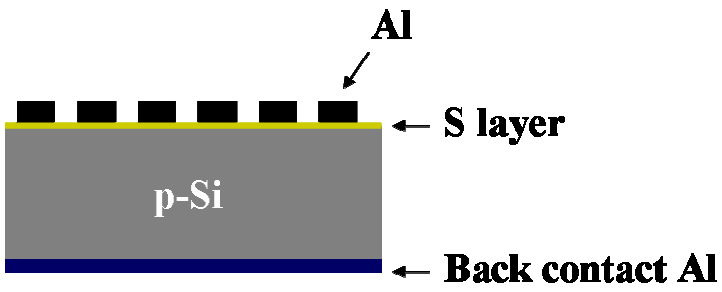


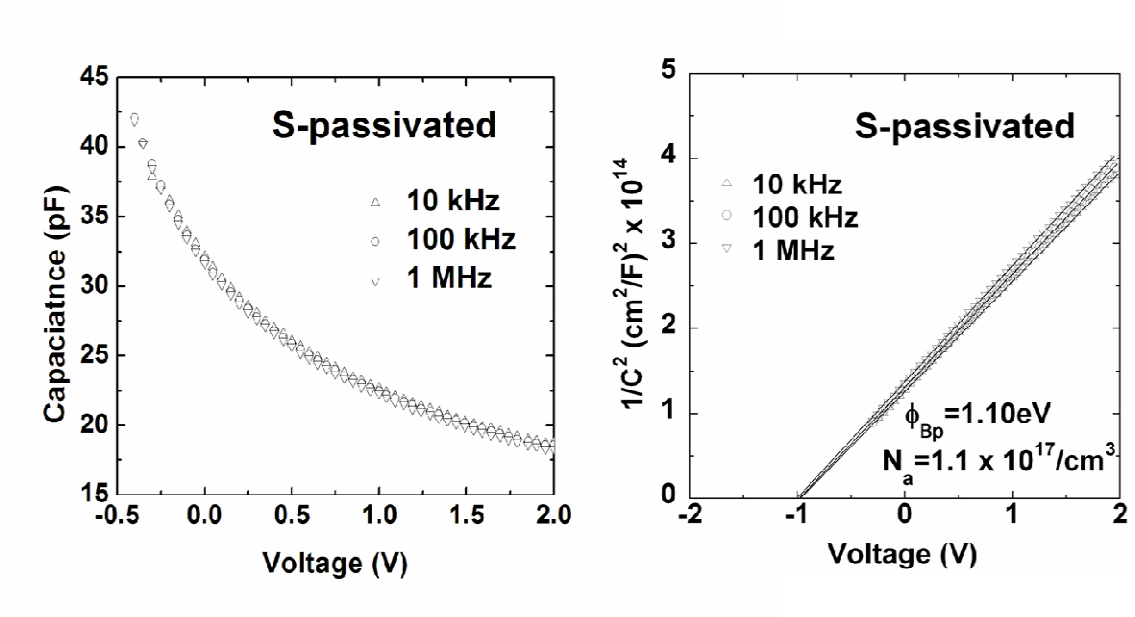
Figure 6.1 The Schottky diodes built on a p-type Si(100). The S layer is underneath the front Al contact and the diode size is 216 μm in diameter.

6.2 Capacitance-voltage (C-V) characteristics

6.2.1. C-V characteristics for Al/S-passivated p-type Si(100) diodes

Figure 6.2 (a) shows the measured C-V curves at frequencies of 10 kHz, 100 kHz and 1 MHz of Al/S-passivated p-type Si(100) diodes. The $1/C^2$-V characteristics for these curves are shown in Figure 6.2 (b). The intercept of the fitting lines with the

voltage axis is 0.98 V, which represents the amount of surface band bending or surface potential ϕ_s at the zero voltage on the structure. The extracted doping concentration is 1.1×10^{17} cm^{-3}, which is consistent with the wafer specification (ρ = 0.2-0.3 Ω-cm). For p-type Si with 1×10^{17} cm^{-3} doping concentration, the difference between Fermi-level E_F and valance band E_V in the bulk, ϕ_p, is about 0.12 eV. With $\phi_{Bp} = q\phi_s + \phi_p$, where q is electron's charge and the flat-band Schottky barrier ϕ_{Bp} is thus 1.1 eV.



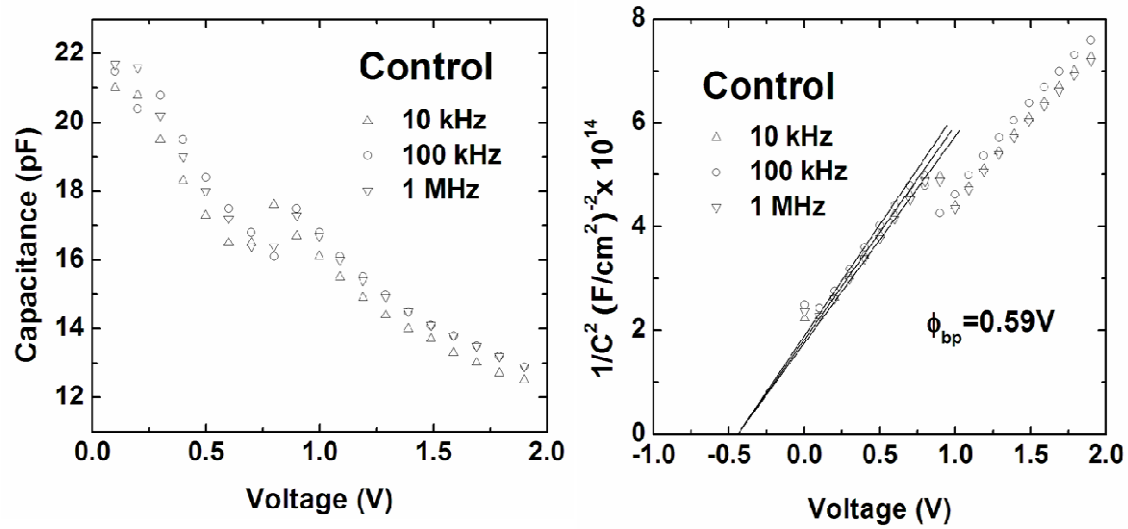
(a) (b)

Figure 6.2 The measured C-V (a) and $1/C^2$-V characteristics (b) of Al/S-passivated p-type Si(100) diodes at frequencies of 10 kHz, 100 kHz and 1 MHz.

6.2.2. C-V characteristics for Al/ p-type Si(100) control diodes

Figure 6.3 (a) shows the measured C-V curves at frequencies of 10 kHz, 100 kHz and 1 MHz of Al/p-type Si(100) control samples. The $1/C^2$-V characteristics for these curves are shown in Figure 6.3 (b). The intercept of the fitting lines with the

voltage axis is 0.47 V. With consideration of ϕ_p, the extracted barrier height is 0.59 eV for control samples, ~ 0.5 eV lower than that of Al/S-passivated p-type Si(100) samples.



(a) (b)

Figure 6.3 The measured C-V (a) and $1/C^2$-V characteristics (b) of Al/p-type Si(100) control diodes at frequencies of 10 kHz, 100 kHz and 1 MHz.

6.3 S-Si dipole moment on the surface

The ideal barrier height between Al and p-type Si(100) is 0.89 eV, assuming 4.28 eV for Al work function ϕ_M and 4.05 eV for Si electron affinity χ_s. This value is obtained from the Mott-Schottky theory, $\phi_{Bp} = \chi_s + E_g - \phi_M$, where E_g is the Si band gap, 1.12 eV. The difference of ~ 0.2 eV between the measured flat-band barrier height and the ideal barrier height is attributed to the S-Si dipole moment on the passivated surface.

Figure 6.4 shows the Si(100) surface configuration from (110) point of view after S passivation. Due to the higher electronegativity of S than Si, the S atom is more

negatively charged close to Si side and the Si atom is more positively charged close to S side. Hence the dipole-induced electric field is normal to Si surface and pointed out, causing barrier decrease for an n-type Si and increase for a p-type Si.

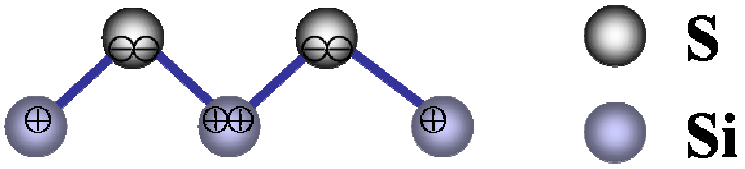


Figure 6.4 S-passivtaed Si(100) surface from (110) point of view.

The increase in barrier height $\Delta\phi$ due to surface dipole is given by

$$\Delta\phi = \frac{qpN_s}{\varepsilon_o \varepsilon_i} \text{ [62]} \qquad (6.\ 1)$$

where ε_o is the permittivity of vacuum, ε_i is the relative permittivity of Si near the interface and is about half of the bulk Si permittivity [69], often taken by 4 [62,70], p is the dipole moment, and N_s is the atomic density of S on the Si(100) surface. Assuming complete monolayer passivation, N_s is 6.78×10^{14} atoms/cm^2. The dipole moment is expressed by

$$p = (\Delta q)d \qquad (6.\ 2)$$

where Δq is the ionicity of the S-Si bond and d is the separation between the S monolayer and the Si(100) surface, taken by 1.09 Å [44,71]. Δq is given by

$$\Delta q = 0.16\left|X_A - X_B\right| + 0.035(X_A - X_B)^2 \text{ [62]}, \qquad (6.\ 3)$$

where X_A and X_B are the electronegativities of the atoms involved. For S, it is 2.58 and for Si, it is 1.9. The calculated Δq is thus 0.12e for a single S-Si bond. On the S-passivated Si(100) surface, each S atom bonds with two Si surface atoms and vice versa. Therefore, the real Δq should be 0.06e. Using above parameters, the calculated $\Delta\phi$ is 0.20 eV, which accounts for the difference between measured barrier height and ideal barrier height.

6.4 Energy-band diagram for a p-type Si(100) with 1.1 eV barrier height

For p-type Si with 1×10^{17} cm^{-3} doping concentration, a barrier height of 1.1 eV suggests that the conduction band is only 0.02 eV above the Fermi level at the interface, indicating the degenerate inversion on the Si surface, which is defined by $E_C - E_F < 0.08$ eV at the interface. Figure 6.5 shows the band diagram of 1.1 eV barrier height for Al on p-type Si(100) where the doping concentration is ~$1\times10^{17}/cm^3$. This requires Fermi statistics to describe its electrostatics [72,73]. (See appendix A).

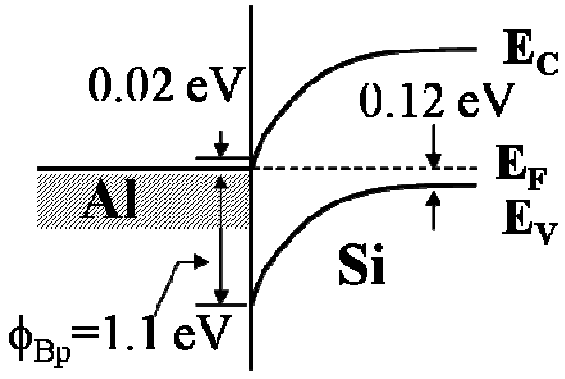


Figure 6.5 The energy-band diagram of Al on p-type Si(100) with 1.1 eV barrier height. The substrate has doping concentration about $1\times10^{17}/cm^3$.

6.5 Definition of surface inversion for p-type Si

As indicated in Figure 6.6, $q\phi_B$ is defined as E_i-E_F where E_i is the intrinsic Fermi level and E_F is the Fermi level depending on the doping concentration, and $q\phi_s$ is the surface potential or band bending measured with respect to the intrinsic Fermi level. The band banding is negative once the band is bent upward and positive once bent downward. The accumulation occurs when $\phi_s < 0$ shown in Figure 6.6 (a), the depletion occurs when $\phi_B > \phi_s > 0$ shown in Figure 6.6 (b) and the inversion occurs when $\phi_s > \phi_B$ shown in Figure 6.6 (c). The strong inversion begins at $\phi_s = 2\phi_B$. Once the strong inversion occurs, the width of depletion layer reaches a maximum. When the bands are bent downward away from $\phi_s = 2\phi_B$, the semiconductor is effectively shielded from further penetration of the electric field by the inversion layer and even very small increase in band bending results in a very large increase in charge density within the inversion layer. Figure 6.7 shows the surface charge density Q_s versus the surface potential ϕ_s for p-type Si at different doping concentrations, indicating a big increase of Q_s with a small increase of ϕ_s once $\phi_s > 2\phi_B$. For p-type Si with doping concentration of $1\times10^{17}/cm^3$ (ϕ_p = 0.12 eV), the ϕ_B is about 0.44 eV and the strong inversion starts at 0.88 eV, corresponding to a 1.0 eV barrier height. Beyond this, the Si surface is degenerately inverted. In the case of the 1.1-eV barrier height, the electric field at the interface is extremely high, resulting in a relatively large image force lowering. Hence the effective barrier height extracted from I-V characteristics will be lower than the flat-band barrier height extracted from $1/C^2$-V characteristics.

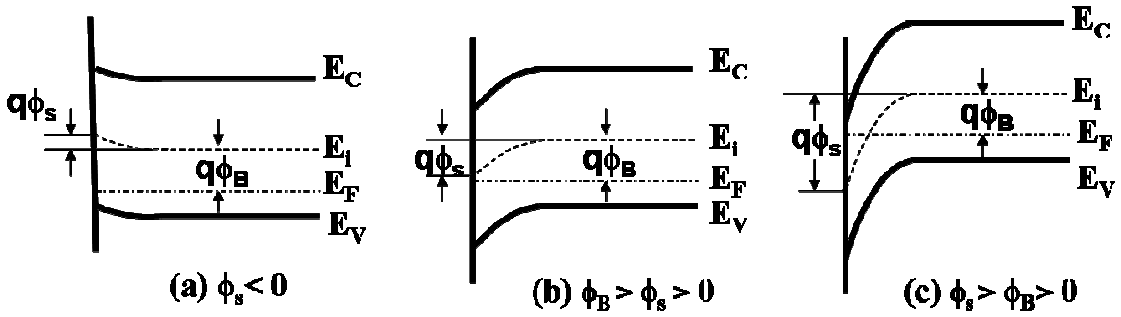


Figure 6.6 Energy-band diagrams at the surface of a p-type Si. The surface potential or band-bending ϕ_s is measured with respect to the intrinsic Fermi level E_i. (a) Accumulation occurs when $\phi_s<0$. (b) Depletion occurs when $\phi_B>\phi_s>0$. (c) Inversion occurs when $\phi_s>\phi_B$.

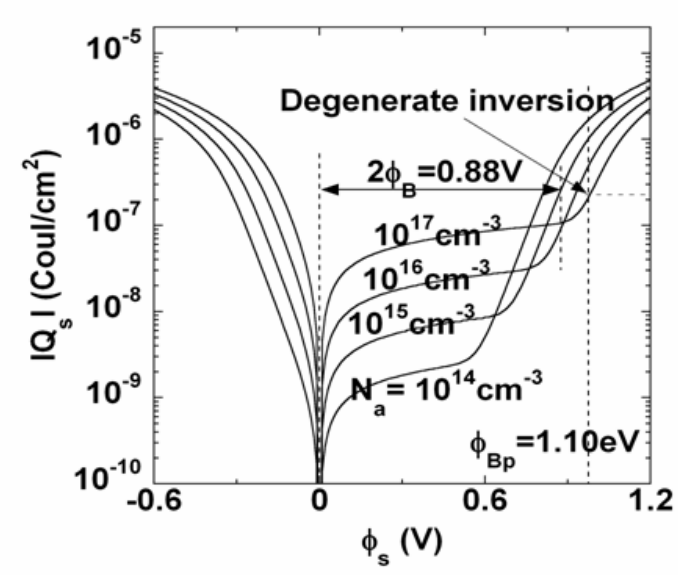


Figure 6.7 Surface charges versus surface potential for the p-type Si(100) at different doping concentrations.

6.6 Band-bending near the interface, electric field and image force lowering effect

Figure 6.8 shows the band bending in the valence band E_V near the interface (solid lines) and its correction by image-force lowering (dash lines) for three cases: $E_C - E_F = \pm 0.08$ eV and 0.02 eV at the interface. The inset is the energy band diagram where the Δ is defined by $E_C - E_F$ at interface. Surface electric field, the derivative of band bending, is 1×10^6 V/cm for $E_C - E_F$ = -0.08 eV (strong degeneracy) and lowered to 2×10^5 V/cm for $E_C - E_F$ = 0.02 eV (weak degeneracy). Image-force lowering amounts to 0.08 eV for $E_C - E_F$ = 0.02 eV resulting from 1.1 eV barrier height on Si(100) with doping concentration of $1\times10^{17}/cm^3$. The image-force lowering $\Delta\phi$ is calculated by

$$\Delta\phi = \sqrt{\frac{qE}{4\pi\varepsilon_s}} \text{ [74]} \qquad (6.4)$$

where q is electron's charge, E is the electric field at interface and ε_s is e permittivity of Si.

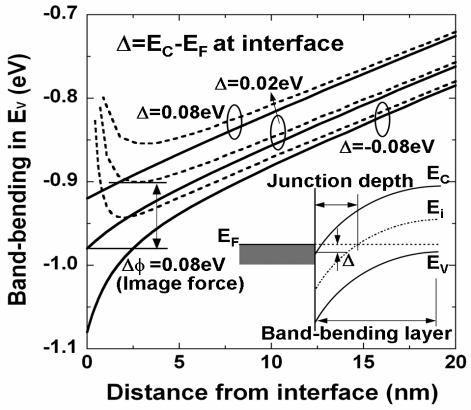


Figure 6.8 Band-bending in valence band E_V near the interface and its correction by image-force lowering for three cases: $E_C - E_F = \pm 0.08$ eV and 0.02 eV. Inset is a schematic band alignment for the Al/S-passivated p-type Si(100) diode where the Δ is defined.

Although this device is fabricated like a Schottky diode, it works like a p-n junction diode, i.e., holes are injected from the p-type bulk and electrons from the n-type surface under forward bias. The concept of depletion region has no meaning here, since the surface goes into degenerate inversion. Instead, it is better to use "band-bending region" shown in the inset of Figure 6.8. The point where the Fermi level passes the mid-gap can be defined as the junction depth, if this is considered a p-n junction. The calculated junction depth is nearly three times smaller than the band-bending region, which is about 0.19 μm for $1\times10^{17}/cm^3$ doping concentration. Table 6.2 shows the width of the surface band-bending region (Ls) and junction depth (xj) at $E_C - E_F = 0$ and ±0.08 eV for p-type Si with different doping levels.

TABLE 6.2. The width of the surface band-bending region (L_s) and the junction depth (x_j) at $E_C - E_F = 0$ and ±0.08 eV for p-type Si with different doping levels.

		0.08 eV	**0 eV**	**-0.08 eV**
$10^{15}/cm^3$	L_s(μm)	1.710	1.717	1.719
	x_j(μm)	0.560	0.567	0.569
$10^{16}/cm^3$	L_s(μm)	0.573	0.579	0.581
	x_j(μm)	0.181	0.187	0.189
$10^{17}/cm^3$	L_s(μm)	0.188	0.193	0.195
	x_j(μm)	0.056	0.061	0.063

6.7 Barrier height extracted from activation-energy plot

Figure 6.9 shows the activation-energy plot (I_F/T^2-1/T) between 20°C and 140ºC for S-passivated samples, which gives a barrier height of 0.94-0.97 eV. The forward current (I_F) is used at high forward voltages from 0.2-0.35 V in an attempt to reduce the image-force lowering effect. The effect of series resistance on the measured barrier

height is minimal, as shown later in Figure 6.11. The barrier height from Figure 6.9 is about 0.15 eV smaller than the flat-band barrier height. C-V measurements from 20°C to 140ºC indicate that the barrier height decreases quickly from 1.1 eV to 0.82 eV, which is shown in Figure 6.10, suggesting that elevated temperatures cause the Al/S-passivated Si(100) interface to react to some extent. Therefore, the barrier height extracted from the activation-energy method is averaged over the temperature range, leading to the barrier decrease.

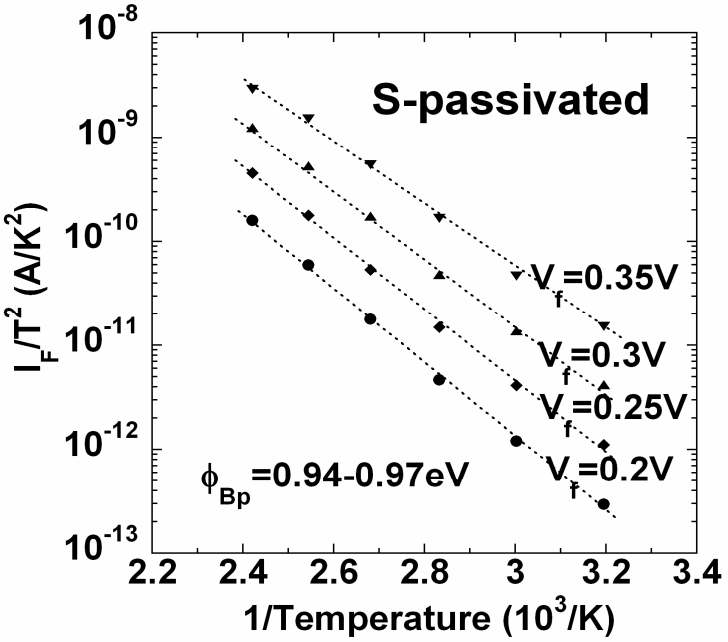


Figure 6.9 Determination of Schottky barrier height from activation-energy measurements for Al/S-passivated p-type Si(100) diodes with a bulk resistivity of 0.2-0.3 Ω-cm. Forward current is used to extract the barrier height at several forward voltages.

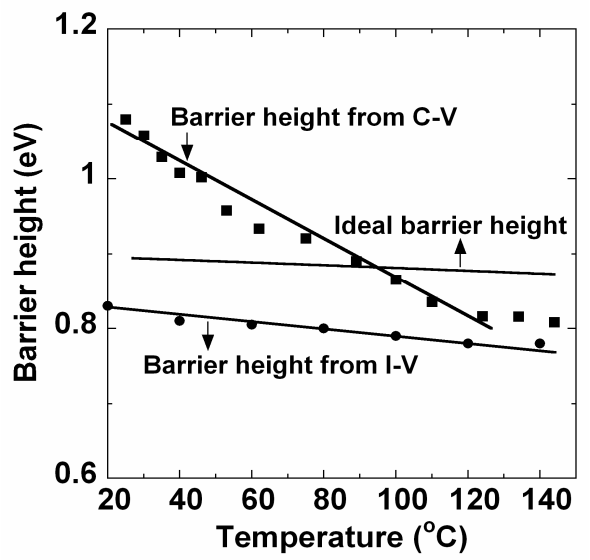


Figure 6.10 Barrier height at elevated temperatures extracted from C-V and forward I_F fitting. The ideal barrier height is shown for reference.

6.8 Barrier height extracted from I_F fitting

Figure 6.11 shows the I-V characteristics of the S-passivated samples at room temperature. The forward I-V is linear over six orders of magnitude in the logarithmic plot, suggesting minimal effect from series resistance. The solid line is the fitting result of the forward I-V by the thermionic-emission model. The fitting yields an effective barrier height ϕ_{eff} of 0.84 eV, an ideality factor of 1.25 and a series resistance of 22 Ω.

One reason for the low effective barrier height and high ideality factor might be due to the limitations of the model in high barrier measurement [75]. Another reason might be attributed to inhomogeneity in barrier height [76-79], i.e., the existence of a few low-barrier regions in the Schottky diode. The barrier heights extracted from the I-V fitting from 20°C to 140°C (Figure 6.12) are shown in Figure 10, and it also indicates the barrier decrease with elevated temperatures.

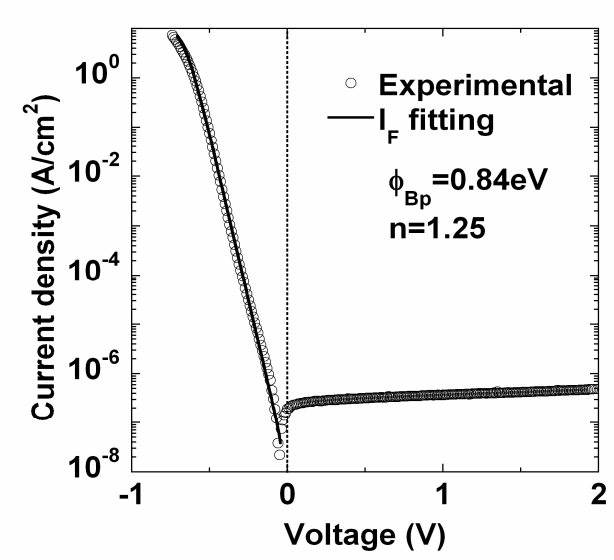


Figure 6.11 I-V characteristic at room temperature for an Al/S-passivated p-type Si(100) diode where the bulk resistivity of Si is 0.2-0.3 Ω-cm. The solid line is the fitting result of the forward current by the thermionic-emission model.

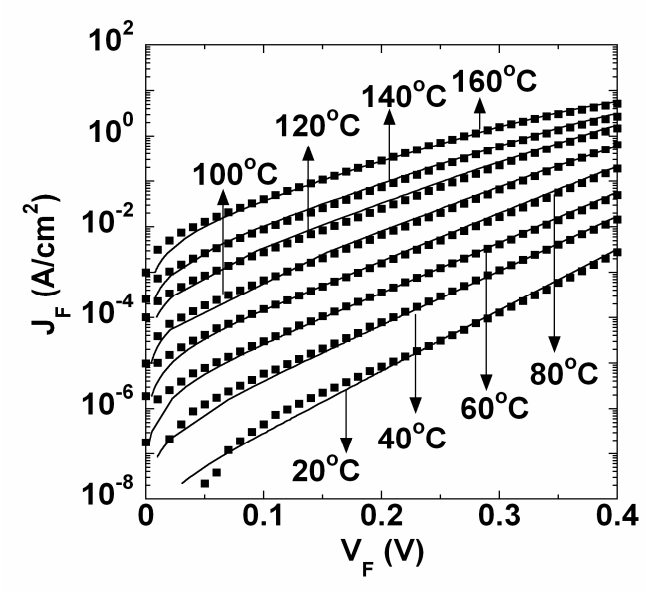


Figure 6.12. Fitting results of the forward currents (I_F) at different temperatures. The extracted barrier heights are shown in Figure 6.10.

Wet-chemical passivation can not guarantee perfect passivation with complete S

coverage, and the unpassivated regions will have a much lower barrier height (0.5 eV lower). This can lead to a large difference between the effective barrier height from I-V and the flat-band barrier height from $1/C^2$-V [80]. A barrier height of 0.74 eV from the reverse saturation current in Figure 6.11 suggests that the reverse current is dominated by an edge-related leakage current.

6.9 Temperature-dependent I-V characteristics and thermalstability studies for Al/S-passivated p-type Si(100) diodes

Figure 6.13 shows the I-V characteristics of both S-passivated and control samples at different temperatures. The reverse saturation current is 4.5×10^{-7} A/cm^2 for the S-passivated sample at room temperature, while the control sample show a reverse current which is more than six orders of magnitude higher. This significant reduction in reverse current is a result of the 0.5-eV increase in barrier height by S passivation. The reverse current for the S-passivated sample at 160ºC is about ten times smaller than that of the control sample at room temperature. Eventually, the S-passivated sample loses rectification above 200ºC.

The thermalstability studies of the S-passivated samples indicates that, after 40-minute vacuum (10^{-6} torr) annealing at 100ºC and 150ºC, the reverse current for the passivated samples rises to ~10^{-6} and ~10^{-3} A/cm^2, respectively (Figure 6.14). This indicates the S-passivation is not thermally stable.

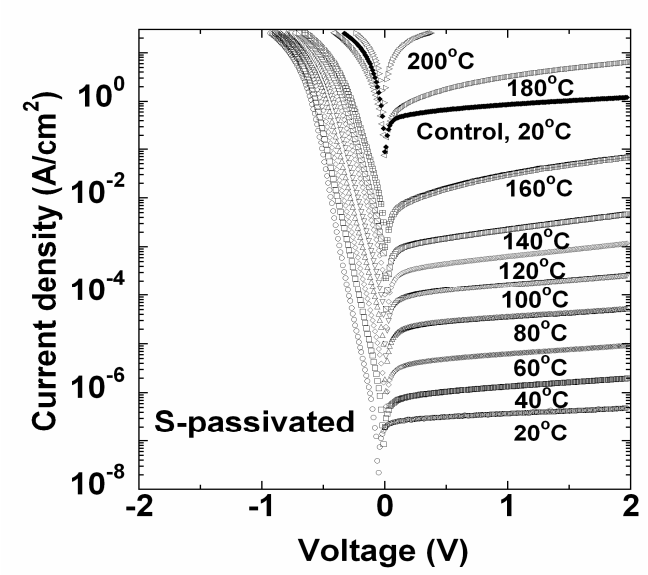


Figure 6.13 Temperature-dependent I-V measurements for Al/p-type Si(100) diodes with and without S passivation, where the bulk resistivity of Si is 0.2-0.3 Ω-cm. The reverse saturation current is reduced over six orders of magnitude by S passivation.

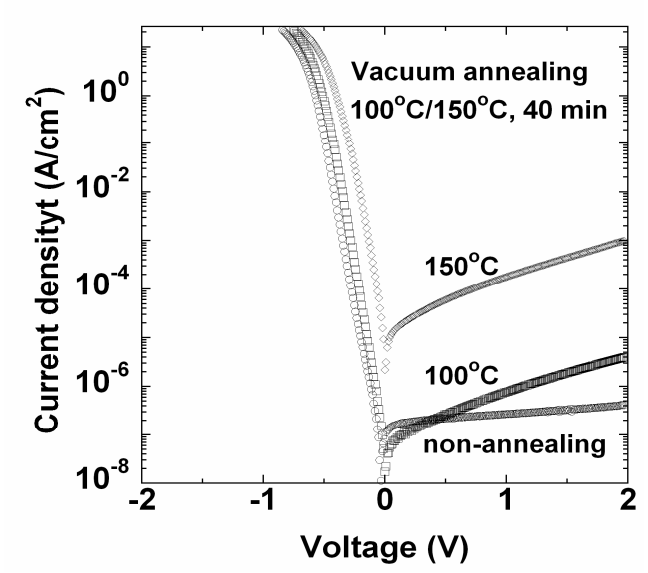


Figure 6.14. Thermalstability studies of the Al/S-passivated Si(100) diodes, which are annealed in a vacuum chamber (10^{-6} torr) for 40 min at 100ºC and 150ºC.

6.10 Summary

A high Schottky barrier of 1.1 eV is achieved between Al and S-passivated p-type Si(100) surface. The high barrier is confirmed by both C-V and activation-energy measurements. Such a high barrier leads to degenerate inversion of the p-type Si(100) surface and requires Fermi statistics to describe its electrostatics. Although this Al/S-passivated p-type Si(100) diode is fabricated like a Schottky diode, it works like a p-n junction diode. I-V measurements reveal that S passivation reduces the reverse saturation current of Al/p-type Si(100) diodes by over six orders of magnitude. Thermalstability studies of the S-passivated samples indicate that wet-chemically S-passivated Si(100) surface is not thermally stable.

CHAPTER 7

HIGH SCHOTTKY BARRIER ON N-TYPE SI(100)

The Chapter 6 has demonstrated Al/S-passivated p-type Si(100) diodes with a world-record barrier height of 1.1 eV. Following this, a continuing work is to obtain a high Schottky barrier between high work-function metals and S-passivated n-type Si(100). To realize this, high work-function metals such as Pt (ϕ_M = 5.65 eV) and Ni (ϕ_M = 5.15 eV) are selected. Two different types of n-type Si(100) are used, one is moderately arsenic (As) doped Si with resistivity between 0.075-0.085 Ω-cm, which corresponds to basically same doping level of ~1×10^{17}/cm^3 as previous p-type Si(100), and the other is low phosphorus (Ph) doped Si with resistivity between 1-2 Ω-cm, which corresponds to doping level about 6×10^{15}/cm^3. It was observed that the extracted barrier height is more or less dependent on the doping levels.

7.1 Experimental

Two different types of n-type Si(100) wafers are used in the experiment. The first is arsenic (As) doped Si with resistivity between 0.075-0.085 Ω-cm. The other is phosphorus (Ph) doped Si with resistivity between 1-2 Ω-cm. Three sets of experiments were conducted using As doped Si wafers, while the different metal electrodes are tested, including Pt, Ni, or Pt with several angstroms of Ni as adhesion layer. Using Ni as adhesion layer is due to the weak adhesion between Pt and Si surface. One set of experiments were conducted using low Ph doped Si wafers, and the metal electrode is just Ni. The diode fabrication process is similar to Al on p-type Si(100). Figure 7.1

shows a Schottky-contact structure of Pt or Ni on S-passivated n-type Si(100) that contains multiple identical single diodes. Capacitance-voltage (C-V) and current-voltage (I-V) were performed on the diodes built on As doped n-type Si(100). Additional temperature-dependent I-V measurements were only performed on the diodes built on Ph doped n-type Si(100).

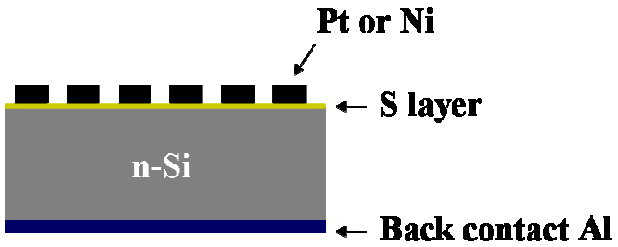


Figure 7.1 The Schottky diodes made by Pt or Ni on S-passivated n-type Si(100).

7.2 Pt/S-pasivated As doped n-type Si(100) diodes and control diodes

The ideal barrier height between Pt and n-type Si(100) is 1.60 eV according to Mott-Schottky theory, $\phi_{Bn} = \phi_M - \chi$, assuming Pt work-function ϕ_M = 5.65 eV and Si electron affinity χ = 4.05 eV. The ideal barrier height of 1.60 eV is unable to achieve. Assuming it is true, such a high barrier will cause an extremely thin potential well near the interface that is transparent to the carriers. Because of this, the real barrier height should be far less than the ideal barrier height. Our interest here is that, is it possible to obtain a high Schottky barrier that can cause degenerate inversion on Si surface between Pt and S-passivated n-type Si(100) with doping level of $1\times10^{17}/cm^3$?

7.2.1. C-V characteristics of Pt/S-passivated As doped n-type Si(100) diodes

Figure 7.2 shows the measured C-V curves and $1/C^2$-V characteristics of Pt/S

passivated As doped n-type Si(100) diodes at frequency of 1 MHz. The measured C-V curves and $1/C^2$-V characteristics at low frequencies are not shown. The extracted barrier height from $1/C^2$-V characteristics is 1.06 eV. Figure 7.3 shows the energy-band diagram of this n-type Schottky diode with barrier height of 1.06 eV. At this barrier height, the valence band is 0.06 eV below the Fermi-level.

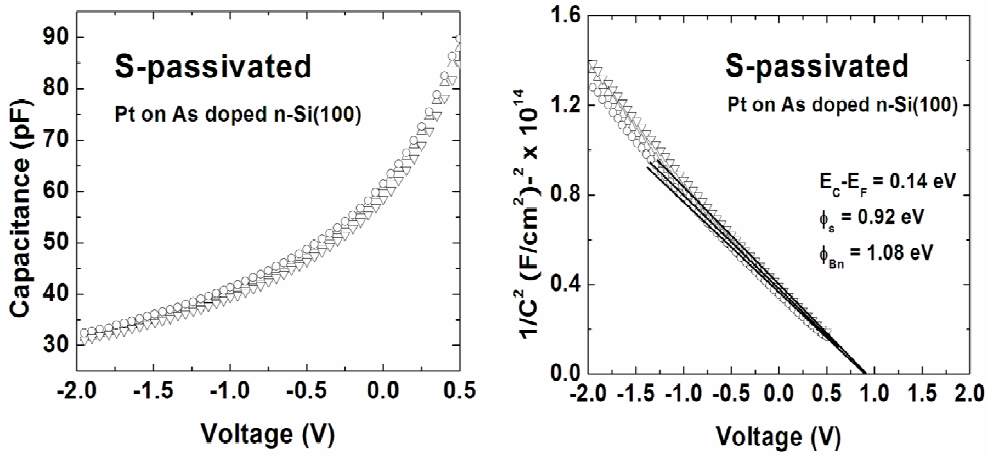


Figure 7.2 The measured C-V and $1/C^2$-V characteristics of Pt/S-passivated As doped n-type Si(100) diodes at frequency of 1 MHz.

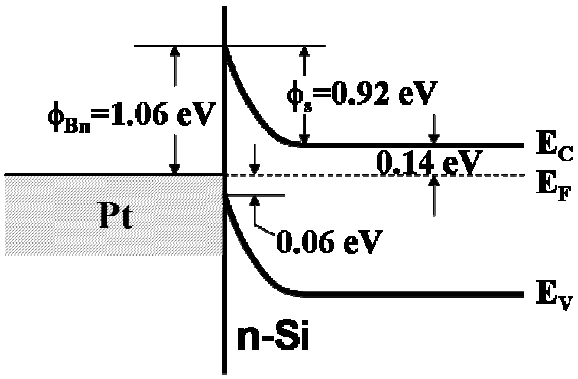


Figure 7.3 Energy-band diagram of Pt on a n-type Si(100) with 1.06-eV barrier height.

7.2.2. C-V characteristics of Pt/As doped n-type Si(100) control diodes

Figure 7.4 shows the measured C-V curves and $1/C^2$-V characteristics of Pt/As doped n-type Si(100) control diodes at frequency of 1 MHz. $1/C^2$-V characteristics expresses a strange behavior, the expected straight lines bent at low reverse bias. The extracted barrier height is 0.67 eV by using the straight part of the curves near the zero bias. It was observed that the capacitance even had 50 pF near the forward bias of 0.5 V. This is impossible for a Schottky diode with low barrier height of 0.67 eV because at this barrier height forward bias of 0.5 V will completely cause an ohmic behavior. It means no capacitance reading at all from the measured C-V curves. This strange phenomenon might attribute to the weak adhesion between Pt and Si surface, which also causes a strange I-V behavior.

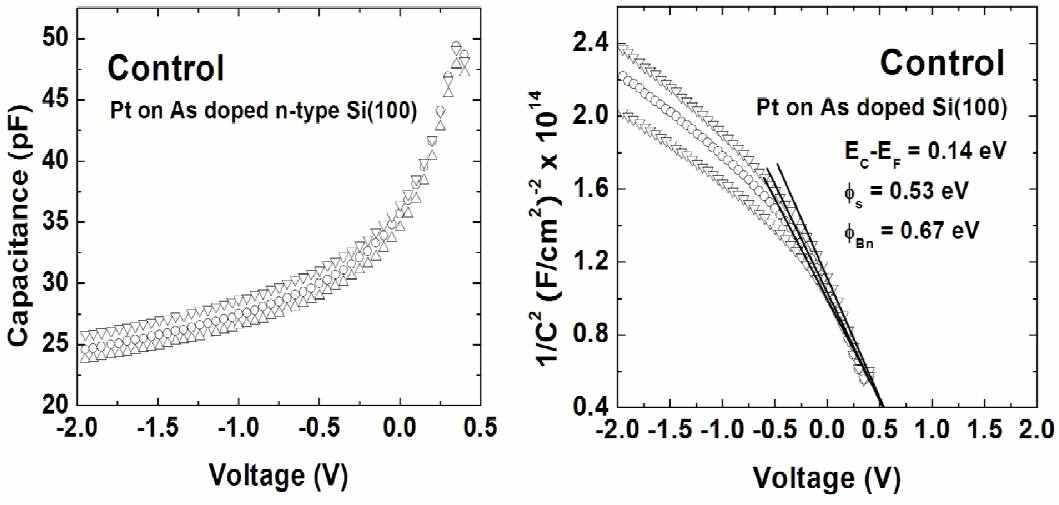


Figure 7.4 The measured C-V and $1/C^2$-V characteristics of Pt/ As doped n-type Si(100) control diodes at frequency of 1 MHz.

7.2.3. I-V characteristics of Pt/S-passivated As doped n-type Si(100) diodes and control diodes

The I-V characteristics of both S-passivated samples and control samples are plotted in same figure shown in Figure 7.5. The S-passivated samples gave the reverse current density almost two orders higher than the control samples. This contradicts the high barrier height extracted from S-passivated samples. The high barrier height should correspond to a low reverse current. Besides this, the series resistance R_s for S-passivated samples is also higher than the control samples, which is disclosed by the lower slope in the forward current region than control samples. Such a phenomenon is not observed for Al on p-type Si(100) where the I-V curves for S-passivated samples even gives a lower series resistance than control samples. The experiments for Pt on As doped n-type Si(100) were repeated several times, and they all produced similar results.

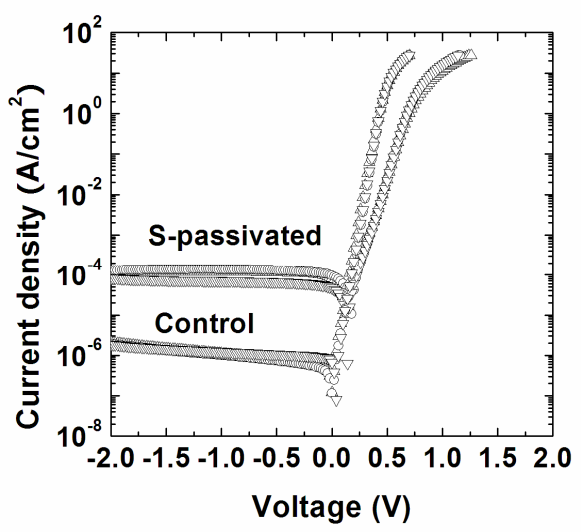


Figure 7.5 The I-V characteristics of Pt/S-passivated As doped n-type Si(100) diodes and control diodes.

The conclusion made here is that S-passivation seems not to improve the interface properties between Pt and Si(100) surface. This should attribute to the weak adhesion between Pt and Si(100) surface. The weak adhesion means a gap between Pt and Si(100) surface, which might behave like a variable capacitor serially connected to Pt/As doped n-type Si(100) diodes, making the S-passivated Si(100) surface invalid to improve the diode performances.

7.3 Ni/S-passivated As doped n-type Si(100) diodes and control diodes

Some strange behaviors in both C-V characteristics and I-V characteristics were observed from Pt/As doped n-type Si(100) diodes. These unstable diode performances for Pt/S-passivated As doped n-type Si(100) can not consolidate the barrier height of 1.06 eV extracted from the $1/C^2$-V characteristics. Ni is supposed to be a good candidate because it has no adhesion problem with Si surface and its work-function of 5.15 eV can lead to a 1.1 eV ideal barrier height, comparative to Al/S-passivated p-type Si(100).

7.3.1. $1/C^2$-V characteristics of Ni/S-passivated As doped n-type Si(100) diodes and control diodes

The measured C-V curves for both Ni/S-passivated samples and control samples are not shown because they have basically same curve shape as Pt on n-type Si(100) diodes. Several rules are helpful to remind the C-V curve shape for both metal on n-type semiconductor and p-type semiconductor. For example, the metal on n-type semiconductor, the positively applied voltage is forward bias and the negatively applied voltage is reverse bias. When the reverse bias is applied, the capacitance is decreased with the increasing of the applied voltage because the depletion region is getting wider

till it reaches a maximum. The capacitance is inversely proportional to the width of depletion region according to C=ε/W, where C is capacitance, ε is the medium permittivity and W is the width of the depletion region. The highest capacitance is usually measured in the region near zero bias, and then suddenly drops or disappears with applied forward bias because the capacitor is changed to a conductor with a small resistance. The same rules can be applied to metal on p-type semiconductor, where the positively applied voltage is reverse bias and the negatively applied voltage is forward bias. All these are clearly illustrated in Figure 7.6. Based on these understandings, the measured C-V curves will not be demonstrated in later sections, and the $1/C^2$-V characteristics will be given only.

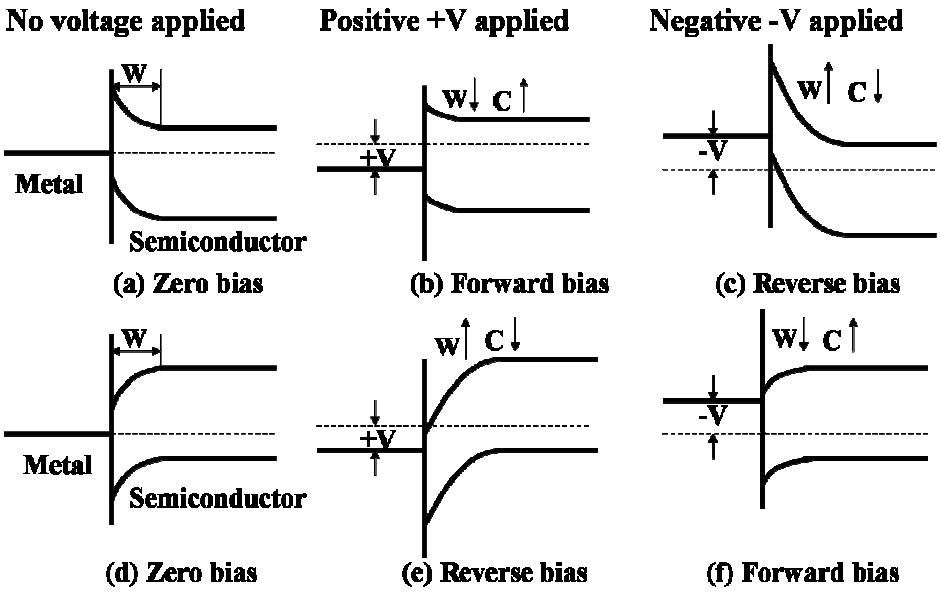


Figure 7.6 Energy-band diagrams for metal on n-type semiconductor-(a), (b) and (c), and p-type semiconductor-(d), (e) and (f) under zero bias, forward bias and reverse bias. These diagrams clearly show how the depletion width W changed with applied voltage, and the dependence of capacitance on the depletion width.

Figure 7.7 shows the $1/C^2$-V characteristics for both Ni/S-passivated Si(100) samples and control samples without S passivation. The barrier height extracted from the Ni/S-passivated samples is 0.93 eV, about 0.2 eV higher than the control samples without S passivation. The barrier height of 0.93 eV is about 0.2 eV lower than the ideal barrier height of 1.1 eV between Ni and n-type Si. The discrepancy can be explained by the barrier decrease due to S-Si dipole moment on the surface, which has been discussed in Chapter 6.3.

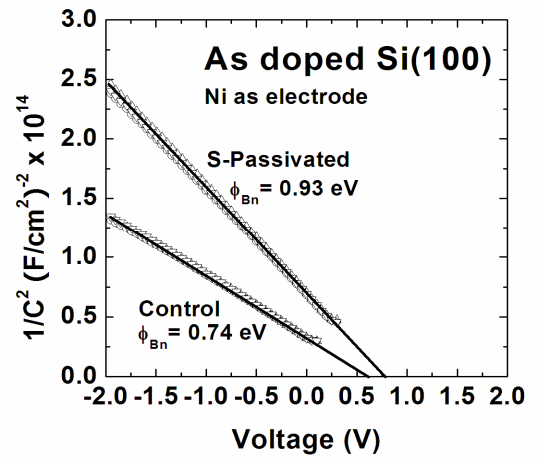


Figure 7.7 The $1/C^2$-V characteristics of Ni/S-passivated As doped n-type Si(100) diodes and control diodes.

7.3.2. I-V characteristics of Ni/S-passivated As doped n-type Si(100) diodes and control diodes

Figure 7.8 shows the I-V characteristics for both Ni/S-passivated As dopded n-type Si(100) samples and control samples without S passivation. The current density for S-passivated samples is about three orders lower than the control samples. This is consistent with the relatively high barrier height obtained from S-passivated samples. However, the reverse currents for both S-passivated samples and control samples are

much higher than the expected values with respect to the flat-band barrier height of 0.93 eV and 0.74 eV, respectively. It was observed that for both types of samples the reverse currents significantly rise up with applied reverse bias, indicating the high edge-leakage current that is field-dependent. Another contribution causing high reverse current might be from tunneling current because the As doped n-type Si(100) wafer is near-highly doped with resistivity between 0.075-0.085 Ω-cm [81] , which is three times lower than previous p-type Si(100) wafer.

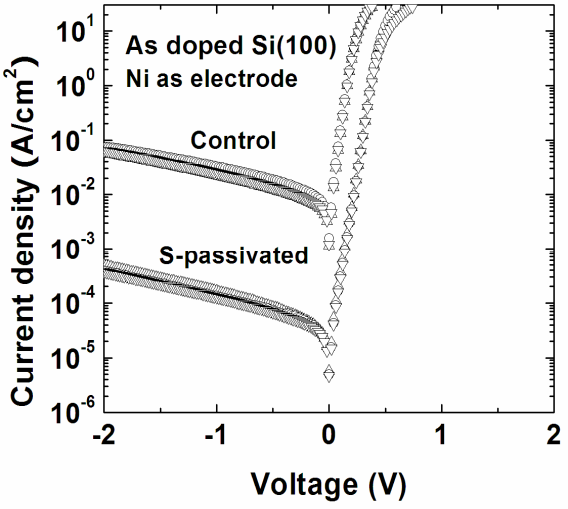


Figure 7.8 The I-V characteristics of Ni/S-passivated As doped n-type Si(100) diodes and control diodes.

7.4 Pt/S-passivated As doped n-type Si(100) diodes and control diodes with Ni as adhesion layer

To obtain the high Schottky barrier on n-type Si, Pt/Ni as electrodes has been tested on S-passivated As doped n-type Si(100) . The barrier height extracted from $1/C^2$-V characteristics of Pt/S-passivated As doped n-type Si(100) diodes is 1.06 eV, which is not confirmed by I-V measurements because the weak adhesion between Pt

and Si surface. The barrier height extracted from $1/C^2$-V characteristics of Ni/S-passivated As doped n-type Si(100) diodes is 0.93 eV, which is lower than the ideal barrier height of 1.1 eV due to the barrier decrease resulting from S-Si dipole moment on the surface. The reverse current density for this type of diodes might be dominated by edge-leakage current or tunneling current due to the near-highly doped Si substrate.

Is there any way to still utilize the high work-function metal Pt meanwhile avoiding the adhesion problem between Pt and Si surface to obtain an even higher Schottky barrier?

The method was attempted with a 5-Å Ni as adhesion layer between Pt and Si surface. This ultrathin Ni layer should slightly tune Pt work-function to somehow a lower level but solve the adhesion problem. However, the fabricated diodes using this method did not improve the diode performances. The $1/C^2$-V characteristics (Figure 7.9) and the I-V characteristics (Figure 7.10) for these fabricated diodes are quite similar to those with Ni itself as electrodes. The subsequent attempts using 10-Å/15-Å Ni as adhesion layer gave similar results. This indicates that the interface property could be well-defined by a thin metal layer even with several angstroms. Another explanation is that, the interface property has to be defined by a thick metal layer at least in tens of angstroms [82]. If this is true, it means that the 5-Å Ni layer given by thickness monitor might be wrong, and the grown Ni layer by e-beam evaporator could be much thicker than 5 Å, causing a Ni-defined interface, so that the barrier height for S-passivated samples is only dependent on Ni work-function and electron affinity of Si. Due to the difficulty of the thickness control by e-beam evaporation, this method left no answer but

it is worth to be investigated if a more precisely controlled thickness monitor is available.

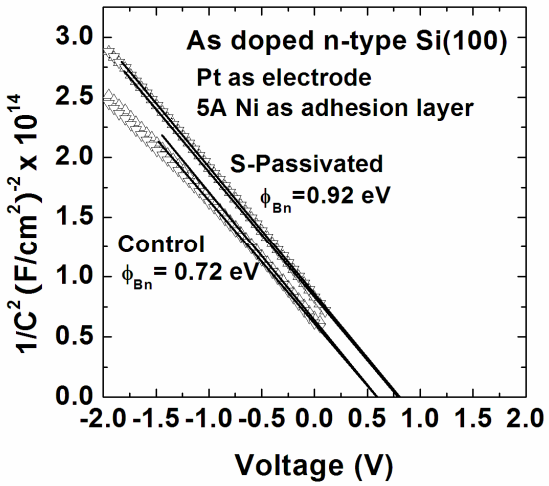


Figure 7.9 The $1/C^2$-V characteristics of Pt/S-passivated As doped n-type Si(100) diodes and control diodes. A 5-Å Ni underneath Pt is to serve as an adhesion layer.

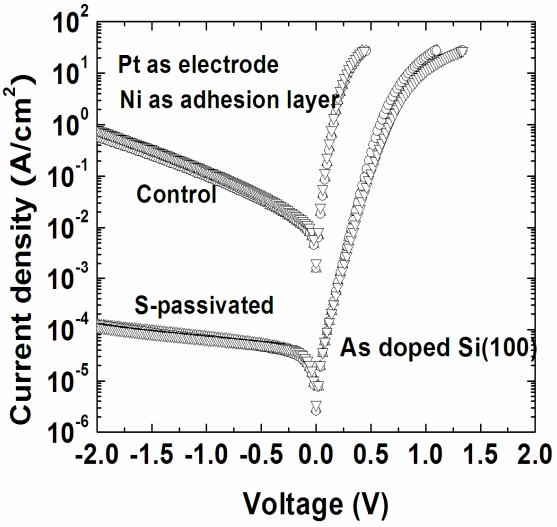


Figure 7.10 The I-V characteristics of Pt/S-passivated As doped n-type Si(100) diodes and control diodes. A 5-Å Ni underneath Pt is to serve as an adhesion layer.

7.5 Ni/S-passivated Ph doped n-type Si(100) diodes and control diodes

As mentioned in sections 7.3 and 7.4, the near-highly doped n-type Si(100) substrates might be a reason causing unexpected high reverse current. To avoid this, a low Ph doped n-type Si(100) substrates with resistivity between 1-2 Ω-cm are used. The Ni itself is used as electrode.

7.5.1. $1/C^2$-V and I-V characteristics for Ni/S-passivated Ph doped n-type Si(100) diodes and control diodes

The barrier height extracted from $1/C^2$-V characteristics (Figure 7.11) for Ni/S-passivated Ph doped n-type Si(100) diodes is 0.97 eV, about 0.04 eV higher than Ni/S-passivated As doped n-type Si(100) diodes (See 7.3). The extracted doping concentration is about $6\times10^{15}/cm^3$, which matches the wafer specification (ρ=1-2 Ω-cm).

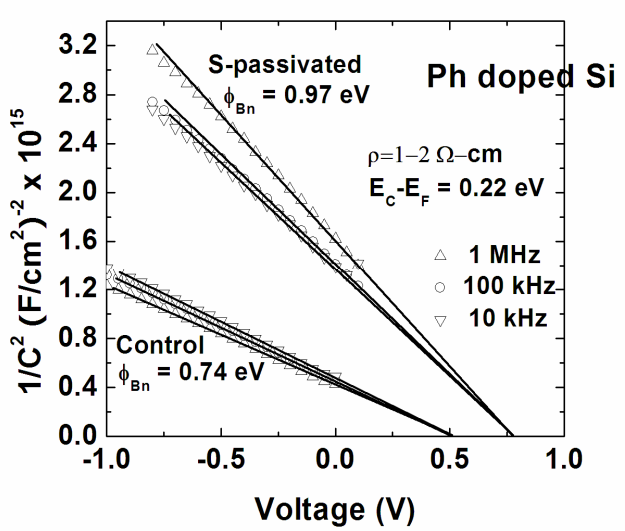


Figure 7.11 The $1/C^2$-V characteristics of Ni/S-passivated Ph doped Si(100) diodes and control diodes.

Based on this doping level, the difference between the conduction band E_C and the Fermi level E_F is 0.22 eV. Figure 7.12 shows the energy-band diagram of Ni/S

passivated Ph doped n-type Si(100). The barrier height for control samples almost remains unchanged in comparison with using As doped n-type Si(100) as substrate.

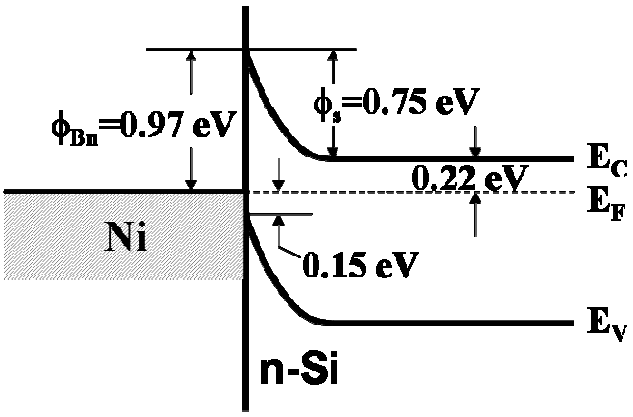


Figure 7.12 Energy-band diagram for Ni/S-passivated Ph doped n-type Si(100) with 0.97eV barrier height.

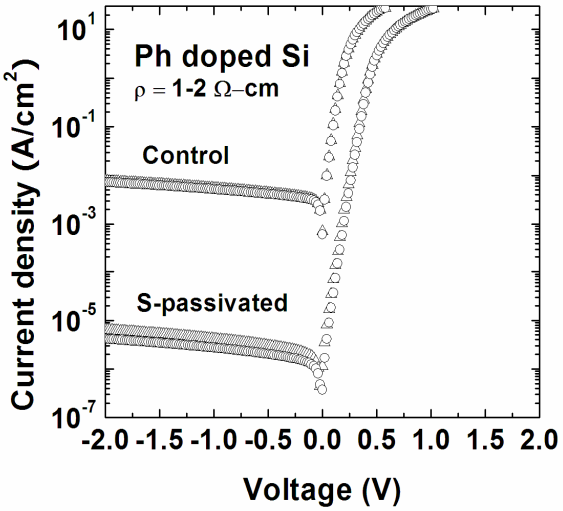


Figure 7.13 The I-V characteristics of Ni/S-passivated Ph doped Si(100) diodes and control diodes.

The reverse current density for Ni/S-passivated low Ph doped Si(100) (Figure 7.13) is about 4×10^{-6} A/cm^2, which is more than three orders less than the control diodes.

If this diode compares with the Al/S-passivated p-type Si(100) diode, its reverse current density is only one order higher due to ~0.1 eV barrier decrease.

The forward current fitting (Figure 7.14) by thermionic emission model for S-passivated samples gave an effective barrier height of 0.74 eV and high ideality factor of 1.2 due to the limitations of this model in high barrier measurement. Another reason might be attributed to inhomogeneity in barrier height, i.e., the existence of a few low-barrier regions in the Schottky diode. These have been explained in Chapter 6.7.

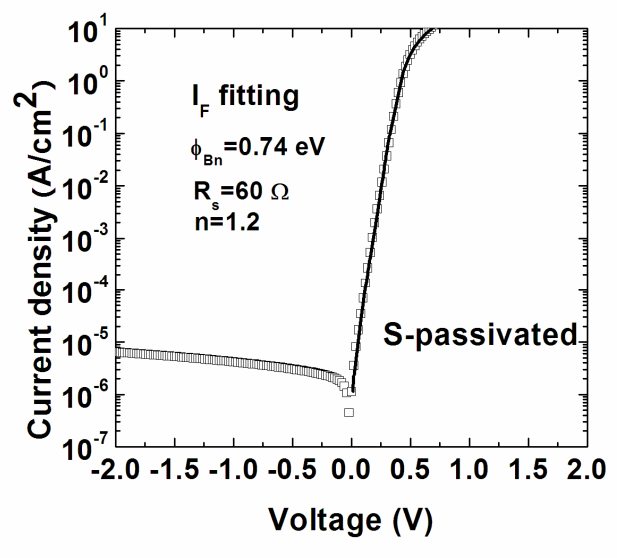


Figure 7.14 I_F fitting of Ni/S-passivated Ph doped n-type Si(100) diodes.

7.5.2. Barrier height extracted from activation-energy plot

Another method to extract barrier height is from the activation-energy plot, which is shown in Figure 7.15. The temperature range is selected from 20°C-140°C, a standard range for I_F-fitting. The forward current density at 0.02 V-0.08 V are used for the fitting. The extracted barrier height ϕ_{Bn} is between 0.80-0.82 eV, about 0.15 eV

lower than the flat-band barrier height extracted from $1/C^2$-V characteristics. The reason is that the extracted barrier height from the activation-energy plot is averaged over the temperature range (See Chapter 6.6).

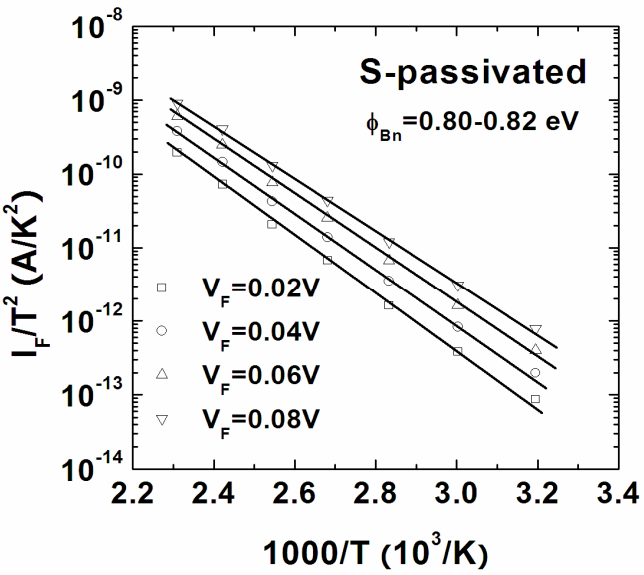


Figure 7.15 Determination of Schottky barrier height from activation-energy measurements for Ni/S-passivated Ph doped n-type Si(100) diodes with a bulk resistivity of 1-2 Ω-cm. Forward current is used to extract the barrier height at several voltages.

7.5.3. Temperature-dependent I-V characteristics for Ni/S-passivated Ph doped n-type Si(100) diodes

The barrier height of 0.97 eV for Ni/S-passivated Ph doped n-type Si(100) diodes does not result in the degenerate inversion on Si surface. The energy-band diagram shown in Figure 7.12 shows that the valence band is 0.15 eV lower than Fermi level. However, this barrier height causes a low reverse current density of ~10^{-6}A/cm^2, comparative to that of Al/S-passivated p-type Si(100) diodes. Such a low reverse current for n-type Si diodes also arise our interest to investigate the effect of elevated temperatures on the reverse current. Figure 7.16 shows the temperature-dependent I-V

measurements for Ni/S-passivated Ph doped n-type Si(100) diodes. The reverse current is increased with the elevated temperatures. This is due to barrier height lowering with the elevated temperatures. Unlike the Al/S-passivated p-type Si(100) diodes, the I-V rectification for Ni/S-passivated n-type Si diodes still remains at 200°C. Due to the facility limitation, the measurements of I-V above 200°C were not conducted. This phenomenon seems impossible due to unstable S passivation indicated by thermalstability studies for Al/S-passivated p-type Si(100) (See Chapter 6.8). A reasonable explanation might be due to the Ni silicidation at temperature around 200°C [83]. The formed Ni silicide phase can still assist the barrier height without a big drop at high temperature.

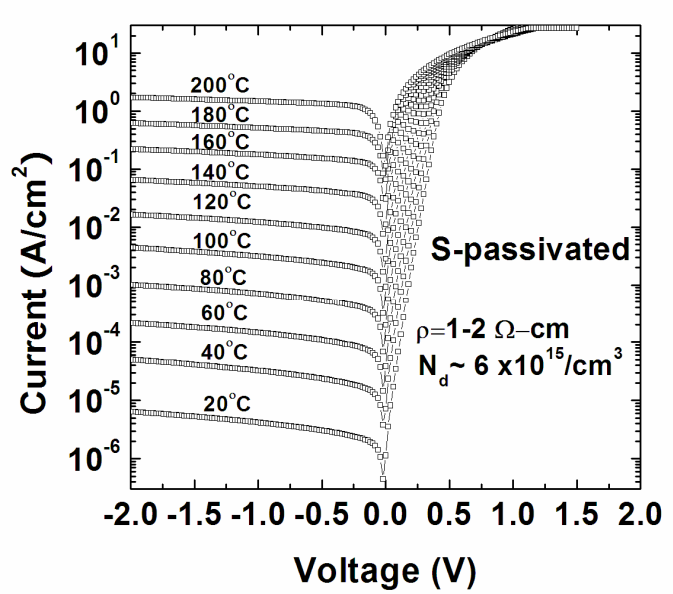


Figure 7.16 Temperature-dependent I-V measurements for Ni/S-passivated Ph doped n-type Si(100) diodes, where the bulk resistivity of Si is 1-2 Ω-cm.

7.6 Summary

A 1.1 eV barrier height obtained from the Al/S-passivated p-type Si(100) diodes prompts a similar work conducted on n-type Si(100). In accordance with Mott-Schottky theory, high work-function metals such as Pt and Ni are used for this purpose. Two different n-type Si(100) wafers are used for the substrates, one is near-highly As-doped Si(100) and the other is low Ph doped Si(100). The Pt/S-passivated As doped Si(100) diodes gave a high Schottky barrier of 1.06 eV, which is not convinced by I-V characteristics because of the weak adhesion between Pt and Si surface. The Ni/S-passivated As doped Si(100) diodes gave the barrier height of 0.92 eV, which is lower than the ideal barrier height of 1.1 eV due to the barrier decrease resulting from S-Si dipole moment on the surface. The only concern for this type of diodes is an unexpected high reverse current. This might be due to either edge-leakage current or tunneling current because the near-highly doped Si substrates are used. Using Ni as adhesion layer for Pt/S-passivated As doped Si(100) diodes does not improve the diode performances.

Finally, the Ni/S-passivated low Ph doped Si(100) diodes gave a extremely high Schottky barrier about 0.97 eV, resulting in low reverse current of ~10^{-6} A/cm^2. The barrier height of 0.97 eV does not cause the degenerate inversion on Si surface. The dependence of Schottky barrier on the doping levels is not investigated in this wok.

CHAPTER 8

DIFFUSION-FREE BACK CONTACT SOLAR CELLS

Chapter 6 and Chapter 7 introduced the important work to obtain the extremely high Schottky barriers between metal and p-type Si(100) or n-type Si(100), in which the "valence-mending concept" is applied, and experimentally realized by a wet-chemical S passivation. By engineering the Si(100) surface using closely monolayer S passivation, the surface states are significantly removed, making it possible an ideal barrier height between metals and S-passivated Si(100) surface. Proper selection of the metals, such as low work-function metals for p-type Si(100) and high work-function metals for n-type Si(100), the extremely high Schottky barriers can be achieved

From our experimental results, the barrier height of 1.1 eV was achieved with Al/S-passivated boron (B) doped p-type Si(100) diodes and 0.97 eV for Ni/S-passivated phosphorus (Ph) doped n-type Si(100) diodes. Investigations of energy-band diagrams disclose that the barrier height of 1.1 eV results in degenerate inversion on Si surface, making this type of diodes behave like a p-n junction diodes, i.e., holes are injected from the p-type bulk and electrons from the n-type surface under forward bias. Such a junction is actually field-induced free of any diffusion or ion implantation process that needs high energy input.

In this chapter, our task is to integrate the self-developed S-passivation technique into the fabrication of solar cells where the diffused p-n junction is replaced with the field-induced junction, or in other words a diffusion-free p-n junction. This is

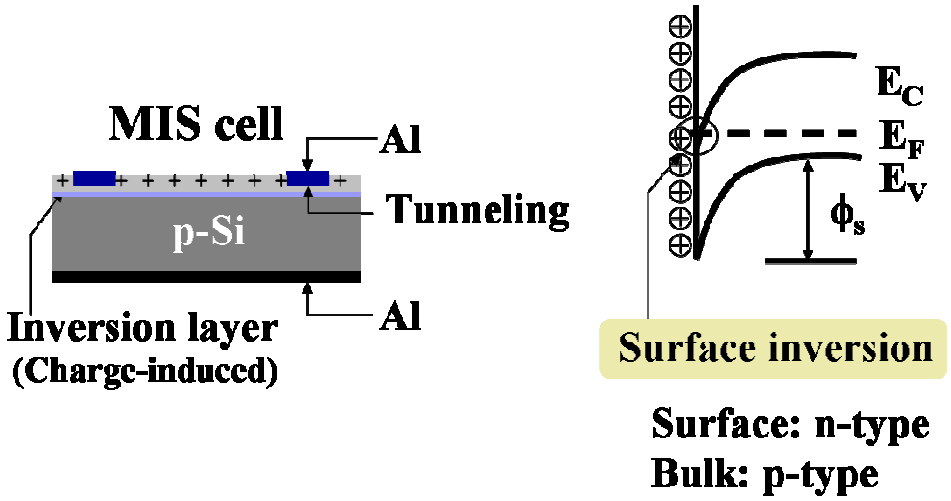
an absolutely new method which enables a low-cost process and worth to try whatever success or fail.

8.1 MIS solar cells

Back to Chapter 2, a typical conventional solar cell and three historical back-contact solar cells have been simply introduced. The difference among these cells is how to position emitter region and back-surface field. The emitter is usually a diffused p^+-n/n^+-p junction and the back-surface field is a diffused high-low (p^+-p or n^+-n) junction. The concept of diffusion-free junction as emitter used for solar cell design was first presented in a MIS structure [84,85] shown in Figure 8.1 (a). The diffusion-free junction in this structure is charge-induced due to the large amount of positive charges in the dielectric layer that will cause degenerate inversion on Si surface if p-type Si substrate is used. The energy-band diagram for this emitter region is shown in Figure 8.1 (b) where the conduction band is bent below the Fermi level, indication of degenerate inversion. The reported conversion efficiency for this type of solar cells can be above 15%.

As indicated by Figure 8.1 (a), the emitter region is on the front side of the p-type Si substrate. This design does not require an atomically flat surface, which is required for S passivation. For a crystalline Si solar cell, the front side has to be textured such as by an anisotropic etching process to enhance the light trapping, usually performed in a weak aqueous NaOH or KOH solution. The etched Si surface is unable to perform S passivation. Because of this, in the design of the proposed solar cells, the rough side of the single-side polished wafer serves as front side to be etched and the

atomically flat (shiny) side is used as back side for S passivation. Deposition of Al on S-passivated region enables a diffusion-free p-n junction or field-induced junction as the emitter region, together with the back-surface field on the same side, a new back-contact solar cell becomes possible with integration of the self-developed S passivation. This design has to consider other factors such as surface recombination velocity (SRV) and minority-carrier diffusion length that could significantly affect the conversion efficiency.



(a) (b)

Figure 8.1 Solar cell structure with a charge-induced junction as emitter region (a) and the energy-band diagram for this region (b).

8.2 Design of back contact solar cells using field-induced diffusion-free p-n junction as emitter region

8.2.1. Materials selection and sample preparation

The substrate is single-side polished boron (B) doped p-type Cz Si(100) with resistivity between 0.2-0.3 Ω-cm. Using this near-highly doped substrate is because the

1.1-eV barrier height causing diffusion-free p-n junction is obtained from it. Usually, the highly doped Cz Si is supposed to have a low minority-carrier diffusion length that will be a reason for the low conversion efficiency for the fabricated solar cells. So the Si substrates possessing a high minority-carrier lifetime (or diffusion length) might/should be used. This type of substrates is usually highly-purified float zone (Fz) Si. A conventional solar cell built on Fz Si with 0.2-0.3 Ω-cm resistivity can give conversion efficiency about 19% [86]. The bulk minority-carrier lifetime for the used Cz Si is not measured, how this affects the conversion efficiency remains unknown.

A basic requirement for the back-contact solar cell design is that the bulk minority-carrier diffusion length should be higher than the wafer thickness. The ratio between diffusion length and wafer thickness is usually at least 3 [87] to ensure the generated carriers in the bulk successfully diffused to the collecting contacts on the back side.

The wafer thickness for most of back-contact solar cells is around 200 μm or even less. Since the thickness of the wafers used in this experiment is about 380 μm, much thicker than the bottom-line of 200 μm, it has to be reduced. The method is mechanical grinding introduced in next section.

8.2.2. Cell fabrication

The samples with area of 2×2 cm^2 were cut from the single-side polished B doped 3 inch Cz Si wafers with resistivity between 0.2-0.3 Ω-cm. These samples were first etched in 2% HF for 60 seconds to remove native oxide and followed by DI water rinsing for 2 minutes. After that, the thick SiO_2 layer ~4000 Å was grown on the

samples by wet oxidation (PECVD preferred-facility issue) to protect the shiny side. The rough side of the samples was then mechanically grinded, making the samples thinned down to 200 μm. After thinning process, the samples were ultrasonically cleaned in acetone and followed by IPA rinsing to remove the organic contaminations. The native oxide on the rough side was etched off by 2% HF for 60 seconds and then the samples were rinsed by DI water for 2 minutes. After this step, the well-cleaned samples with required thickness are ready for further processing. Figure 8.2 shows the most of the important steps of the cell design. Each step number in Figure 8.2 corresponds to the number-matched subtitle described as below.

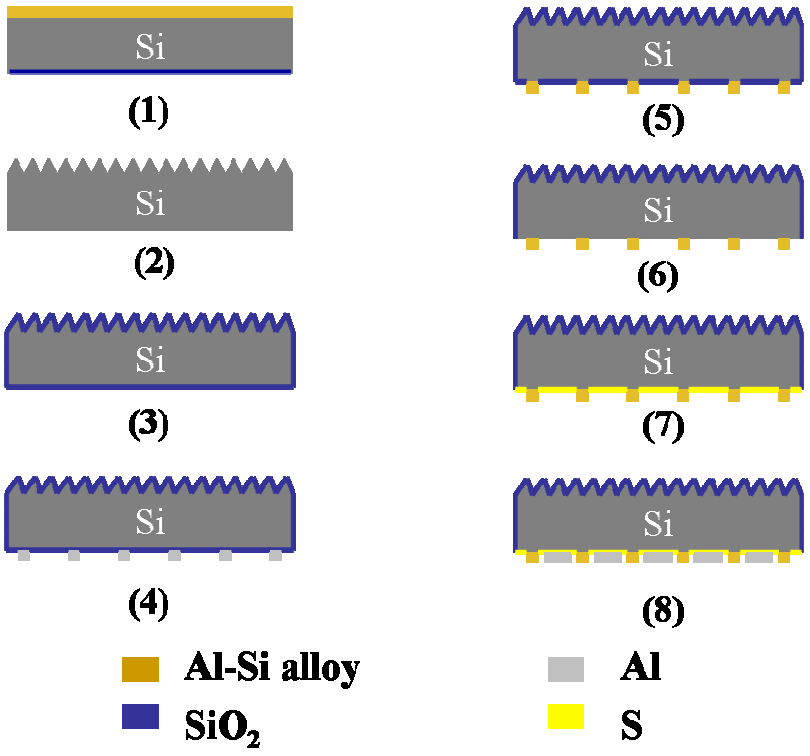


Figure 8.2 The process flow for the proposed diffusion-free back contact solar cells.

8.2.2.1 Al gettering

The samples used in this experiment are Cz Si that may possesses a low bulk minority-carrier lifetime that corresponds to a low diffusion length. Al gettering step is a regular method used in industry to absorb the bulk impurities to the molten Al-Si alloy, thus reducing the bulk defects-the recombination-center terminating the carrier transportation. In industry, Al gettering can be preceded by alloying a screen-printed thick Al layer up to 20 μm on Si at high temperature (~800°C) with a short period (1-5 min) [19,20]. In this experiment, instead of screen-printing method, the e-beam evaporated 1 μm Al on Si was used for the gettering step, which was performed by a rapid temperature annealing (RTA). The annealing condition is at 800°C for 3 min.

8.2.2.2 Removal of Al-Si alloy and front surface texturing

After Al gettering step, the samples were put into the 20% NaOH solution to etch off the Al-Si alloy at 80°C for 30 minutes [88]. Under this condition, the 30-40 μm material can be etched off including Al-Si alloy and part of Si behind it. The other side (shiny side) is still thick SiO_2 covered because the low etching rate for SiO_2 in 20% NaOH solution. After etching, the original rough side shows a polishing surface, which is supposed to be free of most of damages and defects on the surface.

The samples were then put into 2-3% NaOH solution with addition of 10% IPA in volume for an anisotropic etching to create micro-sized pyramids on the surface [89-91]. The optimized etching condition was found to be at 80°C for 30 minutes with a magnetic bar rotating at 600 rpm on the bottom of the etching container. Figure 8.3 shows the SEM images for the etched Si surface at different etching conditions. The

etched Si surface with covering of micro-sized pyramids can significantly reduce the reflectance R, and thus enhance the light trapping. Normally the reflectance for a polished Si surface is above 30% and it can drop to about 10% with a well-textured Si surface. After surface texturing, the SiO_2 on the shiny side was removed by the buffer-oxide etchant.

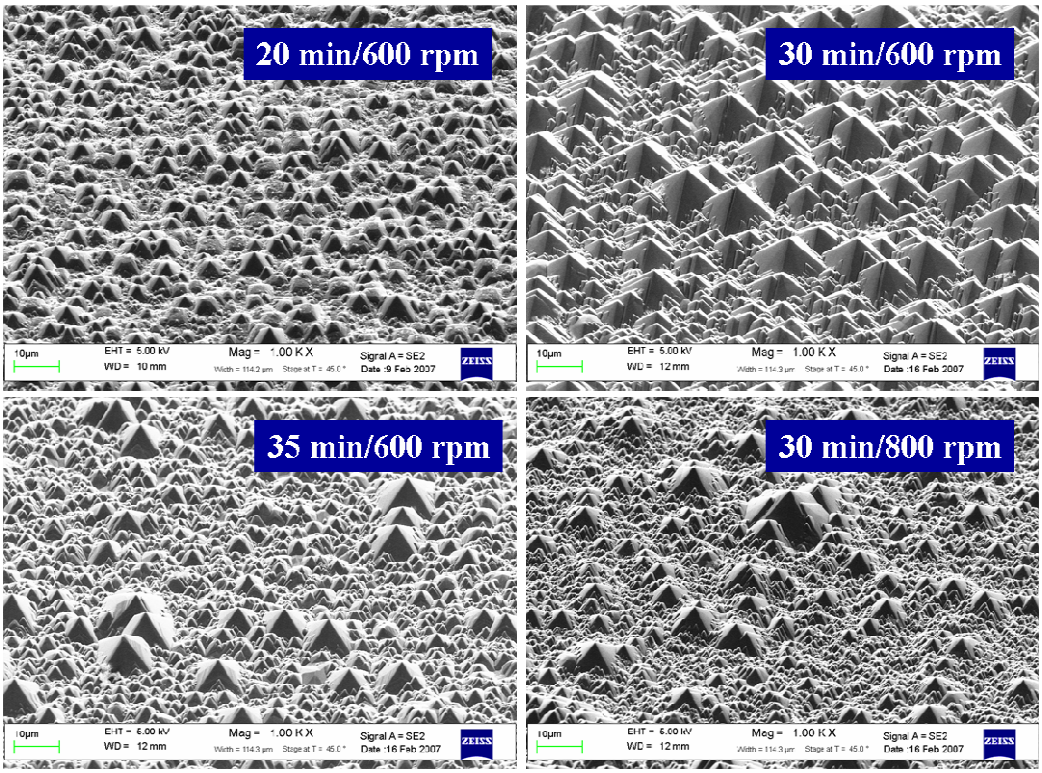


Figure 8.3 SEM images of the etched Si surface by 2-3% NaOH + 10% IPA in volume at different etching conditions. The optimized etching condition is at 80°C for 30 min with magnetic bar rotating at 600 rpm.

8.2.2.3 Surface cleaning and antireflection coating

Surface cleaning is very important after surface texturing step. It can reduce the metallic particles to a low level before a high temperature treatment. Reduction of metallic particles can somehow increase the minority-carrier diffusion length.

Traditionally, RCA cleaning is used [92]. Recently, a new IMEC-clean [93] reveals a perfect removal of metallic particles. If removal of metallic contaminations is the only issue, a single cleaning step in 1% diluted HCl yields excellent results, which is selected as the cleaning method here. The 1% HCl-cleaned Si surface also experiences a 2% HF etching and followed by DI water rinsing. This cleaning process is repeated three times.

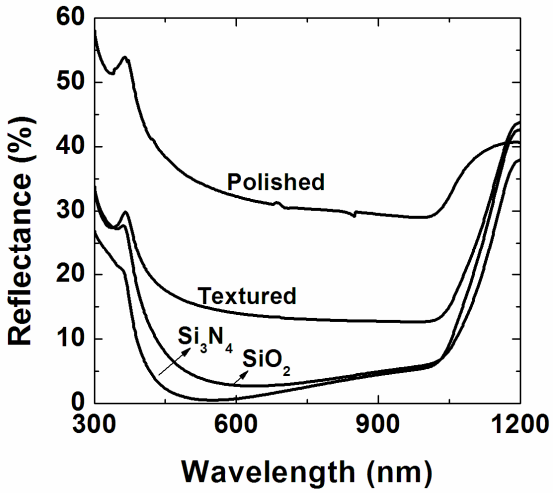


Figure 8.4 Reflectance of p-type Si(100) surfaces after texturing and antireflection coating with ~100 nm SiO_2/Si_3N_4.

Antireflection coating on the textured Si surface can further reduce the reflectance. PECVD Si_3N_4 (normally written as SiN_x: H) coating is usually used in industry [94] because firstly it has a matched index of reflection and secondly it can passivate both the surface and the bulk defects by hydrogenation step [95]. Due to the facility issue, in our experiment the SiO_2 is used to serve both antireflection coating and Si surface passivation. Figure 8.4 shows the reflectance of p-type Si(100) surfaces after polishing, texturing and antireflection coating with ~100 nm thermal-SiO_2/PECVD-

Si_3N_4. The lowest reflectance less than 1 % is observed from PECVD-Si_3N_4 coating. The surface passivation mentioned here is extremely important and will be discussed in 8.4.2.

8.2.2.4 Definition of narrow finger pattern

The conventional back-contact solar cell uses the diffused p-n junction for the emitter region and diffused high-low junction (p^+-p or n^+-n) as the ohmic contact region reducing the contact resistance and series resistance. The metallization of emitter region is wide finger-defined and the ohmic contact region is the narrow finger-defined. For the proposed diffusion-free back-contact solar cell, the emitter region is replaced with Al on S-passivated region (high barrier induced p-n junction), and the ohmic contact region is first to use Pt on S-passivated region (low barrier induced ohmic contact). The fabricated solar cell based on this design shows a bad cell performance because the ohmic contact region is not stable due to weak adhesion between Pt and Si surface. For this reason, the Al-Si alloy is used for the ohmic contact region. The narrow finger pattern is formed by e-beam evaporated 1μm Al through a designed shadow mask on 100-nm SiO_2 covered Si surface.

8.2.2.5 Al-Si alloy as ohmic contact region

The RTA annealing is used to form the Al-Si alloy. The annealing condition is at 800°C for 3 min. Once the annealing temperature is above the eutectic temperature of 577°C between Al and Si, Al can penetrate the SiO_2 layer and diffuse into the Si to form a p^+ layer or back-surface field that is highly conductive, confirmed by I-V measurements.

8.2.2.6 Removal of the rest of SiO_2 on the passivating side

The rest of SiO_2 on the shiny side was removed by buffer-oxide etchant. Before doing this, the coating side is protected by spin-coated photoresist that is stripped out after removal of SiO_2 on the shiny side. The samples were then cleaned in acetone and rinsed by IPA to remove the residual of the photoresist.

8.2.2.7 S passivation

The samples were etched in 2% HF for 60 seconds and followed by DI water rinsing. The dilute HF solution does not hurt the interface between the coated SiO_2 and Si surface due to its low etching rate to SiO_2 assuming no damage on this layer. The thickness of the coated SiO_2 may be slightly reduced due to dilute HF etching, but having minor effect on the reflectance. The samples were then grown with ~ 20 Å SiO_2 by either a RTA annealing at 800°C for 1 min or a hot-plate ozone oxidation at 500°C for 17 min. After this, the wet-chemical S passivation was performed on these samples.

8.2.2.8 Definition of wide finger pattern

After S passivation, Al with 2000 Å or less was e-beam evaporated through another shadow mask on the S-passivated region. The mask is visibly aligned with previously formed narrow finger pattern. Figure 8.5 shows the rear side and front side of the finally fabricated solar cell. The width of the wide finger is 1100 μm and the width of narrow finger is 600 μm. The gap between wide finger and narrow finger is 200 μm. The round testing dots are used to identify the S passivation quality and the markers are used for visible alignment.

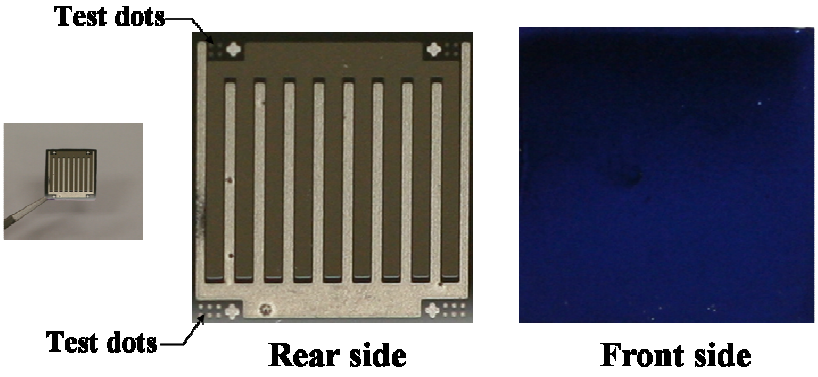


Figure 8.5 The camera-image of the fabricated back contact solar cell. The wide finger is emitter region and the narrow finger is ohmic contact region and all shown in the rear side. The test dots are used to evaluate the S passivation quality by conducting back-to-back diodes I-V measurements.

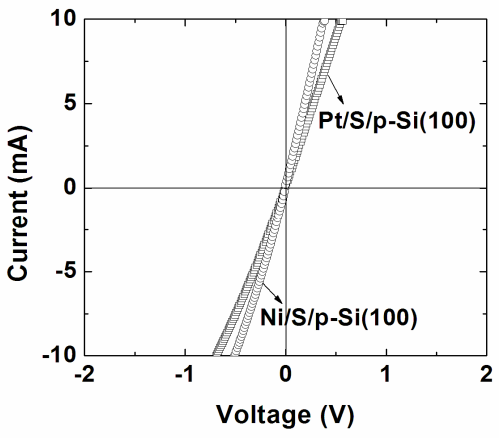


Figure 8.6 I-V measurements of back-to-back diodes made by Pt/Ni on S-passivated p-type Si(100).

8.3 Photo I-V measurements

8.3.1. Diffusion-free back contact solar cells with Al/S-passivated p-type Si as emitter region and Pt or Ni/S-passivated p-type Si as ohmic contact region

The first attempts to form the ohmic contact region are to use high work-function metals such as Pt or Ni on p-type Si. The I-V measurements shows an ohmic

behavior for the test diodes made by Pt or Ni on S-passivated p-type Si(100), which are shown in Figure 8.6. The lower slope in I-V curves for Pt/S-passivated p-type Si(100) diodes might be due to the weak adhesion between Pt on Si surface.

8.3.1.1 Pt/S-passivated p-type Si(100) as ohmic contact region

The deposition of Pt on S-passivated region was performed right after the contact formation of the diffusion-free p-n junction, making the process simplified. The drawback is that the S layer on the Si surface will experience two-time e-beam evaporation. The second deposition of Pt causes the chamber much hotter than Al deposition because of its high melting point. The hot environment will heat the samples, degrading the interface between previously deposited Al or as deposited Pt and S-passivated Si surface, and thus worsening the device performances.

Figure 8.7 shows the photo current and dark current measurements for the fabricated cells with Al/S-passivated Si region as emitter and Pt/S-passivated Si region as ohmic contact. The photo current was obtained under an illumination source with AM ~1.5. One type of cells give relatively low I_{sc} ~0.8 mA/cm^2 but relatively high V_{oc} ~ 320 mV like the cell 1 in Figure 8.7 (a), and the other type of cells give relatively high I_{sc} ~1.1 mA/cm^2 but relatively low V_{oc} ~270 mV like cell 2 in Figure 8.6 (a) as well. The relatively high V_{oc} for cell 1 is due to its lower reverse current in comparison with cell 2, which is shown in Figure 8.6 (b). The relatively high I_{sc} for cell 2 might be due to its low series resistance in comparison with cell 1, indicated by a high slope of its forward I-V shown in Figure 8.6 (b). All cells have a low fill factor FF around 0.40, which can be improved by a 4 wire measurements by reducing the contact resistance.

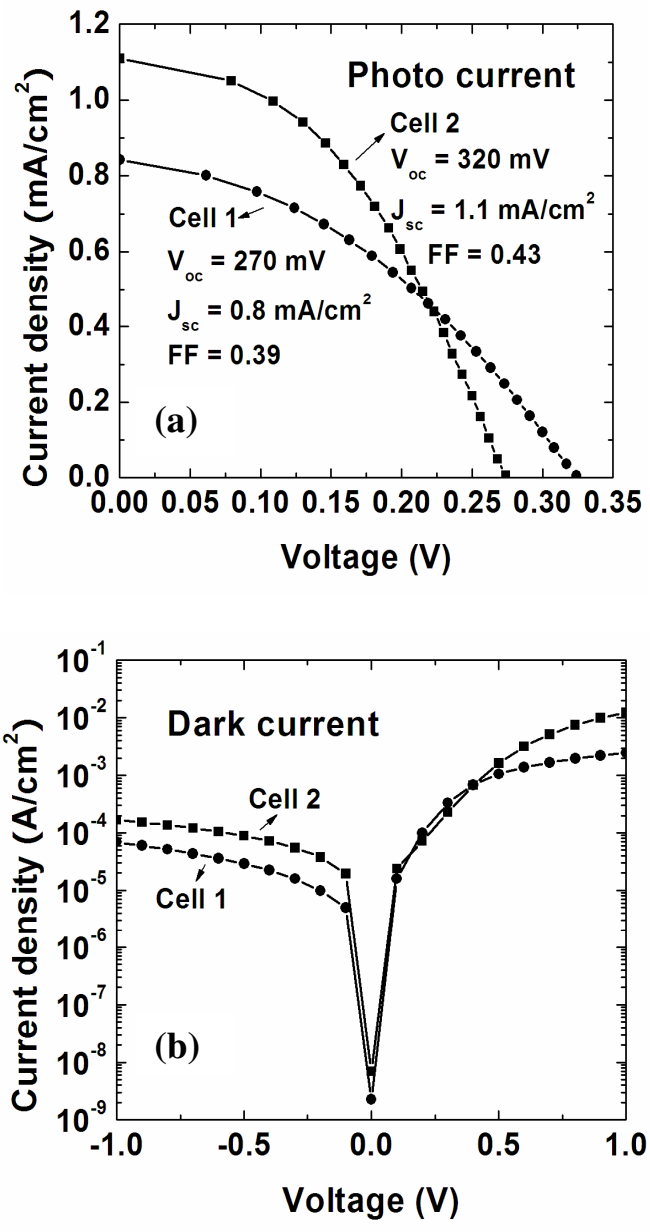
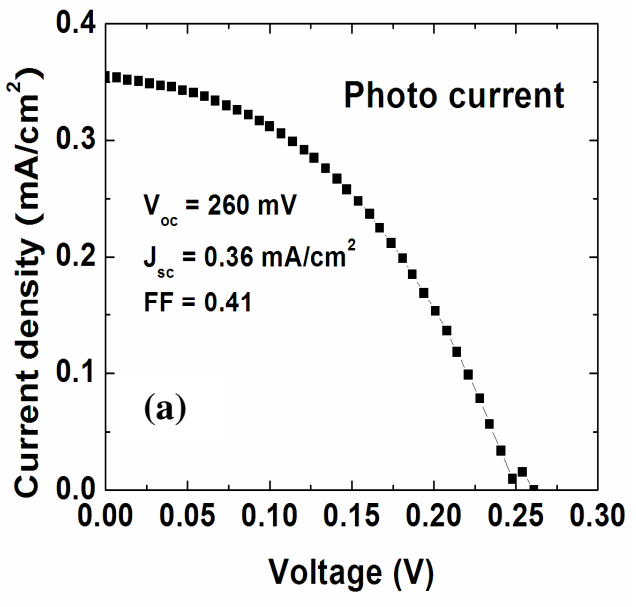


Figure 8.7 Photo (a) and dark (b) I-V for the fabricated cells with Pt/S-passivated p-type Si(100) as ohmic contact region.



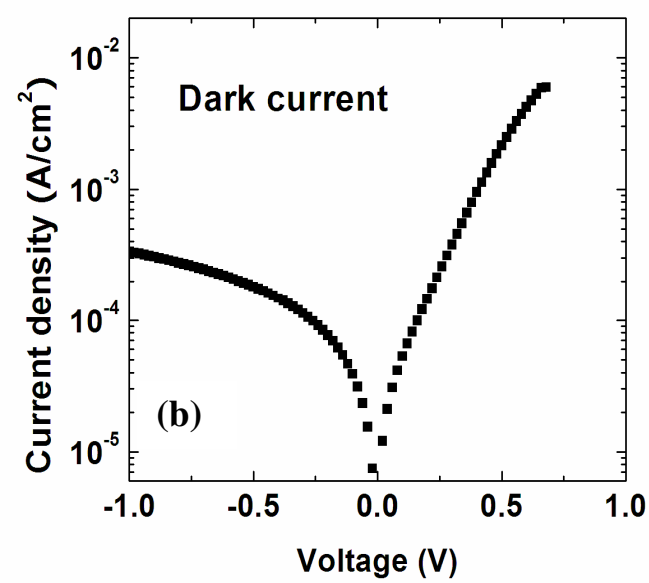


Figure 8.8 Photo (a) and dark (b) I-V for the fabricated cells with Ni/S-passivated p-type Si(100) as ohmic contact region.

8.3.1.2 Ni/S-passivated p-type Si(100) as ohmic contact region

Instead of Pt/S-passivated region as ohmic contact, the cells using Ni/S-passivaed region as ohmic contact shows even worse photo I-V behavior, which is

shown in Figure 8.8 (a). The V_{oc} and I_{sc} of this type of cells are low in 0.36 mA/cm^2 and 260 mV respectively. The reverse current of this type of cells shown in Figure 8.7 (b) is almost one order higher than those cells with Pt/S-passivated region as ohmic contact. The better forward I-V behavior shown in Figure 8.7 (b) did not increase the I_{sc}.

8.3.1.3 Summary of the fabricated solar cells using Pt or Ni on S-passivated p-type Si(100) as ohmic contact region

In fact, all the cells mentioned above give a very low V_{oc} and I_{sc} if comparing with commercial solar cells that can have V_{oc} around 600 mV and I_{sc} around 30 mA/cm^2, producing the conversion efficiency η higher than 10%. Is there any room to improve the device performances in both V_{oc} and I_{sc} for the proposed diffusion-free back-contact solar cells?

To answer this, let's first examine the dark current of these cells. The reverse current of these cells is almost 2-3 orders higher than that of a single Al/S-passivated p-type Si(100) diode which gives the reverse current density about 4×10^{-7} A/cm^2. Equation 3.15 indicated that the lower reverse current the higher open-circuit voltage. Actually, the expected low reverse current is limited by S passivation quality, and the wet-chemical passivating method can not guarantee a perfect surface passivation for a large area (2×2 cm^2) unlike a single diode with diameter of 200 μm. The badly-passivated region will eventually express a relatively high Schottky barrier, corresponding to a high reverse current, thus degrading the cell performance. S passivation quality depends on how carefully it was performed and it is not a systematically-controlled factor.

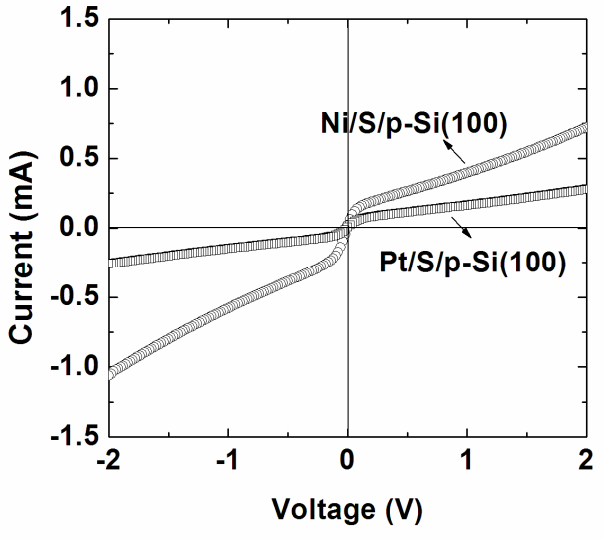


Figure 8.9 I-V measurements of the testing back-to-back diodes made by Pt/Ni on S-passivated p-type Si(100).

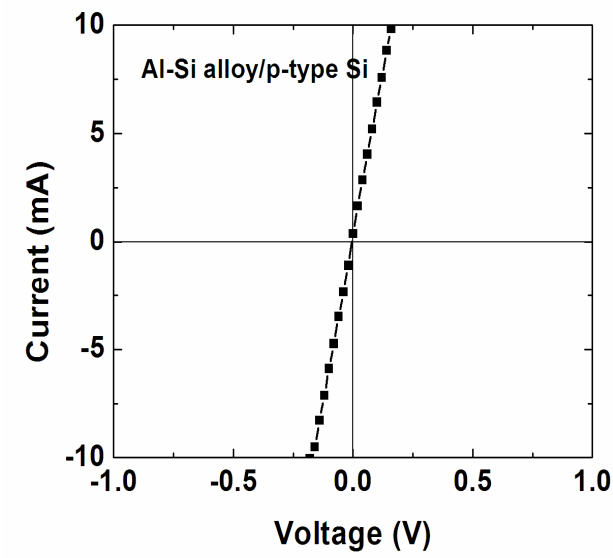


Figure 8.10 I-V measurements of the testing back-to-back diodes using Al-Si alloy as contact.

Secondly, the forward current would be a factor to affect the short-circuit current.

Figure 8.9 shows the I-V measurements of the testing back-to-back diodes made by Pt or Ni on S-passivated p-type Si(100). These diodes are formed by the second deposition of Pt or Ni on S-passivated area right after the first Al deposition. The curves shown in Figure 8.9 actually demonstrate a reification behavior instead of the ohmic behavior. This might be due to the possible damage of S layer by environment heating mentioned above. Because of this, the high series resistance is introduced, resulting in a low I_{sc} for the fabricated cells under illumination. To avoid this high series resistance, the Al-Si alloy is used for the ohmic contact. Figure 8.10 shows a perfect ohmic behavior for the testing back-to-back diodes using Al-Si alloy as contact. This contact has been proved to be thermally stable.

8.3.2. Al-Si alloy as ohmic contact region

Using Al-Si alloy as ohmic contact has two advantages. One is to reduce the series resistance and the other is that the S-passivated Si surface experiences only one time of e-beam evaporation for junction formation. Degradation of interface property by the second evaporation previously used for Pt/Ni is eliminated. The fabricated cells should possess a better photo I-V behavior than previous cells. Figure 8.11 shows the photo and dark I-V curves for the fabricated cells using Al-Si alloy region as ohmic contact. The V_{oc} is increased to 450 mV due to the given relatively low reverse current shown in Figure 8.11(b) and the I_{sc} is increased to 3.8 mA/cm^2 due to reduction of series resistance. The calculated conversion efficiency under illumination with AM~1.5 is close to 1%. Although this cell efficiency is much lower than the commercial cells, it is still a reasonable value if considering other factors such as SRV and bulk minority-

carrier lifetime, which will be discussed in next section.

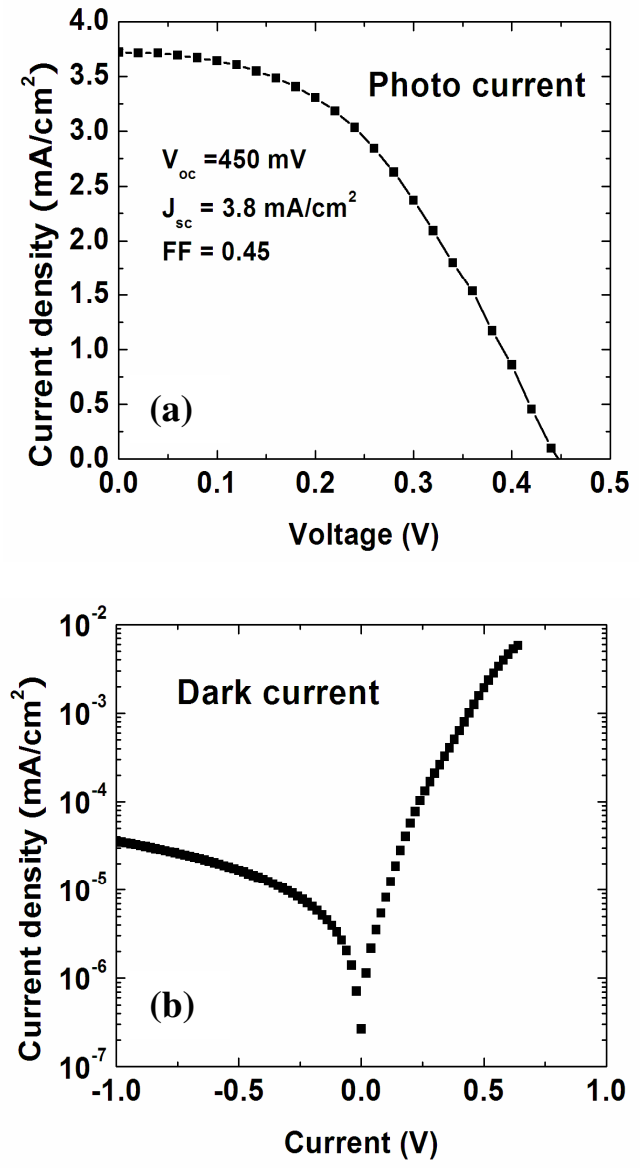


Figure 8.11 Photo (a) and dark (b) I-V for the fabricated cells with Al-Si alloy as ohmic contact region.

Figure 8.12 shows a strange photo I-V behavior for some cells fabricated with the exactly same process. Both I_{sc} and V_{oc} are extremely low. The cells have almost no

power generated. This might be due to the recombination effects both in the bulk and on the Si surface.

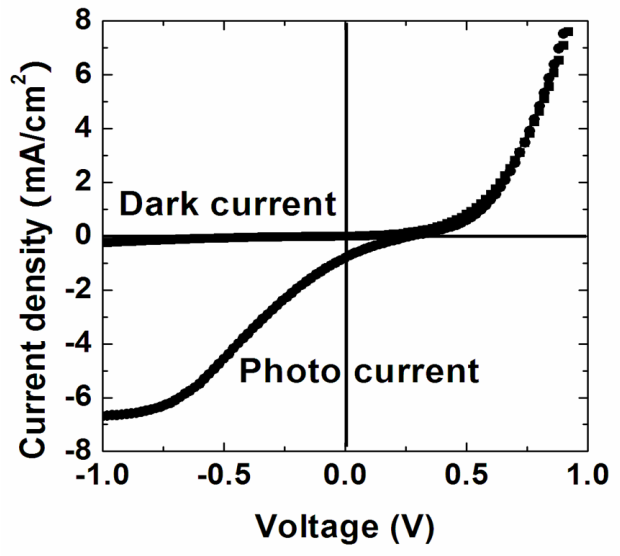


Figure 8.12 Photo and dark I-V for some of the fabricated cells with Al-Si alloy as ohmic contact region. The photo I-V shows a strange behavior.

8.4 Discussion and future plan

8.4.1. S passivation

S passivation plays the most important role in the fabrication of the proposed diffusion-free back contact solar cells. Its importance involves two aspects. One is to enable a diffusion-free p-n junction, and the other is to reduce the surface recombination velocity (SRV). Both aspects originate from one point that is removal of surface states by terminating the dangling bonds and releasing strained bonds and dimmer bonds on Si(100). The only concern for the passivating S layer is its reliability and stability on the Si surface. The wet-chemical method can not guarantee a perfect passivation on the surface. This is indicated by a much higher reverse current for the fabricated cells in

comparison with a single diode with diameter of 200 μm. The low reverse current corresponds to the high V_{oc} for the fabricated cells. Table 8.1 indicated that with one order of reverse current drop the V_{oc} can be increased by 150 mV. If the reverse current for the fabricated cells can be comparative to a single diode in the level of 10^{-7} A/cm^2, it is believed that the V_{oc} should be significantly increased. The reverse current is increased by 1.5 times after one week, indicating wet-chemical S passivation is not stable. Due to the stability issues for wet-chemical S passivation, a new passivation method needs to be developed in the future. The low cost CVD (chemical vapor deposition) might be a way to pursue, making a more reliable and stable monolayer S on the Si(100).

Table 8.1 Effects of surface passivation quality on the reverse current, V_{oc} and I_{sc} of the fabricated cell. A: As fabricated cells and B: After one week.

	J_R at -1 V (A/cm^2)	V_{oc} ((mV)	I_{sc} (mA/cm^2)
A	5×10^{-4}	300	1.5
	3×10^{-5}	450	3.7
B	4.5×10^{-5}	411	2.0

8.4.2. Surface recombination velocity-SRV

The surface recombination velocity (SRV) is another important factor to affect the conversion efficiency. The fabricated cells have 100 nm thermal SiO_2 serving both surface passivation and antireflection coating on the frond side. The thermal SiO_2 passivation is supposed to be the best method to reduce the SRV, but the measured SRV for the same type of wafer with 500 Å thermal SiO_2 gives a very high SRV about 850 cm/s shown in Table 8.2. Wet-chemical S-passivation yields SRV of 724 cm/s, the same

level as thermal SiO_2 passivation. With this level of front SRV, the simulated photo I-V (Figure 8.13) under AM = 1.5 for the back-contact solar cells shows only ~10 mA/cm^2 of I_{sc}, and the expected highest conversion efficiency is about 5% based on the photo I-V shown in Figure 8.12. If considering the high SRV on the back side of cell, the efficiency should be lower than 5%. It means that the 1% efficiency given by the fabricated cells is a reasonable value.

Table 8.2 SRV and minority-carrier lifetime τ for the wafers with different surface passivation treatments.

Passivation	SRV (cm/s)	Carrier τ (μs)
Thermal SiO_2	847	29.5
MBE Se	60	417
Wet-chemical S	724	34.5
Native oxide	3571	7

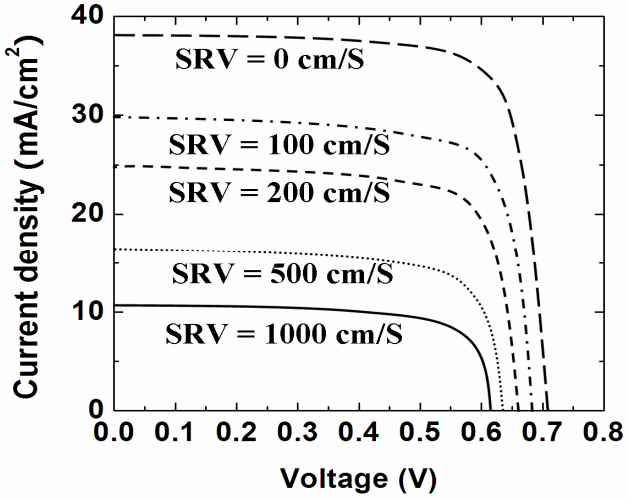


Figure 8.13 Simulated Photo I-V of the back contact solar cells at different SRV on the front side with respect to a high solar grade Si substrate with bulk minority-carrier lifetime of 1 ms. (Data reproduced from [96,97]).

In order to minimize SRV, thus improving the conversion efficiency for the

fabricated solar cells, the front surface has to be well treated, requiring a forming gas annealing (95%N_2 + 5%H_2). The alternative methods can be PECVD SiN_x:H passivation or amorphous Si passivation to form a hetero-junction on the front side [97]. S passivation by wet-chemical method has to be replaced by another to significantly reduce the SRV. Another possible contribution to the high SRV might be due to the metal induced gap states (MIGS) in the junction contacts [98], which will be investigated in the future work.

8.4.3. Bulk minority-carrier lifetime τ

For back contact solar cells, the Si substrate with high minority-carrier lifetime τ is usually needed. The high minority-carrier lifetime corresponds to the long diffusion length that must be at least larger than the Si substrate thickness. It is about 200 μm for Sunpower's back-contact solar cells. The longer diffusion length means the higher collection possibility for minority carriers generated in the bulk and junction region. For some of back-contact solar cells producing high efficiency, the diffusion length is even three times larger than the Si substrate thickness. Therefore, for our proposed back-contact solar cells, using highly purified Si substrate with high bulk minority-carrier lifetime is worthy to try.

8.4.4. Other factors affecting the conversion efficiency

Most of the back contact solar cells have either a high-low junction or a rectifying junction. The high-low junction is to provide a built-in field at the surface which will keep the minority carriers away from the high recombination surface. For the rectifying junction, the generated carriers in this region cause this junction to become

forward biased and to inject minority carriers into the base region of the cells. Based on these, an amorphous Si layer can be deposited on the front surface of the proposed cells to form a high-low junction, pushing away the minority carriers back to the base region.

Another factor is the gap distance between the wide finger contact and narrow finger contact. The lowest gap distance in our mask design is 150 μm. If this is larger than the minority-carrier diffusion length, some of the minority carriers generated in the back-side junction region will recombine before they can be collected. Reducing the gap distance is suggested.

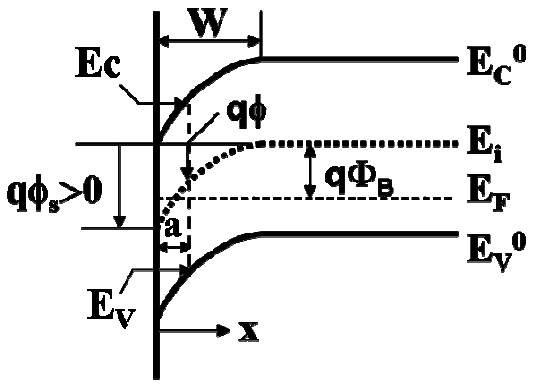
8.4.5. Expectation of future work

Based on the discussion in the Chapter 8.4, it will not be surprised with a low efficiency (η ~1%) obtained from the currently-fabricated solar cells. If all the factors mentioned in Chapter 8.4 are considered for future cell design, a high efficiency is possible to be achieved. It has to mention that the future work proposed here involves several facility issues and it may not be treated as a short-term goal to be realized.

APPENDIX A

ELECTROSTATICS BASED ON FERMI STATISTICS

ϕ_s: surface potential
W: depletion width
x: distance from surface
ϕ: potential at x=a
E_C^0: conduction band at x=W (bulk)
E_V^0: valence band at x=W (bulk)
E_C: conduction band at x=a
E_V: valence band at x=a
E_i: intrinsic level
E_F: Fermi level



Question: With given ϕ_s to solve ϕ, electric field E and surface charge Q_s

ϕ_s and ϕ are referred with respect to the intrinsic level E_i, they are positive as indicated by the band diagram.

Using Poisson equation

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{q}{\varepsilon_s}\left[-N_A + (p_p - n_p)\right] \qquad \text{(A-1)}$$

ρ: charge density, ε_s: permittivity of semiconductor, q: electron charge, N_A: ionized acceptor, p_p: hole (majority) density, n_p: electron (minority) density

With Boltzmann statistics, n_p and p_p are expressed by Equation A-2 and A-3,

$$n_p = N_c \exp(-\frac{E_C - E_F}{\kappa_B T}) = N_c \exp(-\frac{E_C^o - E_F - q\phi}{\kappa_B T}) n_{p0} \exp(\beta\phi) \qquad \text{(A-2)}$$

$$p_p = N_v \exp(-\frac{E_F - E_V}{\kappa_B T}) = N_c \exp(-\frac{E_F - E_V^0 + q\phi}{\kappa_B T}) = p_{p0} \exp(-\beta\phi) \qquad \text{(A-3)}$$

With Fermi statistics, n_p and p_p are expressed by Equation A-4 and A-5,

$$n_p = N_c \frac{2}{\sqrt{\pi}} F_{1/2}(-\frac{E_C - E_F}{\kappa_B T}) = N_c \frac{2}{\sqrt{\pi}} F_{1/2}(-\frac{E_C^o - E_F - q\phi}{\kappa_B T}) = N_c \frac{2}{\sqrt{\pi}} F_{1/2}(\beta\phi - \frac{E_C^0 - E_F}{\kappa_B T})$$

(A-4)

$$p_p = N_v \frac{2}{\sqrt{\pi}} F_{1/2}(-\frac{E_F - E_V}{\kappa_B T}) = N_v \frac{2}{\sqrt{\pi}} F_{1/2}(-\frac{E_F - E_V^0 + q\phi}{\kappa_B T}) = N_v \frac{2}{\sqrt{\pi}} F_{1/2}(-\beta\phi - \frac{E_F - E_V^0}{\kappa_B T})$$

(A-5)

N_c: effective density of states in the conduction band

N_v: effective density of states in the valence band

If ϕ_s is large, E_C may bend below E_F, causing degenerate inversion on the surface-a thin inversion layer containing large amount of electrons

Using Boltzmann statistics is less accurate than Fermi statistics to solve ϕ, electric field **E**, and surface charge Q_s in the case of degeneration inversion on the surface. The most accurate method is using Quantum theory to solve because the energy levels in the inversion layer are discrete. In this work, Fermi statistics is used.

Charge neutrality must exist in the bulk, making

$$-N_A = n_{p0} - p_{p0} \tag{A-6}$$

n_{p0}: electron (minority) density in the bulk, p_{p0}: hole (majority) density in the bulk

Poisson equation is rewritten as Equation A-7 and A-8

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{q}{\varepsilon_s}\left[(p_p - p_{p0}) - (n_p - n_{p0})\right] \tag{A-7}$$

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{q}{\varepsilon_s}\left\{N_v \frac{2}{\sqrt{\pi}}\left[F_{1/2}(-\beta\phi - \frac{E_F - E_V^0}{\kappa_B T}) - F_{1/2}(-\frac{E_F - E_V^0}{\kappa_B T})\right] - N_c \frac{2}{\sqrt{\pi}}\left[F_{1/2}(\beta\phi - \frac{E_C^o - E_F}{\kappa_B T}) - F_{1/2}(-\frac{E_C^0 - E_F}{\kappa_B T})\right]\right\}$$

(A-8)

Integrating both sides of Equation A-8 with $d\phi$,

Equation A-8 is altered as A-9

$$\int_0^{\frac{\partial\phi}{\partial x}} (\frac{\partial\phi}{\partial x}) d(\frac{\partial\phi}{\partial x}) = \frac{1}{2}(-\frac{\partial\phi}{\partial x})^2 = \frac{1}{2}\mathrm{E}^2 =$$

$$-\frac{q}{\varepsilon_s}\int_0^{\phi}\left\{N_v\frac{2}{\sqrt{\pi}}\left[F_{1/2}(-\beta\phi-\frac{E_F-E_V^0}{\kappa_B T})-F_{1/2}(-\frac{E_F-E_V^0}{\kappa_B T})\right]-N_c\frac{2}{\sqrt{\pi}}\left[F_{1/2}(\beta\phi-\frac{E_C^o-E_F}{\kappa_B T})-F_{1/2}(-\frac{E_C^0-E_F}{\kappa_B T})\right]\right\}d\phi \tag{A-9}$$

Using Fermi relationships shown in Equation A-10 to integrate the right side of Equation A-9.

$$\frac{\partial F_j(\eta)}{\partial\eta} = jF_{j-1}(\eta), \qquad \frac{\partial F_{3/2}(\eta)}{\partial\eta} = \frac{3}{2}F_{1/2}(\eta), \qquad \frac{2}{3}\partial F_{3/2}(\eta) = F_{1/2}(\eta)\partial\eta \tag{A-10}$$

After integration, the right side of Equation A-9 is changed to A-11,

$$\begin{aligned}&=\frac{4qN_v}{3\varepsilon_s\beta\sqrt{\pi}}\left[F_{3/2}(-\beta\phi-\frac{E_F-E_V^0}{\kappa_B T})-F_{3/2}(-\frac{E_F-E_V^0}{\kappa_B T})+F_{1/2}(-\frac{E_F-E_V^0}{\kappa_B T})\beta\phi\right]+\\ &\frac{4qN_c}{3\varepsilon_s\beta\sqrt{\pi}}\left[F_{3/2}(\beta\phi-\frac{E_C^0-E_F}{\kappa_B T})-F_{3/2}(-\frac{E_C^0-E_F}{\kappa_B T})-F_{1/2}(-\frac{E_C^0-E_F}{\kappa_B T})\beta\phi\right]\end{aligned} \tag{A-11}$$

so that the electric field **E** and ϕ are solved.

$$\mathrm{E}=-\frac{\partial\phi}{\partial x}=\pm\left\{\begin{aligned}&\frac{4qN_v}{3\varepsilon_s\beta\sqrt{\pi}}\left[F_{3/2}(-\beta\phi-\frac{E_F-E_V^0}{\kappa_B T})-F_{3/2}(-\frac{E_F-E_V^0}{\kappa_B T})+F_{1/2}(-\frac{E_F-E_V^0}{\kappa_B T})\beta\phi\right]+\\ &\frac{4qN_c}{3\varepsilon_s\beta\sqrt{\pi}}\left[F_{3/2}(\beta\phi-\frac{E_C^0-E_F}{\kappa_B T})-F_{3/2}(-\frac{E_C^0-E_F}{\kappa_B T})-F_{1/2}(-\frac{E_C^0-E_F}{\kappa_B T})\beta\phi\right]\end{aligned}\right\}^{\frac{1}{2}} \tag{A-12}$$

The electric field at surface $\mathbf{E_s}$ is actually obtained by plugging surface potential ϕ_s in Equation A-12.

Surface charge Q_s is given by Equation A-13.

$$Q_s = -\varepsilon_s \mathrm{E}_s = \varepsilon_s \frac{\partial \phi}{\partial x}\Big|_s$$

$$= \mp \left\{ \begin{array}{l} \frac{4qN_v}{3\beta\sqrt{\pi}} \left[F_{3/2}(-\beta\phi_s - \frac{E_F - E_V^0}{\kappa_B T}) - F_{3/2}(-\frac{E_F - E_V^0}{\kappa_B T}) + F_{1/2}(-\frac{E_F - E_V^0}{\kappa_B T})\beta\phi_s \right] + \\ \frac{4qN_c}{3\beta\sqrt{\pi}} \left[F_{3/2}(\beta\phi_s - \frac{E_C^0 - E_F}{\kappa_B T}) - F_{3/2}(-\frac{E_C^0 - E_F}{\kappa_B T}) - F_{1/2}(-\frac{E_C^0 - E_F}{\kappa_B T})\beta\phi_s \right] \end{array} \right\}^{\frac{1}{2}}$$

(A-13)

C_D is the differential capacitance of the semiconductor, given by Equation A-14.

$$C_D = \frac{\partial Q_s}{\partial \phi_s} = \mp \frac{4qN_v}{3\beta\sqrt{\pi}} \left[\frac{3}{2}(-\beta) F_{1/2}(-\beta\phi_s - \frac{E_F - E_V^0}{\kappa_B T}) + F_{1/2}(-\frac{E_F - E_V^0}{\kappa_B T})\beta \right]$$

(A-14)

The calculation is using a self-developed MATLAB program.

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BIOGRAPHICAL INFORMATION

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